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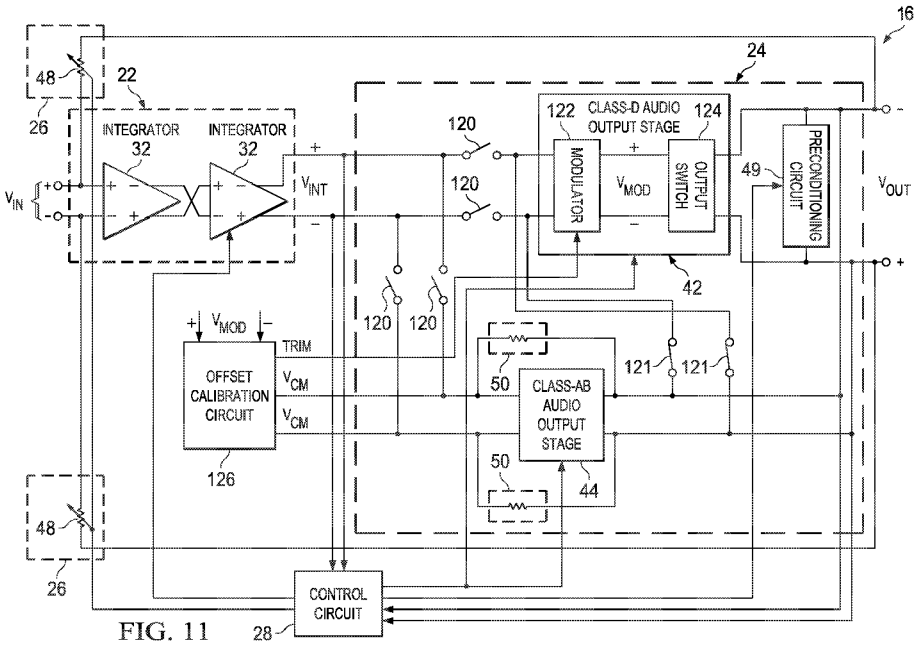

FIG. 11

(57) Abstract: A method for offset calibration may include decoupling a modulator input of a first path from a first stage output, coupling a second path output to the modulator input, applying a common-mode voltage to a second path input, receiving a calibration signal from the modulator output generated in response to the common-mode voltage, and modifying one or more parameters of the modulator to compensate for an offset between the first path and the second path indicated by the calibration signal. A method for gain calibration may include decoupling a modulator input from a first stage output, decoupling a second path from the first stage output, applying a first test signal to the modulator input, applying a second test signal to a second path input, wherein the second test signal is of opposite phase as the first test signal, coupling a second path output to an amplifier input via a calibration feedback network, receiving a calibration signal from the first stage output generated in response to the first test signal and the second test signal, and

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modifying one or more parameters of the second path to compensate for a difference in respective gains of the modulator and the second path indicated by the calibration signal.

CALIBRATION FOR AMPLIFIER WITH CONFIGURABLE FINAL OUTPUT STAGE

RELATED APPLICATION

The present disclosure is related to U.S. Pat. App. Ser. No. 15/277,465, filed September 27, 2016, and entitled "Amplifier with Configurable Final Output Stage," which is incorporated herein by reference.

FIELD OF DISCLOSURE

The present disclosure relates in general to circuits for audio devices, including without limitation personal audio devices, such as wireless telephones and media players, and more specifically, to systems and methods relating to switching between configurations of an amplifier with a configurable final output stage.

BACKGROUND

Personal audio devices, including wireless telephones, such as mobile/cellular telephones, cordless telephones, mp3 players, and other consumer audio devices, are in widespread use. Such personal audio devices may include circuitry for driving a pair of headphones or one or more speakers. Such circuitry often includes a power amplifier for driving an audio output signal to headphones or speakers. Generally speaking, a power amplifier amplifies an audio signal by taking energy from a power supply and controlling an audio output signal to match an input signal shape but with a larger amplitude.

One example of an audio amplifier is a class-D amplifier. A class-D amplifier (also known as a "switching amplifier") may comprise an electronic amplifier in which the amplifying devices (e.g., transistors, typically metal-oxide-semiconductor field effect transistors) operate as electronic switches, and not as linear gain devices as in other amplifiers (e.g., class-A, class-B, and class-AB amplifiers). In a class-D amplifier, an analog signal to be amplified may be converted to a series of pulses by pulse-width modulation, pulse-density modulation, or another method of modulation, such that the analog signal is converted into a modulated signal in which a characteristic of the pulses of the modulated signal (e.g., pulse widths, pulse density, etc.) is a function of the

magnitude of the analog signal. After amplification with a class-D amplifier, the output pulse train may be converted back to an unmodulated analog signal by passing through a passive low-pass filter, wherein such low-pass filter may be inherent in the class-D amplifier or a load driven by the class-D amplifier. Class-D amplifiers are often used due to the fact that they may be more power efficient than linear analog amplifiers, in that class-D amplifiers may dissipate less power as heat in active devices as compared to linear analog amplifiers. However, class-D amplifiers may have high quiescent power when amplifying low-magnitude signals and may require a large amount of area in order to meet stringent dynamic range requirements in audio devices.

Accordingly, it may be desired to have an amplifier that has a configurable final output stage, wherein the final output stage is configurable between a Class-AB output stage and a Class-D output stage. However, having an amplifier with a configurable output stage may be susceptible to audio artifacts caused by switching between the modes of the final output stage.

SUMMARY

In accordance with the teachings of the present disclosure, one or more disadvantages and problems associated with existing approaches to signal amplification in an audio system may be reduced or eliminated.

In accordance with embodiments of the present disclosure, an amplifier may include a plurality of stages and a calibration subsystem. The plurality of stages may include at least a first stage configured to receive an input signal at an amplifier input and generate at a first stage output an intermediate signal which is a function of the input signal, and a final output stage configured to generate an output signal which is a function of the intermediate signal at an amplifier output. The final output stage may include a first path comprising a modulator having a modulator input for receiving the intermediate signal and configured to generate at a modulator output a modulated signal from the intermediate signal and a plurality of output switches configured to generate the output signal from the modulated signal when the first path is selected to generate the output signal. The final output stage may also include a second path having a second path input for receiving the intermediate signal configured to generate at a second path output the

output signal from the intermediate signal when the second path is selected to generate the output signal. The calibration subsystem may be configured to, in a calibration mode, decouple the modulator input from the first stage output, couple the second path output to the modulator input, apply a common-mode voltage to the second path input, receive a calibration signal from the modulator output generated in response to the common-mode voltage, and modify one or more parameters of the modulator to compensate for an offset between the first path and the second path indicated by the calibration signal.

In accordance with these and other embodiments of the present disclosure, an amplifier may include a plurality of stages, a signal feedback network, and a calibration subsystem. The plurality of stages may include at least a first stage configured to receive an input signal at an amplifier input and generate at a first stage output an intermediate signal which is a function of the input signal, and a final output stage configured to generate an output signal which is a function of the intermediate signal at an amplifier output. The final output stage may include a first path comprising a modulator having a modulator input for receiving the intermediate signal and configured to generate at a modulator output a modulated signal from the intermediate signal and a plurality of output switches configured to generate the output signal from the modulated signal when the first path is selected to generate the output signal. The final output stage may also include a second path having a second path input for receiving the intermediate signal configured to generate at a second path output the output signal from the intermediate signal when the second path is selected to generate the output signal. The signal feedback network may be coupled between the amplifier output and the amplifier input. The calibration subsystem may be configured to, in a calibration mode, decouple the modulator input from the first stage output, decouple the second path from the first stage output, apply a first test signal to the modulator input, apply a second test signal to the second path input, wherein the second test signal is of opposite phase as the first test signal, couple the second path output to the amplifier input via a calibration feedback network, receive a calibration signal from the first stage output generated in response to the first test signal and the second test signal, and modify one or more parameters of the second path to compensate for a difference in respective gains of the modulator and the second path indicated by the calibration signal.

In accordance with these and other embodiments of the present disclosure, a method may be provided for a calibration mode of an amplifier comprising a plurality of stages comprising at least a first stage configured to receive an input signal at an amplifier input and generate at a first stage output an intermediate signal which is a function of the input signal, and a final output stage configured to generate an output signal which is a function of the intermediate signal at an amplifier output, and wherein the final output stage comprises a first path comprising a modulator having a modulator input for receiving the intermediate signal and configured to generate at a modulator output a modulated signal from the intermediate signal and a plurality of output switches configured to generate the output signal from the modulated signal when the first path is selected to generate the output signal wherein the final output stage further comprises a second path having a second path input for receiving the intermediate signal configured to generate at a second path output the output signal from the intermediate signal when the second path is selected to generate the output signal. The method may include decoupling the modulator input from the first stage output, coupling the second path output to the modulator input, applying a common-mode voltage to the second path input, receiving a calibration signal from the modulator output generated in response to the common-mode voltage, and modifying one or more parameters of the modulator to compensate for an offset between the first path and the second path indicated by the calibration signal.

In accordance with these and other embodiments of the present disclosure, a method may be provided for a calibration mode of an amplifier comprising a plurality of stages comprising at least a first stage configured to receive an input signal at an amplifier input and generate at a first stage output an intermediate signal which is a function of the input signal, and a final output stage configured to generate an output signal which is a function of the intermediate signal at an amplifier output, and wherein the final output stage comprises a first path comprising a modulator having a modulator input for receiving the intermediate signal and configured to generate at a modulator output a modulated signal from the intermediate signal and a plurality of output switches configured to generate the output signal from the modulated signal when the first path is selected to generate the output signal wherein the final output stage further comprises a

second path having a second path input for receiving the intermediate signal configured to generate at a second path output the output signal from the intermediate signal when the second path is selected to generate the output signal. The method may include decoupling the modulator input from the first stage output, decoupling the second path from the first stage output, applying a first test signal to the modulator input, applying a second test signal to the second path input, wherein the second test signal is of opposite phase as the first test signal, coupling the second path output to the amplifier input via a calibration feedback network, receiving a calibration signal from the first stage output generated in response to the first test signal and the second test signal, and modifying one or more parameters of the second path to compensate for a difference in respective gains of the modulator and the second path indicated by the calibration signal.

Technical advantages of the present disclosure may be readily apparent to one skilled in the art from the figures, description and claims included herein. The objects and advantages of the embodiments will be realized and achieved at least by the elements, features, and combinations particularly pointed out in the claims.

It is to be understood that both the foregoing general description and the following detailed description are examples and explanatory and are not restrictive of the claims set forth in this disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present embodiments and advantages thereof may be acquired by referring to the following description taken in conjunction with the accompanying drawings, in which like reference numbers indicate like features, and wherein:

FIGURE 1 is an illustration of an example personal audio device, in accordance with embodiments of the present disclosure;

FIGURE 2 is a block diagram of selected components of an example audio integrated circuit of a personal audio device, in accordance with embodiments of the present disclosure;

FIGURE 3 is a block diagram of selected components of an example amplifier, in accordance with embodiments of the present disclosure;

FIGURE 4 is a block diagram of selected components of an example class-AB audio output stage, in accordance with embodiments of the present disclosure;

FIGURE 5 is a block diagram of selected components of another example class-AB audio output stage, in accordance with embodiments of the present disclosure;

FIGURE 6 is a block diagram of selected components of an example preconditioning circuit, in accordance with embodiments of the present disclosure;

FIGURE 7 is a circuit diagram of selected components of an example quick charge circuit, in accordance with embodiments of the present disclosure;

FIGURE 8 is a block diagram of selected components of another example preconditioning circuit, in accordance with embodiments of the present disclosure;

FIGURE 9 is a flow chart of an example method for switching between a first mode of a final output stage of an amplifier and a second mode of the final output stage of the amplifier, in accordance with embodiments of the present disclosure;

FIGURE 10 is a flow chart of an example method for switching between a second mode of a final output stage of an amplifier and a first mode of the final output stage of the amplifier, in accordance with embodiments of the present disclosure;

FIGURE 11 is a block diagram of selected components of the example amplifier of FIGURE 3 modified to include an offset calibration circuit, in accordance with embodiments of the present disclosure; and

FIGURE 12 is a block diagram of selected components of the example amplifier of FIGURE 3 modified to include a gain calibration circuit, in accordance with embodiments of the present disclosure.

DETAILED DESCRIPTION

FIGURE 1 is an illustration of an example personal audio device 1, in accordance with embodiments of the present disclosure. FIGURE 1 depicts personal audio device 1 coupled to a headset 3 in the form of a pair of earbud speakers 8A and 8B. Headset 3 depicted in FIGURE 1 is merely an example, and it is understood that personal audio device 1 may be used in connection with a variety of audio transducers, including without limitation, headphones, earbuds, in-ear earphones, and external speakers. A plug 4 may provide for connection of headset 3 to an electrical terminal of personal audio device 1.

Personal audio device 1 may provide a display to a user and receive user input using a touch screen 2, or alternatively, a standard liquid crystal display (LCD) may be combined with various buttons, sliders, and/or dials disposed on the face and/or sides of personal audio device 1. As also shown in FIGURE 1, personal audio device 1 may include an audio integrated circuit (IC) 9 for generating an analog audio signal for transmission to headset 3 and/or another audio transducer.

FIGURE 2 is a block diagram of selected components of an example audio IC 9 of a personal audio device, in accordance with embodiments of the present disclosure. In some embodiments, example audio IC 9 may be used to implement audio IC 9 of FIGURE 1. As shown in FIGURE 2, a microcontroller core 18 may supply a digital audio input signal DIG_IN to a digital-to-analog converter (DAC) 14, which may convert the digital audio input signal to an analog input signal V_{IN}. DAC 14 may supply analog signal V_{IN} to an amplifier 16 which may amplify or attenuate analog input signal V_{IN} to provide an audio output signal V_{OUT}, which may operate a speaker, headphone transducer, a line level signal output, and/or other suitable output.

FIGURE 3 is a block diagram of selected components of an example amplifier 16, in accordance with embodiments of the present disclosure. As shown in FIGURE 3, amplifier 16 may include a first stage 22 (e.g., an analog front end) configured to receive analog input signal V_{IN} at an amplifier input of amplifier 16 and generate an intermediate signal V_{INT} which is a function of analog input signal V_{IN}, a final output stage 24 configured to generate audio output signal V_{OUT} at an amplifier output of amplifier 16 as a function of intermediate signal V_{INT}, a signal feedback network 26 coupled between the amplifier output and the amplifier input, and a control circuit 28 for controlling the operation of certain components of amplifier 16, as described in greater detail below.

First stage 22 may include any suitable analog front end circuit for conditioning analog input signal V_{IN} for use by final output stage 24. For example, first stage 22 may include one or more analog integrators 32 cascaded in series, as shown in FIGURE 3.

Final output stage 24 may include any suitable driving circuit for driving audio output signal V_{OUT} as a function of intermediate signal V_{INT} (thus, also making audio output signal V_{OUT} a function of analog input signal V_{IN}) wherein final output stage 24 is switchable among a plurality of modes including at least a first mode in which final

output stage 24 generates audio output signal V_{OUT} as a modulated output signal which is a function of intermediate signal V_{INT} and a second mode in which final output stage 24 generates audio output signal V_{OUT} as an unmodulated output signal which is a function of intermediate signal V_{INT}. To carry out this functionality, final output stage 24 may include a class-D audio output stage 42 which may be enabled in the first mode (and disabled in the second mode) to generate audio output signal V_{OUT} as a modulated output signal which is a function of intermediate signal V_{INT} and a class-AB audio output stage 44 which may be enabled in the second mode (and disabled in the first mode) to generate audio output signal V_{OUT} as an unmodulated output signal which is a function of intermediate signal V_{INT}.

Class-D audio output stage 42 may comprise any suitable system, device, or apparatus configured to amplify intermediate signal V_{INT} and convert intermediate signal V_{INT} into a series of pulses by pulse-width modulation, pulse-density modulation, or another method of modulation, such that intermediate signal V_{INT} is converted into a modulated signal in which a characteristic of the pulses of the modulated signal (e.g., pulse widths, pulse density, etc.) is a function of the magnitude of intermediate signal V_{INT}. After amplification by class-D audio output stage 42, its output pulse train may be converted back to an unmodulated analog signal by passing through a passive low-pass filter, wherein such low-pass filter may be inherent in output circuitry of class-D audio output stage 42 or a load driven by final output stage 24. As shown in FIGURE 3, class-D audio output stage 42 may include a control input for receiving a control input from control circuit 28 in order to selectively enable class-D audio output stage 42 during the first mode and disable class-D audio output stage 42 during the second mode (e.g., prevent class-D audio output stage 42 from driving the amplifier output of amplifier 16 by disabling or decoupling a supply voltage from class-D audio output stage 42 or by disabling or decoupling driving devices of the amplifier output of amplifier 16). As shown in FIGURE 3, class-D audio output stage 42 may include a modulator 122 having a modulator input for receiving intermediate signal V_{INT} and configured to generate at a modulator output a modulated signal from intermediate signal V_{INT} and also having an output switch block 124 comprising a plurality of output switches configured to generate audio output signal V_{OUT} from the modulated signal when the first mode is enabled.

Class-AB audio output stage 44 may comprise any suitable system, device, or apparatus configured to amplify intermediate signal V_{INT} with a linear gain and convert intermediate signal V_{INT} into an unmodulated audio output signal V_{OUT}. For example, in some embodiments, unmodulated audio output signal V_{OUT} may include a continuous-time baseband signal (e.g., an audio baseband signal). As shown in FIGURE 3, class-AB audio output stage 44 may include a control input for receiving a control input from control circuit 28 in order to selectively enable class-AB audio output stage 44 during the second mode and disable class-AB audio output stage 44 during the first mode (e.g., prevent class-AB audio output stage 44 from driving the amplifier output of amplifier 16 by disabling or decoupling a supply voltage from class-AB audio output stage 44 or by disabling or decoupling driving devices of the amplifier output of amplifier 16). Example implementations of class-AB audio output stage 44 are depicted in FIGURES 4 and 5 and described in greater detail below.

As shown in FIGURE 3, final output stage 24 may include a signal feedback network 50 for feeding back a signal indicative of audio output signal V_{OUT} to the input of final output stage 24, thus forming a feedback loop around Class-AB audio output stage 44. For example, as shown in FIGURE 3, signal feedback network 50 may include resistors and/or other suitable circuit elements.

In some embodiments, a signal gain (e.g., V_{OUT}/V_{INT}) of final output stage 24 in the first mode may be approximately equal to the signal gain of final output stage 24 in the second mode. In these and other embodiments, an offset (e.g., direct current offset) of final output stage 24 in the first mode may be approximately equal to the offset of final output stage 24 in the second mode.

As shown in FIGURE 3, final output stage 24 may also include a preconditioning circuit 49 coupled to one or both of the output terminals of the amplifier output of amplifier 16, with preconditioning circuit 49 having a control input received from control circuit 28 for controlling functionality of preconditioning circuit 49, as described in greater detail below. In some embodiments, preconditioning circuit 49 may be configured to precondition at least one of a voltage (e.g., voltage V_{OUT}) and a current of the output (e.g., a current flowing into a load coupled across the terminals of voltage V_{OUT}) of final output stage 24 prior to switching between modes of final output stage 24

in order to limit audio artifacts caused by switching final output stage 24 between modes. For example, preconditioning circuit 49 may precondition at least one of the voltage and the current of the output of final output stage 24 prior to switching between modes of final output stage 24 by charging each of the output terminals of the output of final output stage 24 to a common mode voltage of a class-AB output driver stage integral to class-AB audio output stage 44. In these and other embodiments, preconditioning circuit 49 may be configured to perform a switching sequence to switch between modes of final output stage 24, such that at all points of the switching sequence, output terminals of the output of final output stage 24 have a known impedance.

Signal feedback network 26 may include any suitable feedback network for feeding back a signal indicative of audio output signal V_{OUT} to the amplifier input of amplifier 16. For example, as shown in FIGURE 3, signal feedback network 26 may include variable feedback resistors 48, wherein resistances of variable feedback resistors 48 are controlled by control signals received from control circuit 28, as described in greater detail below.

Thus, final output stage 24 may operate as an open-loop switched-mode driver in the first mode and may operate as a continuous-time closed-loop amplifier in the second mode. In addition, when the final output stage is operating in the second mode, amplifier 16 may comprise a first feedback loop including signal feedback network 26 and a second feedback loop coupled between the amplifier output and the intermediate output implemented by signal feedback network 50.

Control circuit 28 may include any suitable system, device, or apparatus configured to receive information indicative of audio output voltage V_{OUT}, intermediate signal V_{INT}, and/or other operational characteristic of amplifier 16, and based at least thereon, control operation of one or more components of amplifier 16. For example, control circuit 28 may be configured to, based on a characteristic of analog input signal V_{IN} (e.g., which may be determined from receiving and analyzing intermediate signal V_{INT} and/or audio output signal V_{OUT}), switch between the first mode and the second mode of final output stage 24. Such characteristic may include one or more of a frequency of analog input signal V_{IN}, an amplitude of analog input signal V_{IN}, a signal-to-noise ratio of analog input signal V_{IN}, a noise floor of analog input signal V_{IN}, or another

noise characteristic of analog input signal V_{IN}. For example, in some embodiments, control circuit 28 may be configured to switch final output stage 24 from the first mode to the second mode when an amplitude of analog input signal V_{IN} decreases below a threshold amplitude, and may be configured to switch final output stage 24 from the second mode to the first mode when an amplitude of analog input signal V_{IN} increases above the same threshold amplitude or another threshold amplitude. In some embodiments, to reduce audio artifacts associated with switching between modes, control circuit 28 may also be configured to switch between modes only when the amplitude of audio output signal V_{OUT} is approximately zero (e.g., when a modulated signal generated by class-D audio output stage 42 is at its minimum voltage in its generated pulse train).

In these and other embodiments, control circuit 28 may further be configured to, in order to reduce audio artifacts induced by switching between the two modes, cause final output stage 24 to switch between the first mode and the second mode at an approximate completion of a modulation period of the modulated output signal output by Class-D audio output stage 42, and cause final output stage 24 to switch between the second mode and the first mode at an approximate beginning of another modulation period of the modulated output signal output by Class-D audio output stage 42.

In these and other embodiments, control circuit 28 may further be configured to, in order to reduce audio artifacts induced by switching between the two modes, control preconditioning circuit 49 and components thereof as described elsewhere in this disclosure.

In addition, control circuit 28 may also be configured to perform calibration of final output stage 24. For example, control circuit 28 may receive and analyze intermediate signal V_{INT} and audio output signal V_{OUT} to determine a gain of class-D audio output stage 42 (e.g., the signal gain of final output stage 24 in the first mode) and a gain of class-AB audio output stage 44 (e.g., the signal gain of final output stage 24 in the second mode), and based thereon, modify the gain of class-D audio output stage 42 and/or the gain of class-AB audio output stage 44 in order to calibrate the signal gain of final output stage 24 in the second mode to match the signal gain of final output stage 24 in the first mode. As another example, control circuit 28 may receive and analyze intermediate signal V_{INT} and/or audio output signal V_{OUT} to determine an offset (e.g., direct current

offset) of class-D audio output stage 42 (e.g., the offset of final output stage 24 in the first mode) and an offset of class-AB audio output stage 44 (e.g., the offset of final output stage 24 in the second mode), and based thereon, modify the offset of class-D audio output stage 42 and/or the offset of class-AB audio output stage 44 in order to calibrate the offset of final output stage 24 in the second mode to match the offset of final output stage 24 in the first mode.

In these and other embodiments, control circuit 28 may also be configured to control characteristics of first stage 22 (e.g., integrator 32) and/or signal feedback network 26. Control circuit 28 may maintain such characteristics and structure of first stage 22 and signal feedback network 26 as static when switching between the first mode and the second mode of final output stage 24 and when switching between the second mode and the first mode. Maintaining the characteristics and structure of first stage 22 and signal feedback network 26 as static when switching between modes allows the modes to share the same analog front end and feedback network, thus reducing or minimizing the likelihood of mismatched signal gain and offset between the modes, and thus reducing or minimizing audio artifacts caused by switching between modes. However, after control circuit 28 has switched final output stage 24 to the second mode (e.g., amplifier output driven by class-AB audio output stage 44), control circuit 28 may modify characteristics of first stage 22 and/or signal feedback network 26 in order to decrease a noise floor of amplifier 16. For example, in some embodiments, control circuit 28 may modify characteristics of integrator 32 (e.g., resistances and/or capacitances of filters internal to integrator 32) and/or other components of first stage 22 in order to decrease a noise floor of amplifier 16 when final output stage 24 operates in the second mode. As another example, in these and other embodiments, control circuit 28 may modify characteristics of signal feedback network 26 (e.g., resistances of variable feedback resistors 48) in order to decrease a noise floor of amplifier 16 when final output stage 24 operates in the second mode. When making such modification, control circuit 28 may, before switching final output stage from the second mode to the first mode, return such characteristics to their unmodified states.

FIGURE 4 is a block diagram of selected components of an example class-AB audio output stage 44A, in accordance with embodiments of the present disclosure. In

some embodiments, class-AB audio output stage 44 of amplifier 16 may be implemented using class-AB audio output stage 44A. As depicted, class-AB audio output stage 44A may include a class-AB driver stage 90, switches 92, and switches 94 arranged along with signal feedback network 50 as shown in FIGURE 4. In operation, when switching between modes of final output stage 24 from its class-D mode of operation to class-AB mode of operation, such switching may first involve powering on components of class-AB audio output stage 44A including class-AB driver stage 90 from a powered-off or powered-down state. After powering on components of class-AB audio output stage 44A including class-AB driver stage 90, switches 92 may be activated (e.g., closed, enabled, turned on) and switches 94 deactivated (e.g., opened, disabled, turned off) under the control of control signals communicated from control circuit 28 to allow operation of class-AB audio output stage 44A to settle into a normal steady-state operation before coupling the output of class-AB driver stage 90 to the output of final output stage 24. After class-AB output stage 44A has settled (and other conditions for switching between modes of final output stage 24 have been satisfied, as described elsewhere in this disclosure), switches 94 may be activated and switches 92 deactivated under the control of control signals communicated from control circuit 28 in order to couple the output of class-AB driver stage 90 to the output of final output stage 24.

FIGURE 5 is a block diagram of selected components of another example class-AB audio output stage 44B, in accordance with embodiments of the present disclosure. In some embodiments, class-AB audio output stage 44 of amplifier 16 may be implemented using class-AB audio output stage 44B. Class-AB audio output stage 44B may in many respects be similar to class-AB audio output stage 44A of FIGURE 4, and thus, only the main differences between class-AB audio output stage 44B and class-AB audio output stage 44A may be described below. As shown in FIGURE 5, class-AB audio output stage 44B may include a p-type metal-oxide-semiconductor field-effect transistor (p-MOSFET) 96, an n-type metal-oxide-semiconductor field-effect transistor (n-MOSFET) 98, and additional switches 94 beyond those present in class-AB audio output stage 44A of FIGURE 4. The characteristics of p-MOSFET 96 and n-MOSFET 98 may be such that they replicate characteristics of analogous devices integral to that of class-AB driver stage 90.

Thus, in operation, when switching between modes of final output stage 24 from its class-D mode of operation to class-AB mode of operation, switches 92 may be activated and switches 94 deactivated under the control of control signals communicated from control circuit 28 to allow operation of class-AB audio output stage 44B to settle into a normal steady-state operation before coupling the output of class-AB driver stage 90 to the output of final output stage 24. After class-AB output stage 44B has settled (and other conditions for switching between modes of final output stage 24 have been satisfied, as described elsewhere in this disclosure), switches 94 may be activated and switches 92 deactivated under the control of control signals communicated from control circuit 28 in order to couple the output of class-AB driver stage 90 to the output of final output stage 24. Accordingly, during the process of switching between modes of final output stage 24 from its class-D mode of operation to class-AB mode of operation, the replica of class-AB driver stage 90 formed by p-MOSFET 96 and n-MOSFET 98 may precondition at least one of the voltage (e.g., voltage V_{OUT}) and the current of the output of final output stage 28 by charging the output to a common mode voltage of class-AB driver stage 90 using a replica of class-AB driver stage 90 to provide the common mode voltage.

Although FIGURE 5 depicts that the replica of class-AB driver stage 90 formed by p-MOSFET 96 and n-MOSFET 98 is present within class-AB audio output stage 44B, in some embodiments, such replica and one or more other components depicted in FIGURE 5 as integral to class-AB audio output stage 44B may instead be integral to preconditioning circuit 49 described elsewhere herein.

FIGURE 6 is a block diagram of selected components of an example preconditioning circuit 49A, in accordance with embodiments of the present disclosure. In some embodiments, preconditioning circuit 49 of amplifier 16 may be implemented using preconditioning circuit 49A. As shown in FIGURE 6, preconditioning circuit 49A may include a clamp 46 and a quick charge circuit 47. Clamp 46, which may be embodied as a switch, may be coupled between the output terminals of the amplifier output of amplifier 16, with clamp 46 having a control input received from control circuit 28 for selectively enabling clamp 46 (to short the output terminals together) and disabling clamp 46, as described in greater detail below. Quick charge circuit 47 may include any suitable circuit for preconditioning at least one of the voltage (e.g., voltage V_{OUT}) and the

current of the output of final output stage 24 to a particular voltage and/or current (e.g., to a common-mode voltage of class-AB audio output stage 44).

FIGURE 7 is a circuit diagram of selected components of an example quick charge circuit 47, in accordance with embodiments of the present disclosure. As depicted in FIGURE 7, quick charge circuit 47 may include a flip-flop 100, logic NOR gate 102, n-MOSFET 104, n-MOSFET 106, p-MOSFET 108, n-MOSFET 110, p-MOSFET 112, and n-MOSFET 114 arranged as shown in FIGURE 7. In operation, when quick charge circuit 47 is enabled in accordance with one or more control signals communicated from control circuit 28, quick charge circuit 47 may charge the output terminals (which may be coupled together via clamp 46) of final output stage 24 to a common mode voltage V_{cm}, which may be a common mode voltage of class-AB audio output stage 44. In operation, n-MOSFET 104 and n-MOSFET 106 may charge the output terminals of final output stage 24, with a current-mode feedback which controls the voltage to which the output terminals are charged. Accordingly, quick charge circuit 47 may also precondition a current on the output of final output stage 24 based on a load present across the terminals of the output of final output stage 24.

FIGURE 8 is a block diagram of selected components of another example preconditioning circuit 49B, in accordance with embodiments of the present disclosure. In some embodiments, preconditioning circuit 49 of amplifier 16 may be implemented using preconditioning circuit 49B. As shown in FIGURE 8, preconditioning circuit 49B may include a clamp 46, a capacitor 39, and switches 41 and 43 arranged as shown. Clamp 46 of preconditioning circuit 49B may be similar to that of clamp 46 of preconditioning circuit 49A. When preconditioning circuit 49B is enabled under the control of control signals communicated from control circuit 28, clamp 46 may be enabled to short the output terminals of final output stage 24 together, switch 43 may be activated, and switch 41 deactivated to allow charge present on capacitor 39 to charge each of the output terminals of final output stage 24 to a common mode voltage V_{cm}. When preconditioning circuit 49B is disabled under the control of control signals communicated from control circuit 28, clamp 46 may be disabled, switch 41 may be activated, and switch 43 deactivated to allow capacitor 39 to charge to common mode voltage V_{cm}. Those of skill in the art may recognize that a dual equivalent current source

and inductor may be substituted in place of voltage V_{cm} and capacitor 39 such that the inductor may precondition a current of the output terminals of final output stage 24 when preconditioning circuit 49B is enabled.

FIGURE 9 is a flow chart of an example method 51 for switching between a first mode of a final output stage 24 of amplifier 16 and a second mode of final output stage 24 of amplifier 16, in accordance with embodiments of the present disclosure. According to some embodiments, method 51 begins at step 52. As noted above, teachings of the present disclosure are implemented in a variety of configurations of personal audio device 1. As such, the preferred initialization point for method 51 and the order of the steps comprising method 51 may depend on the implementation chosen.

At step 52, control circuit 28 may monitor intermediate signal V_{INT}, audio output signal V_{OUT}, or another signal indicative of analog input signal V_{IN}, to determine if analog input signal V_{IN} has decreased from above to below a threshold amplitude. If analog input signal V_{IN} has decreased from above to below the threshold amplitude, method 51 may proceed to step 53. Otherwise, method 51 may remain at step 52 until such threshold amplitude crossing occurs.

At step 53, control circuit 28 may monitor audio output signal V_{OUT} to determine when the amplitude of audio output signal V_{OUT} is approximately zero (e.g., when a modulated signal generated by class-D audio output stage 42 is at its minimum voltage in its generated pulse train). If audio output signal V_{OUT} has reached approximately zero, method 51 may proceed to step 54. Otherwise, method 51 may remain at step 53 until audio output signal V_{OUT} reaches approximately zero.

At step 54, control circuit 28 may cause class-AB amplifier 44 to power on from a powered-off or powered-down state, which state class-AB amplifier 44 may operate in order to save power when final output stage 24 is operating in the class-D mode.

At step 55, control circuit 28 may monitor audio output signal V_{OUT} to determine when class-AB amplifier 44 has settled into a steady-state operation from being powered on. Once class-AB amplifier 44 has settled, method 51 may proceed to step 56.

At step 56, control circuit 28 may enable clamp 46, thus shorting the output terminals at the amplifier output of amplifier 16 together, forcing audio output signal V_{OUT} to zero. At step 57, control circuit 28 may disable class-D amplifier 42. For

example, class-D amplifier 42 may be disabled by deactivating switches integral to class-D amplifier 42 such that the output terminals of class-D amplifier 42 are in a high-impedance state.

At step 58, class-AB audio output stage 44 and/or preconditioning circuit 49 may ramp a common mode voltage of audio output signal V_{OUT} to a predetermined value (e.g., a common-mode voltage equal to one-half of a supply voltage for class-AB audio output stage 44). At step 60, control circuit 28 may fully enable class-AB audio output stage 44 such that audio output signal V_{OUT} is an unmodulated signal which is a function of intermediate signal V_{INT}. For example, class-AB amplifier 44 may be enabled by activating switches integral to class-AB amplifier 44 (e.g., switches 94 depicted in FIGURES 4 and 5) such that the output terminals of a class-AB driver stage (e.g., class-AB driver stage 90) integral to class-AB amplifier 44 are coupled to the output terminals of final output stage 24. In some embodiments, steps 56 through 60 may take place when the modulated output signal output by class-D audio output stage 42 is at an approximate completion of a modulation period.

At step 62, control circuit 28 may disable clamp 46, thus allowing audio output signal V_{OUT} to take on a non-zero value driven by class-AB audio output stage 44. After completion of step 62, method 51 may end.

Although FIGURE 9 discloses a particular number of steps to be taken with respect to method 51, method 51 may be executed with greater or fewer steps than those depicted in FIGURE 9. In addition, although FIGURE 9 discloses a certain order of steps to be taken with respect to method 51, the steps comprising method 51 may be completed in any suitable order.

Method 51 may be implemented using personal audio device 1 or any other system operable to implement method 51. In certain embodiments, method 51 may be implemented partially or fully in software and/or firmware embodied in computer-readable media and executable by a controller.

FIGURE 10 is a flow chart of an example method 70 for switching between a second mode of final output stage 24 of amplifier 16 and a first mode of final output stage 24 of amplifier 16, in accordance with embodiments of the present disclosure. According to some embodiments, method 70 begins at step 72. As noted above, teachings of the

present disclosure are implemented in a variety of configurations of personal audio device 1. As such, the preferred initialization point for method 70 and the order of the steps comprising method 70 may depend on the implementation chosen.

At step 72, control circuit 28 may monitor intermediate signal V_{INT}, audio output signal V_{OUT}, or another signal indicative of analog input signal V_{IN}, to determine if analog input signal V_{IN} has increased from below to above a threshold amplitude (which may be the same threshold as that of step 52, or a different threshold). If analog input signal V_{IN} has increased from below to above the threshold amplitude, method 70 may proceed to step 73. Otherwise, method 70 may remain at step 72 until such threshold amplitude crossing occurs.

At step 73, control circuit 28 may monitor audio output signal V_{OUT} to determine when the amplitude of audio output signal V_{OUT} is approximately zero (e.g., when audio output signal V_{OUT} experiences a zero crossing). If audio output signal V_{OUT} is approximately zero, method 70 may proceed to step 74. Otherwise, method 70 may remain at step 73 until audio output signal V_{OUT} is approximately zero.

At step 74, control circuit 28 may cause class-D amplifier 42 to power on from a powered-off or powered-down state, which state class-D amplifier 42 may operate in order to save power when final output stage 24 is operating in the class-AB mode.

At step 75, control circuit 28 may monitor audio output signal V_{OUT} to determine when class-D amplifier 42 has settled into a steady-state operation from being powered on. Once class-D amplifier 42 has settled, method 70 may proceed to step 76.

At step 76, control circuit 28 may enable clamp 46, thus shorting the output terminals at the amplifier output of amplifier 16 together, forcing audio output signal V_{OUT} to zero. At step 77, control circuit 28 may disable class-AB amplifier 44. For example, class-AB amplifier 44 may be disabled by activating switches integral to class-AB amplifier 44 (e.g., switches 94 depicted in FIGURES 4 and 5) such that the output terminals of a class-AB driver stage (e.g., class-AB driver stage 90) integral to class-AB amplifier 44 are decoupled to the output terminals of final output stage 24.

At step 78, preconditioning circuit 49 (or another auxiliary amplifier, not shown in FIGURE 3) may ramp a common mode voltage of audio output signal V_{OUT} to zero. At step 80, control circuit 28 may fully enable class-D audio output stage 42 such that audio

output signal V_{OUT} is a modulated signal which is a function of intermediate signal V_{INT}. For example, class-D amplifier 42 may be enabled by activating switches integral to class-D amplifier 42 such that the output terminals of class-D amplifier 42 are coupled to the output terminals of final output stage 24. In some embodiments, steps 76 through 80 may take place when the modulated output signal output by class-D audio output stage 42 is at an approximate beginning of a modulation period.

At step 82, control circuit 28 may disable clamp 46, thus allowing audio output signal V_{OUT} to take on a non-zero value driven by class-D audio output stage 42. After completion of step 82, method 70 may end.

Although FIGURE 10 discloses a particular number of steps to be taken with respect to method 70, method 70 may be executed with greater or fewer steps than those depicted in FIGURE 10. In addition, although FIGURE 10 discloses a certain order of steps to be taken with respect to method 70, the steps comprising method 70 may be completed in any suitable order.

Method 70 may be implemented using personal audio device 1 or any other system operable to implement method 70. In certain embodiments, method 70 may be implemented partially or fully in software and/or firmware embodied in computer-readable media and executable by a controller.

FIGURE 11 is a block diagram of selected components of the example amplifier 16 of FIGURE 3 modified to include an offset calibration circuit 126, in accordance with embodiments of the present disclosure. As shown in FIGURE 11, to facilitate functionality of offset calibration circuit 126, amplifier 16 may also be modified to include switches 120 and switches 121. Although not explicitly shown in FIGURE 11, switches 120 and switches 121 may be controlled by offset calibration circuit 126. In operation, offset calibration circuit 126 may cause amplifier 16 to enter an offset calibration mode to perform offset calibration between Class-D audio output stage 42 and Class-AB audio output stage 44. In such offset calibration mode, offset calibration circuit 126 may deactivate switches 120 to decouple the modulator input of modulator 122 from the output of first stage 22, and decouple the input of Class-AB audio output stage 44 from the output of first stage 22. In addition, in such offset calibration mode, offset calibration circuit 126 may activate switches 121 to couple output of Class-AB audio

output stage 44 to the modulator input of modulator 122. Furthermore, in such offset calibration mode, offset calibration circuit 126 may apply a common-mode voltage V_{cm} to the input of Class-AB audio output stage 44, receive a calibration signal V_{MOD} from the output of modulator 122 generated in response to common-mode voltage V_{cm}, and based thereon may modify one or more parameters of modulator 122 to compensate for an offset (e.g., a direct current offset) between Class-D audio output stage 42 and Class-AB audio output stage 44 indicated by calibration signal V_{MOD}.

FIGURE 12 is a block diagram of selected components of the example amplifier 116 of FIGURE 3 modified to include a gain calibration circuit 128, in accordance with embodiments of the present disclosure. As shown in FIGURE 12, to facilitate functionality of gain calibration circuit 128, amplifier 16 may also be modified to include switches 120. Although not explicitly shown in FIGURE 12, switches 120 may be controlled by gain calibration circuit 128. In operation, gain calibration circuit 128 may cause amplifier 16 to enter a gain calibration mode to perform gain calibration between Class-D audio output stage 42 and Class-AB audio output stage 44. In such gain calibration mode, gain calibration circuit 128 may deactivate switches 120 to decouple the modulator input of modulator 122 from the output of first stage 22, and decouple the input of Class-AB audio output stage 44 from the output of first stage 22. In addition, in the gain calibration mode, gain calibration circuit 128 may apply a test signal V_{TEST} to the input of Class-AB audio output stage 44 and test signal $-V_{TEST}$ of opposite phase of test signal V_{TEST} to the input of Class-D audio output stage 42. Audio output voltage V_{OUT} generated from the application of such test signals may be a value indicative of a gain mismatch between Class-D audio output stage 42 and Class-AB audio output stage 44. Due to the presence of signal feedback network 26, such audio output voltage V_{OUT} may be fed back to the input of amplifier 16 such that first stage 22 generates intermediate signal V_{INT} as a calibration signal indicative of the gain mismatch between Class-D audio output stage 42 and Class-AB audio output stage 44. Gain calibration circuit 128 may receive such calibration signal from the output of first stage 22, and based thereon, may modify one or more parameters of the Class-AB audio output stage 44 (e.g., modify a gain of Class A-B audio stage 44 by modifying the resistances of signal feedback network

50) to compensate for a difference in respective gains of Class-D audio output stage 42 and Class-AB audio output stage 44.

Although FIGURES 11 and 12 depict offset calibration circuit 126 and gain calibration circuit 128 as separate circuits, in some embodiments offset calibration circuit 126 and gain calibration circuit 128 may be combined into a single calibration circuit capable of performing both offset calibration and gain calibration, as described herein.

As used herein, when two or more elements are referred to as "coupled" to one another, such term indicates that such two or more elements are in electronic communication or mechanical communication, as applicable, whether connected indirectly or directly, with or without intervening elements.

This disclosure encompasses all changes, substitutions, variations, alterations, and modifications to the exemplary embodiments herein that a person having ordinary skill in the art would comprehend. Similarly, where appropriate, the appended claims encompass all changes, substitutions, variations, alterations, and modifications to the exemplary embodiments herein that a person having ordinary skill in the art would comprehend. Moreover, reference in the appended claims to an apparatus or system or a component of an apparatus or system being adapted to, arranged to, capable of, configured to, enabled to, operable to, or operative to perform a particular function encompasses that apparatus, system, or component, whether or not it or that particular function is activated, turned on, or unlocked, as long as that apparatus, system, or component is so adapted, arranged, capable, configured, enabled, operable, or operative.

All examples and conditional language recited herein are intended for pedagogical objects to aid the reader in understanding the invention and the concepts contributed by the inventor to furthering the art, and are construed as being without limitation to such specifically recited examples and conditions. Although embodiments of the present inventions have been described in detail, it should be understood that various changes, substitutions, and alterations could be made hereto without departing from the spirit and scope of the disclosure.

WHAT IS CLAIMED IS:

1. An amplifier comprising:

a plurality of stages comprising at least:

a first stage configured to receive an input signal at an amplifier input and generate at a first stage output an intermediate signal which is a function of the input signal; and

a final output stage configured to generate an output signal which is a function of the intermediate signal at an amplifier output, the final output stage comprising:

a first path comprising:

a modulator having a modulator input for receiving the intermediate signal and configured to generate at a modulator output a modulated signal from the intermediate signal; and

a plurality of output switches configured to generate the output signal from the modulated signal when the first path is selected to generate the output signal; and

a second path having a second path input for receiving the intermediate signal configured to generate at a second path output the output signal from the intermediate signal when the second path is selected to generate the output signal; and

a calibration subsystem configured to, in a calibration mode:

decouple the modulator input from the first stage output;

couple the second path output to the modulator input;

apply a common-mode voltage to the second path input;

receive a calibration signal from the modulator output generated in response to the common-mode voltage; and

modify one or more parameters of the modulator to compensate for an offset between the first path and the second path indicated by the calibration signal.

2. The amplifier of Claim 1, wherein the first path comprises a Class D audio output stage.

3. The amplifier of Claim 1, wherein the second path comprises a Class AB audio output stage.

4. An amplifier comprising:

a plurality of stages comprising at least:

a first stage configured to receive an input signal at an amplifier input and generate at a first stage output an intermediate signal which is a function of the input signal;

a final output stage configured to generate an output signal which is a function of the intermediate signal at an amplifier output, the final output stage comprising:

a first path comprising:

a modulator having a modulator input for receiving the intermediate signal and configured to generate at a modulator output a modulated signal from the intermediate signal; and

a plurality of output switches configured to generate the output signal from the modulated signal when the first path is selected to generate the output signal; and

a second path having a second path input for receiving the intermediate signal configured to generate at a second path output the output signal from the intermediate signal when the second path is selected to generate the output signal; and

a signal feedback network coupled between the amplifier output and the amplifier input; and

a calibration subsystem configured to, in a calibration mode:

decouple the modulator input from the first stage output;

decouple the second path from the first stage output;

apply a first test signal to the modulator input;

apply a second test signal to the second path input, wherein the second test signal is of opposite phase as the first test signal;

receive a calibration signal from the first stage output generated in response to the first test signal and the second test signal; and

modify one or more parameters of the second path to compensate for a difference in respective gains of the first path and the second path indicated by the calibration signal.

5. The amplifier of Claim 4, wherein the first path comprises a Class D audio output stage.

6. The amplifier of Claim 4, wherein the second path comprises a Class AB audio output stage.

7. The amplifier of Claim 4, wherein the calibration subsystem is further configured to, in a second calibration mode:

decouple the modulator input from the first stage output;

couple the second path output to the modulator input;

apply a common-mode voltage to the second path input;

receive a second calibration signal from the modulator output generated in response to the common-mode voltage; and

modify one or more parameters of the modulator to compensate for an offset between the first path and the second path indicated by the second calibration signal.

8. A method comprising, in a calibration mode of an amplifier comprising a plurality of stages comprising at least a first stage configured to receive an input signal at an amplifier input and generate at a first stage output an intermediate signal which is a function of the input signal, and a final output stage configured to generate an output signal which is a function of the intermediate signal at an amplifier output, and wherein the final output stage comprises a first path comprising a modulator having a modulator input for receiving the intermediate signal and configured to generate at a modulator

output a modulated signal from the intermediate signal and a plurality of output switches configured to generate the output signal from the modulated signal when the first path is selected to generate the output signal wherein the final output stage further comprises a second path having a second path input for receiving the intermediate signal configured to generate at a second path output the output signal from the intermediate signal when the second path is selected to generate the output signal:

decoupling the modulator input from the first stage output;

coupling the second path output to the modulator input;

applying a common-mode voltage to the second path input;

receiving a calibration signal from the modulator output generated in response to the common-mode voltage; and

modifying one or more parameters of the modulator to compensate for an offset between the first path and the second path indicated by the calibration signal.

9. The method of Claim 8, wherein the first path comprises a Class D audio output stage.

10. The method of Claim 8, wherein the second path comprises a Class AB audio output stage.

11. A method comprising, in a calibration mode of an amplifier comprising a plurality of stages comprising at least a first stage configured to receive an input signal at an amplifier input and generate at a first stage output an intermediate signal which is a function of the input signal and a final output stage configured to generate an output signal which is a function of the intermediate signal at an amplifier output, and wherein the final output stage comprises a first path comprising a modulator having a modulator input for receiving the intermediate signal and configured to generate at a modulator output a modulated signal from the intermediate signal and a plurality of output switches configured to generate the output signal from the modulated signal when the first path is selected to generate the output signal wherein the final output stage further comprises a second path having a second path input for receiving the intermediate signal configured to

generate at a second path output the output signal from the intermediate signal when the second path is selected to generate the output signal:

decoupling the modulator input from the first stage output;

decoupling the second path from the first stage output;

applying a first test signal to the modulator input;

applying a second test signal to the second path input, wherein the second test signal is of opposite phase as the first test signal;

receiving a calibration signal from the first stage output generated in response to the first test signal and the second test signal; and

modifying one or more parameters of the second path to compensate for a difference in respective gains of the first path and the second path indicated by the calibration signal.

12. The method of Claim 11, wherein the first path comprises a Class D audio output stage.

13. The method of Claim 11, wherein the second path comprises a Class AB audio output stage.

14. The method of Claim 11, further comprising, in a second calibration mode of the amplifier:

decoupling the modulator input from the first stage output;

coupling the second path output to the modulator input;

applying a common-mode voltage to the second path input;

receiving a second calibration signal from the modulator output generated in response to the common-mode voltage; and

modifying one or more parameters of the modulator to compensate for an offset between the first path and the second path indicated by the second calibration signal.

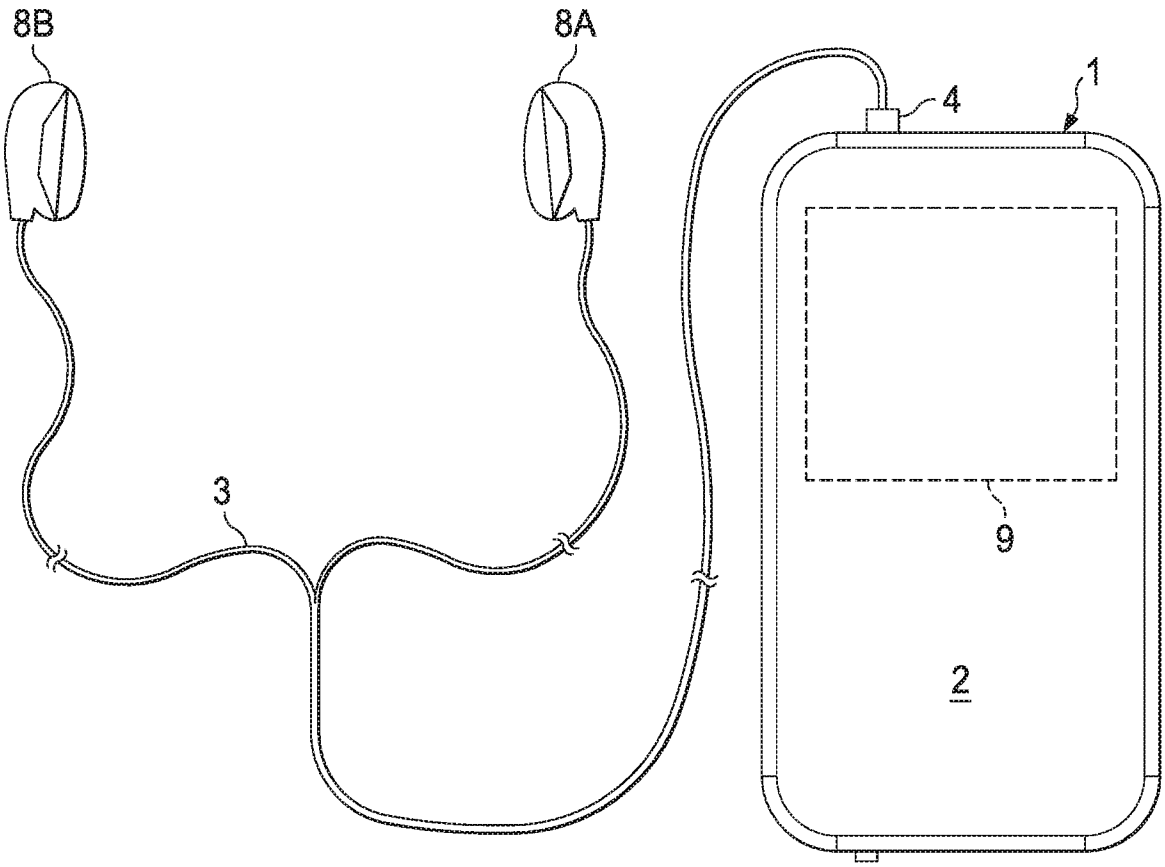
8B
8A
4
1
3
9
2

FIG. 1

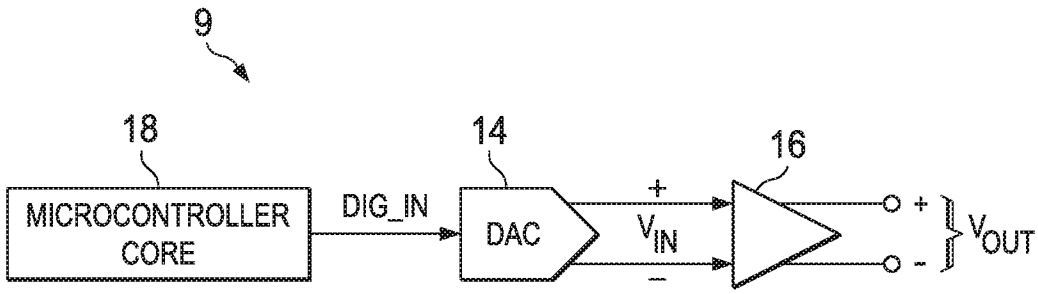
9
18
14
16
MICROCONTROLLER CORE
DIG_IN
DAC
+
V_{IN}
−
+
-
V_{OUT}

FIG. 2

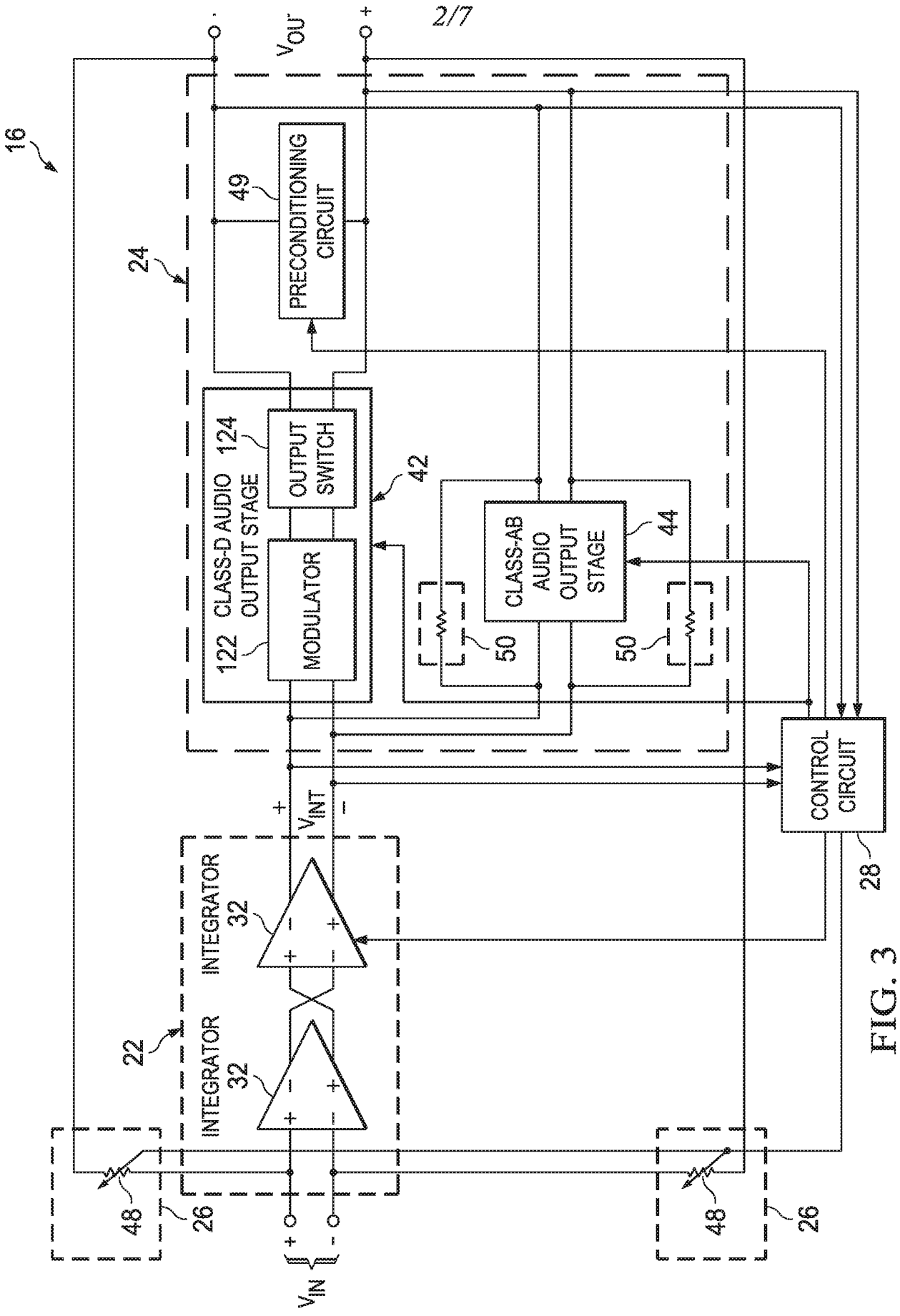
16
24
49
PRECONDITIONING CIRCUIT
V_{OUT}
122
CLASS-D AUDIO OUTPUT STAGE
MODULATOR
124
OUTPUT SWITCH
42
50
CLASS-AB AUDIO OUTPUT STAGE
44
50
CONTROL CIRCUIT
28
V_{INT}
INTEGRATOR
32
INTEGRATOR
32
22
48
26
48
26
V_{IN}

FIG. 3

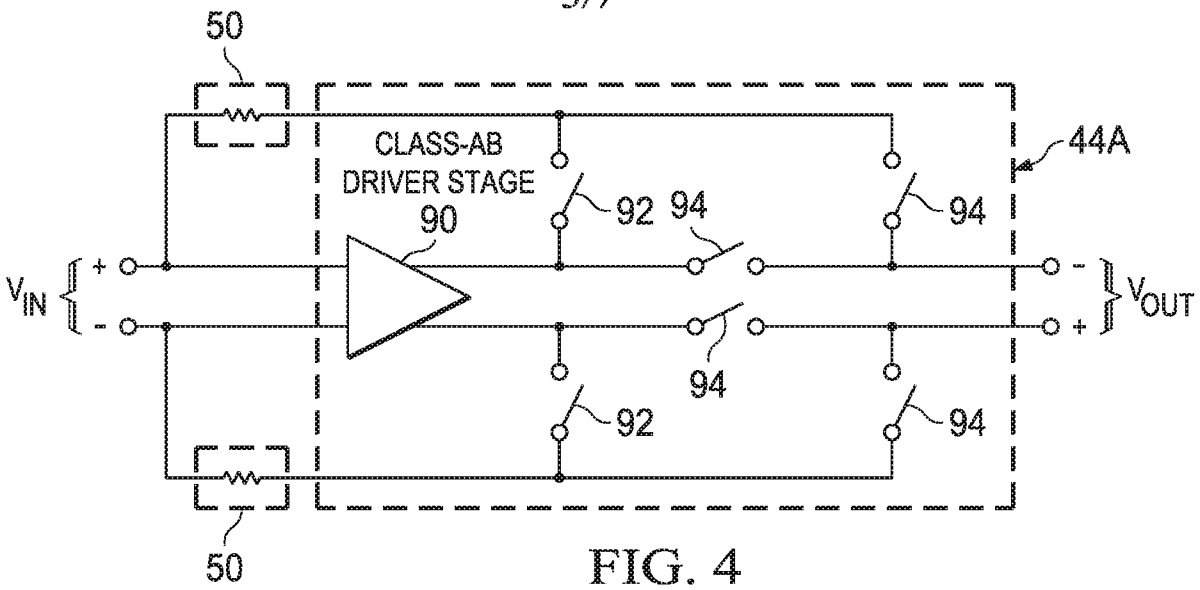
50
CLASS-AB
DRIVER STAGE
90
92
94
94
44A
V_{IN}
+
-
-
+
V_{OUT}
94
92
94
50

FIG. 4

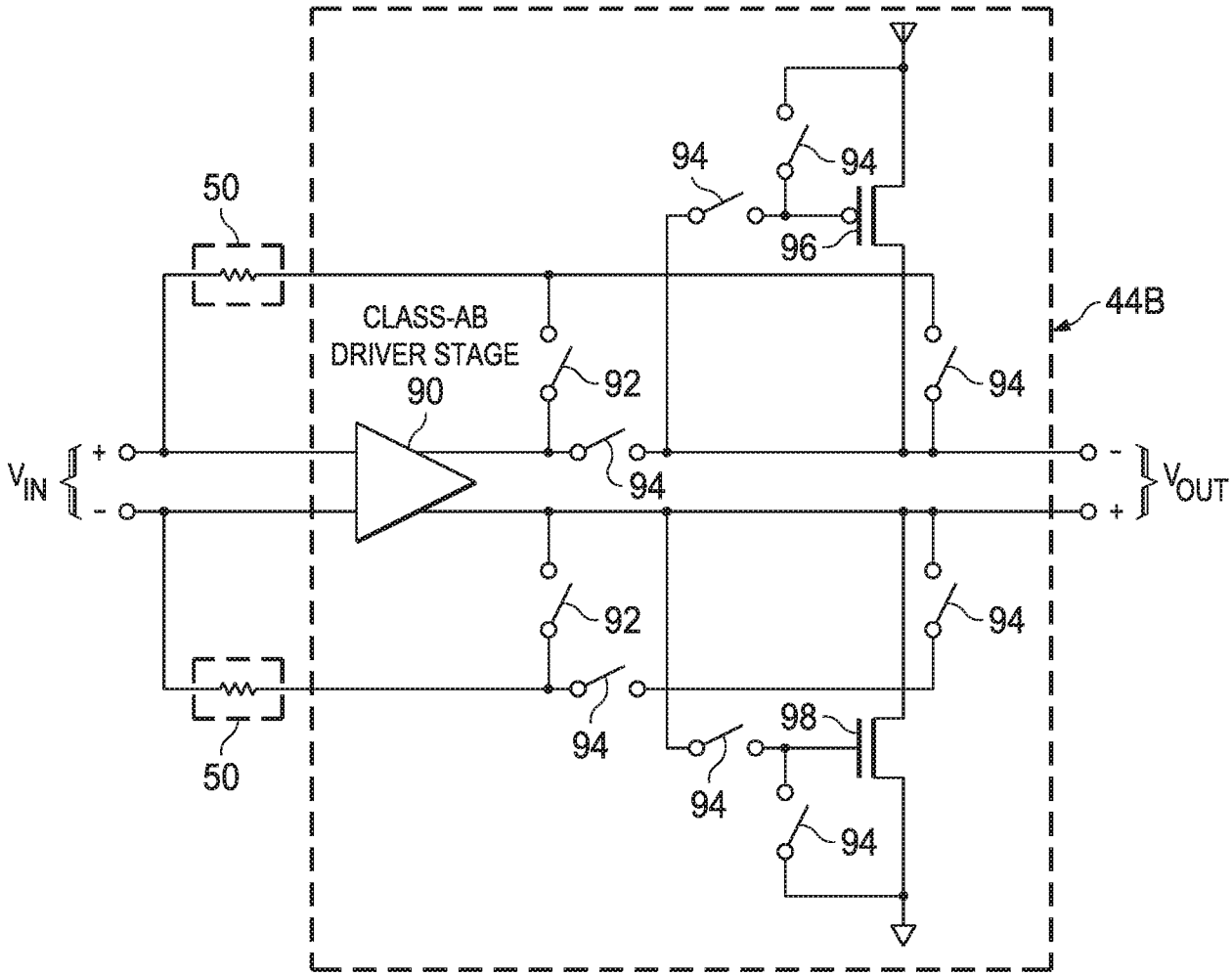
94
94
96
50
CLASS-AB
DRIVER STAGE
90
92
94
44B
V_{IN}
+
-
-
+
V_{OUT}
94
92
94
98
94
94
50

FIG. 5

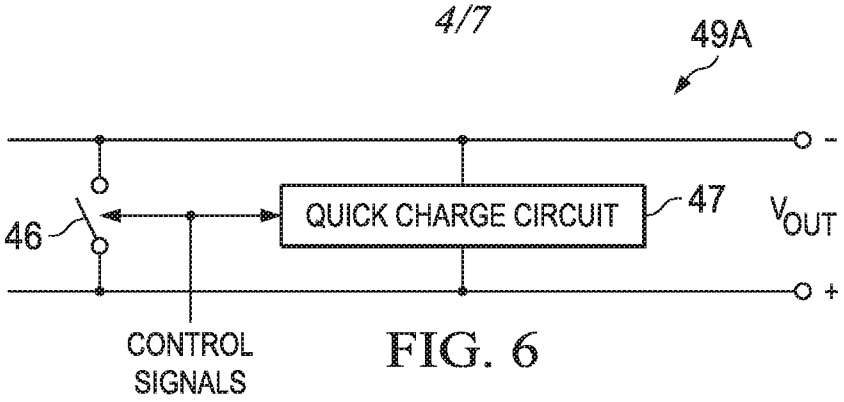

FIG. 6

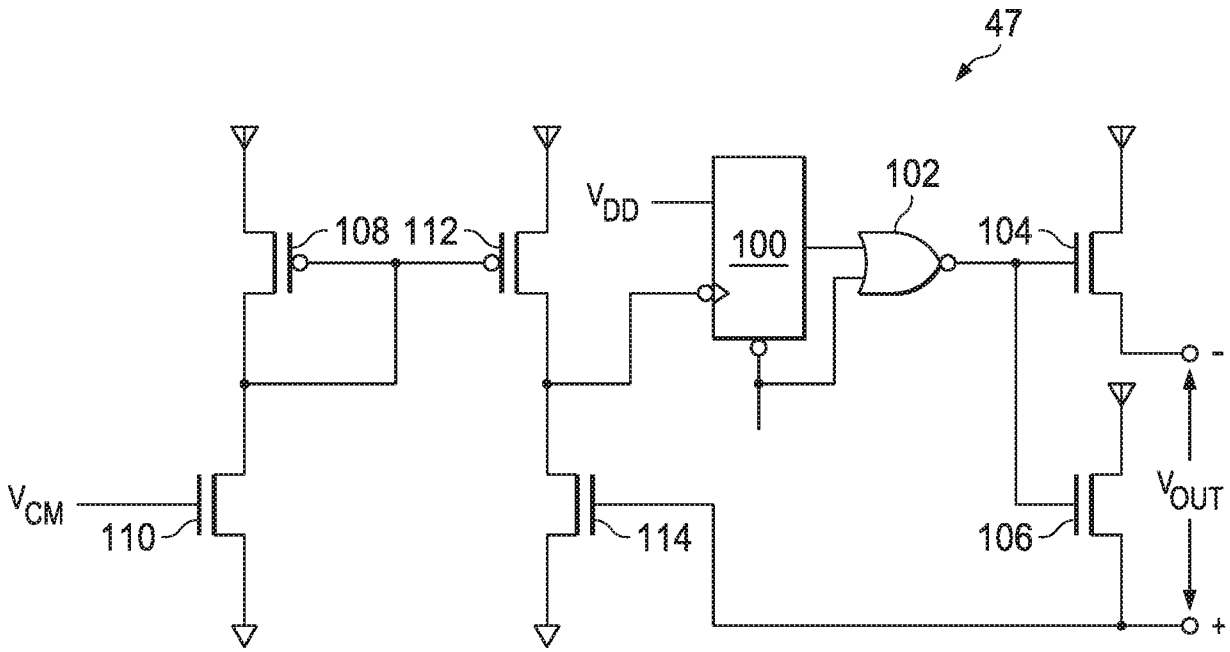

FIG. 7

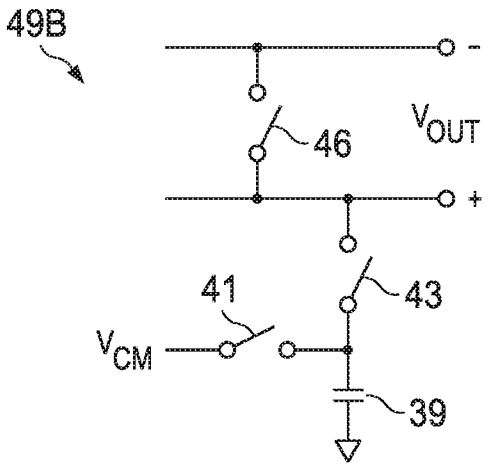

FIG. 8

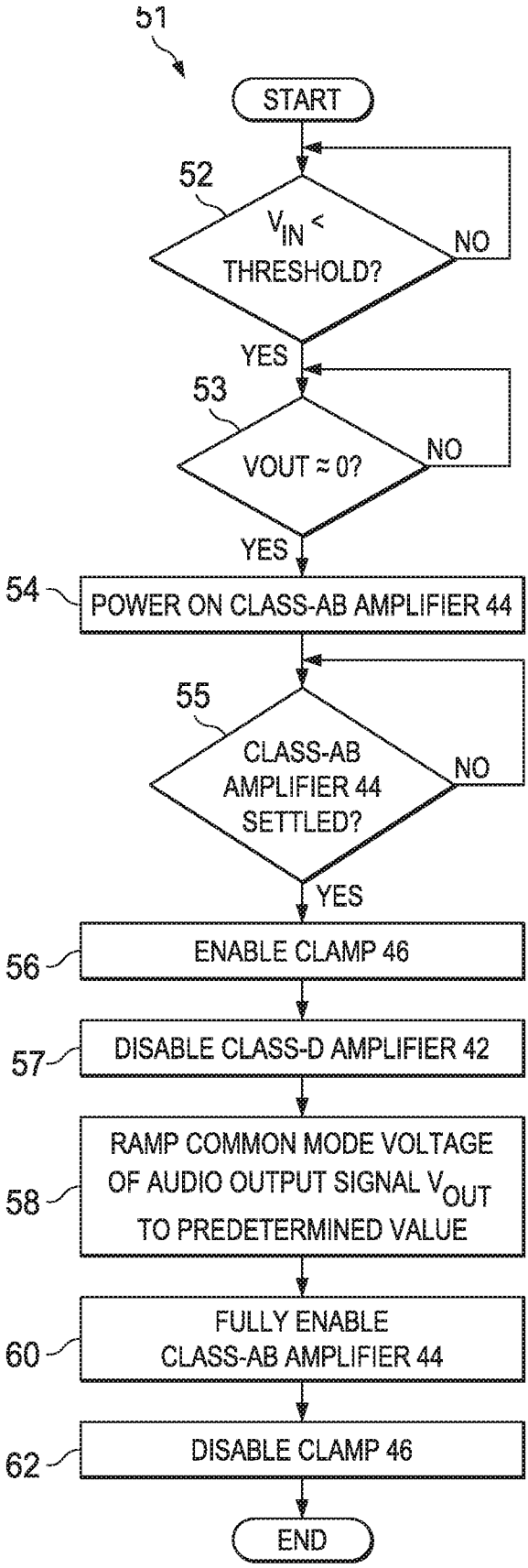
51
START
52
V_{IN} < THRESHOLD?
NO
YES
53
VOUT ≈ 0?
NO
YES
54
POWER ON CLASS-AB AMPLIFIER 44
55
CLASS-AB AMPLIFIER 44 SETTLED?
NO
YES
56
ENABLE CLAMP 46
57
DISABLE CLASS-D AMPLIFIER 42
58
RAMP COMMON MODE VOLTAGE OF AUDIO OUTPUT SIGNAL V_{OUT} TO PREDETERMINED VALUE
60
FULLY ENABLE CLASS-AB AMPLIFIER 44
62
DISABLE CLAMP 46
END

FIG. 9

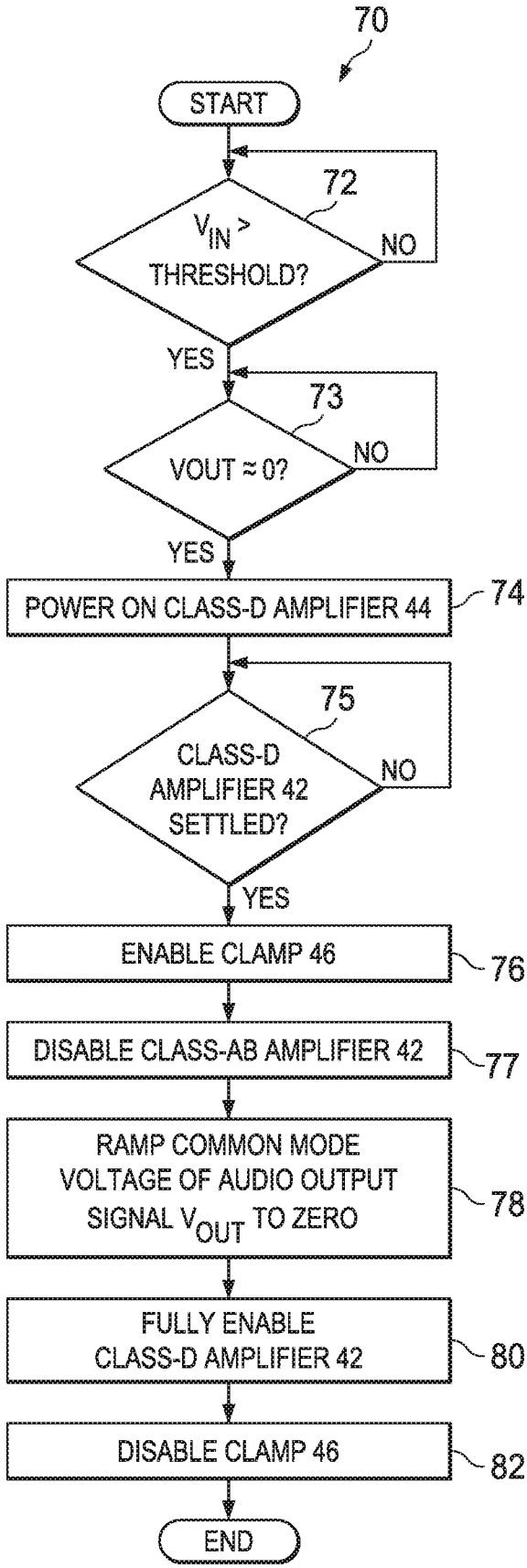
70
START
72
V_{IN} > THRESHOLD?
NO
YES
73
VOUT ≈ 0?
NO
YES
74
POWER ON CLASS-D AMPLIFIER 44
75
CLASS-D AMPLIFIER 42 SETTLED?
NO
YES
76
ENABLE CLAMP 46
77
DISABLE CLASS-AB AMPLIFIER 42
78
RAMP COMMON MODE VOLTAGE OF AUDIO OUTPUT SIGNAL V_{OUT} TO ZERO
80
FULLY ENABLE CLASS-D AMPLIFIER 42
82
DISABLE CLAMP 46
END

FIG. 10

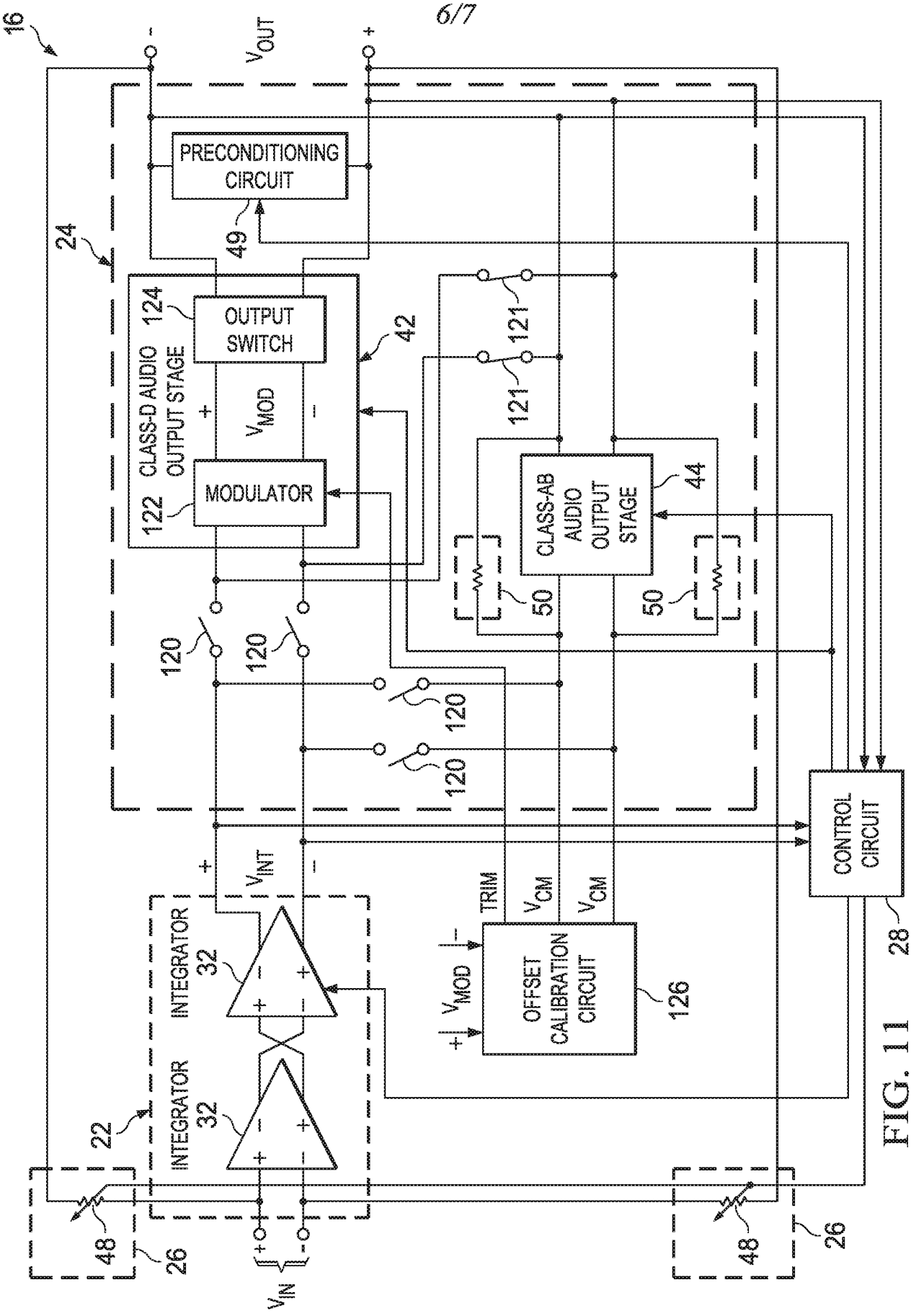
16
V_{OUT}
PRECONDITIONING CIRCUIT
49
24
CLASS-D AUDIO OUTPUT STAGE
124
OUTPUT SWITCH
V_{MOD}
122
MODULATOR
42
121
121
CLASS-AB AUDIO OUTPUT STAGE
44
50
50
120
120
120
120
V_{INT}
INTEGRATOR
32
INTEGRATOR
32
22
TRIM
V_{CM}
V_{CM}
V_{MOD}
OFFSET CALIBRATION CIRCUIT
126
CONTROL CIRCUIT
28
48
26
48
26
V_{IN}

FIG. 11

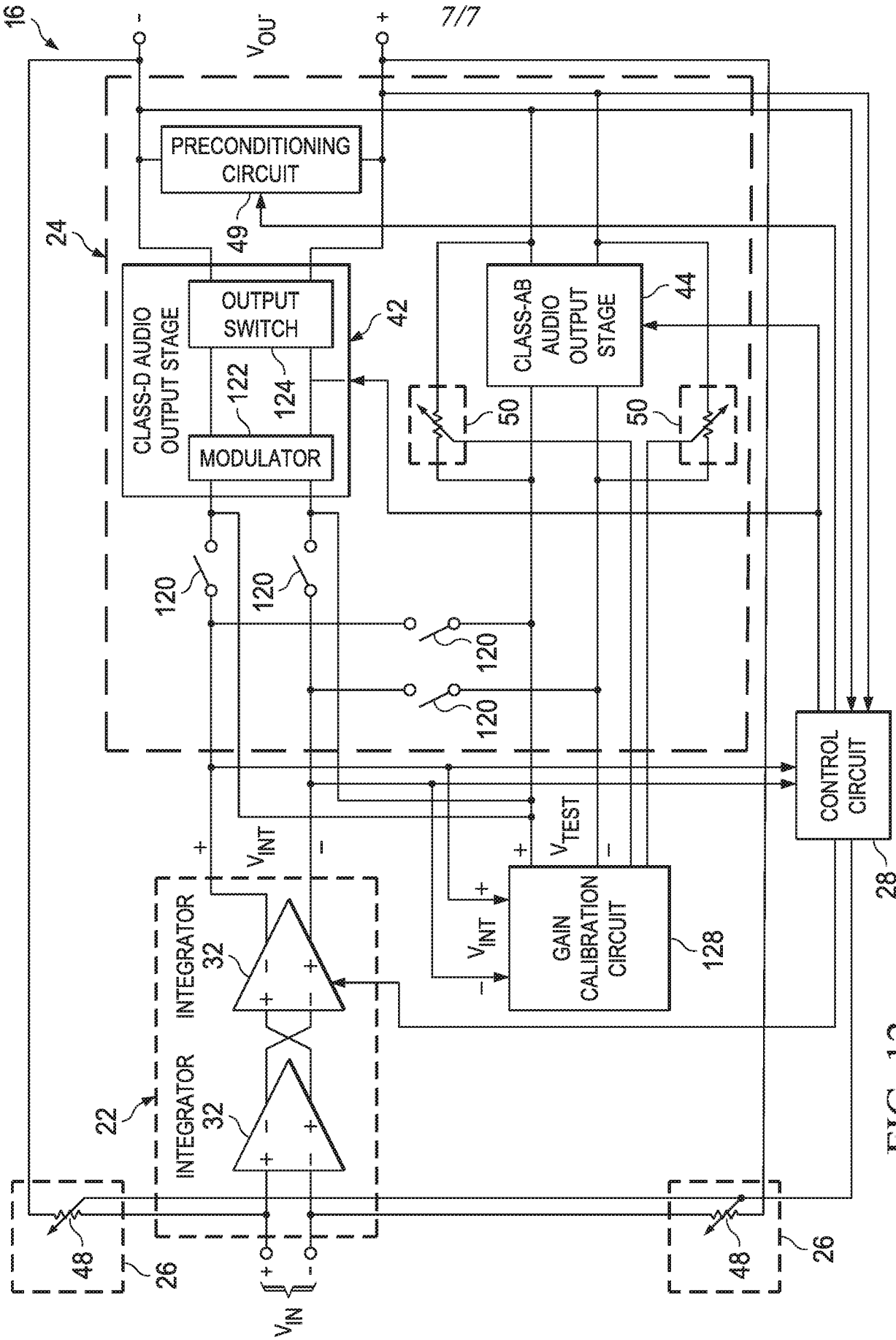
16
V_{OUT}
PRECONDITIONING CIRCUIT
49
24
CLASS-D AUDIO OUTPUT STAGE
OUTPUT SWITCH
42
122
124
MODULATOR
CLASS-AB AUDIO OUTPUT STAGE
44
50
50
120
120
120
120
CONTROL CIRCUIT
28
V_{INT}
V_{TEST}
V_{INT}
GAIN CALIBRATION CIRCUIT
128
INTEGRATOR
32
INTEGRATOR
32
22
48
26
48
26
V_{IN}

FIG. 12

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2018/027763

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F1/02 H03F3/21 H03F3/72 H03F3/217
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008/075194 A1 (RAVI ASHOKE [US] ET AL) 27 March 2008 (2008-03-27) paragraph [0062] - paragraph [0064]; figure 11	4-6, 11-13
A	US 2008/310046 A1 (MENEGOLI PAOLO [US] ET AL) 18 December 2008 (2008-12-18) paragraph [0073] - paragraph [0081]; figure 2	1-3,8-10

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 July 2018	26/07/2018

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Lorenzo, Carlos

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/027763

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☒ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-14

An amplifier comprising: a plurality of stages comprising at least: a first stage configured to receive an input signal at an amplifier input and generate at a first stage output an intermediate signal which is a function of the input signal; and a final output stage configured to generate an output signal which is a function of the intermediate signal at an amplifier output, the final output stage comprising: a first path comprising: a modulator having a modulator input for receiving the intermediate signal and configured to generate at a modulator output a modulated signal from the intermediate signal; and a plurality of output switches configured to generate the output signal from the modulated signal when the first path is selected to generate the output signal; and a second path having a second path input for receiving the intermediate signal configured to generate at a second path output the output signal from the intermediate signal when the second path is selected to generate the output signal; and a calibration subsystem.

1.1. claims: 1-3, 8-10

An amplifier comprising: a plurality of stages comprising at least: a first stage configured to receive an input signal at an amplifier input and generate at a first stage output an intermediate signal which is a function of the input signal; and a final output stage configured to generate an output signal which is a function of the intermediate signal at an amplifier output, the final output stage comprising: a first path comprising: a modulator having a modulator input for receiving the intermediate signal and configured to generate at a modulator output a modulated signal from the intermediate signal; and a plurality of output switches configured to generate the output signal from the modulated signal when the first path is selected to generate the output signal; and a second path having a second path input for receiving the intermediate signal configured to generate at a second path output the output signal from the intermediate signal when the second path is selected to generate the output signal; and a calibration subsystem configured to, in a calibration mode: decouple the modulator input from the first stage output; couple the second path output to the modulator input; apply a common-mode voltage to the second path input; receive a calibration signal from the modulator output generated in response to the common-mode voltage; and modify one or more parameters of the modulator to compensate for an offset between the first path and the second path indicated by the calibration signal.

1.2. claims: 4-7, 11-14

An amplifier comprising: a plurality of stages comprising at least: a first stage configured to receive an input signal at an amplifier input and generate at a first stage output an intermediate signal which is a function of the input signal; a final output stage configured to generate an output signal which is a function of the intermediate signal at an amplifier output, the final output stage comprising: a first path comprising: a modulator having a modulator input for receiving the intermediate signal and configured to generate at a modulator output a modulated signal from the intermediate signal; and a plurality of output switches configured to generate the output signal from the modulated signal when the first path is selected to generate the output signal; and a second path having a second path input for receiving the intermediate signal configured to generate at a second path output the output signal from the intermediate signal when the second path is selected to generate the output signal; and a signal feedback network coupled between the amplifier output and the amplifier input; and a calibration subsystem configured to, in a calibration mode: decouple the modulator input from the first stage output; decouple the second path from the first stage output; apply a first test signal to the modulator input; apply a second test signal to the second path input, wherein the second test signal is of opposite phase as the first test signal; receive a calibration signal from the first stage output generated in response to the first test signal and the second test signal; and modify one or more parameters of the second path to compensate for a difference in respective gains of the first path and the second path indicated by the calibration signal.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2018/027763

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008075194 A1	27-03-2008	NONE	
US 2008310046 A1	18-12-2008	NONE	