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(54) Title: VECTOR PROCESSOR FOR PROCESSING RECURRENT EQUATIONS AT A HIGH SPEED

(57) Abstract

An improved vector processor for processing a modified recurrent equation: $a_i = a_{i-2} \times b_{i-1} \times b_i + b_i \times c_{i-1} + c_i$, where i is an integer: $i = 1, 2, 3, ..., n$, at a high speed. The vector processor includes a data distribution circuit (40a, 40b), at least one odd term calculation circuit (10A, 10AA), and at least one even term calculation circuit (10B, 10BB). The odd term calculation circuit calculates odd terms of the modified recurrent equation: $a_j = (a_{j-2} \times b_{j-1} \times b_j) + (b_j \times c_{j-1}) + c_j$, where j is an odd integer. The even term calculation circuit calculates even terms of the recurrent equations: $a_k = (a_{k-2} \times b_{k-1} \times b_k) + (b_k \times c_{k-1}) + c_k$, where k is an even integer. The data distribution circuit receives an initial, data a_0 and input vector (operand) data (b_i) and (c_i), and distributes that data to the odd and even term calculation circuits in a predetermined manner so that the above odd and even terms are calculated.

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DESCRIPTION

TITLE OF THE INVENTION

Vector Processor for Processing Recurrent Equations at a High Speed

5   TECHNICAL FIELD

The present invention relates to a data processing system, more particularly, to a vector processor for processing recurrent equations at a high speed.

BACKGROUND ART

10   Recent remarkable advances in computer technologies have improved the operation speed of supercomputers by providing, for example, vector processors. These vector processors are used to carry out scientific calculations, such as a numerical solution of linear

15 equations or a numerical solution of differential equations, etc., at a very high speed.

In scientific technical calculations, the following recurrent operational algorithm (or recurrent equation) is frequently used to solve first order linear equations

20 by a numerical solution, or differential equations by a difference method, etc.

$$a_i = a_{i-1} \times b_i + c_i \qquad \qquad \dots (1)$$
$$\text{where, } i = 1, 2, 3, \dots, n$$

This operational algorithm (1) shows the recurrent

25 relationship between a datum a_i and a datum a_{i-1}. In general, the operation of the above recurrent equation is not suitable for calculations by the vector processor at a high speed, since the datum a_{i-1} is used again to calculate the datum a_i, i.e., the term a_i must be

30 calculated after calculation of the term a_{i-1}. Therefore, prior art vector processors cannot calculate the recurrent equations at a high speed. The prior art vector processor used for handling recurrent equation will be described later with reference to the drawings.

35   Nevertheless, there is a strong demand for a capability to calculate the recurrent equation at a high

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speed by using a vector processor, since many recurrent equations are used in the scientific technical calculation field.

DISCLOSURE OF THE INVENTION

5   An object of the present invention is to provide a vector processor which can process recurrent equations at a high speed.

Another object of the present invention is to provide a vector processor having a simple circuit
10   construction which can be easily formed.

According to the present invention, there is provided a vector processor including a vector instruction control unit for controlling vector instructions, a vector storage access unit for accessing input vector
15   data and calculated data to a main storage unit, a vector calculation unit for calculating vector data under the control of the vector instruction unit, and a data distribution unit for transferring data between the vector data access unit and the vector calculation unit,
20   characterized in that the vector processor comprises a vector calculation unit including at least one odd term calculation circuit and at least one even term calculation circuit, and a data distribution unit operatively connected to and cooperative with said vector calcu-
25   lation unit, to process a modified recurrent equation. Each odd term calculation circuit is formed to calculate odd terms of the modified recurrent equation and includes an adding circuit, a multiplication circuit, at least one data storage circuit holding a calculated odd
30   term, and at least one feedback line for feeding back the calculated odd term to the multiplication circuit and/or the adding circuit through the data storage circuit. Each even term calculation circuit is formed to calculated even terms of the recurrent equation and
35   includes another adding circuit, another multiplication circuit, at least one another data storage circuit holding a calculated even term, and at least one another

feedback line for feeding back the calculated even term
to another multiplication circuit and/or another adding
circuit through another data storage circuit. The data
distribution unit includes a first data setter for

5   outputting zero, a second data setter for outputting
one, first to sixth selectors for selecting input
operands using for calculating the recurrent equation,
constant data 0 and 1 from the setters, and the
calculated odd and even terms, and a selector control

10 circuit for controlling the selectors in a predetermined
manner defined by the modified recurrent equation, to
supply selected data to the odd and even term calcu-
lation circuits.

The recurrent equation expressed by the formula (1)

15 can be modified as shown in the following formula, when
a first-order development is applied:

$$\begin{aligned}
a_i &= a_{i-1} \times b_i + c_i \\
&= \{(a_{i-2} \times b_{i-1}) + c_{i-1}\} \times b_i + c_i \\
&= a_{i-2} \times b_{i-1} \times b_i + b_i \times c_{i-1} + c_i
\end{aligned}$$

$$\dots \dots (2)$$

When an index i is even, for example, an even
index $k = 2$, 4, and 6.

$$\begin{aligned}
a_2 &= a_6 \times b_1 \times b_2 + b_2 \times c_1 + c_2 \\
a_4 &= a_2 \times b_3 \times b_4 + b_4 \times c_3 + c_4 \\
a_6 &= a_4 \times b_5 \times b_6 + b_6 \times c_5 + c_6 \quad \dots (3)
\end{aligned}$$

When an index i is odd, for example, an odd index j
= 1, 3, 5, and 7.

$$\begin{aligned}
a_1 &= a_0 \times b_1 \times 1 + 1 \times c_1 + 0 \\
a_3 &= a_1 \times b_2 \times b_3 + b_3 \times c_2 + c_3 \\
a_5 &= a_3 \times b_4 \times b_5 + b_5 \times c_4 + c_5 \\
a_7 &= a_5 \times b_6 \times b_7 + b_7 \times c_6 + c_7 \quad \dots (4)
\end{aligned}$$

Note that there is no direct recurrent relationship
between the terms a_2 and a_0 , a_4 and a_2 , and a_6 and a_4.
Similarly, there is no direct recurrent relationship

35 between the terms a_3 and a_1 , a_5 and a_3 , and a_7 and a_5.
Accordingly, the odd term calculation circuit can
calculate odd terms a_j without a delay by the direct

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recurrence, and the even term calculation circuit can calculate even terms a_k without a delay by the direct recurrence, and thus contribute to a high speed calculation of the recurrent equations.

5   BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a high speed data processing system which includes a vector processor of the present invention;

Figure 2 is a block diagram of a general vector
10 processor used in the data processing system shown in Fig. 1;

Figure 3 is a circuit diagram of a prior art vector processor;

Figure 4 is an operation timing chart of the vector
15 processor shown in Fig 3;

Figure 5 is a circuit diagram of an embodiment of a vector processor in accordance with the present invention;

Figure 6 is an operation timing chart of the vector
20 processor shown in Fig. 5;

Figure 7 is a circuit diagram of another embodiment of a vector processor in accordance with the present invention; and,

Figure 8 is an operation timing chart of the vector
25 processor shown in Fig. 7.

BEST MODE OF CARRYING OUT THE INVENTION

Before describing preferred embodiments of a vector processor in accordance with the present invention, a high speed data processing system in which the vector
30 processor is provided will be described with reference to Fig. 1.

In Fig. 1, the high speed data processing system consists of a main storage unit (MSU) 1, a main storage control unit (MSCU) 1, an input/output (I/O) processing
35 unit 3, a scalar data processing unit (scalar processor) 4, and a vector data processing unit (vector processor) 5. The I/O processing unit 3 inputs data to

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be calculated and outputs data calculated at the scalar
processor 4 and/or the vector processor 5. The MSU 1
stores the input data and the calculated data. The
scalar processor 4 controls all calculations. When
5 operation commands concern a scalar operation, the
scalar processor 4, per se, executes a scalar data
calculation. When operation commands concern a vector
operation, the scalar processor 4 transfers control to
the vector processor 5 to carry out a vector calculation
10 at the vector processor 5. Namely, the vector
processor 5 is triggered by the scalar processor 4 when
the vector calculation is requested, and carries out the
vector calculation. The MSCU 2 controls the data flow
among the MSU 1, the I/O processing unit 3, the scalar
15 processor 4, and the vector processor 5.

A general configuration of the vector processor 5
shown in Fig. 1 is shown in Fig. 2. In Fig. 2, the
vector processor 5 includes a vector instruction control
unit (VICU) 51 having a decoder and a control register,
20 a vector storage access unit (VSAU) 52 having a vector
address generator, an access data processor and a vector
register unit, a data distribution unit 54, and a vector
calculation portion having an adding and subtracting
unit 55, a multiplication unit 56, and a division
25 unit 57. The VICS 51 receives data control instructions
from the scalar processor 4. The control register saves
control data of the data control instructions. The
decoder decodes the data control instructions. The
VSAU 52 transfers data between the MSU 1 and the vector
30 calculation portion through the MSCU 2 and the data
distribution unit 54. The vector address generator
generates addresses for accessing data in the MSU 1 in
accordance with the decoded· instructions. The access
data processor controls data between the MSU 1 and the
35 vector register unit. Data to be used for a vector
calculation are once stored in the vector register unit.
Also, data calculated at the vector calculation portion

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are stored in the vector register unit. The data
distribution unit 40 distributes the data from the
vector register unit to supply the same to the adding-
subtracting unit 55, the multiplication unit 56, and
5   the division unit 57 in accordance with the decoded
instruction. The units 55, 56, and 57 are operatively
connected to perform the vector calculation. The vector
calculated data are stored in the vector register unit
through the data distribution unit 40, thereafter, are
10   stored in the MSU 1.

A prior art of a vector processor will be described
with reference to Figs. 3 and 4. Figure 3 shows an
elementary circuit diagram for processing the recurrent
equation discussed above. Figure 4 shows an operation
15   timing chart of the vector processor of Fig. 3.

In Fig. 3, the vector processor includes a selec-
tor 30, registers 14, 15 and 16, a multiplication
circuit 17, registers 18 and 19, an adder 110, a
register 112, and a feedback line 31 connected between
20   an output terminal of the register 112 and an input
terminal of the selector 30. These circuit components
are a part of the vector calculation portion shown in
Fig. 3. The multiplication circuit 17 calculating a
term: $a_{i-1} \times b_i$. The adder 110 adds c_i and the result
25   from the multiplication circuit 17. On one hand, the
added data is fed back to the multiplication circuit 17
through the feedback line 31, the selector 30 and the
register 15 to use a next term calculation, and on other
hand, is output to the vector register unit. The
30   selector 30 outputs an initial vector data a_0 at an
initial time. The registers 14, 15, and 16, the
registers 18 and 19, and the register 112 are provided
to hold the data, respectively. The register 112 and
the feedback line 31 are provided to feed back the
35   calculated data a_i to the register 15 for calculating a
next term a_{i+1}.

Note that, since subtraction and division are not

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needed to calculate the recurrent equation, a sub-
tracting circuit and a division circuit are omitted in
Fig. 3.

5   The operation of the vector processor shown in
Fig. 3 will be described in more detail with reference
to Fig. 4.

When an integer i indicating an index of the
recurrent equation is 1, the recurrent equation is
expressed as follows:

10                    $a_1 = a_0 \times b_1 + c_1$

Thus, at the operation cycle 01, initial data c_1 ,
a_0 , and b_1 are loaded into the registers 14, 15, and 16
from the vector register unit shown in Fig. 2. Then, a
multiplication of ($a_0 \times b_1$) is carried out at the

15 multiplication circuit 17. At the operation cycle 02,
the data c_1 loaded in the register 14 is transferred to
the register 18. Also, the data calculated at the
multiplication circuit 17 is transferred to the
register 19. Thereafter, the adder 110 adds the data c_1

20 and the data stored in the register 19, to obtain the
result a_1. At the operation cycle 03, the result a_1 is
stored in the register 112, and is then output to the
vector register unit shown in Fig. 2 through the data
distribution unit 54.

25   At the operation cycle 04, the next vector data b_2
and c_2 are loaded into the registers 16 and 14 through
the vector register unit. At the same time, the data a_1
stored in the register 112 is loaded into the regis-
ter 15 through the feedback line 31 and the selector 30.

30 During the operation cycles 04 - 06, a calculation of a
next term: $a_2 = a_1 \times b_2 + c_2$ is carried out.

Similarly, during the operation cycles 07 = 09, a
calculation of a term: $a_3 = a_2 \times b_3 + c_3$ is carried
out. During the operation cycles 10 - 12, a calculation
35 of a term: $a_4 = a_3 \times b_4 + c_4$ is carried out. During
the operation cycles 13 - 15, a calculation of a term:
$a_5 = a_4 \times b_5 + c_5$ is carried out.

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As described above, a calculation time for ob-
taining one term a_i requires three operation cycles. If
100 terms of vector processing are required, 300 oper-
ation cycles are needed to obtain calculated data of 100
5 recurrent equations. Accordingly, a high speed oper-
ation for calculating the recurrent equations, in
particular, for high order recurrent equations, can not
be achieved by the prior art vector processor.

The above defect depends upon a recurrence rela-
10 tionship wherein a calculation of a term a_i must be
carried out after a calculation of a just previous
term a_{i-1}. Thus, the prior art vector processor is made
idle in order to calculate the just previous term before
proceeding to a calculation of a next term. Therefore,
15 even though the vector processor correctly solves the
above recurrent equation, the vector processor still
suffers from the above described low speed operation.

The present invention solves the above defect by
modifying the recurrent equation.

20 The recurrent equation described above can be
modified as follows:

$$a_i = a_{i-1} \times b_i + c_i$$
$$= (a_{i-2} \times b_{i-1} + c_{i-1}) \times b_i + c_i$$
$$= (a_{i-2} \times b_{i-1} \times b_i) + b_i \times c_{i-1} + c_i$$
$$\cdots\cdots (2)$$

where, i is an integer indicating an
index, $i = 1, 2, 3, \ldots , n$
a_i are calculated vector data,
b_i are input vector data, and
30   c_i are input vector data.

From the formula (2), it is recognized that there
is no direct recurrent relationship between a term a_i
and another term a_{i-2} like the direct recurrent rela-
tionship between a term a_i and another term a_{i-1}
35 discussed above. According to the above formula (2), a
calculation of the term a_i is not affected by a calcu-
lation of a just previous term a_{i-1}. The term a_{i-2} is

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already calculated two steps prior to a calculation of
the term a_i , and thus a calculation of the term a_i can
be carried out immediately without a delay in the
calculation of the just previous term a_{i-1}. But, the
above concept cannot be realized unless odd terms and
even terms are separately operated.

When an index $\underline{i}$ is even, an even index $\underline{k}$ is used,
and the above formula (2) is expressed as follows:

$$\underline{k} = 2: \quad a_2 = a_0 \times b_1 \times b_2 + b_2 \times c_1 + c_2$$
$$\underline{k} = 4: \quad a_4 = a_2 \times b_3 \times b_4 + b_4 \times c_3 + c_4$$
$$\underline{k} = 6: \quad a_6 = a_4 \times b_5 \times b_6 + b_6 \times c_5 + c_6$$
$$\vdots \qquad\qquad \vdots$$
$$\vdots \qquad\qquad \vdots$$

$$\dots \quad (3)$$

When an index $\underline{i}$ is odd, an odd index $\underline{j}$ is used, and
the above formula (1) is expressed as follows:

$$\underline{j} = 1: \quad a_1 = a_0 \times b_1 \times 1 + 1 \times c_1 + 0$$
$$\underline{j} = 3: \quad a_3 = a_1 \times b_2 \times b_3 + b_3 \times c_2 + c_3$$
$$\underline{j} = 5: \quad a_5 = a_3 \times b_4 \times b_5 + b_5 \times c_4 + c_5$$
$$\vdots \qquad\qquad \vdots$$
$$\vdots \qquad\qquad \vdots$$

$$\dots \quad (4)$$

Note that, since there is no direct recurrent
relationship between, for example, the terms a_0 and a_2 ,
the terms a_2 and a_4 , the terms a_4 and a_6 , the terms a_1
and a_3 , or the terms a_3 and a_5 , except for the terms a_0
and a_1 , a pair of terms, for example, a_3 and a_4 , can
be calculated in parallel. This enables a high speed
vector data calculation. Nevertheless, a calculation of
the terms a_3 and a_4 must be carried out after the calcu-
lation of the terms a_1 and a_2.

A first embodiment of a vector processor in accor-
dance with the present invention will be specifically
described with reference to Fig. 5.

In Fig. 5, the vector processor includes a data
distribution circuit 40a, and a vector data calculation
unit consisting of an odd term calculation circuit 10A

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and an even term calculation circuit 10B.

The data distribution circuit 40a is provided in
the vector register unit shown in Fig. 2, the odd term
calculation circuit 10A, and the even term calculation

5   circuit 10B, to supply an initial operand (data) a_0 ,
and operands (input vector data) b_i and c_i to the odd
and even term calculation circuits 10A and 10B, in a
predetermined manner discussed later. The data dis-
tribution circuit 40a also receives odd term data a_j
10   calculated at the odd term calculation circuit 10A and
even term data a_k calculated at the even term calcu-
lation circuit 10B, and outputs the same to the vector
register unit.

The data distribution circuit 40a includes a
15   selector control circuit 41a, a B-buffer (B-BUFF) 42 of
a first-in first-out type (FIFO) buffer, for first
inputting the operands b_i and first outputting the same,
and a C-buffer (C-BUFF) 43, which is also a FIFO buffer,
for first inputting the operands c_i and first outputting
20   the same. The data distribution circuit 40a also
includes selectors 46A, 47A, 48A, 46B, 47B, and 48B.
The data distribution circuit 40a further includes a
zero (0) setter (not shown) for outputting zero to the
selectors 46A and 46B, and a one (1) setter (not shown)
25   for outputting one to the setters 47A, 48A, 47B, and 48B.

The odd term calculation circuit 10A for calcu-
lating the odd terms a_j includes first stage regis-
ters 14A, 15A and 16A, a multiplication circuit 17A,
second stage registers 18A and 19A, an adder 110A, a
30   third stage registers 111A, a fourth stage regis-
ter 112A, a first feedback line 21A connected between an
output terminal of the register 19A and an input
terminal of the selector 48A, and a second feedback
line 22A connected between an output terminal of the
35   register 112A and an input terminal of the selector 46A,
and a third feedback line 23A connected between an
output terminal of the register 111A and an input

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terminal of the selector 47A. Calculated odd terms a_j are sequentially output from the register 111A to the vector register unit.

The registers 111A and/or 112A can be included in the data distribution circuit 40a.

The even term calculation circuit 10B for calculating the even terms a_k has the same circuit construction as that of the odd term calculation circuit 10A, because the operational algorithms, per se, are the same in both cases. Since both the odd and even term calculation circuits 10A and 10B can have the identical construction, the design, production and mounting thereof on a printed circuit board (PCB) are greatly simplified. Both of the odd and even term calculation circuits 10A and 10B are operable independently and simultaneously.

The operation of the vector processor shown in Fig. 5 will be described.

Supposing that the operands a_i , c_i and the initial operand a_0 are previously stored in the MSU 2 shown in Fig. 1, and the following instruction set is detected at the scalar processor 4, the scalar processor 4 transfers control of the operation to the vector processor shown in Fig. 5, triggering the vector processor.

TABLE 1

```
VL    A(0)  TO VR00
VL    B(I)  TO VR01
VL    C(i)  TO VR02
VCAL  A(i). = A(i-1) X B(I) + C(i)
VST   A(i)  TO VR00
```

where, VL indicates a "Vector Load" instruction,
VCAL indicates a "Vector Calculation" instruction,
VST indicates a "Vector Store" instruction
A(i), B(i) and C(i) correspond to a_i , b_i

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and c_i , and

VR00, VR01 and VR02 indicate vector
registers 00, 01 and 02 in the vector
register unit shown in Fig. 2. Note, in
this embodiment, each vector register has
a memory capacity of 100 words.

First, the vector storage access unit (VSAU) 52
shown in Fig. 2 loads vector data a_0 , b_1 -- b_{100} , and
c_1 -- c_{100} stored in the main storage unit (MSU) 1 into
the vector registers VR00, VR01 and VR02 of the vector
register unit through the main storage control unit
(MSCU) 2, in response to the above "Vector Load"
instruction, under the control of the vector instruction
control unit (VICU) 51 shown in Fig. 2.

During the above vector data loading, a calculation
of recurrent equation: $a_i = a_{i-1} \times b_i + c_i$ at the
circuit shown in Fig. 5, and a store of calculated
data a_i into the vector register VR00 are carried out,
in response to the above "Vector Calculation" and
"Vector Store" instructions, under the control of the
VICU 51.

The calculated data a_i in the vector register VR00
can be stored in the MSU 1 during the above operation.

Now, a detailed operation of the circuit of Fig. 5
will be described with reference to Fig. 6.

A calculation consists of an initial term calcu-
lation for calculating the initial terms a_1 and a_2 , and
a normal term calculation for calculating subsequent
terms, for example, a_3 and a_4 , a_5 and a_6 , etc.

First, the initial term calculation will be
described.

Below TABLE 2 and TABLE 3 show data loaded into the
registers 14A, 15A, 16A and 111A, and the registers
14B, 15B, and 16B, and 111B under the control of the
selector control circuit 40b.

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TABLE 2

OP CYCLE	REG 14A	REG 15A	REG 16A	REG 111A
01	c_1	b_1	a_0	
02				
03				
04	0	$a_0 \times b_1 + c_1$		1
05				
06				a_1

TABLE 3

OP CYCLE	REG 14B	REG 15B	REG 16B	REG 111B
01	c_1	b_1	a_0	
02				
03				
04	c_2	$a_0 \times b_1 + c_1$	b_2	
05				
06				a_2

The data distribution circuit 40a loads initial operands a_0 , b_1 and c_1 therein; the operands b_1 and c_1 being stored in the B-BUFF 42 and the C-BUFF 43, respectively.

OPERATION CYCLE 01

30   At the operation cycle 01, the selector control circuit 41a controls the selectors 46A, 47A, and 48A to output the operands c_1 , b_1 , and a_0 to the registers 14A, 15A, and 16A in the odd term calculation circuit 10A. These registers 14A, 15A, and 16A store

35   the operands c_1 , b_1 , and a_0. At the same time, the selector control circuit 41a controls the selectors 46B, 47B, and 48B to output the operands c_1 , b_1 , and a_0 to

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the registers 14B, 15B, and 16B in the even term calcu-
lation circuit 10B. These registers 14B, 15B, and 16B
also save the operands a_0 , b_1 , and c_1.

    In the odd term calculation circuit 10A, the
5 register 16A outputs the saved operand a_0 to the
multiplication circuit 17A as a multiplicand, and the
register 15A outputs the saved operand b_1 to the
multiplication circuit 17A as a multiplier. Thus, the
multiplication circuit 17A calculates $(a_0 \times b_1)$.

10   At the same time, in the even term calculation
circuit 10B, the register 16B outputs the saved
operand a_0 to the multiplication circuit 17B as a
multiplicand, and the register 15B outputs the saved
operand b_1 to the multiplication circuit 17B as a
15 multiplier. The multiplication circuit 17B calculates
$(a_0 \times b_1)$.

    OPERATION CYCLE 02

    In the odd term calculation circuit 10A, data $(a_0$
$\times b_1)$ calculated at the multiplication circuit 17A is
20 transferred to the register 19A and saved therein. The
data c_1 saved at the register 14A is also transferred to
the register 18A and saved therein.

    At the same time, in the even term calculation
circuit 10B, data $(a_0 \times b_1)$ calculated at the multi-
25 plication circuit 17B is transferred to the register 19B
and saved therein. The data c_1 saved at the regis-
ter 14B is transferred to the register 18B.

    Thereafter, in the odd term calculation cir-
cuit 10A, the adder 110A adds the data $(a_0 \times b_1)$ and the
30 data c_1. As a result, the following first odd term is
obtained.

$$a_1 = a_0 \times b_1 + c_1$$

    Similarly, at the same time, in the even term
calculation circuit 10B, the above first odd term a_1 is
35 obtained by the adder 110B.

    OPERATION CYCLE 03

    In the odd term calculation circuit 10A, the

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calculated first odd term a_1 is transferred to the register 111A and saved therein.

Also, in the even term calculation circuit 10B, the calculated first odd term a_1 is transferred to the register 111B and saved therein.

During the above operation, the data distribution circuit 40a loads operands (b_2 , b_3 , b_4) and (c_2 , c_3 , c_4) into the B-BUFF 42 and the C-BUFF 43 from the vector registers VR01 and VR02, respectively.

Note that, although having obtained the first odd term a_1 , the data distribution circuit 40a does not output the same to the vector register VR00 at this time, because a first even term a_2 has not been obtained.

OPERATION CYCLES 04 - 06

Until the first even term a_2 is obtained at the even term calculation circuit 10B, the odd term calculation circuit 10A and the data distribution circuit 40a cooperate to keep the data a_1 as is, and to prepare operands used for calculating a second odd term a_3.

As the operation cycle 04, the selector control circuit 41a controls the selectors 46A, 47A, and 48A to set zero data to the register 14A, the calculated first odd term a_1 to the register 15A through the register 111A and the feedback line 23A, and a data of one (1) to the register 16A. As a result, at the operation cycle 04, the multiplication circuit 17A calculates $(a_1$ x 1), and at the operation cycle 06, the adder 110A adds the data $(a_1$ x 1) from the register 19A and the data of zero (0) from the registers 18A. Namely, the following dummy calculation is effected.

$$a_1 = (a_1 \text{ x } 1) + 0$$

During the above operation, at the operation cycle 05, the selector control circuit 41a controls the selectors 47A and 48A to set an operand b_3 to the register 15A, and an operand b_2 to the register 16A. The data a_1 is transferred to the register 111A at the

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operation cycle 05, and is further stored in the register 112A at the operation cycle 06.

Conversely, in the even term calculation circuit 10B, the following first even term a_2 is calculated
5 by using the first odd term a_1 calculated therein and saved in the registers 112B.

$$a_2 = (a_1 \times b_2) + c_2$$

For this purpose, at the operation cycle 04, the selector control circuit 41a controls the selectors 46B,
10 47B, and 48B to set the operand c_2 to the register 14B, the first odd term a_1 saved in the register 111B to the register 15B through the feedback line 23B, and the operand b_2 to the register 16B. At the operation cycle 05, the first even term a_2 is obtained at the
15 adder 110B, and at the operation cycle 06, the first even term a_2 is stored in the registers 111B.

The data distribution circuit 40a transfers the pair of first odd and even terms a_1 and a_2 to the vector register VR00 from the register 111A and 111B.

20 The initial term calculation is thus completed.

The normal term calculation will now be described.

OPERATION CYCLES 03 - 09

First, a calculation of a second odd term a_3 in the odd term calculation circuit 10A will be described.

25 Since the second odd term a_3 is defined by the following formula, the selector control circuit 41a controls the selectors 46A, 47A, and 48A to load data as shown in TABLE 4 into the registers 14A, 15A, and 16A at the following operation cycles shown in TABLE 4.

$$a_3 = a_1 \times (b_2 \times b_3) + b_3 \times c_3 + c_3$$

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TABLE 4

OP CYCLE	REG 14A	REG 15A	REG 16A
03	c_3	b_3	c_2
04			
05	---	b_3	b_2
06			
07	$b_3 \times c_2 + c_3$	a_1	$b_2 \times b_3$
08			
09			

At the operation cycle 03, a multiplication value $(b_3 \times c_2)$ is obtained at the multiplication circuit 17A. At the operation cycle 05, a sum $(b_3 \times c_2) + c_3$ is obtained at the adder 110A. At the operation cycle 05, a multiplication value $(b_2 \times b_3)$ is obtained at the multiplication circuit 17A. At the operation cycle 07, a multiplication value $(a_1 \times b_2 \times b_3)$ is obtained at the multiplication circuit 17A. At the operation cycle 08, the calculated data $(a_1 \times b_2 \times b_3)$ is supplied to the adder 110A. The above second odd term a_3 is obtained at the adder 111A. The calculated second odd term a_3 is saved at the register 111A at the operation cycle 08. At the operation cycle 09, the second odd term a_3 saved in the register 111A is transferred to the vector register VR00 and saved in the register 112A.

In the above, the data a_1 saved in the register 112A is fed back to the register 15A through the feedback line 22A. Also, the data $(b_2 \times b_3)$ saved in the register 19A is fed back to the register 16A through the feedback line 21A. The sum $(b_3 \times c_2) + c_3$ stored in the register 111A is fed back to the register 14A through the feedback line 23A.

Similarly, the following second even term a_4 is

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obtained at the even term calculation circuit 10B.

$$a_4 = a_2 \times b_3 \times b_4 + b_4 \times c_3 + c_4$$

The selector control circuit 41a also controls the selectors 46B, 47B, and 47B to load the following data shown in TABLE 5 into the registers 14B, 15B, and 16B.

TABLE 5

OP CYCLE	REG 14B	REG 15B	REG 16B
03	c_4	b_4	c_3
04			
05		b_4	b_3
06			
07	$c_3 \times b_4 + c_4$	a_2	$b_3 \times b_4$
08			
09			

At the operation cycle 09, the odd and even terms a_3 and a_4 are transferred to the vector register VR00 in the vector register unit.

OPERATION CYCLES 06 - 12

Similarly, during the operation cycles 06 - 12, the following third odd and even terms a_5 and a_6 are obtained at the odd and even term calculation circuits 10A and 10B.

$$a_5 = a_3 \times b_4 \times b_5 + b_5 \times c_4 + c_5$$
$$a_6 = a_4 \times b_5 \times b_6 + b_6 \times c_5 + c_6$$

To achieve the above calculation, the selector control circuit 41a controls the selectors 46A, 47A, 48A, 46B, 47B and 48B to load the following data shown in TABLE 6 and TABLE 7 to the registers 14A, 15A, 16A, 14B, 15B and 16B.

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TABLE 6

OP CYCLE	REG 14A	REG 15A	REG 16A
06	c_5	b_5	c_4
07			
08	--	b_5	b_4
09			
10	$c_4 \times b_5 + c_5$	a_3	$b_4 \times b_5$
11			
12			

TABLE 7

OP CYCLE	REG 14B	REG 15B	REG 16B
06	c_6	b_6	c_5
07			
08	--	b_6	b_5
09			
10	$c_5 \times b_6 + c_6$	a_4	$b_5 \times b_6$
11			
12			

At the operation cycle 11, the odd and even terms a_5 and a_6 are obtained at the adders 111A and 111B and are transferred to the vector register VR00.

Other pluralities of pairs of odd and even terms are obtained in the same way as described above.

A calculation of a pair of odd and even terms requires only three operation cycles, except for a calculation of the first odd and even terms. This time is same as that of the prior art vector processor.

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According to the vector processor shown in Fig. 5, twice
the amount of data can be obtained in three operation
cycles, except for the initial calculation. Thus, the
vector processor shown in Fig. 5 doubles the calculation
5   performance compared with that of the prior art vector
processor, when many terms of the recurrent equations
are to be calculated.

Another embodiment of the vector processor in
accordance with the present invention will be described
10   with reference to Fig. 7.

In Fig. 7, the vector processor includes a data
distribution circuit 40a and a vector data calculation
unit consisting of an odd term calculation circuit 10AA
and an even term calculation circuit 10BB.

15   The data distribution circuit 40b is provided in
the vector register unit shown in Fig. 2, the odd term
calculation circuit 10AA, and the even term calculation
circuit 10BB, to supply an initial operand a_0 and
operands (input data) b_i and c_i to the odd and even term
20   calculation circuits 10AA and 10BB in a predetermined
manner, as described later. The data distribution
circuit 40b also receives a pair of odd term data a_j
calculated at the odd term calculation circuit 10AA and
even term data a_k calculated at the even term calcu-
25   lation circuit 10BB, and outputs the same to the vector
register unit.

The data distribution circuit 40b includes a
selector control circuit 41b, the B-BUFF 42, the
C-BUFF 43, buffer registers 51A and 52A, selectors 53A,
30   54A, and 55A, registers 51B and 52B, and selectors 53B,
54B and 55B. The data distribution circuit 40b also
includes the zero setter and the one setter (not shown).

The odd term calculation circuit 10AA includes the
first-stage registers 14A, 15A, and 16A, the multi-
35   plication circuit 17A, the second-stage registers 18A
and 19A, the adder 110A, the third-stage register 111A,
and a feedback line 24A connected between an output

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terminal of the register 111A and an input terminal of
the register 51A.

The even term calculation circuit 10BB has the same
circuit construction as that of the odd term calculation

5   circuit 10AA.

The vector processor shown in Fig. 7 calculates the
recurrent equation defined by the formula (2). The odd
term calculation circuit 10AA and the data distribution
circuit 40b cooperate to calculate the recurrent

10 equations defined by the formula (4), and the even term
calculation circuit 10BB and the data distribution
circuit 40b also cooperate to calculate the recurrent
equations defined by the formula (3).

The operation of the vector processor shown in

15 Fig. 7 will be specifically described with reference to
Fig. 8, when the instruction set shown in TABLE 1 is
given.

The operation of the MSU 1, the MSCU 2, the
VICU 51, and the VSAU 52, shown in Fig. 2, is omitted,

20 since the operation thereof is substantially the same as
that described above.

In Fig. 8, the cooperation cycles consist of
initial operation cycles 01 - 08, and normal operation
cycles 04 - 11, 10 - 14, etc.

25   <u>OPERATION CYCLE 01 - 08</u>

The following TABLE 8 and TABLE 9 show data in the
registers 14A, 15A, 16A, and 111A, and data in the
registers 14B, 15B, 16B, and 111B, during the initial
operation cycles.

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TABLE 8

OP CYCLE	REG 14A	REG 15A	REG 16A	REG 111A
01	0	b_1	1	
02	c_1	0	b_1	
03	0	a_0	1	
04				
05				
06	$b_1 \times 0 + c_1$	$1 \times a_0 + 0$	$1 \times b_1 + 0$	
07				
08				a_1

TABLE 9

OP CYCLE	REG 14B	REG 15B	REG 16B	REG 111B
01	0	b_2	b_1	
02	c_2	c_1	b_2	
03	0	a_0	1	
04				
05				
06	$c_1 \times b_2 + c_2$	$1 \times a_0 + 0$	$b_1 \times b_2 + 0$	
07				
08				a_2

The selector control circuit 41b controls the selectors 53A, 54A, and 55A to load data into the registers 14A, 15A, and 16A, as shown in TABLE 8, and the selector control circuit 41b controls the selectors 53B, 54B, and 55B to load data into the registers 14B, 15B, and 16B, as shown in TABLE 9.

First, a calculation of the term a_j in the odd term

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calculation circuit 10AA will be described.

OPERATION CYCLE 01

Data 0, b_1 , and 1 are loaded into the registers 14A, 15B, and 16A, and a calculation of (b_1 x 1) is
5 carried out at the multiplication circuit 17A.

OPERATION CYCLE 02

Data 0 and (b_1 x 1) are loaded into the registers 18A and 19A, and both data are added at the adder 110A, to obtain the result (b_1 x 1 + 0). At the
10 same time, data c_1 , b_1 and 0 are loaded into the registers 14A, 15A, and 16A, and a calculation of (b_1 x 0) is carried out at the multiplication circuit 17A.

OPERATION CYCLE 03

The data (b_1 x 1 + 0) is stored in the regis-
15 ter 111A.

The data c_1 stored in the register 18A and the data (b_1 x 0) stored in the register 19A are added at the adder 110A, to obtain the result (b_1 x 0 + c_1). At the same time, data 0, a_0 , and 1 are loaded into the
20 registers 14A, 15A, and 16A, and a calculation of (a_0 x 1) is carried out at the multiplication circuit 17A.

OPERATION CYCLE 04

The data (b_1 x 1 + 0) stored in the register 111A is transferred to the register 51A. The data 0 stored
25 in the register 18A and the data (a_0 x 1) stored in the register 19A are added at the adder 111A, to obtain the result (a_0 x 1 + 0).

OPERATION CYCLE 05

The data (b_1 x 1 + c_1) and (b_1 x 0 + c_1) are
30 sequentially loaded into the registers 51A and 52A, respectively. The data (a_0 x 1 + 0) is stored in the register 111A.

OPERATION CYCLE 06

The data (a_0 x 1 + 0) stored in the register 111A
35 is transferred to the register 15A, and the data (b_1 x 1 + 0) stored in the register 52A is transferred to the register 16A. As a result, the data (a_0 x 1 + 0) x (1

x b_1 + 0) is obtained at the multiplication circuit 17A.

The data (b_1 x 0 + c_1) stored in the register 51 is loaded into the register 14A.

OPERATION CYCLE 07

The data (b_1 x 0 + c_1) from the register 14A is loaded into the register 18A.

The data (b_1 x 0 + c_1) stored in the register 18A and the data (a_0 x 1 + 0) x (1 x b_1 + 0) stored in the registser 19A are added at the adder 110A, to obtain the resulting data

$$(a_0 \times 1 + 0) \times (1 \times b_1 + 0) + (b_1 \times 0 + c_1)$$
$$= a_0 \times b_1 + c_1$$
$$= a_1$$

OPERATION CYCLE 08

The calculated data a_1 is stored in the register 111A and transferred to the vector register VR00.

Next, a calculation of the term a_2 in the even term calculation circuit 10BB will be described with reference to TABLE 9.

OPERATION CYCLE 01

Data 0, b_2 , and b_1 are loaded into the registers 14B, 15B, and 16B, and a calculation of (b_1 x b_2) is carried out at the multiplication circuit 17B.

OPERATION CYCLE 02

Data 0, and (b_1 x b_2) are loaded into the registers 18B and 19B, and both data are added at the adder 110B, to obtain the result (b_1 x b_2 + 0). At the same time, data c_2 , c_1 , and b_2 are loaded into the registers 14B, 15B, and 16B, and a calculation of (c_1 x b_1) is carried out at the multiplication circuit 17B.

OPERATION CYCLE 03

The data (b_1 x b_2 + 0) is stored in the register 111B. The data c_2 stored in the register 18B and the data (c_1 x b_2) stored in the register 19B are added at the adder 110B, to obtain the result (c_1 x b_2 + c_2). At the same time, data 0, a_1 , and 1 are loaded into the registers 14B, 15B, and 16B, and a calculation of (a_0

x 1) is carried out at the multiplication circuit 17B.

OPERATION CYCLE 04

The data $(b_1 \times b_2 + 0)$ stored in the register 111B is transferred to the register 51B. The data $(c_1 \times b_2$

5    $+ c_2)$ is stored in the register 111B. The data 0 stored in the register 18B and the data $(a_0 \times 1 + 0)$ stored in the register 19B are added at the adder 110B to obtain the result $(a_0 \times 1 + 0)$.

OPERATION CYCLE 05

10   The data $(c_1 \times b_2 + c_2)$ and $(b_1 \times b_2 + 0)$ are loaded into the registers 51B and 52B, respectively. The data $(a_0 \times 1 + 0)$ is stored in the register 111B.

OPERATION CYCLE 06

The data $(c_1 \times b_2 + c_2)$ is loaded into the

15   register 14B.

The data stored in the register 111B is transferred to the register 15B, and the data $(b_1 \times b_2 + 0)$ stored in the register 52B is transferred to the register 16B. As a result, data $(a_0 \times 1 + 0) \times (b_1 \times b_2 + 0)$ is

20   obtained at the multiplication circuit 17B.

OPERATION CYCLE 07

The data $(c_1 \times b_2 + c_2)$ stored in the register 18B and the data $(a_0 \times 1 + 0) \times (b_1 \times b_2 + 0)$ are added at the adder 110B, to obtain the resulting data.

25           $(a_0 \times 1 + 0) \times (b_1 \times b_2 + 0) + (c_1 \times b_2 + c_2)$

$$= a_0 \times b_1 \times b_2 + b_2 \times c_1 + c_2$$

$$= a_2$$

OPERATION CYCLE 08

The calculated data a_2 is stored in the regis-

30   ter 111B and transferred to the vector register VR00 together with the data a_1.

The initial calculation is terminated.

Now, the normal calculation will be briefly described. The normal calculation is similar to the

35   initial calculation, except for the data loading and transferring. Thus, the following description is mainly of the data loading.

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OPERATION CYCLE 04 - 11

During these cycles, the odd term a_3 and the even term a_4 are calculated.

The following TABLE 10 and TABLE 11 show data in the registers 14A, 15B, 16A and 111A, and data in the registers 14B, 15B, and 16B, and 111B.

TABLE 10

OP CYCLE	REG 14A	REG 15A	REG 16A	REG 111A
04	0	b_3	b_2	
05	c_3	c_2	b_3	
06				
07				
08				
09	$b_3 \times c_2 + c_3$	a_1	$b_2 \times b_3 + 0$	
10				
11				a_3

TABLE 11

OP CYCLE	REG 14B	REG 15B	REG 16B	REG 111B
04	0	b_4	b_3	
05	c_4	c_3	b_4	
06				
07				
08				
09	$b_4 \times c_3 + c_4$	a_2	$b_3 \times b_4 + 0$	
10				
11				a_4

<u>OPERATION CYCLES 07 - 14</u>

During these operation cycles, the odd term a_5 and the even term a_6 are calculated.

The following TABLE 12 and TABLE 13 show data in the registers 14A, 15A, 16A, and 111A, and data in the registers 14b, 15b, 16b, and 111B.

TABLE 12

OP CYCLE	REG 14A	REG 15A	REG 16A	REG 111A
07	0	b_5	b_4	
08	c_5	c_4	b_5	
09				
10				
11				
12	$b_5 \times c_4 + c_5$	a_3	$b_4 \times b_5 + 0$	
13				
14				a_5

TABLE 13

OP CYCLE	REG 14B	REG 15B	REG 16B	REG 111B
07	0	b_6	b_5	
08	c_6	c_5	b_6	
09				
10				
11				
12	$b_6 \times b_5 + c_6$	a_4	$b_5 \times b_6 + 0$	
13				a_6
14				

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Other pluralities of pairs of odd and even terms
can be calculated in the same way as described above.

The present invention is not limited by the above
embodiments. For example, in the above embodiments,
first-order developed recurrent equations as expressed
by the formulas (2) to (4) were described. When the
recurrent equation as expressed by the formula (1) is
modified by using a second-order development, the
following formula is obtained.

$$
\begin{aligned}
a_i &= a_{i-1} \times b_i + c_i \\
&= a_{i-2} \times b_{i-1} \times b_i + b_i \times c_{i-1} + c_i \\
&= a_{i-3} \times b_{i-2} \times b_{i-1} \times b_1 + b_{i-2} \times b_{i-1} \times c_{i-2} \\
&\quad + b_i \times c_{i-1} + c_i
\end{aligned}
$$

$$\ldots \text{(5)}$$

Apparently, the above formula shows that there is
no direct recurrent relationship between the terms a_i
and a_{i-3}.

When an index $\underline{i}$ is odd, for example, an odd index $\underline{j}$
is 3 and 5, the above formula is expressed as follows:

$$
\begin{aligned}
j = 3: \quad a_3 &= a_0 \times b_1 \times b_2 \times b_3 + b_1 \times b_2 \times c_1 \\
&\quad + b_3 \times c_2 + c_3
\end{aligned}
$$

$$\ldots \text{(6)}$$

$$
\begin{aligned}
j = 5: \quad a_5 &= a_2 \times b_3 \times b_4 \times b_5 + b_3 \times b_4 \times c_3 \\
&\quad + b_5 \times c_4 + c_5
\end{aligned}
$$

$$\ldots \text{(7)}$$

When an index $\underline{i}$ is even, for example, an even
index $\underline{k}$ is 4 and 6, the above formula is expressed as
follows:

$$
\begin{aligned}
k = 4: \quad a_4 &= a_1 \times b_2 \times b_3 \times b_4 + b_2 \times b_3 \times c_2 \\
&\quad + b_4 \times c_3 + c_4
\end{aligned}
$$

$$\ldots \text{(8)}$$

$$
\begin{aligned}
k = 6: \quad a_6 &= a_3 \times b_4 \times b_5 \times b_1 + b_4 \times b_5 \times c_4 \\
&\quad + b_6 \times c_5 + c_6
\end{aligned}
$$

$$\ldots \text{(9)}$$

From the above formulas (6) to (9), two odd
terms a_3 and a_5, and two even terms a_4 and a_6 can be
simultaneously calculated at a same timing. Thus, the

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operation time is further shortened. In this embodi-
ment, an odd term calculation circuit is formed to
calculate two adjacent odd terms, for example, a_3
and a_5 , at a same timing. Similarly, an even term
5   calculation circuit is formed to calculate two adjacent
even terms at a same timing. A data distribution
circuit is formed to distribute data to the odd and even
term calculation circuits so that the above formulas can
be calculated.
10   INDUSTRIAL APPLICABILITY
        The vector processor of the present invention can
be applied to a variety of data processing systems.

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CLAIMS

1.   A vector processor including a vector instruc-
tion control unit (51) for controlling vector instruc-
tions, a vector storage access unit (52) for accessing
input vector data and calculated data to a main storage

5   unit, a vector calculation unit for calculating vector
data under the control of the vector instruction unit,
and a data distribution unit (54) for transferring data
between the vector data access unit and the vector
calculation unit,

10   characterized in that the vector
processor comprises a vector calculation unit including
at least one odd term calculation circuit (10A, 10AA)
and at least one even term calculation circuit (10B,
10BB), and a data distribution unit (40a, 40b) opera-

15 tively connected to and cooperative with said vector
calculation unit, to process a modified recurrent
equation,

            each odd term calculation circuit being
formed to calculate odd terms of said modified recurrent

20 equation and include an adding circuit (110A), a multi-
plication circuit (17A), at least one data storage
circuit (112A, 51A, 52A) holding a calculated odd term,
and at least one feedback line (21A, 22A, 23A, 24A) for
feeding back the calculated odd term to said

25 multiplication circuit and/or said adding circuit
through said data storage circuit,

            each even term calculation circuit being
formed to calculate even terms of said modified recurrent
equation and include another adding circuit (110B),

30 another multiplication circuit (17B), at least one
another data storage circuit (112B, 51B, 52B) holding a
calculated even term, and at least one another feedback
line (21B, 22B, 23B, 24B) for feeding back the calculated
even term to said another multiplication circuit and/or

35 said another adding circuit through said another data
storage circuit, and

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said data distribution unit including a
first data setter for outputting zero, a second data
setter for outputting one, first to sixth selec-
tors (46A, 47A, 48A, 46B, 47B, 48B) for selecting input
5   operands (a_i , b_i) using for calculating said recurrent
equation, constant data 0 and 1 from said setters, and
the calculated odd and even terms, and a selector
control unit (40a, 40b) for controlling said selectors
in a predetermined manner defined by said modified
10   recurrent equation, to supply selected data to said odd
and even term calculation circuits.

2.   A vector processor according to claim 1,
wherein said odd and even term calculation circuits are
independently and simultaneously operable to calculate
15   at least one pair of adjacent odd and even terms (a_i ,
a_{i+1}) of said recurrent equation, at a same operation
time.

3.   A vector processor according to claim 2,
wherein said data distribution unit (40a, 40b) comprises
20   a first first-in and first-out type buffer (42) for
inputting and outputting a plurality of said first
operands (b_i) as source multipliers and/or multipli-
cands, and a second first-in and first-out type
buffer (43) for inputting and outputting a plurality of
25   said second operands (c_i) as source addends.

4.   A vector processor according to claim 3,
wherein said modified recurrent equation is expressed by
the following formula when first order developed,

$$a_i = a_{i-2} \times b_{i-1} \times b_i + b_i \times c_{i-1} + c_i$$
$$.... (1)$$

said odd term calculation circuit
calculating the following formulas, and

$$a_1 = a_0 \times b_1 + c_1$$
$$a_j = a_{j-2} \times b_{j-1} \times b_j + b_j \times c_{j-1} + c_j$$
$$.... (2)$$

where, j is as odd integer,

$$j = 1, 3, \ldots , n$$

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said even term calculation circuit
calculating the following formula:

$$a_k = a_{k-2} \times b_{k-1} \times b_k + b_k \times c_{k-1} + c_k$$

$$\dots \quad (3)$$

5   where, $\underline{k}$ is an even integer,

$$\underline{k} = 2, 4, \dots, n+1$$

5.   A vector processor according to claim 4,
wherein said odd term calculation circuit comprises
first to third feedback lines (21A, 22A, 23A), and is

10   formed so that

(a)   said adding circuit (110A) receives
an addend from said first selector (46A),

(b)   said multiplication circuit (17A)
receives a multiplier and a multiplicand from said

15   second and third selectors (47A, 48A),

(c)   said adding circuit (110A) receives
a data multiplied at said multiplication circuit,

(d)   said data storage circuit (112A)
receives a data added at said adding circuit,

20   (e)   said first selector (46A) receives
constant of zero, said second operand (c_i) from said
second buffer (43), and said data stored in said data
storage circuit (112A) through said second feedback
line (22A),

25   (f)   said second selector (47A) receives
said constant of one, said first operand (b_i), and said
added data through said third feedback line (23A), and

(g)   said third selector (48A) receives
said constant of one, an initial data (a_0), said first

30   and second operands from said first and second
buffers (42, 43), and said multiplied data from said
multiplication circuit (17A) through said first feedback
line (21A), and

said even term calculation circuit

35   comprises another first to third feedback lines (21B,
22B, 23B), and is formed so that

(h)   said another adding circuit (110B)

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receives an addend from said fourth selector (46B),

(i) said another multiplication circuit (17B) receives a multiplier and a multiplicand from said fifth and sixth selectors (47B, 48B),

5   (j) said another adding circuit (110B) receives a data multiplied at said another multiplication circuit.

(k) said another data storage circuit (112B) receives a data added at said another adding

10   circuit,

(l) said fourth selector (46B) receives said constant of zero, said second operand (c_i) from said second buffer (43), and said data stored in said data storage circuit (112B) through said second feedback

15   line (22B),

(m) said fifth selector (47B) receives said constant of one, said first operand (b_i), and said added data through said another third feedback line (23B), and

20   (n) said sixth selector (48B) receives said constant of one, said initial data (a_0), said first and second operand (b_i, c_i) from said first and second buffer (42, 43), line (22B), and said multiplied data from said multiplication circuit (17B) through said

25   another first feedback line (21B).

6.   A vector processor according to claim 5, wherein said odd term calculation circuit (10A) comprises

a first-stage first data storage cir-

30   cuit (14A) connected to said first selector (46A), for temporarily storing data therefrom,

first stage second and third data storage circuits (15A, 16A) connected between said second and third selectors (47A, 48A), and said multiplication

35   circuit (17A), for temporarily storing data from said second and third selectors,

a second-stage first data storage cir-

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cuit (18A) connected between said first-stage first data
storage circuit and said adding circuit, for temporarily
storing data from said first-stage first data storage
circuit,

5   a second-stage second data storage
circuit (19A), an input terminal thereof being connected
to said multiplication circuit and an output terminal
thereof being connected to said adding circuit and said
first feedback line, said second-stage second data
10   storage circuit temporarily storing data multiplied at
said multiplication circuit, and

                    a third-stage data storage circuit (111A)
connected between said adding circuit and said data
storage circuit (112A) and to said third feedback line,
15   for temporarily storing data added at said adding
circuit, and

                    said even term calculation circuit (10B)
comprises

                    another first-stage first data storage
20   circuit (14B) connected to said another first selec-
tor (46B), for temporarily storing data therefrom,

                    another first-stage second and third data
storage circuits (15B, 16B) connected between said
another second and third selectors (47B, 48B), and said
25   another multiplication circuit (17B), for temporarily
storing data from said another second and third
selectors,

                    another second-stage first data storage
circuit (18B) connected between said another first-stage
30   first data storage circuit and said another adding
circuit, for temporarily storing data from said another
first-stage first data storage circuit,

                    another second-stage second data storage
circuit (19B), an input terminal thereof being connected
35   to said another multiplication circuit and an output
terminal thereof being connected to said another adding
circuit and said another first feedback line, said

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another second-stage second data storage circuit
temporarily storing data multiplied at said another
multiplication circuit, and

another third-stage data storage cir-
5 cuit (111B) connected between said another adding
circuit and said another data storage circuit (112A)
and to said another third feedback line, for temporarily
storing data added at said another adding circuit.

7.   A vector processor according to claim 6,
10 wherein,

at an initial operation time,

said odd term calculation circuit and
said data distribution circuit cooperate to calculate
the following terms during two operation times,

$$a_1 = a_0 \times b_1 + c_1$$
$$a_1 = a_1 \times 1 + 0$$

said even term calculation circuit and
said data distribution circuit cooperate to calculate
the following terms during said two operation times,

$$a_1 = a_0 \times b_1 + c_1$$
$$a_2 = a_1 \times b_2 + c_2$$

at a normal operation time after said
initial operation time,

said odd term calculation circuit and
25 said data distribution circuit cooperate to calculate
each odd term of the following formula in each operation
time, and

$$a_j = a_{j-2} \times b_{j-1} \times b_j + b_j \times c_{j-1} + c_j$$
$$\text{where, } j = 3, 5, \ldots, n$$

30   said even term calculation circuit and
said data distribution circuit cooperate to calculate
each even term of the following formula in said
operation time.

$$a_k = a_{k-2} \times b_{k-1} \times b_k + b_k \times c_{k-1} + c_k$$
35             $$\text{where, } k = 4, 6, \ldots, n+1$$

8.   A vector processor according to claim 7,
wherein each said operation time comprises a plurality

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of operation cycles of said vector processor,

said operation times are identical for
calculating each term, and

adjacent operation times for calculating

5   adjacent terms are partially overlapped.

9.   A vector processor according to claim 8,
wherein said data distribution unit (40a) receives data
from said third-stage and said another third-stage data
storage circuits (110A, 110B), and outputs said data to

10   said vector storage access unit (52).

10.   A vector processor according to claim 9,
wherein said vector storage access unit comprises a
vector register unit for temporarily storing said input
operands and said calculated odd and even terms, and

15   said data distribution circuit transfers
said input operands and said calculated odd and even
terms.

11.   A vector processor according to claim 4,
wherein said odd term calculation circuit comprises

20   a feedback line (24A), and first and second data storage
circuits (51A, 52A) connected in series for storing
calculated odd terms supplied through said feedback line
(24A), and is formed so that

(a)   said adding circuit (110A) receives

25   an addend from said first selector (53A),

(b)   said multiplication circuit (17A)
receives a multiplier and a multiplicand from said
second and third selectors (54A, 55A),

(c)   said adding circuit (110A) receives

30   a data multiplied at said multiplication circuit,

(d)   said first data storage cir-
cuit (51A) receives a data added at said adding circuit,

(e)   said second data storage circuit
(52A) receives a data from said first data storage

35   circuit,

(f)   said first selector (53A) receives
said constant of zero, said second operand (c_i) from

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said second buffer (43), and a data from said first data
storage circuit,

          (g)   said second selector (54A) receives
said constant of zero, an initial data (a_0), said first

5   and second operand (b_i , c_i), and said data added at
said adding circuit through said feedback line, and

          (h)   said third selector (55A) receives
said constant of one, said first operand from said first
buffer (42), and said data stored in said second data

10 storage circuit (52A),

         said even term calculation circuit
comprises another feedback line (24B), and another first
and second data storage circuits (51B, 52B) connected in
series and for storing said calculated even terms

15 supplied through said another feedback line (24B), and
is formed so that

          (i)   said another adding circuit (110B)
receives an addend from said fourth selector (53B),

          (j)   said another multiplication cir-

20 cuit (17B) receives a multiplier and a multiplicand from
said fifth and sixth selectors (54B, 55B),

          (k)   said another adding circuit (110B)
receives a data multiplied at said another multi-
plication circuit,

25   (l)   said another first data storage
circuit (51B) receives a data added at said another
adding circuit,

          (m)   said another second data storage
circuit (52B) receives a data from said another first

30 data storage circuit,

          (n)   said fourth selector (53B) receives
said constant of zero, said second operand (c_i) from
said second buffer (43), and a data from said first data
storage circuit,

35   (o)   said fifth selector (54B) receives
said constant of zero, said initial data (a_0), said
first and second operands (b_i , c_i), and said data added

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at said another adding circuit through said another
feedback line, and

(p)   said sixth selector (55B) receives
said constant of one, said first operand from said first
5 buffer (42), and said data stored in said another second
data storage circuit (52B),

12.   A vector processor according to claim 11,
wherein said odd term calculation circuit (10AA) com-
prises

10   a first-stage first data storage cir-
cuit (14A) connected to said first selector (53A), for
temporarily storing a data therefrom,

first-stage second and third data storage
circuits (15A, 16A) connected between said second and
15 third selectors (54A, 55A) and said multiplication
circuit (17A), for temporarily storing data from said
second and third selectors,

a second-stage first data storage cir-
cuit (18A) connected between said first-stage first data
20 storage circuit and said adding circuit, for temporarily
storing data from said first-stage first data storage
circuit,

a second-stage second data storage
circuit (19A), an input terminal thereof being connected
25 to said multiplication circuit and an output terminal
thereof being connected to said adding circuit, said
second-stage second data storage circuit temporarily
storing data multiplied at said multiplication
circuit, and

30   a third-stage data storage circuit (111A)
connected between said adding circuit and said data
storage circuit (51A) through said feedback line, for
temporarily storing data added at said adding circuit,
and

35   said even term calculation circuit (10B)
comprises

another first-stage first data storage

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circuit (14B) connected to said another first
selector (53B), for temporarily storing data therefrom,

another first-stage second and third data
storage circuits (15B, 16B) connected between said
5 another second and third selectors (54B, 55B) and said
another multiplication circuit (17B), for temporarily
storing data from said another second and third
selectors,

another second-stage first data storage
10 circuit (18B) connected between said another first-stage
first data storage circuit and said another adding
circuit, for temporarily storing data from said another
first-stage first data storage circuit,

another second-stage second data storage
15 circuit (19B), an input terminal thereof being connected
to said another multiplication circuit and an output
terminal thereof being connected to said another adding
circuit, said another second-stage second data storage
circuit temporarily storing data multiplied at said
20 another multiplication circuit, and

another third-stage data storage cir-
cuit (111B) connected between said another adding
circuit and said another data storage circuit (51B)
through said another feedback line, for temporarily
25 storing data added at said another adding circuit.

13.   A vector processor according to claim 12,
wherein,

at an initial operation time,
said odd term calculation circuit and
30 said data distribution circuit cooperate to calculate
the following terms during two operation times,

$$a_1 = a_0 \times b_1 + c_1$$
$$a_1 = a_1 \times 1 + 0$$

said even term calculation circuit and
35 said data distribution circuit cooperate to calculate
the following terms during said two operation times,

$$a_1 = a_0 \times b_1 + c_1$$

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$$a_2 = a_1 \times b_2 + c_2$$

at a normal operation time after said initial operation time,

said odd term calculation circuit and said data distribution circuit cooperate to calculate each odd term of the following formula in each operation time, and

$$a_j = a_{j-2} \times b_{j-1} \times b_j + b_j \times c_{j-1} + c_j$$

where, $j = 3, 5, \ldots, n$

said even term calculation circuit and said data distribution circuit cooperate to calculate each even term of the following formula in said operation time.

$$a_k = a_{k-2} \times b_{k-1} \times b_k + b_k \times c_{k-1} \times c_k$$

where, $k = 4, 6, \ldots, n+1$

14.   A vector processor according to claim 13, wherein each said operation time comprises a plurality of operation cycles of said vector processor,

said operation times are identical for calculation each term, and

adjacent operation times for calculating adjacent terms are partially overlapped.

15.   A vector processor according to claim 14, wherein said data distribution unit (40b) receives data from said third-stage and said another third-stage data storage circuits (110A, 110B), and outputs said data to said vector storage access unit (52).

16.   A vector processor according to claim 15, wherein said vector storage access unit comprises a vector register unit for temporarily storing said input operands and said calculated odd and even terms, and

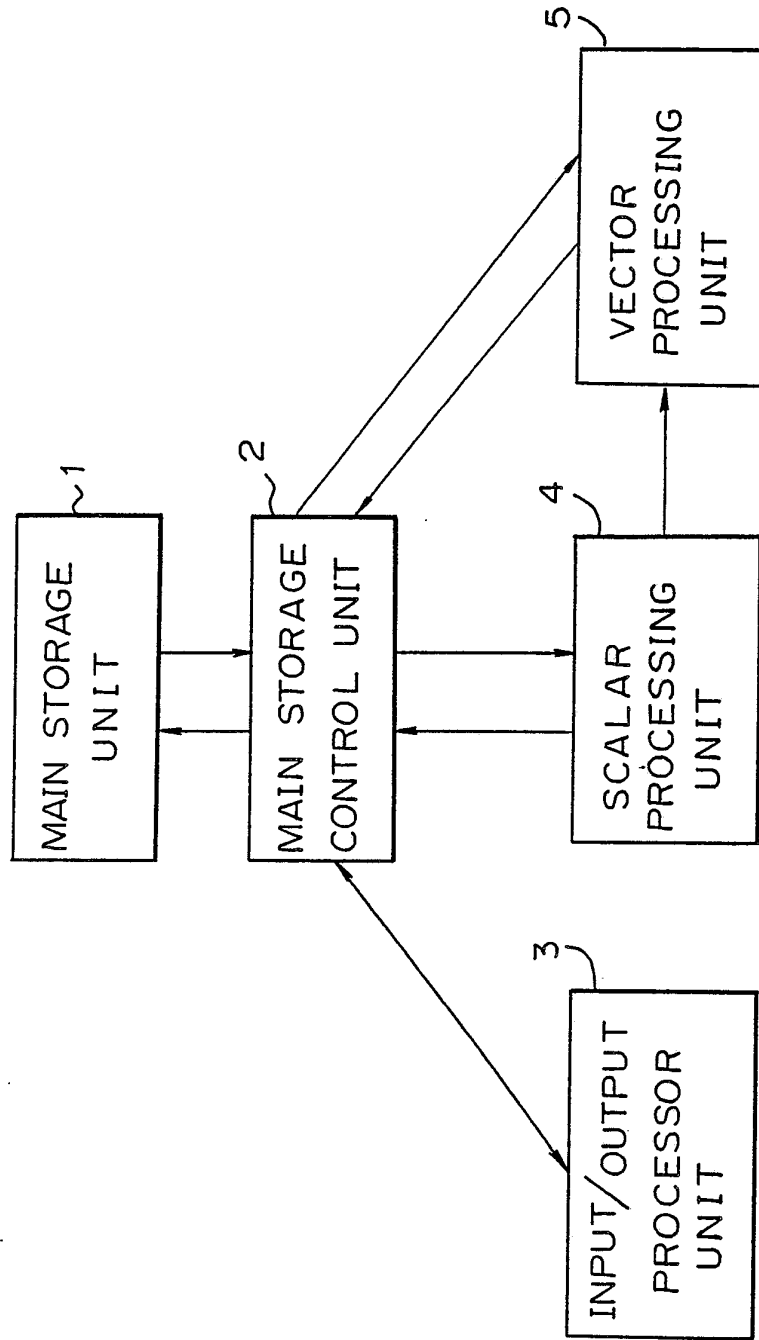said data distribution circuit transfers said input operands and said calculated odd and even terms.
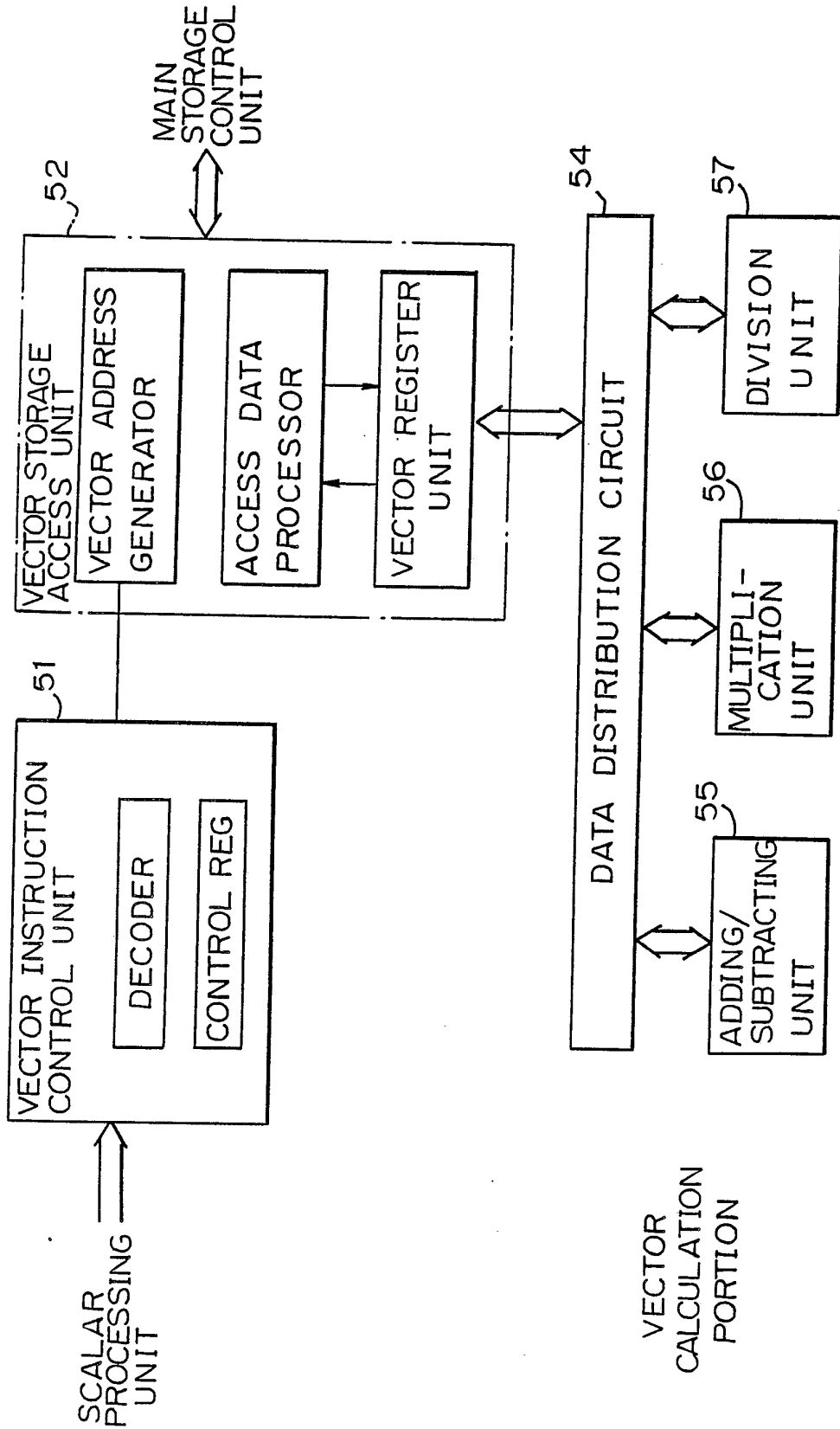
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Fig. I

Fig. 2
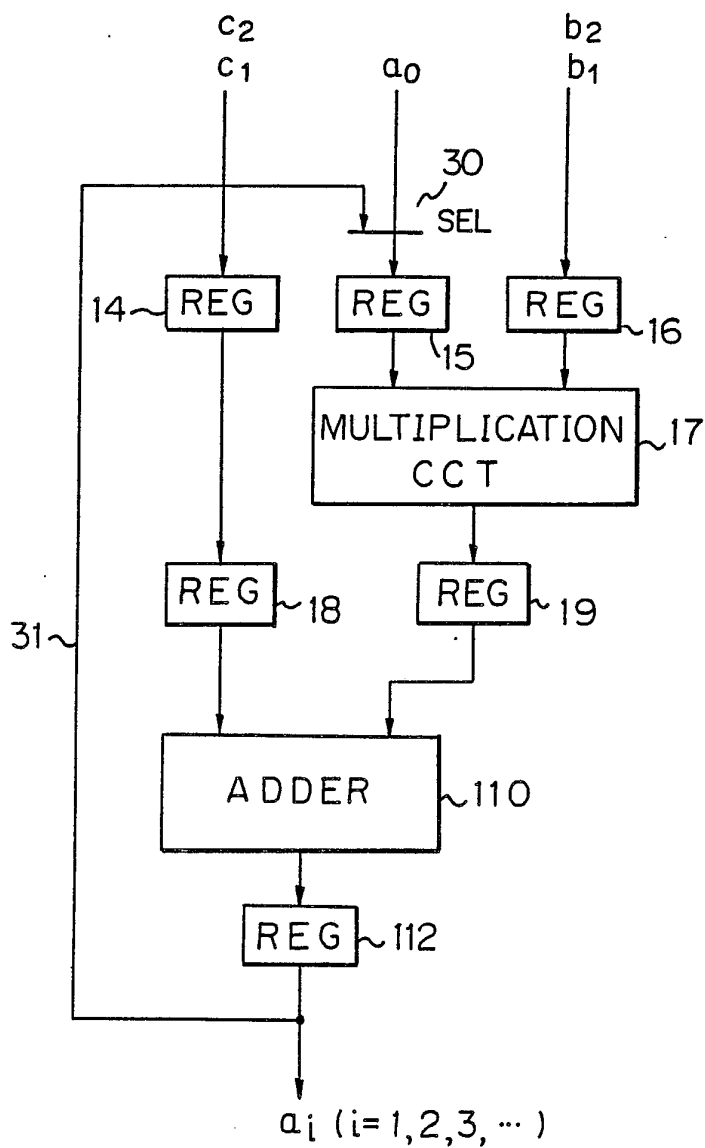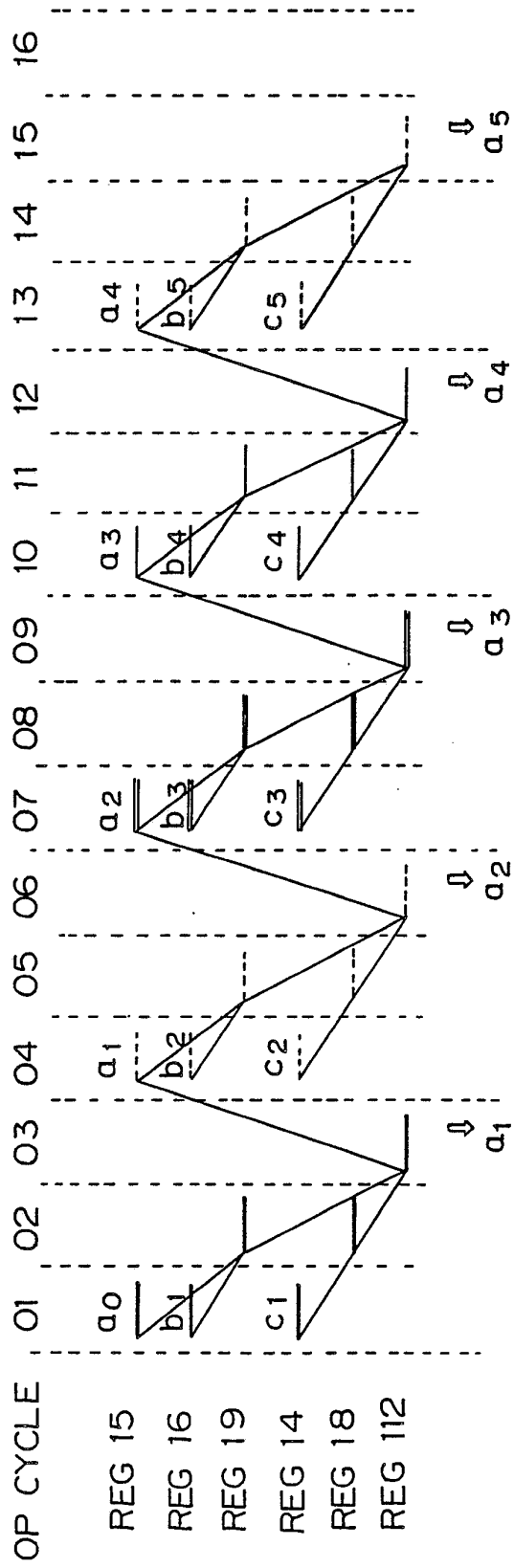
Fig. 3

a_i (i=1,2,3, ⋯)

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Fig. 4

Fig. 5

DATA DISTRIBUTION CIRCUIT 40a

CALCULATION CIRCUITS 10A & 10B
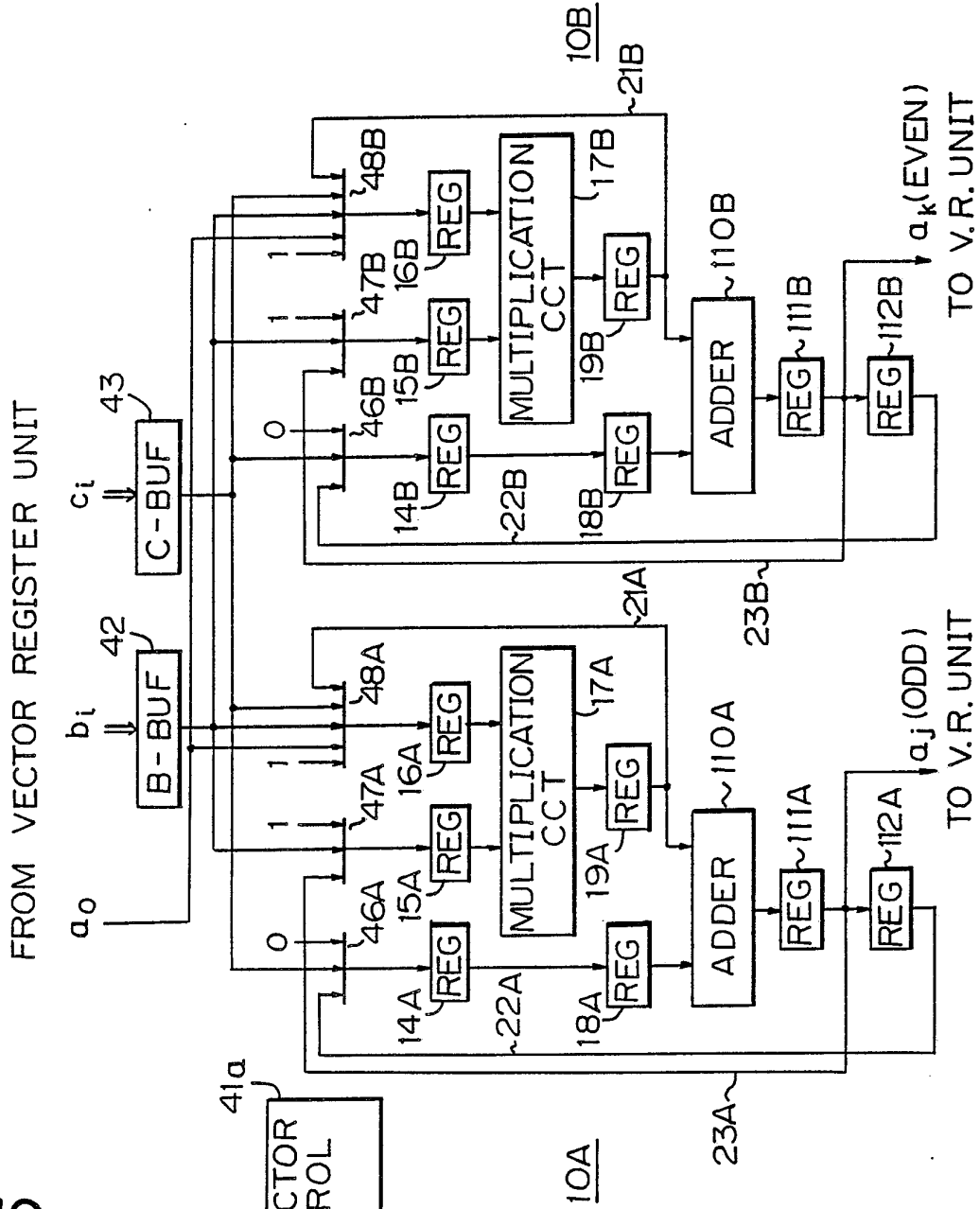
FROM VECTOR REGISTER UNIT
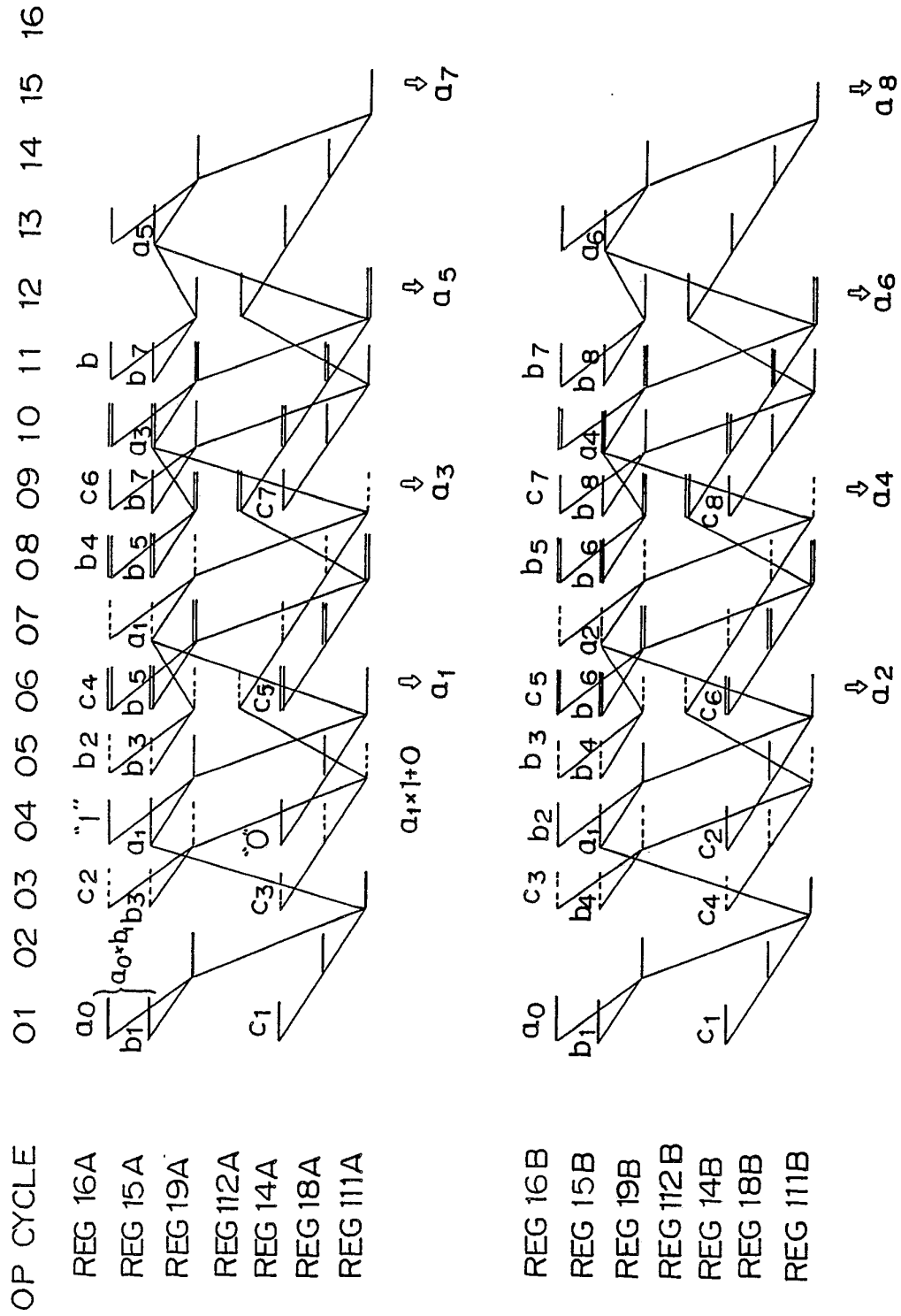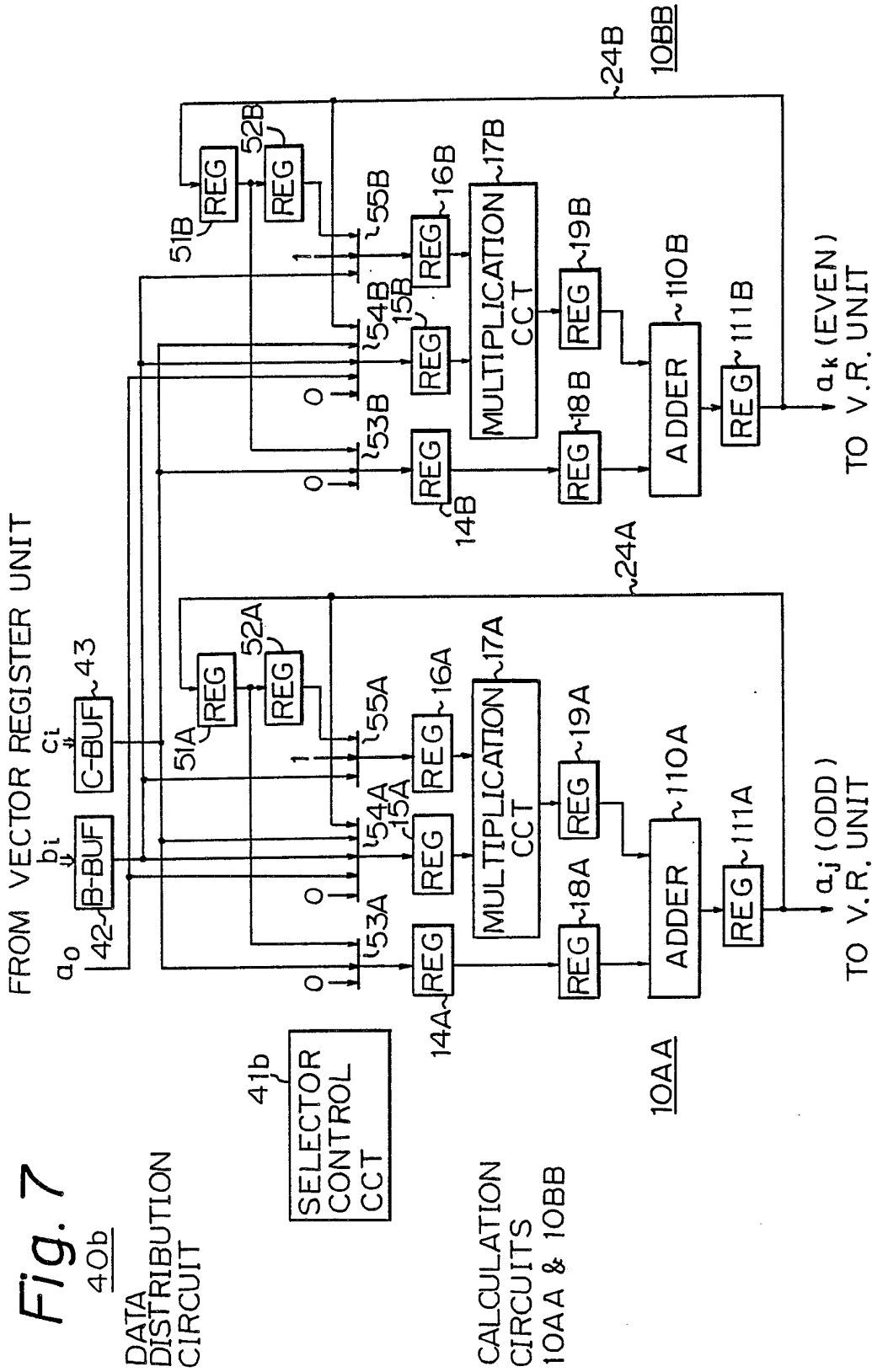
a_o b_i 42 c_i 43

B-BUF   C-BUF

SELECTOR CONTROL CCT   41a

10A   10B

REG   14A   REG   15A   REG   16A
46A   47A   48A
22A
MULTIPLICATION CCT   17A
REG   18A   REG   19A
21A
ADDER   110A
REG   111A
REG   112A
23A
a_j (ODD) TO V.R. UNIT

REG   14B   REG   15B   REG   16B
46B   47B   48B
22B
MULTIPLICATION CCT   17B
REG   18B   REG   19B
21B
ADDER   110B
REG   111B
REG   112B
23B
a_k (EVEN) TO V.R. UNIT

Fig. 6

| OP CYCLE | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |

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Fig. 7

4Ob

DATA
DISTRIBUTION
CIRCUIT

FROM VECTOR REGISTER UNIT

CALCULATION
CIRCUITS
10AA & 10BB

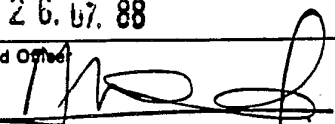# Fig. 8

REFERENCE

10A, 10AA	odd term calculation circuit
10B, 10BB	even term calculation circuit
14A - 16A	register
14B - 16B	register
17A, 17B	multiplication circuit
18A, 19A	register
18B, 19B	register
21A, 22A	feedback line
21B, 22B	feedback line
40a, 40b	data distribution circuit
41a, 41b	selector control circuit
42	B-buffer
43	C-buffer
46A - 48A	selector
46B - 48B	selector
51A, 52A	register
51B, 52B	register
53A - 55A	selector
53B - 55B	selector
110A, 110B ...	adder
111A, 112A ...	register
111B, 112B ...	register

INTERNATIONAL SEARCH REPORT

International Application No PCT/JP 88/00464

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) *

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC^4:   G 06 F 15/06; G 06 F 15/32 .

II. FIELDS SEARCHED

Minimum Documentation Searched [7]	
Classification System	Classification Symbols
IPC^4	G 06 F 15/06; G 06 F 15/32; G 06 F 7/48; G 06 F 7/544

Documentation Searched other than Minimum Documentation
to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
Y	P.M. Kogge: "The Architecture of Pipelined Computers", 1981, Hemisphere Publishing Corp., McGraw-Hill Book Co., (New York, US), pages 181-187, chapter 5 see pages 181-186	4
A	--	1-3,5-16
X	EP, A, 0167061 (CONVEX COMPUTER CORP.) 8 January 1986 see page 38, line 24 - page 44, line 26; figures 10-11	1-3
Y		4
A	--	5-16
A	EP, A, 0169030 (NEC CORP.) 22 January 1986 see page 11, line 20 - page 18, line 18	1-16

-- -- -- -- -- -- -- --

* Special categories of cited documents: [10]

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
4th July 1988	2 6. 07. 88
International Searching Authority	Signature of Authorized Officer
EUROPEAN PATENT OFFICE	M. VAN MOL

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on 18/07/88
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A- 0167061	08-01-86	None	
EP-A- 0169030	22-01-86	JP-A- 61023276	31-01-86