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(54) Title: STORAGE BITCELL

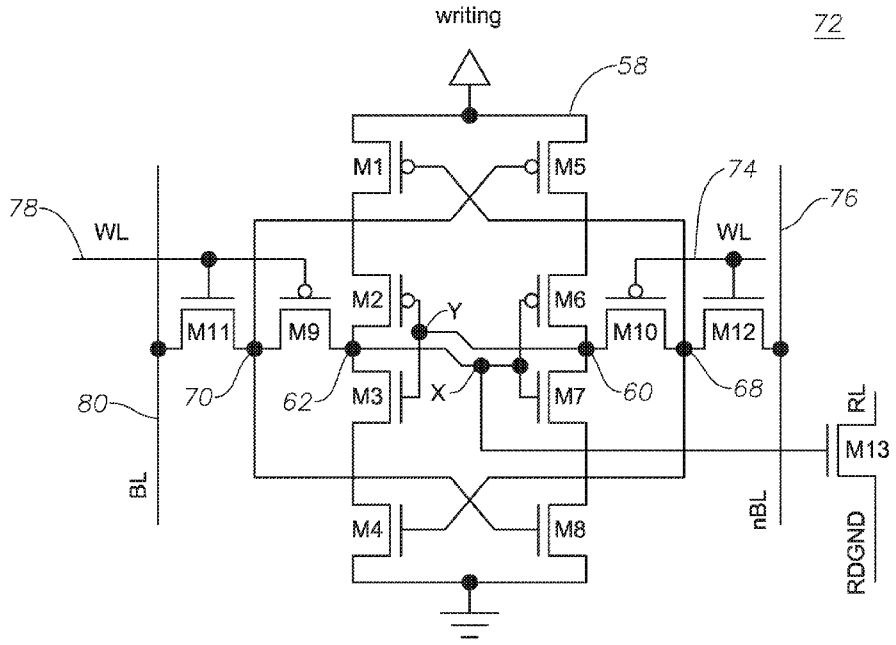

FIG. 4A

(57) Abstract: A storage bitcell comprising a first inverter cross-coupled with a second inverter, both the first and second inverter being in a path between a first potential and a second potential; wherein a first isolator is connected in the path between the first inverter and the first potential. The storage bitcell has particular application as Static Random-Access Memory (SRAM) circuitry.

WO 2017/174979 A1

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Published:

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Storage Bitcell

[0001] The present techniques relate to a storage bitcell. More particularly, the techniques relate to Static Random-Access Memory (SRAM) circuitry and read and write functions associated on the circuitry that allow retention of the bit state and read at ultra-low supply voltages. Memory bitcells according to present techniques with low voltage retention and low read energy have particular, although not exclusive, application for use in energy harvested sensor nodes, such as solar cell powered nodes.

[0002] Cloud computing services are becoming more common. More and more devices are being connected to the cloud, for example as part of the "Internet of Things". For example, relatively small devices such as wireless sensor nodes can be connected to the cloud so that they can be accessed and controlled using remote systems. For example, data from a temperature sensor may be periodically aggregated at a remote location and accessed from another device. Hence, there is an increasing amount of data being sensed and then collected by cloud platforms and their providers. Data may be held in memory bitcells and those bitcells with low voltage retention and low read energy provide greater efficiency of power usage. Efficient power usage is desired where sources of energy may be harvested by a sensor node incorporating a solar cell or where power supply is aggregated across many, perhaps thousands, of sensors.

[0003] Accordingly, providing an electronic storage device with a low retention voltage and low read energy is particularly beneficial.

[0004] According to a first technique, there is provided a storage bitcell comprising a first inverter cross-coupled with a second inverter, both the first and second inverter being in a path between a first potential and a second potential; wherein a first isolator is connected in the path between the first inverter and the first potential.

[0005] In techniques, the storage bitcell is a SRAM cell and the first and second inverters each comprise two transistors in each inverter. The skilled person will be familiar with characterising an SRAM cell by Static Noise Margin (SNM) and SNM can be characterised by the magnitude of noise voltage required to flip a stored state. Noise may occur on both first and second potential sources such as on supply and ground lines, a substrate upon which the inverters are formed and through capacitive

coupling on internal nodes of the storage circuitry. When an external noise is larger than the SNM, the state of the SRAM cell can change and data can be lost.

[0006] In operation, the first inverter may hold a "1" at a first potential and may only flip to a "0" in the presence of a second potential, such as a ground voltage. Accordingly, present techniques provide an isolator between the second potential and the first inverter to increase the magnitude of noise required to cause the flip.

[0007] Techniques include a second isolator connected in the path between the first inverter and the second potential, a third isolator connected in the path between the second inverter and the first potential, a fourth isolator connected in the path between the second inverter and the second potential.

[0008] Accordingly, a second technique provides a storage bitcell comprising a first inverter cross-coupled with a second inverter, each inverter connected in a path between a first potential and a second potential; wherein a first isolator is connected in the path between the first inverter and the first potential, a second isolator is connected in the path between the first inverter and the second potential, a third isolator is connected in the path between the second inverter and the first potential and a fourth isolator is connected in the path between the second inverter and the second potential.

[0009] In the first and the second techniques when writing into the storage bitcell, the inverter is not isolated so as to enable the data to be written correctly. But in read/retention mode the isolator uses the state already stored to isolate the inverter from the appropriate potential to improve SNM.

[0010] Embodiments will now be described with reference to the accompanying figures of which:

[0011] Figures 1A, 1B, and 1C are schematic diagrams of a read optimised memory system;

[0012] Figure 2 is a schematic diagram of a 6T SRAM storage bitcell;

[0013] Figure 3A is a schematic diagram of a latch structure forming part of a SRAM storage bitcell;

[0014] Figure 3B is a schematic diagram of a latch structure forming part of a SRAM storage bitcell according to a first embodiment;

[0015] Figure 3C is a schematic diagram of a latch structure forming part of a SRAM storage bitcell according to a second embodiment;

[0016] Figures 4A and 4B are schematic diagrams of a 13T SRAM cell according to a third embodiment;

[0017] Figure 5A is a schematic diagram of the 13T SRAM cell in a writing operation and a reading operation; and

[0018] Figure 5B is a schematic diagram of associated timing waveforms for the 13T SRAM cell.

[0019] Referring to Figure 1a, a memory system 10 comprises code for the sensor node Central Processing Unit 12 (CPU) stored in some form of a Non-volatile Memory (NVM) 14 to provide random access memory and a SRAM 16 for a scratch-pad memory. The NVM 14 may be a Flash memory, having a high-voltage operation (say, greater than 1.2V) and an active power operation (say, in the order of a mW). Typically, the SRAM 16 can operate at much lower voltages and have μW order power dissipation.

[0020] A memory system 18 designed for low power operation is illustrated in Figure 1b where the NVM 20 is only turned on during boot-up and code is copied into the SRAM 22. The CPU 24 executes the code from the SRAM 22 while the NVM can be switched off.

[0021] Unlike conventional mobile or high performance computing systems, wireless sensor nodes benefit from a relatively fixed workload for long periods of time. Such wireless sensor nodes may perform the same activity periodically and enter low-power modes upon completion. The periodic activity, which may be initiated by an interrupt, can be specified using a small percentage of the code memory which in its entirety would could comprise of boot-up initialisation routines, communication and network routines as well as cryptographic and security protocol algorithms.

[0022] A memory system 26 in Figure 1c seeks further optimisation. According to present techniques, an ultra-low voltage read-optimized memory 28 is used to allow SRAM 30 to be retained or powered down when not used.

[0023] Referring to Figure 2, a latch circuit such as a 6T SRAM memory cell 32 is shown such as may be used in an SRAM memory system. The 6T SRAM memory cell

32 comprises two p-channel transistors 34, 36 and two n-channel transistors 38, 40. A node 42 is provided between 34 and 38, and similarly a node 44 is provided between 36 and 40. A bit line BL 46 is connected to the node 42 via an access transistor 48. Similarly, an inverted bit line nBL 50 is connected to the node 44 by an access transistor 52. In use, the two sets of transistors 34 and 38, and 36 and 40 are cross-coupled inverters forming a bistable device capable of storing binary information and having both read and write capabilities. A first state can be configured when the node 42 is at ground potential (GND) and the node 44 is at supply voltage potential Vdd. A second state can be configured when the node 42 is at the supply voltage potential Vdd and the node 44 is at the ground potential (GND).

[0024] A schematic diagram of a latch structure 54 forming part of a SRAM storage bitcell is illustrated in Figure 3a with a 1 and 0 being stored by M2, M3 and M6, M7 transistor pairs respectively. Static Noise Margin can be characterised by the magnitude of noise voltage required to flip the stored state and such noise may occur on supply or ground lines, the substrate and through capacitive coupling on internal nodes. Nodes X and Y may be tested using noise voltage sources in order test the stability of the latch structure 54.

[0025] The transistor M2 and M3 pair holds a 1 and can flip to a 0 in the presence of a ground voltage. The transistor M6 and M7 pair holds a 0 and can flip to a 1 in the presence of supply voltage. Referring to Figure 3b, according to an embodiment, the latch structure 54 is modified to a latch structure 56 by isolating the transistor pair M2 and M3 from ground. In this way, the magnitude of noise required to cause the flip of state from a 1 to 0 can be increased. The noise margin can be further improved by isolating a supply voltage potential Vdd to the transistor pair M6 and M7. According to present techniques, the isolation can be provided by using a latch structure 58 as illustrated in Figure 3c.

[0026] Referring to Figure 3c, a latch structure 58 forming part of a SRAM storage bitcell comprises two p-channel transistors M2, M6 and two n-channel transistors M3 and M7. A node Y is provided between a gate terminal of M2 and a gate terminal of M3 and connected to a node 60 between a drain terminal of M6 and a source terminal of M7. The node 60 is connected to further circuitry B, shown in greater detail in Figure 4.

[0027] A node X is provided between a gate terminal of M6 and a gate terminal of M7 and connected to a node 62 between a drain terminal of M2 and a source terminal

of M3. The node 62 is connected to control circuitry A, shown in greater detail in Figure 4.

[0028] In Figure 3c, isolation from a voltage supply rail 64 is provided by using M1 located in an electrical path between M2 and the voltage supply rail 64, and transistor M5 located in an electrical path between M6 and the voltage supply rail 64. Isolation from a ground potential 66 is provided by M4 located in an electrical path between M3 and the ground potential 66, and M8 located in an electrical path between M7 and the ground potential 66.

[0029] In Figure 3c, a gate terminal of isolator M1 is shown connected to a gate terminal of isolator M4 and a gate terminal of isolator M5 is shown connected to a gate terminal of isolator M8. Referring to Figure 4, the connection of isolators M1 and M4 occurs through a node 68 and connection of isolators M5 and M8 occurs through a node 70.

[0030] Figure 4 is a schematic diagram of a bitcell 72 according to present techniques. In operation, bitcell 72 is shown in a writing mode (Figure 4a) and a reading mode (Figure 4b).

[0031] Referring to Figure 4a, the latch structure 58 forming part of the SRAM storage bitcell 72 comprises two p-channel transistors M2, M6 and two n-channel transistors M3 and M7. A node Y is provided between a gate terminal of M2 and a gate terminal of M3 and connected to the node 60 between a drain terminal of M6 and a source terminal of M7. The node 60 is connected to control circuitry B (not shown in Figure 4) comprising a source terminal of a p-channel transistor M10 having a drain terminal connected to node 68, which sits in an electrical path between isolators M1 and M4. A gate terminal of M10 is connected to a word-line WL 74. The n-channel transistor M12 comprises a source terminal connected to the node 68, a gate terminal connected to the word-line WL 74 and a drain terminal connected to an inverted bit line nBL 76.

[0032] Also in Figure 4, the node X is provided between a gate terminal of M6 and a gate terminal of M7 and is connected to the node 62 between a drain terminal of M2 and a source terminal of M3. The node 62 is connected to control circuitry A (not shown in Figure 4) comprising of a drain terminal of a p-channel transistor M9 having a source terminal connected to node 70, which sits in an electrical path between isolators M5 and M8. A gate terminal of M9 is connected to a word-line WL 78. The

n-channel transistor M11 comprises a drain terminal connected to the node 70, a gate terminal connected to the word-line WL 78 and a source terminal connected to a bit line, BL 80. As also seen in Figure 4, a gate terminal of n-channel transistor M13 is connected to node X having source terminal connected to read line to ground (RDGND) and drain terminal connected to read line (RL). Although not shown in Figure 4, a sense amplifier can be used for differential reads.

[0033] Accordingly, with reference to Figure 4 in comparison with the techniques illustrated with reference to Figure 3c, transistors M9 and M10 are added to the bitcell layout of Figure 4 to allow differential writes and transistor M13 is added for single-ended read. The bit line BL 80 is connected to the node 62 via the access transistor M11. Similarly, the inverted bit line nBL 76 is connected to the node 60 by the access transistor M12.

[0034] Figure 4a illustrates techniques for writing by placing data on the bitlines BL 80 and nBL 76 and asserting word-line WL 74, 78, which turns off feedback transistors M9 and M10. During retention and read, Figure 4b, word-line WL=0 isolates the bitlines and turns the feedback transistors (M9, M10) on.

[0035] Figure 5a is a schematic diagram of associated timing waveforms for the 13T SRAM cell. The word-line WL 74, 78 is forced high 82 for the simulation. Bit line 80 is high 84 until time period t_w (write delay) commences when it is transitioned to low 86, and inverted bit line nBL 76 is low 88 until time period t_w commences when it is transitioned to high 90. Node 68 (here referred to as inBL) follows the rise and fall of inverted bit line 76, whereas node 70 (here referred to as iBL) follows the rise and fall of bit line 80. Since the access transistors M11 and M12 are NFETS, inBL has a slow rise relative to nBL. IBL=0 turns transistor M5 on causing node Y to build up charge 92. Similarly, inBL=1 turns on transistor M4 causing node X to discharge 94. After a certain time tw dictated by the magnitude of leakage through transistors M3 and M6, nodes X and Y flip to their final states (x=BL and Y=nBL). Using timing techniques described with reference to Figure 5a, the write and read waveforms for different supply voltages, 300mV 96, 600mV 98, 900mV 100 and 1.2V 102, as illustrated in Figure 5b.

[0036] As will be appreciated by one skilled in the art, the present techniques may be embodied as a circuit, a method of driving the circuit and may be controllable by a computer program. Accordingly, the present techniques may take the form of an entirely hardware embodiment or an embodiment combining software and hardware.

[0037] Computer program code for carrying out operations of the present techniques may be written in any combination of one or more programming languages, including object oriented programming languages and conventional procedural programming languages.

[0038] For example, program code for carrying out operations of the present techniques may comprise source, object or executable code in a conventional programming language (interpreted or compiled) such as C, or assembly code, code for setting up or controlling an ASIC (Application Specific Integrated Circuit) or FPGA (Field Programmable Gate Array), or code for a hardware description language such as VerilogTM or VHDL (Very high speed integrated circuit Hardware Description Language).

[0039] It will be clear to one skilled in the art that many improvements and modifications can be made to the foregoing exemplary embodiments without departing from the scope of the present techniques.

[0040] Accordingly, in a first technique a storage bitcell comprises a first inverter cross-coupled with a second inverter, both the first and second inverter being in a path between a first potential and a second potential; wherein a first isolator is connected in the path between the first inverter and the first potential with a state and operation dependent control.

[0041] By state and operation control when writing into the bitcell, the inverter (for example, M2-M3) is not isolated so as to enable the data to be written correctly. But in read/retention mode the isolator uses the state already stored to isolate the inverter from the appropriate rail to improve Signal to Noise Margin.

[0042] In embodiments, a second isolator may be connected in the path between the second inverter and the first potential. Further, a third isolator may be connected in the path between the first invertor and the second potential. A fourth isolator may be connected in the path between the second invertor and the second potential with a state and operation dependent control.

[0043] In embodiments, the first potential is a voltage supply rail and the second potential is a ground rail. The first and second isolators may be p-channel transistors and the third and fourth isolators are n-channel transistors. In embodiments, a gate terminal of the first isolator is connected to gate terminal of the third isolator and a gate terminal of the second isolator is connected to a gate terminal of fourth isolator.

Moreover, a first internal node is located in the path between a gate terminal of the first isolator and the gate terminal of the third isolator and a first access transistor is connected to the first internal node.

[0044] In embodiments, the first access transistor may be connected to a positive bit line and the first access transistor may be a N-channel transistor. In embodiments the first access transistor is connected to the first internal node by a P-channel transistor.

[0045] According to techniques, a second internal node may be located in the path between a gate terminal of the second isolator and the gate terminal of the fourth isolator and a second access transistor is connected to the second internal node.

[0046] Herein, the second access transistor may be connected to an inverted bit line. In embodiments, the second access transistor is an n-channel transistor and the second access transistor may be connected to the second internal node by a p-channel transistor. In embodiments, a read transistor is provided on a read line and is connected to a node of the second invertor and the read transistor is an n-channel transistor.

[0047] In all embodiments, the present techniques are particularly suited to use in a Static Random-Access Memory (SRAM) circuitry comprising a storage bitcell described herein.

CLAIMS

1. A storage bitcell comprising a first inverter cross-coupled with a second inverter, both the first and second inverter being in a path between a first potential and a second potential; wherein a first isolator is connected in the path between the first inverter and the first potential.

2. The storage bitcell of claim 1, wherein a second isolator is connected in the path between the second inverter and the first potential.

3. The storage bitcell of claim 2 wherein a third isolator is connected in the path between the first invertor and the second potential.

4. The storage bitcell of claim 3, wherein a fourth isolator is connected in the path between the second invertor and the second potential.

5. The storage bitcell of claim 1, wherein the first potential is a voltage supply rail and the second potential is a ground rail.

6. The storage bitcell of claim 1, wherein the first and second isolators are p-channel transistors and the third and fourth isolators are n-channel transistors.

7. The storage bitcell of claim 6 wherein a gate terminal of the first isolator is connected to gate terminal of the third isolator and a gate terminal of the second isolator is connected to a gate terminal of fourth isolator.

8. The storage bitcell of claim 7 wherein a first internal node is located in the path between a gate terminal of the first isolator and the gate terminal of the third isolator and a first access transistor is connected to the first internal node.

9. The storage bitcell of claim 8, wherein the first access transistor is connected to a positive bit line.

10. The storage bitcell of claim 9, wherein the first access transistor is a N-channel transistor

11. The storage bitcell of claim 10, wherein the first access transistor is connected

to the first internal node by a p-channel transistor

12. The storage bitcell of claim 6 wherein a second internal node is located in the path between a gate terminal of the second isolator and the gate terminal of the fourth isolator and a second access transistor is connected to the second internal node.

13. The storage bitcell of claim 12 wherein the second access transistor is connected to an inverted bit line.

14. The storage bitcell of claim 13, wherein the second access transistor is an n-channel transistor

15. The storage bitcell of claim 14, wherein the second access transistor is connected to the second internal node by a p-channel transistor

16. The storage bitcell of claim 1, wherein a read transistor is provided on a read line and is connected to a node of the second invertor.

17. The storage bitcell of claim 16, wherein the read transistor is an n-channel transistor.

18. Static Random-Access Memory (SRAM) circuitry comprising the storage bitcell of claim 1.

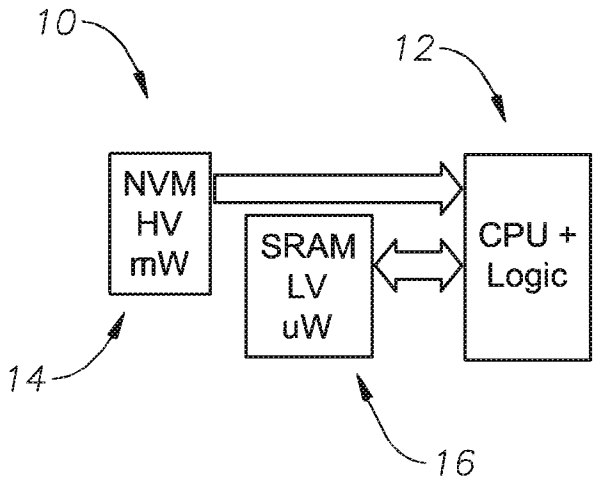


FIG. 1A

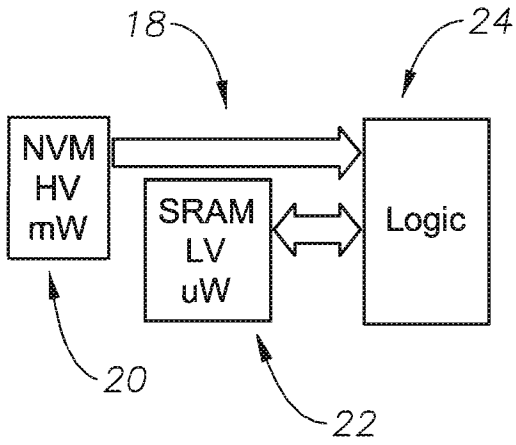


FIG. 1B

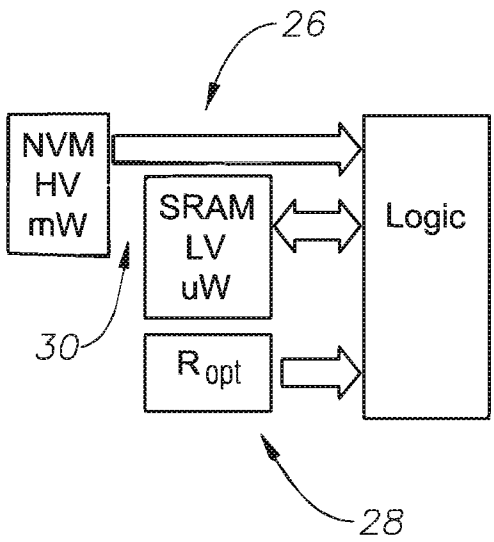


FIG. 1C

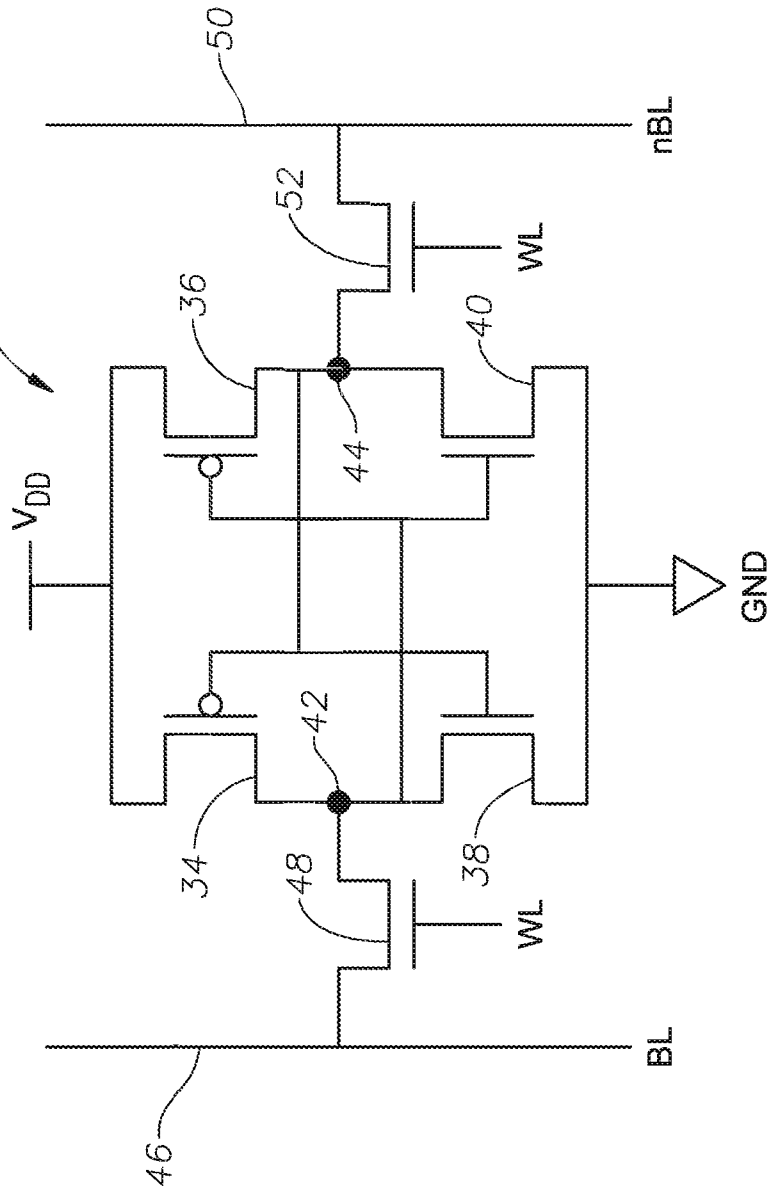


FIG. 2

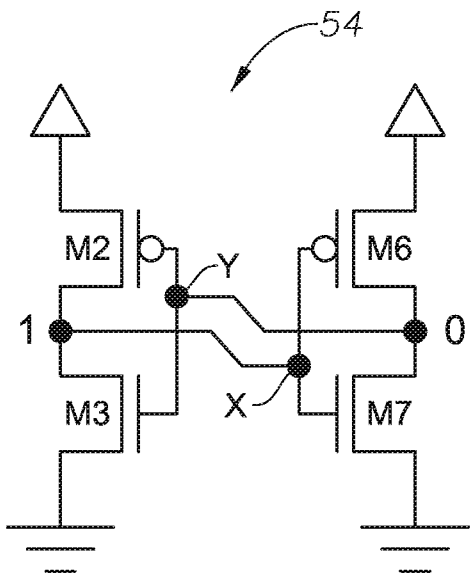


FIG. 3A

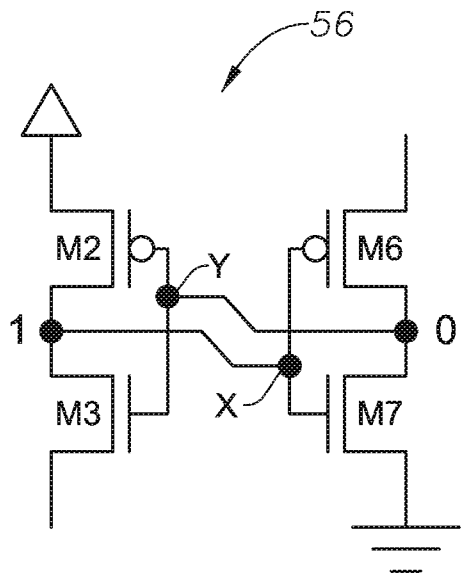


FIG. 3B

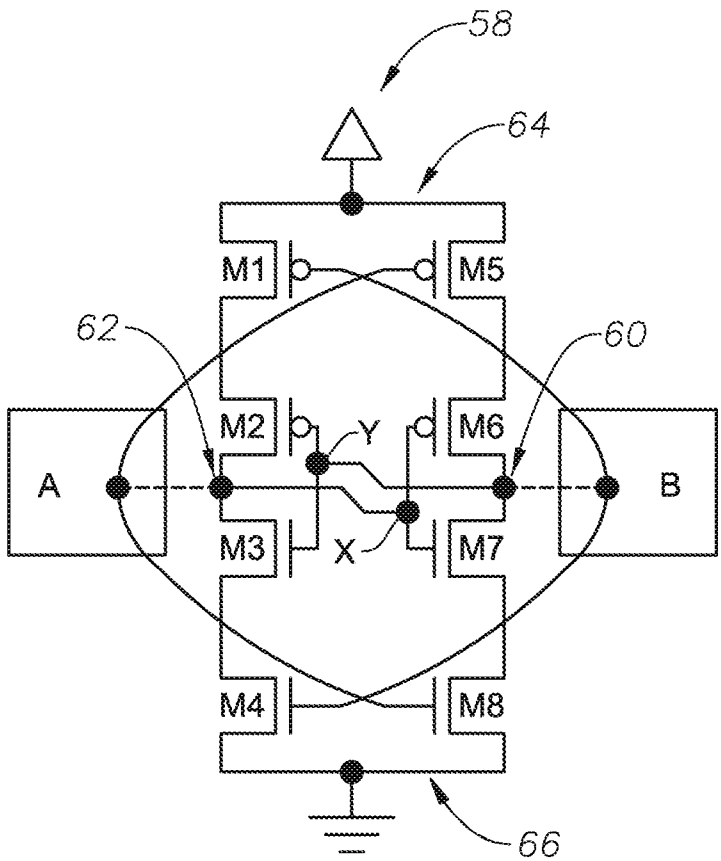
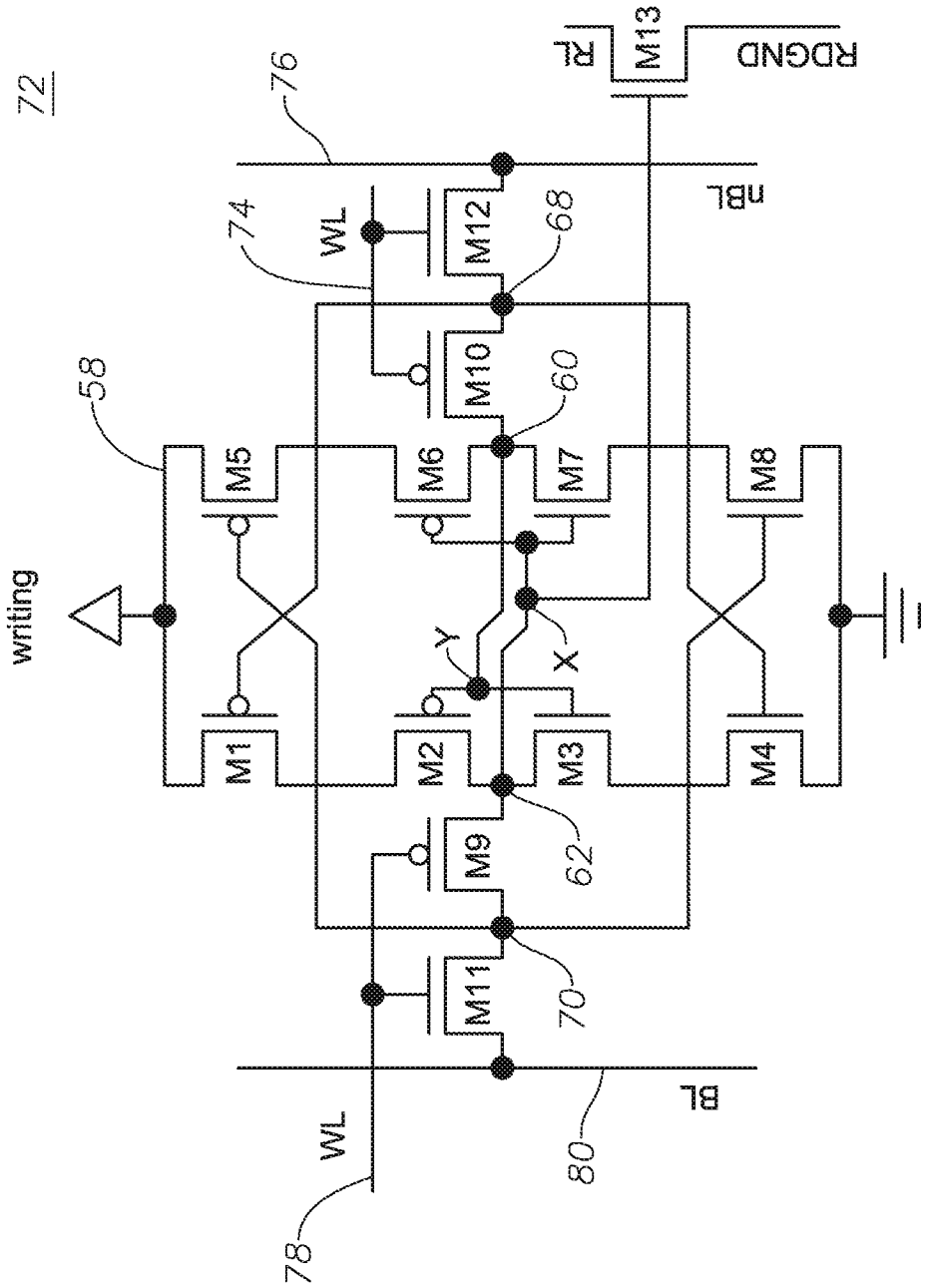


FIG. 3C


72
76
RDGND
RP
M13
nBL
74
WL
M12
68
M10
60
58
M5
M6
M7
M8
writing
Y
X
M1
M2
M3
M4
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M9
M11
70
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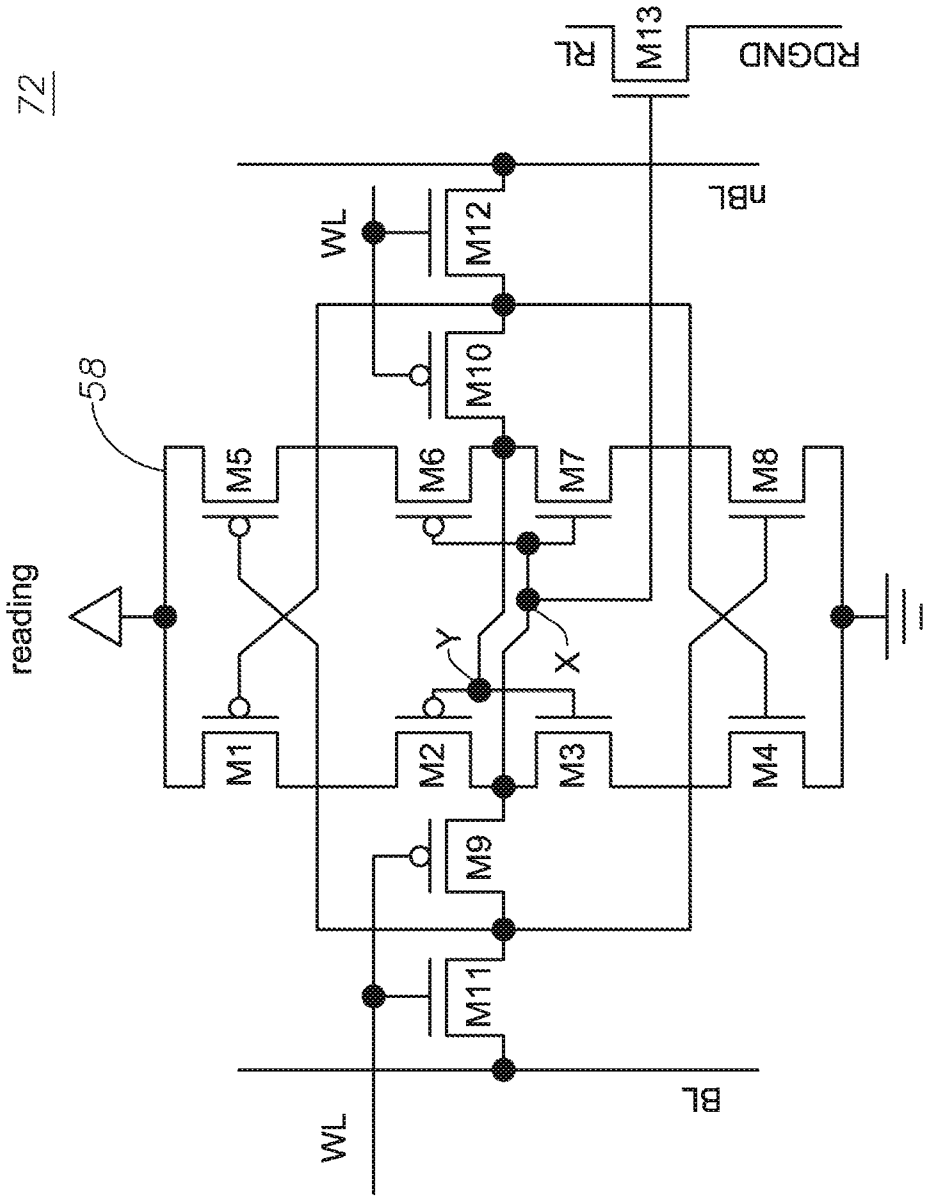
BL
78
80

FIG. 4A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M9
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BL

FIG. 4B

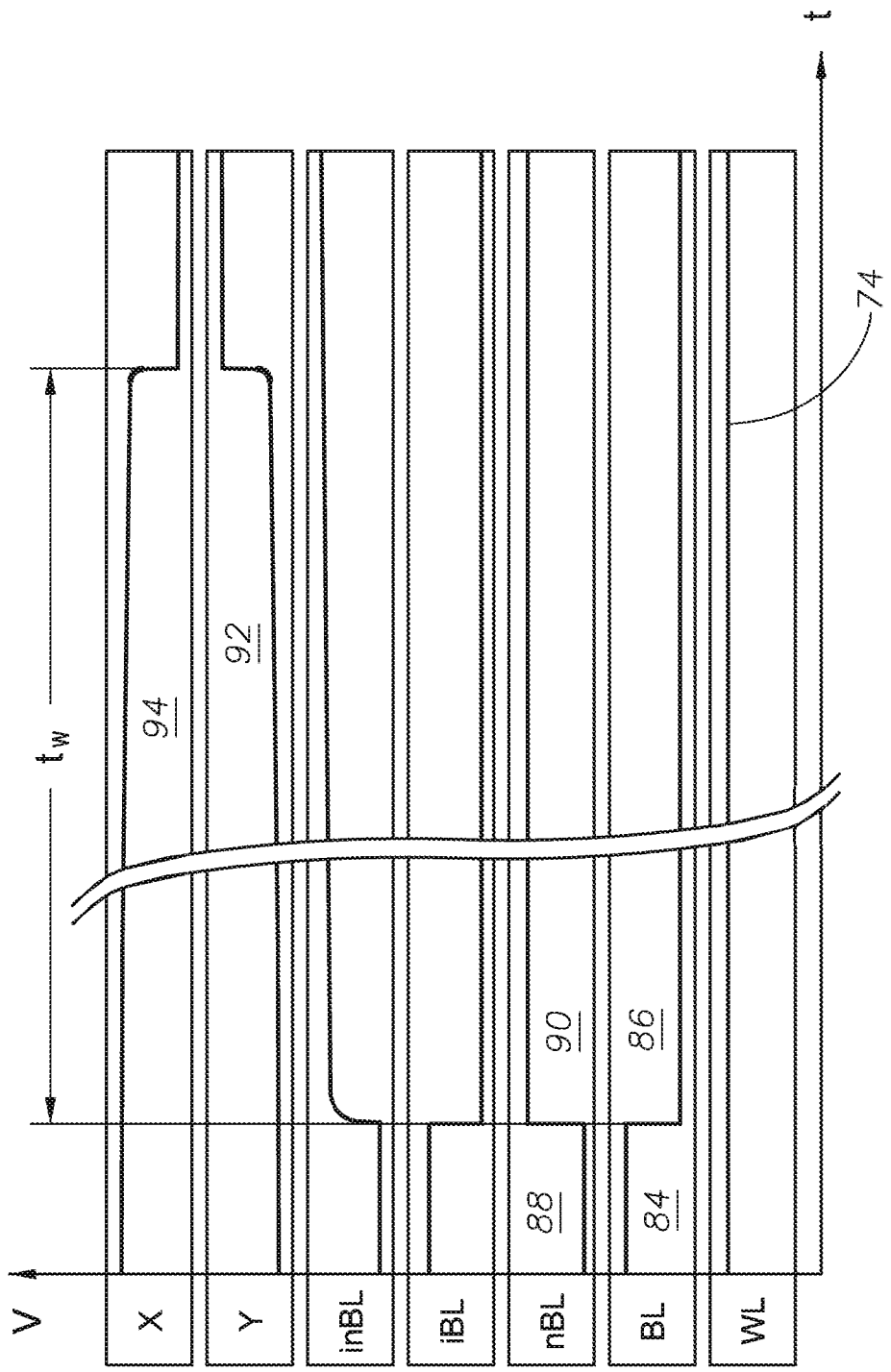
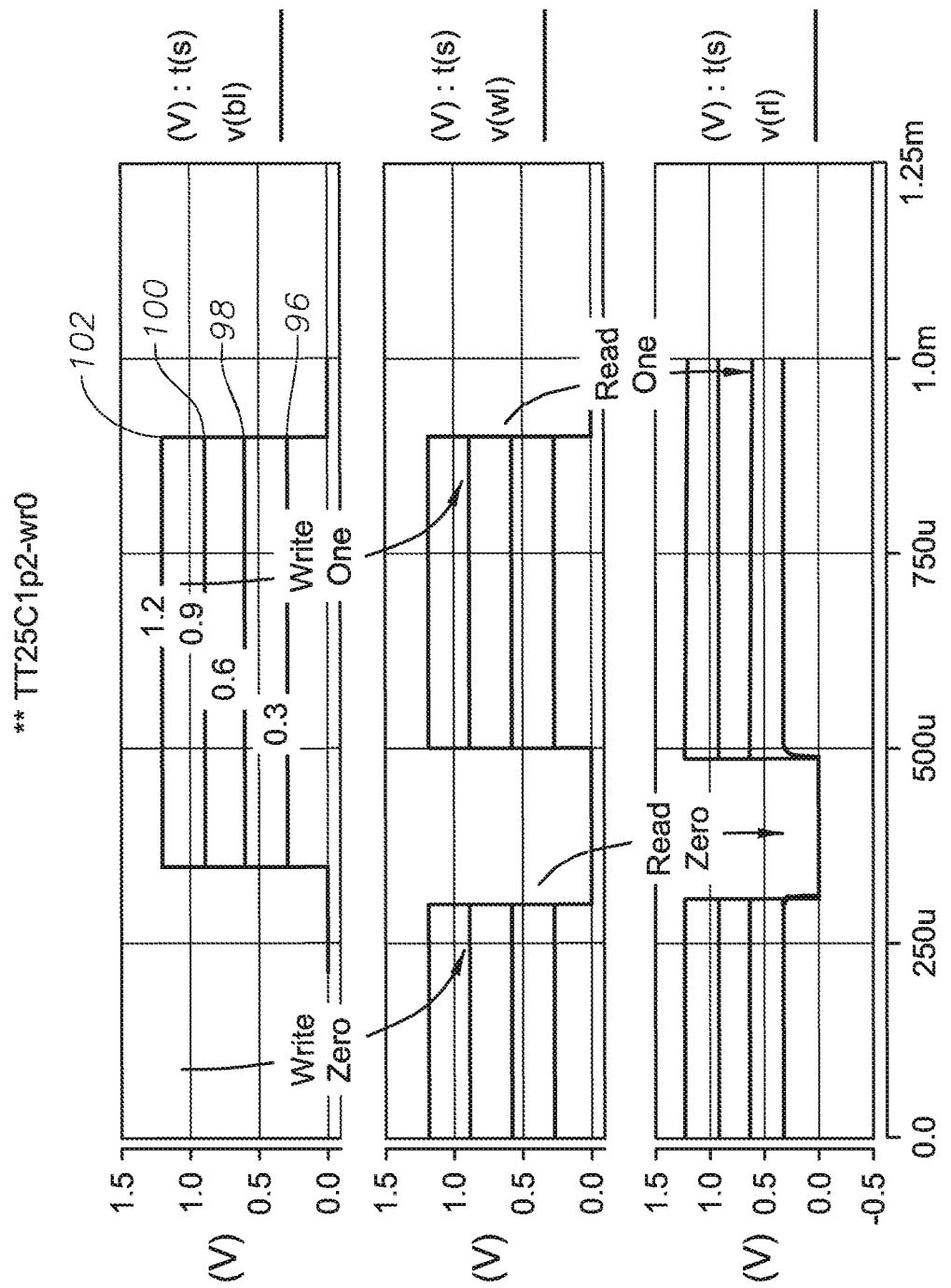


FIG. 5A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Read
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Read
One
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v(bl)
(V) : t(s)
v(wl)
(V) : t(s)
v(rl)
(V)
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750u
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t(s)

FIG. 5B

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2017/050945

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C11/412
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 5 311 070 A (DOOLEY JERRY G [US]) 10 May 1994 (1994-05-10) column 1, line 5 - line 27 column 4, line 65 - column 5, line 13; figure 4 -----	1-7 8,12
X Y	US 5 680 356 A (YAMAUCHI HIROYUKI [JP]) 21 October 1997 (1997-10-21) column 1, line 5 - line 14 column 42, line 54 - column 45, line 14; figures 17a, 17b -----	1-6,9, 10,13, 14,18 8,12,16, 17
Y	US 2014/138776 A1 (CHANG JACKLYN [US] ET AL) 22 May 2014 (2014-05-22) paragraph [0021]; figure 1A ----- -/--	16,17

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search	Date of mailing of the international search report
20 June 2017	13/07/2017

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

International application No
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