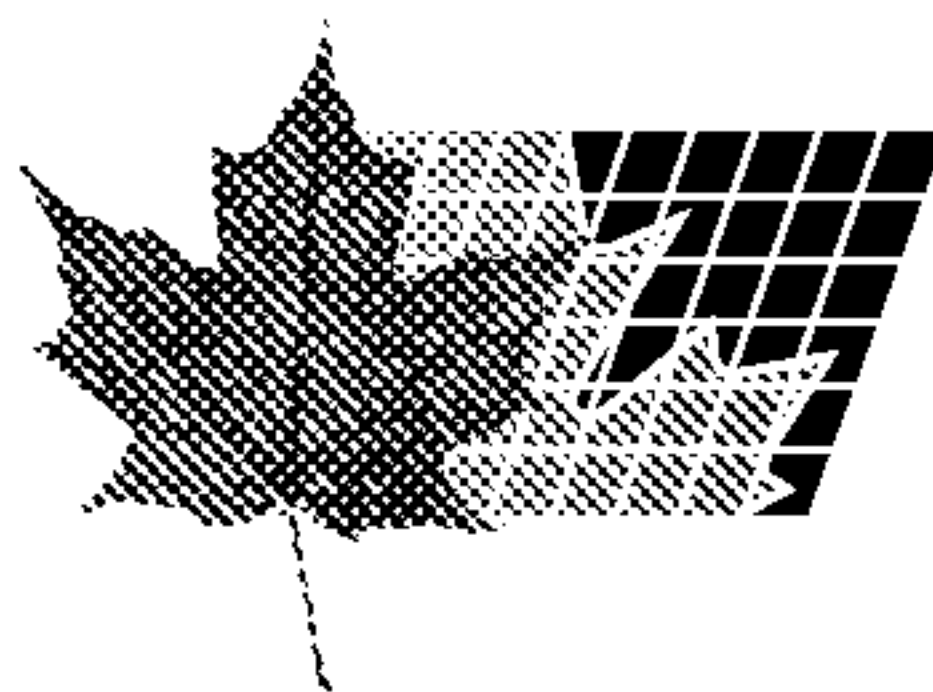




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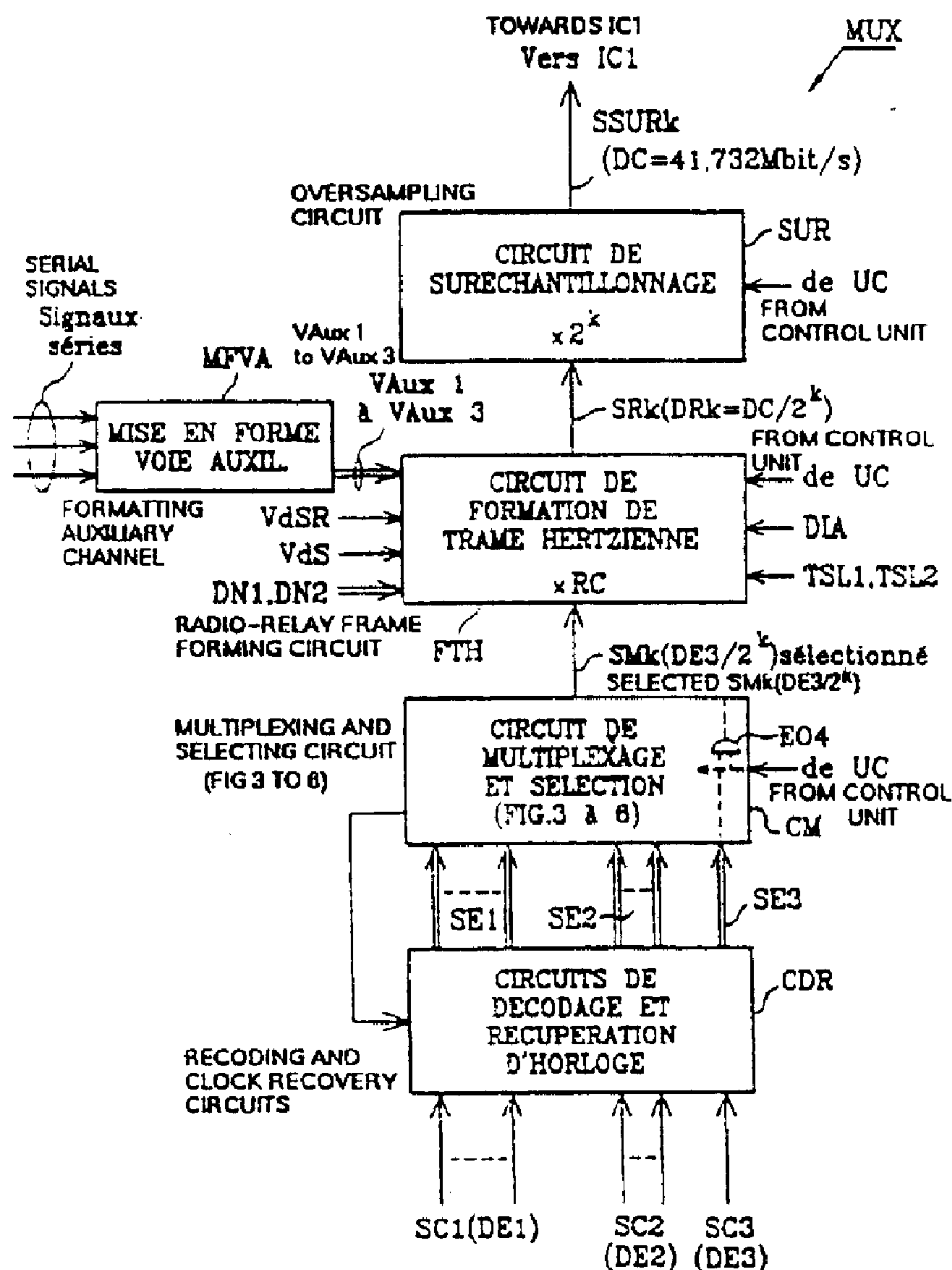
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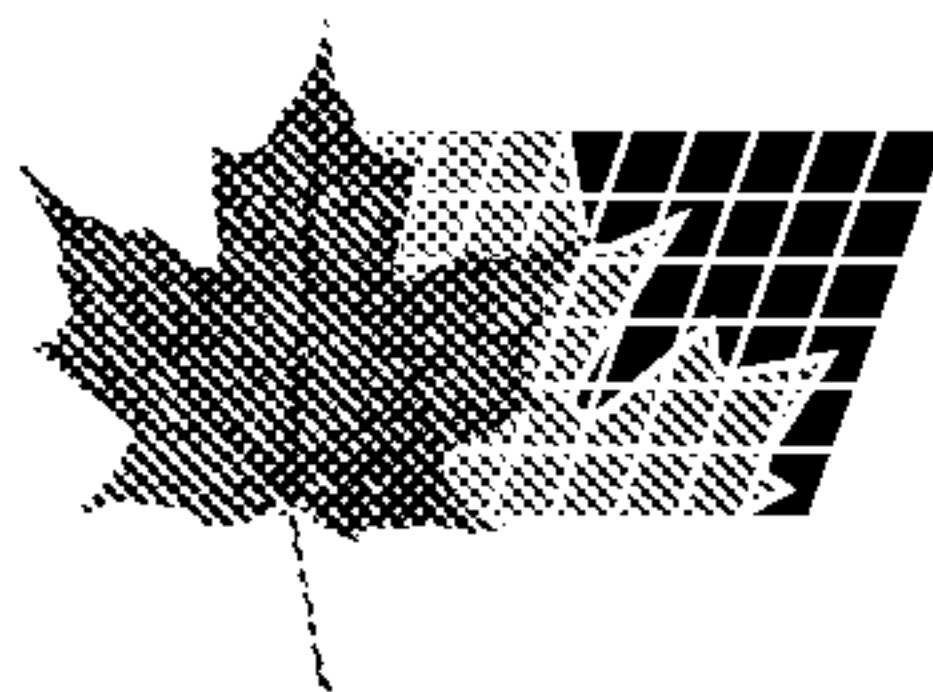
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(54) **TRAME NUMERIQUE POUR STATION HERTZIENNE**

(54) **DIGITAL FRAME FOR RADIO-RELAY STATION**





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(57) Une station hertzienne est rendue compatible avec la transmission d'un groupe sélectionné quelconque parmi des groupes de signaux plésiochrones à multiplexer afin d'inclure dans la station des circuits programmables communs aux groupes, indépendamment du débit du signal résultant du multiplexage. Une trame avec une structure indépendante du débit est formée en constituant des groupes de signaux plésiochrones (SE1, SE2, SE3) ayant des débits (DE1, DE2, DE3) sensiblement multiples entiers entre eux, sélectionnant un groupe, multiplexant les signaux dans le groupe sélectionné en un signal multiplex (SMk), les débits de signaux multiplex étant multiples entiers entre eux, répartissant les bits du signal multiplex dans un champ de longueur prédéterminée dans la trame après multiplication du débit du signal multiplex par une constante, et formant un signal résultant (SRk) par insertion dans la trame d'un mot de verrouillage et d'un champ de bits supplémentaires de longueurs prédéterminées.

(57) The invention concerns a radio-relay station made compatible with any selected group among groups of plesiochronous signals with multiplexer so as to include in the station programmable circuits common to the groups., independently of the signal speed resulting from multiplexing. A frame with a structure independent of the speed is formed by constituting groups of plesiochronous signals (SE1, SE2, SE3) with substantially whole mutually multiple speeds (DE1, DE2, DE3), selecting a group, multiplexing the signals in the selected group into a multiplex signal (SMk), the speeds of the multiplex signals being whole mutually multiple, distributing the multiplex signal bits in a field of predetermined length in the frame after multiplying the multiplex signal speed by a constant, and forming a resulting signal (SRk) by inserting into the frame a lockword and a field of supplementary bits or predetermined length.



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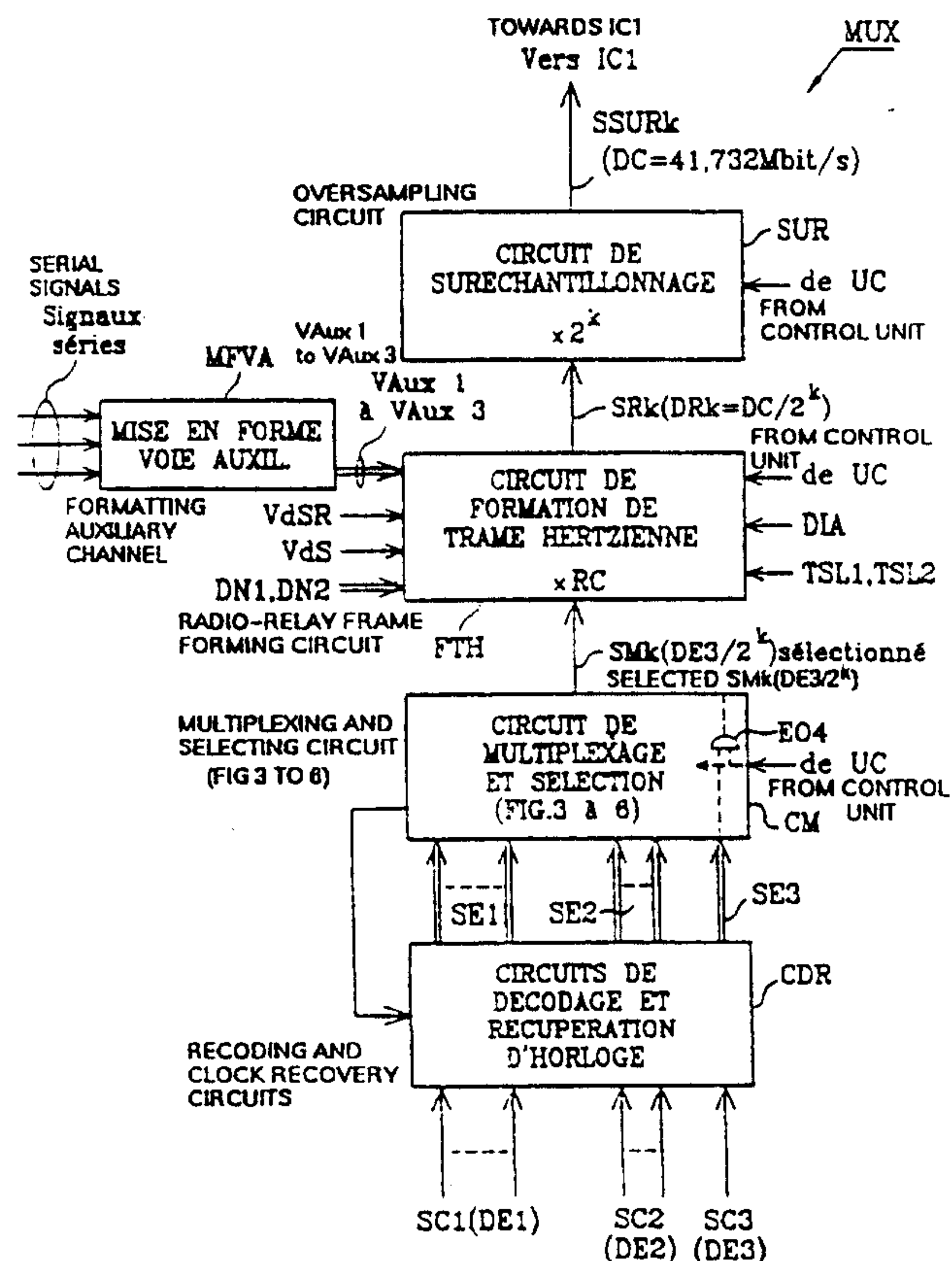
(54) Titre: TRAME NUMERIQUE POUR STATION HERTZIENNE

(57) Abstract

The invention concerns a radio-relay station made compatible with any selected group among groups of plesiochronous signals with multiplexer so as to include in the station programmable circuits common to the groups, independently of the signal speed resulting from multiplexing. A frame with a structure independent of the speed is formed by constituting groups of plesiochronous signals (SE1, SE2, SE3) with substantially whole mutually multiple speeds (DE1, DE2, DE3), selecting a group, multiplexing the signals in the selected group into a multiplex signal (SMk), the speeds of the multiplex signals being whole mutually multiple, distributing the multiplex signal bits in a field of predetermined length in the frame after multiplying the multiplex signal speed by a constant, and forming a resulting signal (SRk) by inserting into the frame a lockword and a field of supplementary bits or predetermined length.

(57) Abrégé

Une station hertzienne est rendue compatible avec la transmission d'un groupe sélectionné quelconque parmi des groupes de signaux plésiochrones à multiplexer afin d'inclure dans la station des circuits programmables communs aux groupes, indépendamment du débit du signal résultant du multiplexage. Une trame avec une structure indépendante du débit est formée en constituant des groupes de signaux plésiochrones (SE1, SE2, SE3) ayant des débits (DE1, DE2, DE3) sensiblement multiples entiers entre eux, sélectionnant un groupe, multiplexant les signaux dans le groupe sélectionné en un signal multiplex (SMk), les débits de signaux multiplex étant multiples entiers entre eux, répartissant les bits du signal multiplex dans un champ de longueur prédéterminée dans la trame après multiplication du débit du signal multiplex par une constante, et formant un signal résultant (SRk) par insertion dans la trame d'un mot de verrouillage et d'un champ de bits supplémentaires de longueurs prédéterminées.



BACKGROUND OF THE INVENTION

5 The present invention concerns a digital frame having a predetermined length, expressed as a number of bits, resulting from multiplexing plesiochronous digital signals, and a method of forming such a frame.

10 The invention is used in particular in a radio station which comprises an essentially digital transceiver at the base of the station and a radio transceiver at the top of a building or a mast, for example, and connected by transmission cable to the first transceiver.

15 A group of plesiochronous digital signals having bit rates standardized at 2.048 Mbit/s or 8.448 Mbit/s, for example, is applied to the transceiver which multiplexes the signals into a particular frame. Each group of plesiochronous signals corresponds to a particular radio station.

20 However, radio beam users are increasingly confronted with the problem of optimizing their radio stations to adapt them to changing customer requirements. For a given radio beam, if the stations exchanging a multiplex signal at 2×2 Mbit/s must exchange a
25 multiplex signal at 4×2 Mbit/s or 8 Mbit/s, for example, many circuits must be modified and changed in all the stations to adapt them to the characteristics of the new multiplex signal to be transmitted, in particular its bit rate and frame characteristics.

30

OBJECTS OF THE INVENTION

An object of the present invention is to reduce the cost of a radio station by introducing into it circuits
35 which can be selected and programmed according to the bit

rate of the signal resulting from multiplexing any group of plesiochronous signals selected from several groups of plesiochronous signals to be multiplexed and possible to be transmitted, so that the radio station can be used
5 whatever the bit rate of the resulting signal corresponding to the selected group. More particularly, another object of the invention is to provide a digital frame having a predetermined length which contributes to achieving the above object and which is intended to
10 transport different bit rates of signals resulting from multiplexing plesiochronous digital signals.

SUMMARY OF THE INVENTION

15 Accordingly, a digital frame having a predetermined length resulting from multiplexing plesiochronous digital signals, is characterized by a constant length and a structure independent of the bit rates of the signals each resulting from multiplexing plesiochronous digital
20 signals constituting a group selected from several groups of plesiochronous digital signals having bit rates which are substantially multiples of each other, the bit rates of the resulting signals being submultiples of the highest bit rate of the resulting signals.

25 The frame structure is therefore constant regardless of the bit rate of the signal resulting from multiplexing. As will emerge in the later description of preferred embodiments of the invention, the same circuits in radio emitting and receiving means of a radio station
30 are programmable only as a function of the bit rate of the resulting signal.

The digital frame of the invention is also used to transmit additional service information by reserving a minimum bit rate for some of that information.

35 More precisely, the frame comprises a frame

alignment word, a multiplexed signal bit field and an additional bit field having respective predetermined lengths. The ratio of the bit rates of the resulting signal including the frame and a selected multiplex
5 signal obtained substantially directly by multiplexing plesiochronous signals of the selected group is constant and independent of the bit rates of the multiplex signals.

The additional bit field can include a constant
10 allocation field, a variable allocation field varying as a function of the bit rate of the selected multiplex signal, and an error correcting code field, the fields having respective predetermined lengths.

The constant allocation field includes bits for
15 collecting error information and/or quality bits.

The variable allocation field can include bits of auxiliary channels whose bit rates increase as the bit rate of the respective multiplex signal increases. The variable allocation field can also include bits which are
20 reserved for a predetermined number of telephone and/or data transmission channels and whose number decreases as the bit rate of the selected multiplex signal increases. The variable allocation field can include bits allocated to a telephone service channel whose number decreases as
25 the bit rate of the selected multiplex signal increases, and the constant allocation field includes a bit indicating a call request on the telephone service channel.

The invention concerns too a method of forming the
30 digital frame defined above. It is characterized by the following steps : constituting groups of plesiochronous digital signals from a plurality of given plesiochronous digital signals having bit rates which are substantially multiples of each other, selecting one of the
35 plesiochronous digital signal groups, multiplexing the

plesiochronous digital signals in the selected group into
a selected multiplex signal, the multiplex signals
respectively resulting from the multiplexing of the
plesiochronous digital signals in the groups having bit
5 rates which are multiples of each other, distributing the
bits of the selected multiplex signal in a field of
predetermined length in the frame after multiplication of
the bit rate of the selected multiplex signal by a
constant, and forming a resulting signal having said
10 frame by inserting therein a frame alignment word and an
additional bit field having predetermined lengths.

If the resulting signal must be transmitted via a
transmission medium at a predetermined bit rate, such as
the transmission cable between the transceivers of a
15 radio station, the bit rate of the resulting signal is at
most equal to the constant bit rate on a transmission
medium, and the resulting signal is oversampled with an
oversampling ratio between the bit rate of the
transmission medium and the bit rate of the resulting
20 signal so as to transmit an oversampled signal at said
constant bit rate on the transmission medium, regardless
of the bit rate of the selected resulting signal and
therefore regardless of the bit rates of the
plesiochronous digital signals of the selected group.

25 In a radio station wherein the transmission medium
such as a cable connects a transceiver at the base of a
radio station and a radio transceiver of the radio
station, the method comprises in the radio transceiver a
step of undersampling the oversampled resulting signal
30 with the reciprocal of the oversampling ratio and a step
of selecting frequency filters as a function of the
oversampling ratio. The width of the frequency bands of
the selected filters increases with the bit rate of the
resulting signal.

35 Often in practice, the bit rates DE1 and DE2 of

first and second plesiochronous digital signals are related by the equation $DE2 \approx N.DE1$, and multiplex signals have bit rates significantly greater than $P.DE2$, N and P being integers not less than 0. The steps of selecting a group and multiplexing plesiochronous digital signals in the selected group comprises steps of selecting and multiplexing $N(2^{K-k}-P)$ signals at the bit rate $DE1$ into $(2^{K-k}-P)$ intermediate multiplex signals at the bit rate $DE2$, selecting P plesiochronous digital signals at the bit rate $DE2$, and multiplexing the P selected plesiochronous digital signals at the bit rate $DE2$ and the $(2^{K-k}-P)$ intermediate multiplex signals into the selected multiplex signal, P being an integer in the range from 0 to $2^{(K-k)}$ and k being an integer in the range from 0 to K .

According to an other aspect of the method of the invention, the insertion of the additional bit field into the frame includes inserting a constant allocation field, a variable allocation field varying as a function of the bit rate of the selected multiplex signal and an error correcting code field, said fields having respective predetermined lengths.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the present invention will become more clearly apparent in the light of the following description of several preferred embodiments of the invention, which is given with reference to the corresponding accompanying drawings, in which:

- FIG. 1 is a block diagram of a radio station emitting a frame according to the invention;
- FIG. 2 is a block diagram of a multiplexing device which is included in a transceiver of the radio

station specifically for implementing the frame forming method of the invention;

- FIGS. 3 to 6 are block diagrams of different multiplexing circuits that can be included in the basic transmitter;

- FIGS. 7 to 9 show respective frames for multiplex signals produced in the multiplexing circuits;

- FIG. 10 shows a radio frame according to the invention produced by the transceiver;

- FIGS. 11 to 13 show the composition of respective variable allocation fields for different operating modes corresponding to different multiplexes; and

- FIG. 14 shows a frame structure of an auxiliary channel in a maximum bit rate resulting signal.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1, a radio link station essentially comprises a station transceiver ETR which is generally installed inside a building and a radio transceiver ERA located either on the roof of the building or on a mast near the building. The transceivers are connected by a bidirectional transmission coaxial cable CA which can be up to several hundred meters long.

The first transceiver ETR time-division multiplexes component plesiochronous digital signals SC1, SC2, SC3 into a resulting signal having a "radio" frame according to the invention to be transmitted on the cable CA with a constant bit rate DC. The second transceiver ERA generates a microwave signal at a frequency of a few gigahertz modulated by the resulting signal from the transceiver ETR in order to emit it via an antenna AN. The transceivers ETR and ERA also receive a radio frequency signal containing a radio frame according to the invention and demultiplex it into plesiochronous

digital signals.

In the embodiment of the invention shown in FIG. 1 the first transceiver ETR essentially comprises a digital multiplexing device MUX and a digital demultiplexing device DMUX, an interface IC1 with the cable CA and a microprocessor-based control unit UC with a keypad. The second transceiver ERA essentially comprises an interface IC2, a modulation and radio emission circuit CEM, an undersampling circuit SOE between the output of the interface IC2 and a programmable digital emit filter FIE preceding the circuit CEM, a radio reception circuit CRE, a duplexer DU between the circuits CEM and CRE and an antenna AN, an oversampling circuit SUE between a demodulation and digital filtering circuit FIR following on from the circuit CRE and the interface IC2, and a microcontroller MC. As will become clear in the course of the remainder of the description, the modifications introduced by the invention are essentially concentrated in the digital multiplexing and demultiplexing devices MUX and DMUX and, to a lesser degree, in the circuits SOE-CEM and CRE-SUE of the transceiver ERA.

The remainder of the description covers in detail the constitution of a digital frame in the multiplexing device MUX according to the invention as a function of numerical values for the bit rate, duration, frequency and length expressed as numbers of bits, and given herein by way of example.

The multiplexing device MUX in the transceiver ETR at the base of the radio link station can receive component plesiochronous digital signals SC1, SC2, SC3 having standardized bit rates $DE1 = 2.048 \text{ Mbit/s}$, $DE2 = 8.448 \text{ Mbit/s}$ and $DE3 = 34.368 \text{ Mbit/s}$, i.e. having bit rates which are substantially integer multiples of each

other, since $DE3 \approx 4.DE2$ and $DE2 \approx 4.DE1$. The bit rate DC on the cable CA is constant and equal to 41.732 Mbit/s, which imposes, as see below, a sum of the bit rates of the plesiochronous signals to be multiplexed together incoming the transceiver ETR not greater than the incoming maximum bit rate $DE3 = 34.368$ Mbit/s.

The frame structure according to the invention transmitted on the cable CA is common to four modes of operation M0 to M3 which respectively correspond to numbers of plesiochronous signals at the lowest bit rate of 2.048 Mbit/s equal to the first four powers of 2. Table 1 below shows the groups of plesiochronous signals corresponding respectively to these operating modes:

15

TABLE 1

MODE		GROUPS
M3	2x2 Mbit/s	2 x 2.048 Mbit/s
M2	4x2 Mbit/s	4 x 2.048 Mbit/s 8.448 Mbit/s
M1	8x2 Mbit/s	8 x 2.048 Mbit/s 4 x 2.048 + 8.448 Mbit/s 2 x 8.448 Mbit/s
M0	16 x 2 Mbit/s	16 x 2.048 Mbit/s 12 x 2.048 Mbit/s + 8.448 Mbit/s 8 x 2.048 Mbit/s + 2 x 8.448 Mbit/s 4 x 2.048 Mbit/s + 3 x 8.448 Mbit/s 4 x 8 Mbit/s 34.368 Mbit/s

Thus at least two multiplexed signals SC1 at 2.048 Mbit/s or one signal SC2 at 8.448 Mbit/s or one signal SC3 at 34.368 Mbit/s are transmitted and at most 16 signals SC1 at 2.048 Mbit/s or four signals SC2 at

8.448 Mbit/s are multiplexed and transmitted. The multiplexing device therefore has at most sixteen inputs for signals SC1, four inputs for signals SC2 and one input for a signal SC3.

5

As shown in FIG. 2, the digital multiplexing device MUX essentially comprises decoding and clock recovering circuits CDR, multiplexing and selecting circuits CM, a radio frame forming circuit FTH and an oversampling circuit SUR.

10

The decoding and clock recovering circuits CDR convert the plesiochronous signals SC1, SC2, SC3 in the line code respectively into incoming plesiochronous binary signals SE1 to SE3 and recover clock signals corresponding to the bit rates of those signals. The line code is a bipolar code such as the HDB3 code, for example. The recovered clock signals correspond to the actual bit rates of the plesiochronous signals and vary within specific limits on either side of the nominal bit rate $DE1 = 2.048$ Mbit/s, $DE2 = 8.448$ Mbit/s and $DE3 = 34.368$ Mbit/s because the original clocks of the plesiochronous signals are independent.

15

20

In the multiplexing and selecting circuits CM, before multiplexing as such, the incoming plesiochronous signals are synchronized as stuffed component signals having respective bit rates significantly greater than the aforementioned nominal bit rates. The synchronous stuffed signals are then multiplexed progressively by one or two multiplexers into multiplexed signals SM3 to SM0 corresponding to the bit rates of modes M3 to M0. The number of incoming plesiochronous signals at 2 Mbit/s or 8 Mbit/s selected is chosen to achieve the standardized bit rates and the bit rates of the operating modes progressively, as soon as the number of incoming signals allows this. The multiplexed signals SM3 to SM0 produced

30

35

by the multiplexing and selecting circuits CM have bit rates $DM3/2^k$ which are integer submultiples of the maximum standardized bit rate $DE3 = 34.368$ Mbit/s. The integer k varies from 0 to 3 for modes M0 to M3. The
 5 multiplexing function is therefore compatible with all the groups of plesiochronous signals of the various modes indicated in table 1 and with the constant radio frame structure described later.

In practice, the bit rate of the multiplexed signal
 10 produced by one of the multiplexing and selecting circuits CM depends on systematically inserting predetermined numbers of bits of an alignment word and stuffing indication bits in each frame of the signal resulting from multiplexing and on inserting positive
 15 stuffing bits in order to make good the difference between the highest constant bit rate of the multiplex signal and the bit rate of each incoming signal to be multiplexed. As is well known in the art, each frame of the multiplexed signal is divided into a plurality of
 20 sectors, generally from two to four sectors, and the sectors have a predetermined length. Hereinafter, the frame and sector or word lengths are expressed in bits.

Each sector comprises a header including bits of the frame alignment word MV and stuffing indication bits
 25 IJ respectively associated with the multiplexed plesiochronous signals. The first sector of the next frame essentially comprises, after the header, stuffing bits BJ associated with respective bits of the multiplexed plesiochronous signals in the preceding
 30 frame. The other bits in each sector are payload bits of the plesiochronous signals which are multiplexed bit by bit.

FIGS. 3 to 6 show block diagrams of respective
 35 multiplexing and selecting circuits CM3 to CM0 which are

generically designated CM hereinafter and are included in the multiplexing device MUX for the four operating modes M3 to M0 thereby deriving the multiplex signal corresponding to one group selected from all the groups defined in table 1. The multiplexing and selecting circuits include multiplexers each of which has the function of synchronization with stuffing of respective incoming plesiochronous signals, and multiplexing respective stuffed signals to form a corresponding frame. The multiplexers fall into two categories, namely a first category made up of known multiplexers and a second category made up of multiplexers specific to the embodiment described here. The known multiplexers are a multiplexer MX1 conforming to ITU-T Recommendation G.742 for multiplexing four plesiochronous signals at the nominal bit rate of $DE1 = 2.048$ Mbit/s into a multiplex signal at the standardized bit rate of $DE2 = 8.448$ Mbit/s, and a second multiplexer MX2 conforming to ITU-T Recommendation G.751 for multiplexing four plesiochronous signals at the bit rate of $DE2 = 8.448$ Mbit/s into a multiplex signal at the standardized bit rate of 34.368 Mbit/s.

For operating mode M3, the multiplexing and selecting circuit CM3 comprises a single multiplexer MX3 for multiplexing two incoming plesiochronous signals at the bit rate $DE1 = 2.048$ Mbit/s into a multiplex signal SM3 at the bit rate of $DE3/8 = 4.296$ Mbit/s, as shown in FIG. 3. The characteristics of the frame of the multiplex signal SM3 are indicated in table 2 below, which relates to FIG. 7:

TABLE 2

Characteristics	Multiplexer MX3
Bit rate of SE1 (Mbit/s)	$DE1 = 2.048$
Number of SE1	2

Resulting bit rate (Mbit/s)	4.296
Frame frequency (kHz)	11.933
Frame length (bits)	360
Number of sectors	4
Composition of sectors:	
- payload bits	86
- additional bits	4
Allocation of frame bits	
- two signals SE1	2 x 172
- frame alignment MV	8
- stuffing indication IJ	2 x 4
Stuffing by SE1:	
- stuffing indication IJ	4
- stuffing bit BJ	1
- minimum stuffing rate	0.368
- nominal stuffing rate	0.38
- maximum stuffing rate	0.392

For operating mode M2, the multiplexing and selecting circuit CM2 comprises a first multiplexer MX1 for multiplexing four incoming plesiochronous signals SE2 at the bit rate DE1 = 2.048 Mbit/s into an intermediate multiplex signal at the bit rate DE2 = 8.448 Mbit/s, and a multiplexer MX4 for raising the standardized bit rate from 8.448 Mbit/s to the bit rate DE3/4 = 8.592 Mbit/s of a multiplex signal SM2, as shown in FIG. 4. In practice, the multiplexer MX4 is a circuit forming a frame, like that shown in FIG. 8, thereby inserting into the headers of four sectors two frame alignment word bits MV, a stuffing indication bit IJ, a meaningless bit SS and, for the first sector, two stuffing bits BJ. The characteristics of the frame in the multiplex signal SM2 are indicated in table 3 below, which relates to FIG. 8 :

TABLE 3

Characteristics	Multiplexer MX4
Bit rate of SE2 (Mbit/s)	DE2 = 8.448
Number of SE2	1
Resulting bit rate (Mbit/s)	8.592
Frame frequency (kHz)	8.523
Frame length (bits)	1008
Number of sectors	4
Composition of sectors:	
- payload bits	248
- additional bits	4
Allocation of frame bits	
- one signal SE2	992
- frame alignment MV	8
- stuffing indication IJ	4
- free bits	4
Stuffing by SE2:	
- stuffing indication IJ	4
- stuffing bit BJ	2
- minimum stuffing rate	0.422
- nominal stuffing rate	0.447
- maximum stuffing rate	0.472

An AND circuit E2 between the output of the multiplexer MX1 and the input of the multiplexer MX4 selects one of the two groups of mode M2. The AND circuit E2 connects the output of the multiplexer MX1 to the input of the multiplexer MX4 when there are four incoming plesiochronous signals SE1 at the bit rate of DE1 = 2.048 Mbit/s to be multiplexed, and applies an incoming signal SE2 at the bit rate of 8.448 Mbit/s directly to the input of the multiplexer MX4 when there is only an input signal of this kind to be transmitted by the radio station.

For operating mode M1 the multiplexing and selecting circuit CM1 comprises two multiplexers MX1 and one multiplexer MX5 specific to the invention, as shown in FIG. 5. Each of the two multiplexers MX0 multiplexes four incoming plesiochronous signals SE1 at the bit rate $DE1 = 2.048$ Mbit/s into an intermediate multiplex signal at the bit rate of $DE2 = 8.448$ Mbit/s. The multiplexer MX5 multiplexes two incoming plesiochronous signals SE2 at the standardized bit rate of $DE2 = 8.448$ Mbit/s into a multiplex signal SM1 at the bit rate of $DE3/2 = 17.184$ Mbit/s. The structure of the frame in the signal SM1 has the characteristics indicated in table 4 below and has four sectors, as in the frame of the signal SM2, and as shown in FIG. 9 :

15

TABLE 4

Characteristics	Multiplexer MX5
Bit rate of SE2 (Mbit/s)	$DE2 = 8.448$
Number of SE2	2
Resulting bit rate (Mbit/s)	17.184
Frame frequency (kHz)	17.047
Frame length (bits)	1008
Number of sectors	4
Composition of sectors:	
- payload bits	248
- additional bits	4
Allocation of frame bits	
- two signals SE2	2×496
- frame alignment MV	8
- stuffing indication IJ	2×4
Stuffing by SE2:	
- stuffing indication IJ	4
- stuffing bit BJ	1
- minimum stuffing rate	0.422
- nominal stuffing rate	0.447
- maximum stuffing rate	0.472

The multiplexing and selecting circuit CM1 for mode M1 also comprises two AND circuits E10 and E11. Each of the two circuits E10 and E11 applies to a respective one of the two inputs of the multiplexer MX5 either the intermediate multiplex signal at the bit rate of 8.448 Mbit/s from the output of a respective one of the multiplexers MX1 or an incoming plesiochronous signal SE2 at the bit rate of 8.448 Mbit/s. If the group of eight signals SE1 at 2.048 Mbit/s is selected, the AND circuits E10 and E11 connect the outputs of the two multiplexers MX1 to the inputs of the multiplexer MX5. If the second group of mode M1 including four incoming signals SE1 at 2.048 Mbit/s and one incoming signal SE2 at 8.448 Mbit/s is selected in the circuit CM1, one of the AND circuits E10 and E11 connects one multiplexer MX1 to one input of multiplexer MX5, and the other circuit applies the incoming signal at 8.448 Mbit/s to the other input of multiplexer MX5. If the group of two incoming signals SE2 at 8.448 Mbit/s is applied to the circuit CM1, the AND circuits E10 and E11 apply the two signals SE2 directly to the inputs of the multiplexer MX5.

For operating mode M0 the multiplexing and selecting circuit CM0 includes four first multiplexers MX1 and one second multiplexer MX2, as shown in FIG. 6. Each multiplexer MX1 can simultaneously multiplex four incoming plesiochronous signals SE1 at the bit rate DE1 = 2.048 Mbit/s to produce four intermediate multiplex signals at the standardized bit rate of DE2 = 8.448 Mbit/s which are applied to the four inputs of the multiplexer MX2 if the group with sixteen incoming plesiochronous signals at 2 Mbit/s is selected ; in this case, four AND circuits E00 to E03 connect the outputs of the multiplexers MX1 to the inputs of the multiplexer

MX2. Other terminals of the AND circuits E00 to E03 are adapted to receive four incoming plesiochronous signals SE2 at the standardized bit rate of $DE2 = 8.448 \text{ Mbit/s}$ to multiplex them in the multiplexer MX1 if the group with
 5 four such incoming plesiochronous signals is selected.

The other groups of mode M0 are selected in the following manner. For the group with twelve incoming signals SE1 at the bit rate of 2.048 Mbit/s and one incoming signal SE2 at the bit rate of 8.448 Mbit/s , for
 10 example, the three AND circuits E00, E01 and E02 connect three multiplexers MX1 to three inputs of the multiplexer MX2, and the AND circuit E03 applies the signal SE2 to the fourth input of the multiplexer MX1. If the third group of mode M0 is selected, and consequently eight
 15 incoming signals SE1 at the bit rate of 2.048 Mbit/s and two incoming signals SE2 at the bit rate of 8.448 Mbit/s must be multiplexed, the AND circuits E00 and E01, for example, connect two multiplexers MX1 to two inputs of the multiplexer MX2, and the AND circuits E02 and E03
 20 apply the two signals SE2 directly to the other two inputs of the multiplexer MX2. If the fourth group of four incoming signals SE1 at the bit rate of 2.048 Mbit/s and three incoming signals SE2 at the bit rate of 8.448 Mbit/s is selected, for example, the AND circuit
 25 E00 connects a multiplexer MX1 to one input of the multiplexer MX2 and the other three AND circuits E01, E02 and E03 apply the signals SE2 to the other three inputs of the multiplexer MX2.

As a general rule, the bit rate of a multiplex signal SM2 to SM0 is of the form $4(2^{2-k}-P).DE1 + P.DE2$ with P in the range from 0 to $2^{2-k} \leq 4$ with $k = 0, 1$ or 2 .
 30

If a single incoming signal SE3 at the bit rate of 34.368 Mbit/s is applied to the radio relay, the corresponding decoding and clock recovering circuit
 35 applies it to the frame forming circuit FTH only via an

AND circuit E04 opened by the unit UC (see FIG. 2).

The output of each multiplexing and selecting circuit CM3 to CM0 is connected to the input of the frame forming circuit FTH by an output AND circuit ES3 to ES0 controlled by the control unit UC which also controls the intermediate AND circuits E2, E10, E11 and E00 to E03. Depending on the mode Mk and the group selected, the characteristics of which are entered into the control unit UC via the keyboard, the AND circuits select the incoming plesiochronous signals to be multiplexed of the selected group and supply the corresponding multiplex signal SM1 to SM4 to the selected group at the input of the circuit FTH.

To reduce the costs of multiplexing, the multiplexing and selecting circuits CM3 and CM2 and the multiplexing and selecting circuits CM1 and CM0 are on respective printed circuit cards which plug into the subrack of the transceiver ETR. These cards can also carry corresponding demultiplexing circuits included in the demultiplexing device DMUX. One card or both cards then plug in the transceiver ETR as required. Alternatively, on the second card, the multiplexing and selecting circuits CM1 and CM0 are preferably combined to eliminate the two multiplexers MX1 in the circuit CM1 by introducing four switching circuits controlled by the unit UC from the outputs of the two multiplexers MX1 and two inputs of signal SE2 in the circuit CM0 and to the AND circuits E10 and E11 and, for example, the AND circuits E00 and E01.

To preserve the integer ratios 2^k with $k = 0$ to 3 between the maximum bit rate DE3 = 34.368 Mbit/s of the multiplex signals SM0 to SM3 and their bit rates, the radio frame forming circuit FTH raises the bit rate of

the multiplex signal SM_k relative to the selected group of plesiochronous signals applied by the selected multiplexing and selecting circuits CM_k in a constant ratio RC to the bit rate of the signal SR_k resulting from radio frame forming, so that the maximum bit rate of the resulting signals is the constant bit rate $DC = 41.732$ Mbit/s in the transmission cable CA. The ratio RC is therefore equal to $41.732/34.368 = 1.214$ and the resulting signals SR_0 to SR_3 for modes M_0 to M_3 have the following bit rates DR_0 to DR_3 :

M_0 ($k=0$): $DR_0 = DC = 34.368 \times RC = 41.732$ Mbit/s
 M_1 ($k=1$): $DR_1 = DC/2 = 17.184 \times RC = 20.886$ Mbit/s
 M_2 ($k=2$): $DR_2 = DC/4 = 8.592 \times RC = 10.433$ Mbit/s
 M_3 ($k=3$): $DR_3 = DC/8 = 4.296 \times RC = 5.216$ Mbit/s.

15

Whichever multiplex signal SM_k is applied by one of the multiplexing circuits CM_0 to CM_3 to the radio frame forming circuit FTH, the frame of the respective resulting signal SR_k has the common radio frame structure shown in FIG. 10. The frame structure conforms to the MPEG2 recommendation and has a constant length of 1 632 bits, regardless of the bit rate of the resulting signal. As shown in FIG. 10, the frequency of the frame, or its duration DT_0 to DT_3 , varies as a function of the bit rate of the resulting signal SR_0 to SR_3 and therefore the bit rate of the multiplex signal SM_0 to SM_3 and is equal to 25.571 kHz, 12.785 kHz, 6.392 kHz, or 3.196 kHz. The width of a bit in the radio frame is also a function of the bit rate of the resulting signal SR_k . These bit width differences are compensated in the oversampling circuit SUR which oversamples the signal SR_k with a sampling ratio 2^k of 1, 2, 4 and 8 so that the bit rate of the signal at the output of the transceiver ETR is always equal to the constant bit rate $DC = 41.732$ Mbit/s. As shown in FIG. 1, the output of the transceiver ETR is

35

that of the cable interface IC1 which encodes the oversampled resulting signal SSUR_k, for example, in the HDB3 bipolar code and matches it to the characteristics of the cable CA. Thus one bit of the signal SR₁, SR₂ or SR₃ is consecutively repeated 2, 4 or 8 times in the signal SSUR₁, SSUR₂ or SSUR₃ at the bit rate DC.

Like an MPEG2 frame, the modular frame shown in FIG. 10 is made up of two sectors ST₁ and ST₂ each including 672 payload bits corresponding to the bits of the selected multiplex signal SM_k and 144 additional bits, so that the total frame length is equal to 1 632 bits. The first sector ST₁ includes in succession 8 bits of the frame alignment word MVT, a first constant allocation field AC₁ of 8 bits, 672 payload bits and 128 first bits of a variable allocation field AV. The second sector S₂ includes in succession 8 last bits of the variable allocation field AV, a second constant allocation field AC₂ of 8 bits, 672 payload bits and an error correcting code field CCE of 128 bits, for example relating to a Reed Solomon code.

The first constant allocation field AC₁ includes a telephone service channel call request bit AVdS, four error information bits E₁ to E₄ and three free bits CL₁ to CL₃.

The AVdS bit at a predetermined state indicates the use of a telephone service channel VdS, i.e. a call being set up or already set up on the telephone service channel VdS whose payload field is included in the variable allocation field AV and has a length inversely proportional to the bit rate of the resulting signal SR_k. The channel VdS transfers call requests between the transceivers ETR of two radio stations communicating in accordance with the invention, and preferably transfers call requests between the transceiver ETR concerned,

which is inside the building, and the radio transceiver ERA, which is several hundred meters away. A telephone call is set up on the telephone service channel by maintenance personnel, for example, without using any
 5 other intermediate transmission system.

The bits E1 to E4 are reserved for collecting error information supplied by an error correction circuit included in the circuit CRE of the transceiver ERA. These bits are local information indicative of a frame
 10 including errors which may or may not have been corrected, and are inserted into the next frame. The bits E1 to E4 are processed when they are received by the transceiver ETR of the radio station to estimate the error rate according to the corresponding transmission
 15 direction of the radio link. For example, bits E1 to E4 indicate that an erroneous byte has been detected and corrected and that a frame includes a number of erroneous bytes greater than the correction capacity of the Reed-Solomon code, i.e. at least 9 bytes, and that these bytes
 20 cannot therefore be corrected. If the radio link includes two transmission channels which back each other up, pairs of bits E1-E2 and E3-E4 are assigned to each transmission channel.

The three bits CL1 to CL3 remain free so that they
 25 can be allocated to new services.

The eight bits in the second constant allocation field AC2 are allocated to the collection of information needed to generate quality criteria for the link between the transceivers of the radio stations. These bits convey
 30 the following information:

- a 4-bit block synchronization word SB1 to SB4, a block comprising one or more frames ;
- a fault bit DEF to signal a loss of alignment in the preceding frame ;
- 35 - two anomaly bits AN1 and AN2 for respectively

signaling code violation on the cable CA and a minimum number of erroneous bytes in the preceding frame ;

5 - an erroneous block return bit RBE corresponding either to the receive direction opposite the emit direction of the local station and indicating reception of a frame carrying an uncorrected frame indication or an indication of a frame including at least one code violation, or reception of a frame carrying a remote frame alignment loss indication, or to the local
10 detection of a frame alignment loss.

 All this data is inserted into the frame following that in which the corresponding event occurs.

15 FIGS. 11, 12 and 13 respectively show the allocation of the bits of the 136-bit variable allocation field AV as a function of mode M3, mode M2 and mode M1 or M0.

 40 bits in M3 mode or 80 bits in M2 mode or 112 bits in M1 or M0 mode are respectively reserved at the
20 start of the field AV for two and three auxiliary channels VAux1 to VAux3 which are processed in an auxiliary channel forming circuit MFVA (FIG. 2) connected to the circuit FTH as a function of the operating mode selected under the control of the unit UC. The data
25 relating to the auxiliary channels is transmitted in the form of serial signals accompanied by a corresponding clock signal and frame synchronization information. Table 5 below gives one example of the distribution of bits and the transmission bit rates for the auxiliary channels.
30 For mode M2, eight bits are unused after the 16 bits of the channel VAux3. Depending on their use, the auxiliary channel signals can be formatted as an auxiliary frame whose structure is not predetermined by the radio frame itself but depends only on the intended application,
35 within the limits of the characteristics set out in table

5.

TABLE 5

	Mode (Mbit/s)	Frame frequency (kHz)	Aux. channel	No. of bits	Bit rate (kbit/s)
M3	2 x 2	3.196	VAux1	24	76.7
			VAux2	16	51.1
M2	4 x 2	6.392	VAux1	48	306.8
			VAux2	16	102.2
			VAux3	16	102.2
M1	8 x 2	12.785	VAux1	96	1 227.4
			VAux2	8	102.2
			VAux3	8	102.2
M0	16 x 2	25.571	VAux1	96	2 454.8
			VAux2	8	204.5
			VAux3	8	204.5

5 According to table 5, the maximum bit rate offered to an auxiliary channel is increased to the bit rate of the respective resulting signal in the circuit MFVA and is equal to the radio frame frequency of the respective resulting signal multiplied by the number of bits
10 available for the auxiliary channel.

The applications described above are based entirely on the transmission capacity of each auxiliary channel and are given by way of non-limiting example only.

15 In mode M3, auxiliary channel VAux1 transmits one asynchronous signal at 9 600 kbit/s or one signal at 64 kbit/s and channel VAux2 transmits one asynchronous signal at 9 600 kbit/s.

20 In mode M2, channel VAux1 routes one signal at 256 kbit/s or four signals at 64 kbit/s, and channels VAux2 and VAux3 each route one signal at 64 kbit/s or two asynchronous signals at 9 600 bit/s or one asynchronous

signal at 19 200 bit/s.

In mode M1, the bit rate offered to the first auxiliary channel VAux1 is significantly higher than in the preceding modes and enables up to four signals at 256 kbit/s to be transmitted. In mode M1, channels VAux2 and VAux3 each transmit one channel at 64 kbit/s or two asynchronous channels at 9 600 bit/s or one asynchronous channel at 19 200 bit/s.

In mode M0, the bit rate offered to the first auxiliary channel VAux1 is still higher. It can be used to transmit one signal at 2.048 Mbit/s and one signal at 256 kbit/s or four signals at 64 kbit/s. Figure 14 shows a frame structure divided into three sectors each of 32 bits. In this example, the first four bits of each sector are respectively allocated to the four signals at 64 kbit/s or allocated to the signal at 256 kbit/s. In mode M0, channels VAux2 and VAux3 each transmit two signals at 64 kbit/s or two asynchronous signals at 19 200 bit/s, for example.

Whichever mode applies, the digital signals are processed in the circuit MFVA by increasing their bit rates as a function of the characteristics of the respective auxiliary channel. The asynchronous signals, typically at 4 800 bit/s to 19 200 bit/s, are transmitted oversampled at five times their nominal bit rate at least. The channels at 64 kbit/s or 256 kbit/s are transmitted in packets. The channel at 2 048 kbit/s, which can be transmitted only in mode M0 (16 x 2 Mbit/s), is treated like an incoming plesiochronous signal. It is inserted into the auxiliary frame after synchronization to its rhythm by positive stuffing.

Still referring to FIGS. 11 to 13, the variable allocation field AV in the radio frame includes 32, 16 or 8 bits in mode M3, M2 or M1, M0 reserved for a 64 kbit/s

network telephone service channel VdSR. Then 4 bits, 2 bits ou 1 bit are allocated to a channel DIA for the dialogue between the control unit UC in the transceiver ETR and the microcontroller MC in the transceiver ERA.

5 The dialogue includes, in the ETR to ERA transmit direction, the "uplinking" of remote control commands such as changing groups of plesiochronous signals and characteristics relative to the group selected, power adjustment, and in the ERA to ETR receive direction, the

10 "downlinking" of status or fault indications such as change of group, alarms, switching status, received radio field level.

12, 6 or 3 bits are then allocated to the telephone service channel VdS for setting up an audio call between

15 the two stations of the radio link or between the transceivers ETR and ERA in the radio station. The associated calls are signaled by the bits AVdS.

12, 6 or 3 bits maximum are then offered to each of two digital data channels DN1 and DN2 in the field AV.

20 Each channel DN1, DN2 transmits through oversampling an asynchronous signal at 9 600 bit/s, for example.

Finally, 8, 4 or 2 and 16, 8 or 4 bits are respectively reserved for two longitudinal telemonitoring channels TSL1 and TSL2 which carry dialogue between

25 transceivers on the same link. The channel TSL1 is used to manage the point-to-point radio link and the channel TSL2 is used for network management.

Referring again to FIG. 1, the encoded oversampled signal SSUK at 41.732 Mbit/s transmitted via the cable

30 interface IC1 in the coaxial cable CA is decoded in the cable interface IC2 of the radio transceiver ERA. The undersampling circuit SOE detects each group of 2^k consecutive bits in the decoded oversampled signal, i.e.

35 each group of 1, 2, 4 or 8 bits for the operating mode

M0, M1, M2 or M3, thereby signalling the oversampling ratio 2^k to the microcontroller MC and thereby undersampling the signal transmitted via the cable CA with a ratio $1/2^k$ to return the resulting signal SRk to
5 the radio frequency emission circuit CEM via the digital filter FIE.

Depending on the oversampling ratio 2^k , and therefore on the operating mode Mk, the microcontroller MC programs the emit digital filter FIE in the baseband.
10 The bandwidths of the programmed filter are compatible with the bit rate DRk of the returned resulting signal SRk corresponding to the selected mode Mk. In the circuit CEM the filtered signal modulates an intermediate frequency carrier which is then transposed to the radio
15 frequency.

At the receiving end, a radio digital frame signal at the bit rate DRk in accordance with the invention is processed by operations which are substantially the
20 reverse of those described in detail above for the emission of a signal of this kind.

In the radio transceiver ERA the received radio frame signal is amplified, transposed and demodulated to yield a baseband signal in the radio frequency reception
25 circuit CRE. In particular, the received signal is filtered by frequency filters selected by the microcontroller MC from a battery of switched filters in the circuit CRE as a function of the operating mode Mk. The receive baseband signal is then filtered according to
30 the operating mode Mk by a programmable digital filter included in the demodulation and digital filtering circuit FIR. The receive baseband signal is then oversampled in the oversampling circuit SUE as a function of the ratio 2^k to transmit a digital signal at the bit
35 rate DC = 41.732 Mbit/s in the coaxial cable CA, encoded

via the cable interface IC2.

After it is decoded in the cable interface IC1 in the transceiver ETR, the demultiplexing device DMUX undersamples the signal received via the cable CA to yield a resulting digital signal at the bit rate DRk as a function of the sampling ratio 2^k relating to the operating mode Mk signalled by the control unit UC. The received resulting signal is then deformatted in order to obtain a multiplex signal SMk. The bits of the fields AC1, AC2, AV and CCE in the frame of the resulting signal (see FIG. 10) are in part processed by the control unit UC, in particular to detect errors and to generate alarm signals, and in part directed to the various channels VAux1 to VAux3, VdSR, VdS, DN1 and DN2. The returned multiplex signal is finally demultiplexed in a demultiplexing circuit selected by the control unit UC from demultiplexing circuits having architectures similar to the multiple xing circuits CM0 to CM3 (see FIGS. 3 to 6). The demultiplexing circuit supplies plesiochronous component signals corresponding to the selected group via HDB3 transcoding circuits.

In the foregoing description, it is apparent that the invention relates to a digital frame made up of a constant number of bits, i.e. having a predetermined length, the benefit of which resides principally in the possibility of:

a) transmitting (or encapsulating) in the same frame structure resulting signals having different bit rates and which result from multiplexing component plesiochronous signals which can themselves have different bit rates,

b) adapting the bit rate in the intermediate

transmission cable to the actual bit rate to be transmitted, given the bit rates of the plesiochronous signals constituting it, and

- 5 c) transmitting additional service (and operating) data by reserving for some data a minimum, or even constant, bit rate between the various possible modes, simultaneously with transmitting the component plesiochronous signals.

10

THE EMBODIMENTS OF THE INVENTION IN WHICH AN EXCLUSIVE
PROPERTY OR PRIVILEGE IS CLAIMED ARE DEFINED AS FOLLOWS :

1 - A digital frame having a predetermined length
resulting from multiplexing plesiochronous digital
5 signals, a constant length and a structure independent of
the bit rates of signals each resulting from multiplexing
plesiochronous digital signals constituting a group
selected from several groups of plesiochronous digital
signals having bit rates which are substantially
10 multiples of each other, the bit rates of said resulting
signals being submultiples of the highest bit rate of
said resulting signals.

2 - A digital frame according to claim 1,
15 comprising a frame alignment word, a multiplexed signal
bit field and an additional bit field having respective
predetermined lengths, the ratio of the bit rates of the
resulting signal including the frame and a selected
multiplex signal obtained substantially directly by
20 multiplexing plesiochronous signals of said selected
group being constant and independent of the bit rates of
the multiplex signals.

3 - The frame according to claim 2, wherein the
25 additional bit field includes a constant allocation
field, a variable allocation field varying as a function
of the bit rate of said selected multiplex signal, and an
error correcting code field, said fields having
respective predetermined lengths.

30

4 - The frame according to claim 3, wherein said
constant allocation field includes bits for collecting
error information and quality bits.

35 5 - The frame according to claim 3, wherein said

variable allocation field includes bits of auxiliary channels whose bit rates increase as the bit rate of said respective multiplex signal increases.

5 6 - The frame according to claim 3, wherein said variable allocation field includes bits which are reserved for a predetermined number of telephone and data transmission channels and whose number decreases as the bit rate of the selected multiplex signal increases.

10

 7 - The frame according to claim 3, wherein said variable allocation field includes bits allocated to a telephone service channel whose number decreases as the bit rate of the selected multiplex signal increases, and
15 said constant allocation field includes a bit indicating a call request on said telephone service channel.

 8 - A method of forming a digital frame, comprising the following steps :

20 - constituting groups of plesiochronous digital signals from a plurality of given plesiochronous digital signals having bit rates which are substantially multiples of each other,

 - selecting one of said plesiochronous digital
25 signal groups,

 - multiplexing the plesiochronous digital signals of said selected group into a selected multiplex signal, said multiplex signals respectively resulting from the multiplexing of the plesiochronous digital signals in the
30 groups having bit rates which are multiples of each other,

 - distributing the bits of said selected multiplex signal in a field of predetermined length in the frame after multiplication of the bit rate of the selected
35 multiplex signal by a constant, and

- forming a resulting signal having said frame by inserting therein a frame alignment word and an additional bit field having predetermined lengths.

5 9 - The method according to claim 8, wherein the bit rate of said resulting signal is at most equal to the constant bit rate on a transmission medium, and said method comprises a step of oversampling said resulting
10 signal with an oversampling ratio between the bit rate of said transmission medium and the bit rate of the resulting signal so as to transmit an oversampled resulting signal at said constant bit rate.

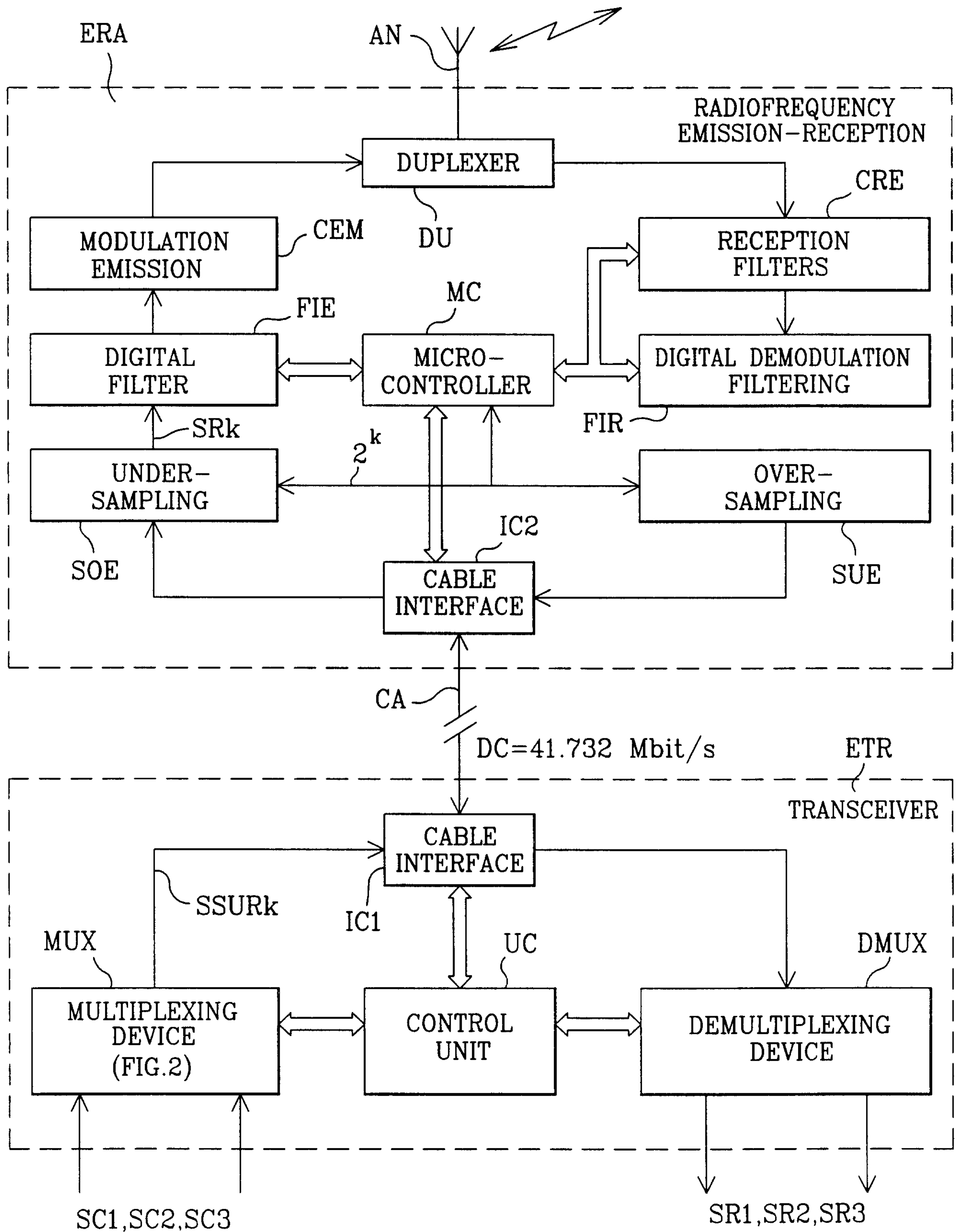
15 10 - The method according to claim 9, wherein the transmission medium connects a transceiver at the base of a radio station and a radio transceiver of said radio station, and the method comprises in said radio transceiver a step of undersampling said oversampled
20 resulting signal with the reciprocal of said oversampling ratio and a step of selecting frequency filters as a function of said oversampling ratio.

25 11 - A method according to claim 8, wherein, if the bit rates DE1 and DE2 of first and second plesiochronous digital signals are related by the equation $DE2 \approx N.DE1$, and multiplex signals have bit rates significantly greater than $P.DE2$, N and P being integers not less than 0, the steps of selecting one group and multiplexing the plesiochronous digital signals in said selected group
30 comprise steps of selecting and multiplexing $N(2^{K-k}-P)$ signals at the bit rate DE1 into $(2^{K-k}-P)$ intermediate multiplex signals at the bit rate DE2, selecting P plesiochronous digital signals at the bit rate DE2, and multiplexing the P selected plesiochronous digital
35 signals at the bit rate DE2 and the $(2^{K-k}-P)$ intermediate

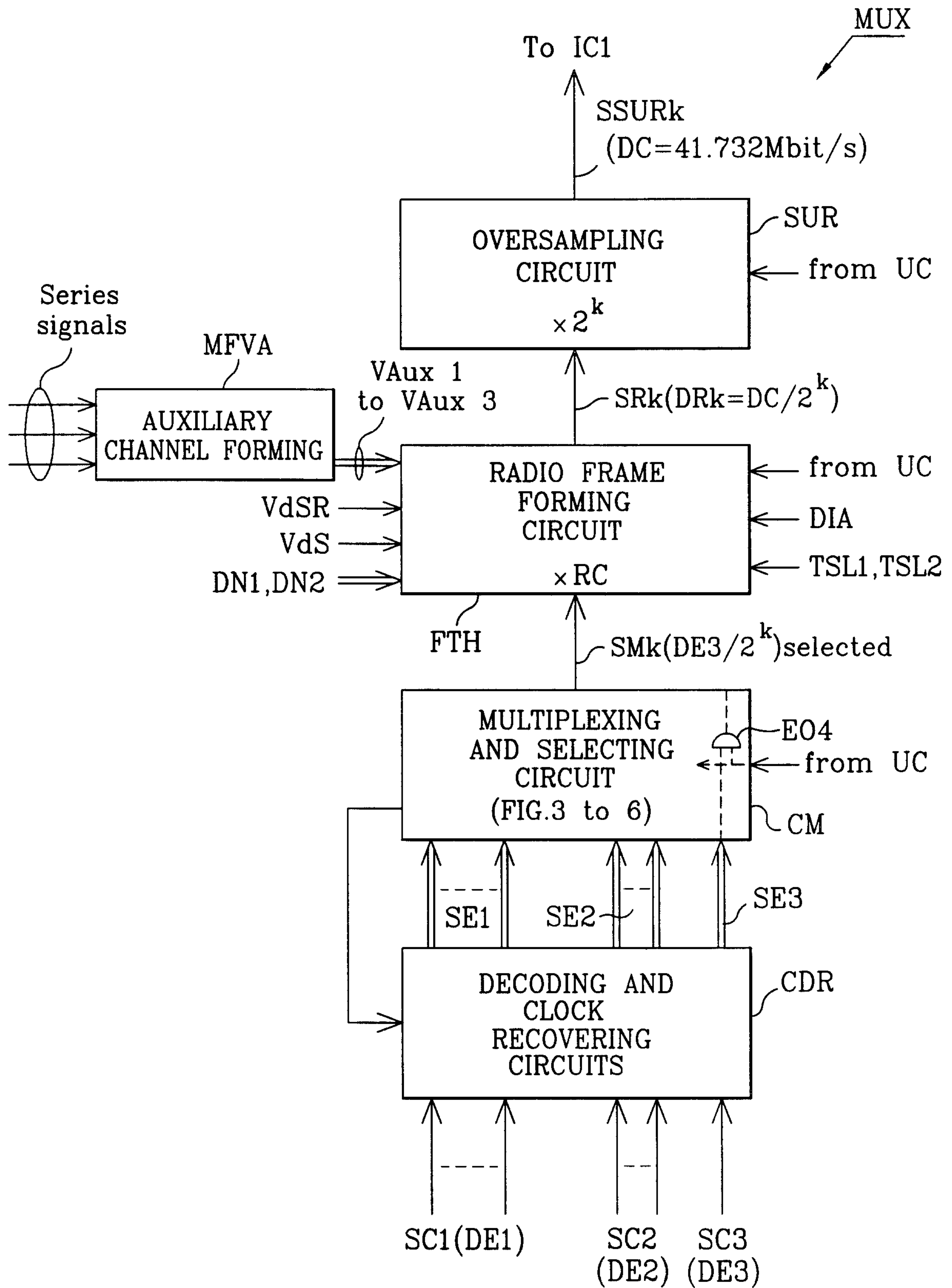
multiplex signals into the selected multiplex signal, P being an integer in the range from 0 to $2^{(K-k)}$ and k being an integer in the range from 0 to K .

5 12 - A method according to claim 8, wherein
inserting said additional bit field into said frame
includes inserting a constant allocation field, a
variable allocation field varying as a function of the
bit rate of said selected multiplex signal and an error
10 correcting code field, said fields having respective
predetermined lengths.

1/6

FIG.1

2/6

FIG.2

3 / 6

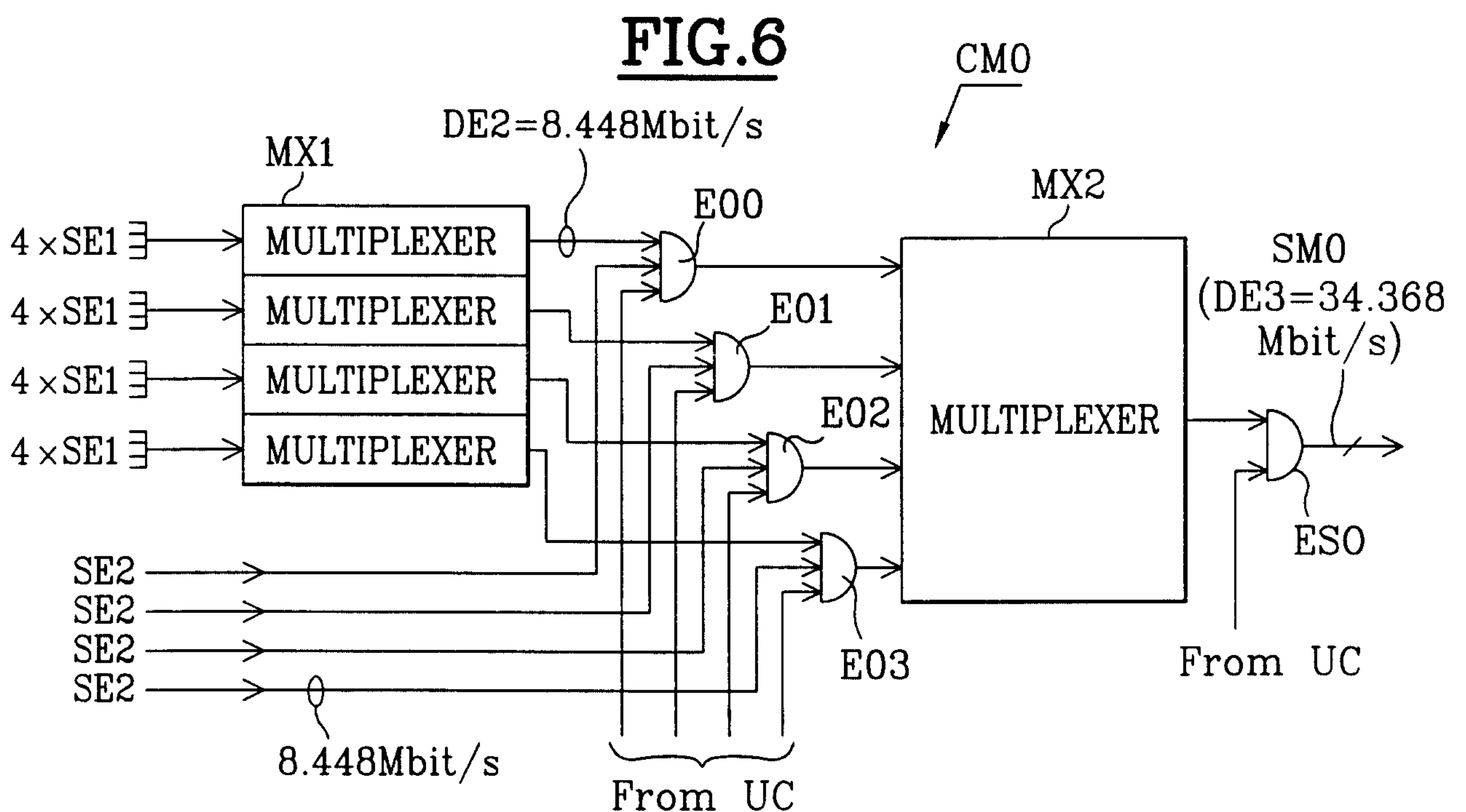
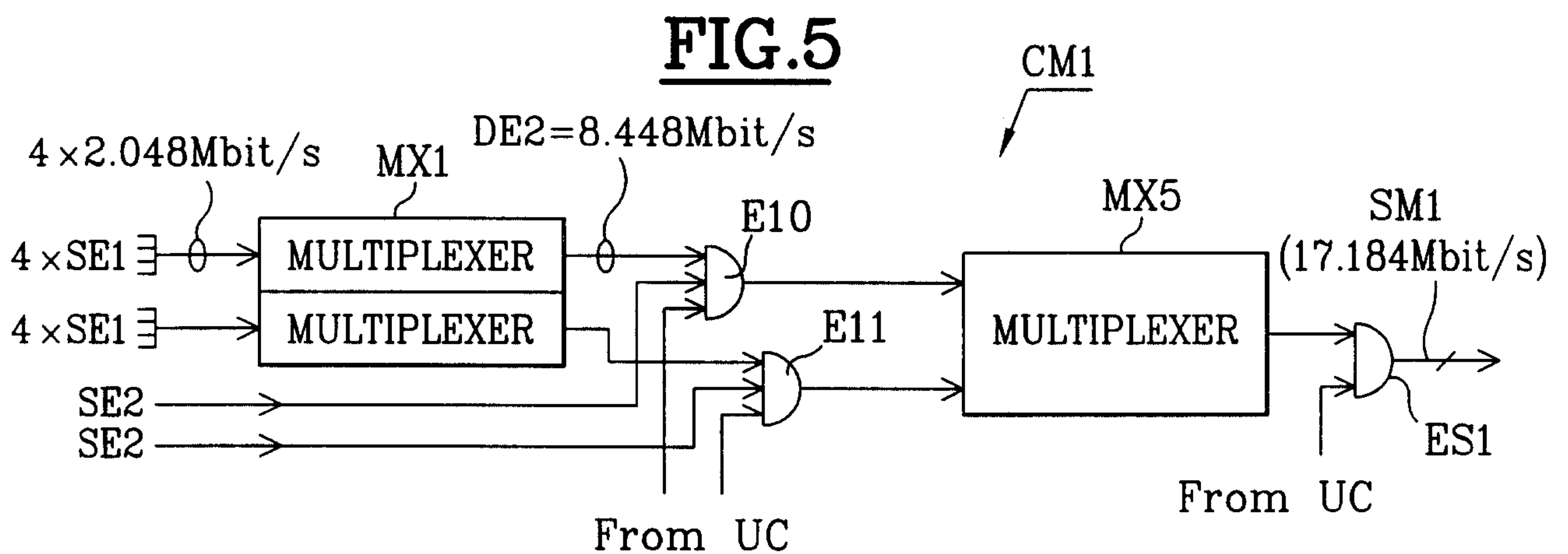
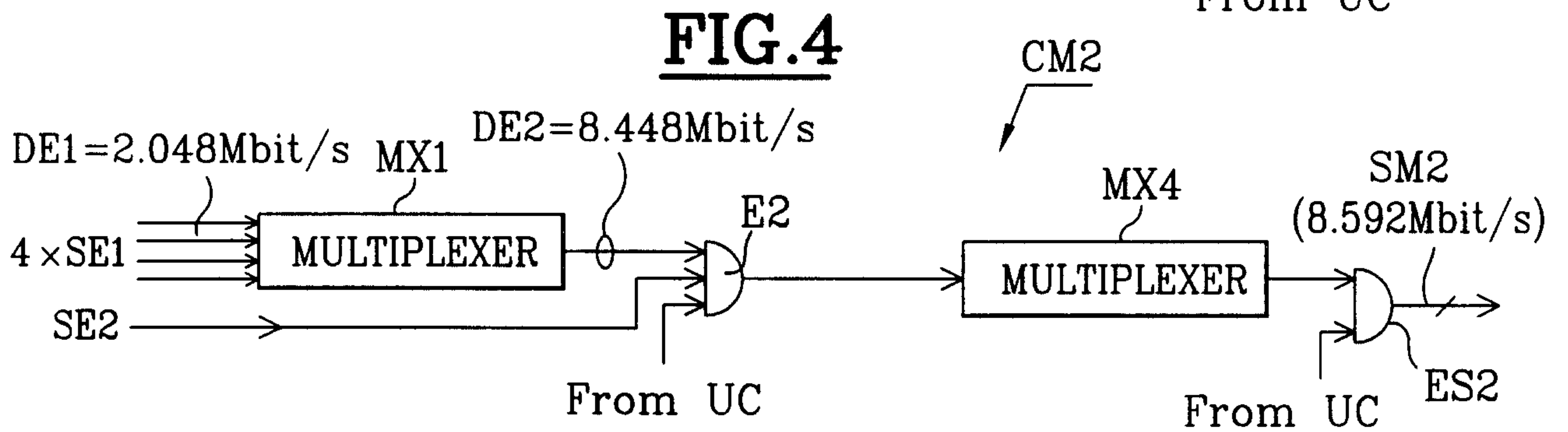
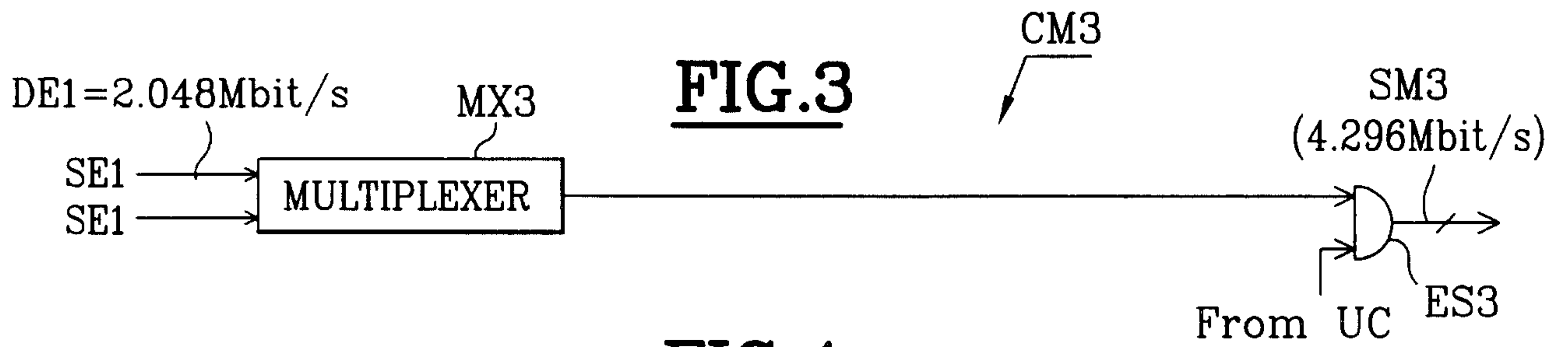


FIG.7

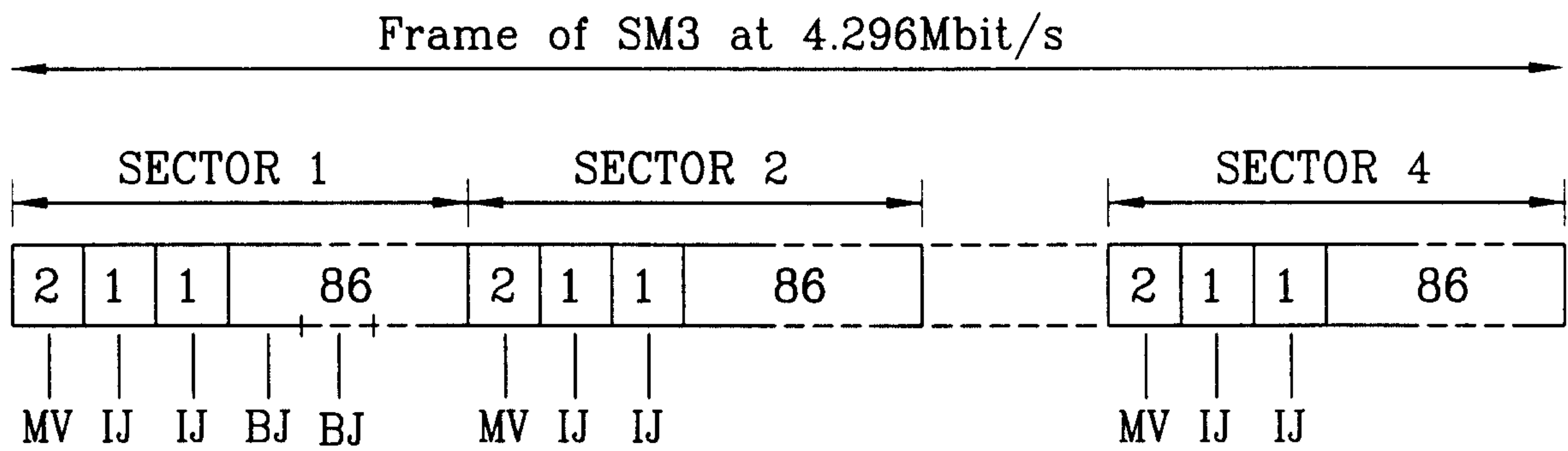


FIG.8

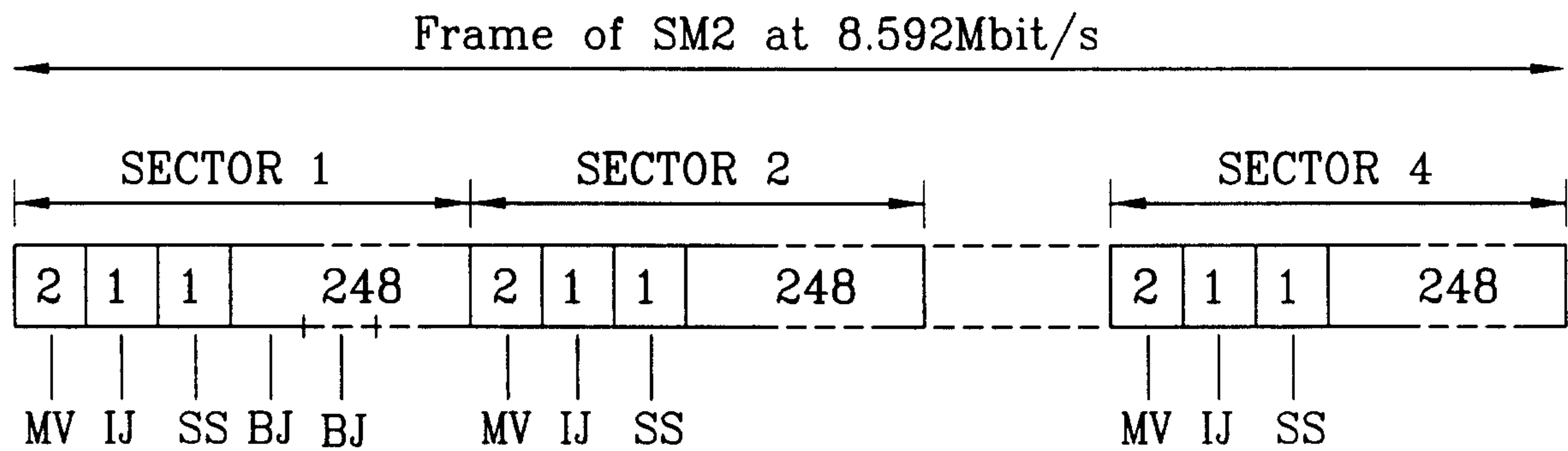


FIG.9

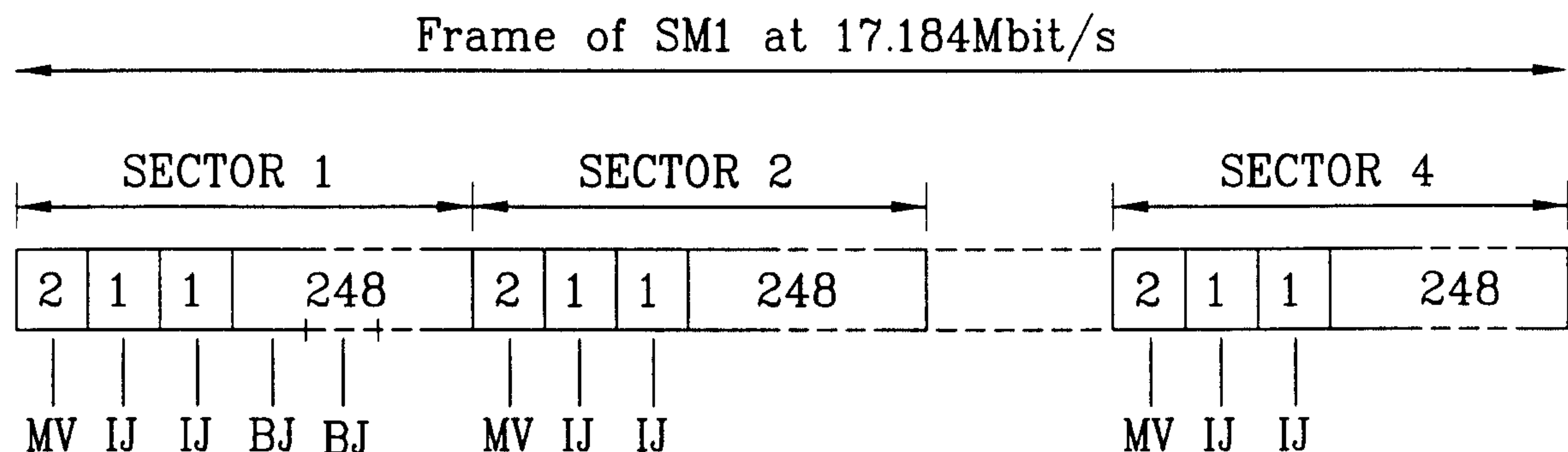


FIG.10

RADIO FRAME of SRk

DT3=8.DT0; or DT2=4.DT0; or DT1=2.DT0; or DT0=39.106 μ s

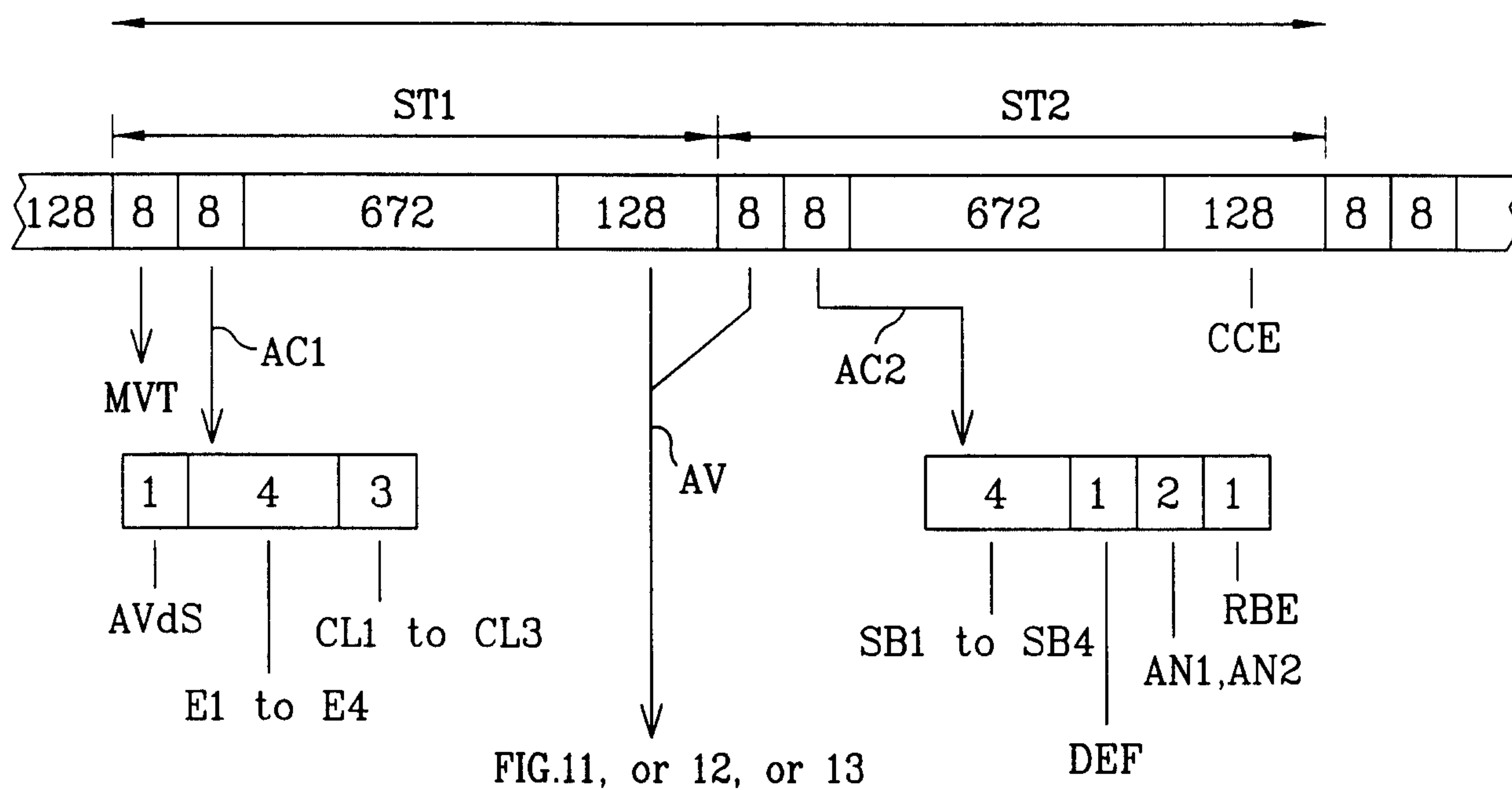


FIG.14

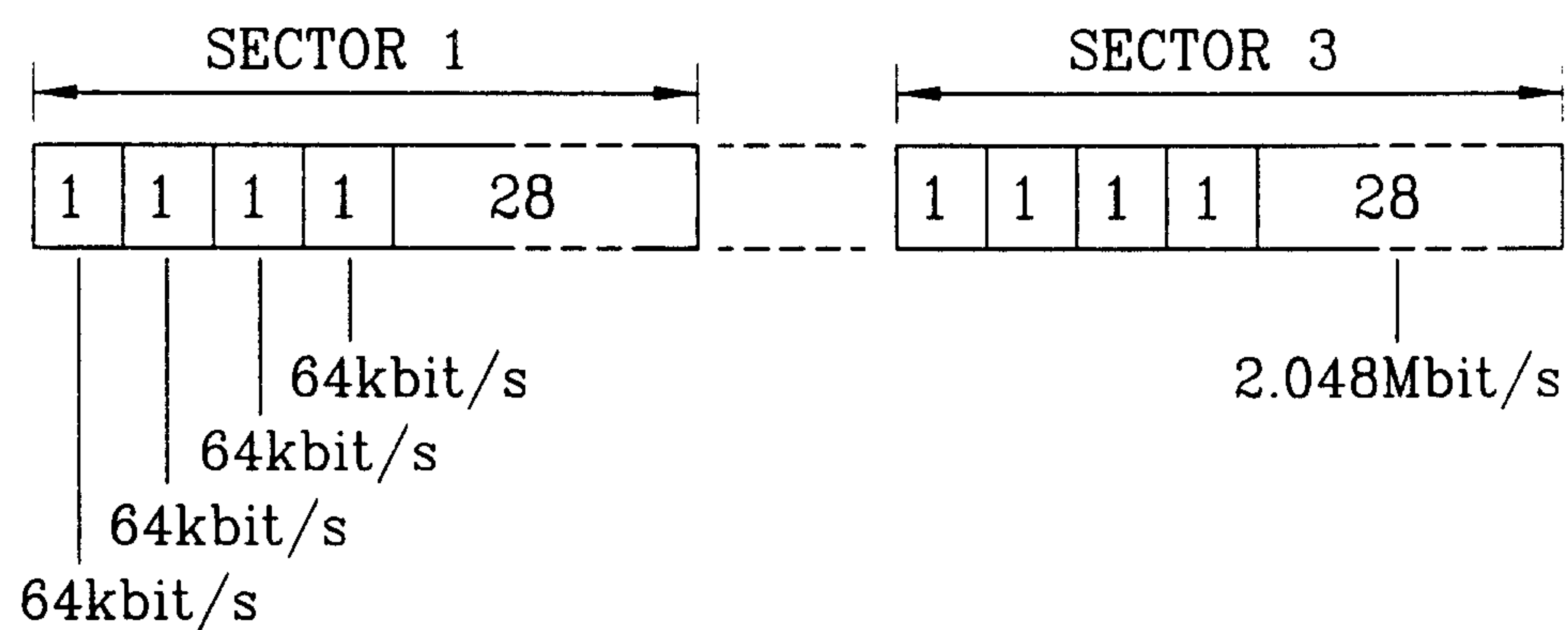


FIG.11

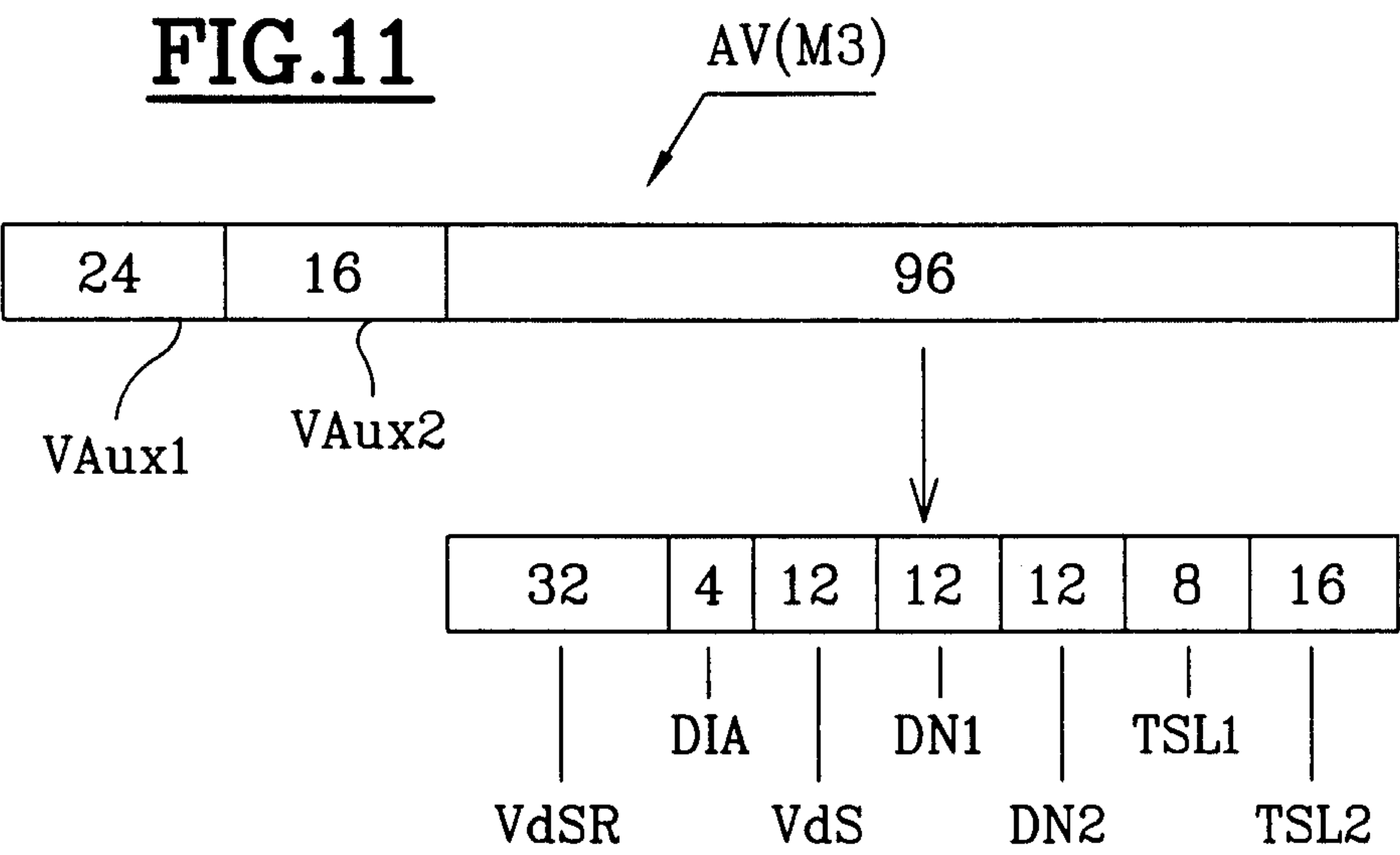


FIG.12

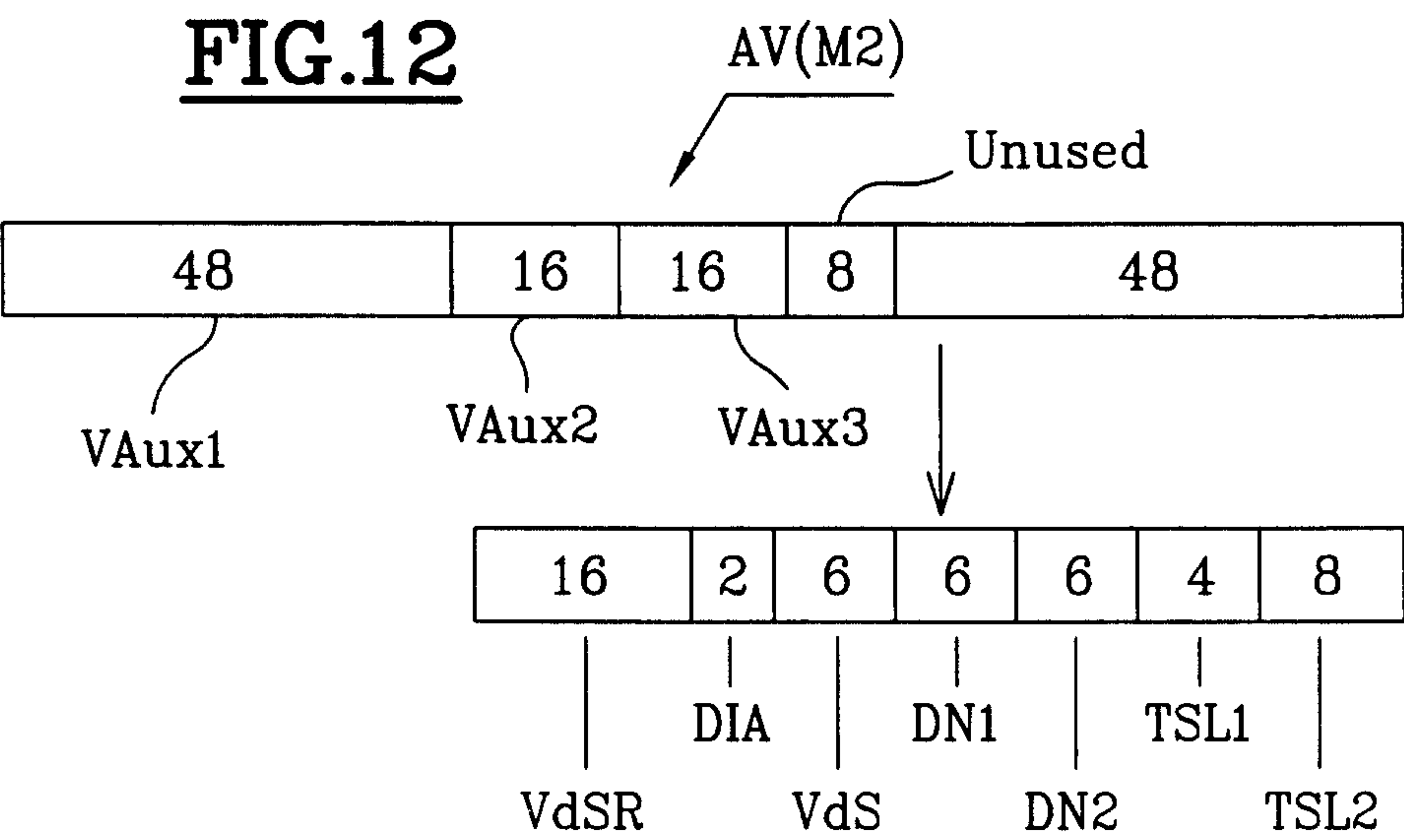


FIG.13

