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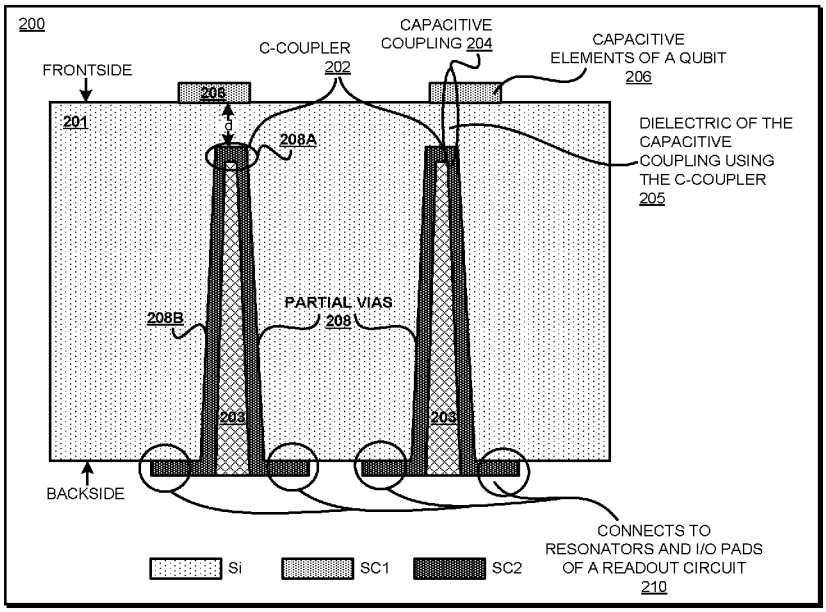
FIGURE 2



(57) **Abstract:** A capacitive coupling device (superconducting C-coupler) includes a trench formed through a substrate, from a backside of the substrate, reaching a depth in the substrate, substantially orthogonal to a plane of fabrication on a frontside of the substrate, the depth being less than a thickness of the substrate. A superconducting material is deposited as a continuous conducting via layer in the trench with a space between surfaces of the via layer in the trench remaining accessible from the backside. A superconducting pad is formed on the frontside, the superconducting pad coupling with a quantum logic circuit element fabricated on the frontside. An extension of the via layer is formed on the backside. The extension couples to a quantum readout circuit element fabricated on the backside.

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BACKSIDE COUPLING WITH SUPERCONDUCTING PARTIAL TSV FOR TRANSMON QUBITS

TECHNICAL FIELD

[0001] The present invention relates generally to a semiconductor device, a fabrication method, and fabrication system for coupling readout circuitry with superconducting quantum logic circuits. More particularly, the present invention relates to a device, method, and system for backside coupling with superconducting partial TSV (Through Silicon Via) for transmon qubits.

BACKGROUND

[0002] Hereinafter, a "Q" or "q" prefix in a word or phrase is indicative of a reference of that word or phrase in a quantum computing context unless expressly distinguished where used.

[0003] Molecules and subatomic particles follow the laws of quantum mechanics, a branch of physics that explores how the physical world works at the most fundamental levels. At this level, particles behave in strange ways, taking on more than one state at the same time, and interacting with other particles that are very far away. Quantum computing harnesses these quantum phenomena to process information.

[0004] The computers we use today are known as classical computers (also referred to herein as "conventional" computers or conventional nodes, or "CN"). A conventional computer uses a conventional processor fabricated using semiconductor materials and technology, a semiconductor memory, and a magnetic or solid-state storage device, in what is known as a Von Neumann architecture. Particularly, the processors in conventional computers are binary processors, i.e., operating on binary data represented in 1 and 0.

[0005] A quantum processor (q-processor) uses the odd nature of entangled qubit devices (compactly referred to herein as "qubit," plural "qubits) to perform computational tasks. In the particular realms where quantum mechanics operates, particles of matter can exist in multiple states—such as an "on" state, an "off" state, and both "on" and "off" states simultaneously. Where binary computing using semiconductor processors is limited to using just the on and off states (equivalent to 1 and 0 in binary code), a quantum processor harnesses these quantum states of matter to output signals that are usable in data computing.

[0006] Conventional computers encode information in bits. Each bit can take the value of 1 or 0. These 1s and 0s act as on/off switches that ultimately drive computer functions. Quantum computers, on the other hand, are based on qubits, which operate according to two key principles of quantum physics: superposition and entanglement. Superposition means that each qubit can represent both a 1 and a 0 at the same time. Entanglement means that qubits in a superposition can be correlated with each other in a non-classical way; that is,

the state of one (whether it is a 1 or a 0 or both) can depend on the state of another, and that there is more information that can be ascertained about the two qubits when they are entangled than when they are treated individually.

[0007] Using these two principles, qubits operate as more sophisticated processors of information, enabling quantum computers to function in ways that allow them to solve difficult problems that are intractable using conventional computers. IBM has successfully constructed and demonstrated the operability of a quantum processor (IBM is a registered trademark of International Business Machines corporation in the United States and in other countries.)

[0008] A superconducting qubit may include a Josephson junction. A Josephson junction is formed by separating two thin-film superconducting metal layers by a non-superconducting material. When the metal in the superconducting layers is caused to become superconducting – e.g. by reducing the temperature of the metal to a specified cryogenic temperature –pairs of electrons can tunnel from one superconducting layer through the non-superconducting layer to the other superconducting layer. In a superconducting qubit, the Josephson junction – which has an inductance - is electrically coupled in parallel with one or more capacitive devices forming a nonlinear resonator.

[0009] The information processed by qubits is emitted in the form of microwave energy in a range of microwave frequencies. The microwave emissions are captured, processed, and analyzed to decipher the quantum information encoded therein. For quantum computing of qubits to be reliable, quantum circuits, e.g., the qubits themselves, the readout circuitry associated with the qubits, and other types of superconducting quantum logic circuits, must not alter the energy states of the particles or the microwave emissions in any significant manner. This operational constraint on any circuit that operates with quantum information necessitates special considerations in fabricating semiconductor and/or superconductor structures that are used in such a circuit.

[0010] The readout circuitry is generally coupled with a qubit by electromagnetic resonance (usually a microwave or radio-frequency resonance) using a resonator. A resonator in the readout circuitry comprises inductive and capacitive elements. Embodiments of the invention recognize that a superconducting capacitive coupling used with a superconducting quantum logic circuit, and particularly to couple a readout circuit with a qubit is significantly larger in size than the size of the Josephson junction therein. Image **100** shows a portion of a qubit chip. Coupling capacitors **102** couple with transmission lines (not visible) that bring the electromagnetic signal out from Josephson junction **104**. Capacitor pads **106** are capacitive devices driving Josephson junction **104** and forming a nonlinear resonator. A ground-plane (not visible) typically surrounds all or a portion of this structure.

[0011] As can be seen, fabricating capacitive coupling structures **102** in a coplanar manner with the structures of qubit **100** takes up the very limited planar real-estate on the fabrication plane of chip **100**. Josephson junction **104**

– which is barely visible in the image of this figure - occupies only a fraction of the exaggerated box drawn around the junction to identify its position. The area occupied by capacitive coupling structures **102** is significantly more than the area of Josephson junction **104**.

[0012] A capacitive coupling structure as in any one of the capacitive coupling structures **102**, is fabricated coplanar with the qubit elements such as the Josephson junction and the junction's driving capacitors. Embodiments of the invention recognize that fabricating capacitive coupling devices as coplanar to the qubit circuit elements limits the number of qubits that can be fabricated per die in a fabrication process. Embodiments of the invention recognize that a need exists for a method of fabricating a capacitive coupling device that is not in the same plane of fabrication as the Josephson junction or its driving capacitors.

[0013] A capacitive coupling structure that can be used in place of any one of the capacitive coupling structures **102**, is interchangeably referred to herein as C-coupler. A superconducting C-coupler according to an illustrative embodiment is not coplanar with the qubit elements. A plane of a fabrication substrate, e.g., a silicon substrate of a semiconducting wafer, on which the superconducting qubit elements are fabricated is referred to herein as a "front" side (front, frontside) regardless of the actual orientation of the plane during fabrication. A "back" side (back, backside) of the substrate is opposite the frontside, to wit, an opposite surface of the same wafer which is substantially parallel to the front side of the wafer.

[0014] The structures of a superconducting C-coupler are fabricated from the backside, through the substrate, in a substantially perpendicular direction from the frontside plane of fabrication of the qubit. A structure that is formed through a silicon substrate in a direction perpendicular to a plane of fabrication is referred to as a "Through-Silicon via" or "TSV" or simply a "via". Normally, a via passes completely through the silicon substrate from one side – e.g. the frontside - to the other side – e.g., the backside. A structure of the superconducting C-coupler protrudes partially through the thickness of the substrate between the frontside and the backside. Such a structure is referred to herein as a "partial via".

[0015] This manner of fabricating a superconducting C-coupler allows the capacitive coupling to be removed from the fabrication plane of the qubit, freeing up space in that plane for more qubit elements but still enabling the capacitive coupling between qubit elements and a readout circuit. Additionally, the partial vias of the superconducting C-coupler allow the readout circuitry to also be desirably placed or fabricated on the back side.

SUMMARY

[0016] Embodiments of the invention provide a superconducting device, and a method and system of fabrication therefor. A superconducting device embodying the invention comprises a capacitive coupling device (superconducting C-coupler) including a trench through a substrate, from a backside of the substrate, reaching a

depth in the substrate, substantially orthogonal to a plane of fabrication on a frontside of the substrate, the depth being less than a thickness of the substrate. A superconducting material is deposited as a via layer in the trench with a space between surfaces of the via layer in the trench remaining accessible from the backside. A superconducting pad is on the frontside, the superconducting pad coupling with a quantum logic circuit element fabricated on the frontside. An extension of the via layer is on the backside, wherein the extension couples to a quantum readout circuit element fabricated on the backside. Thus, there is provided a non-coplanar capacitive coupling partial via that saves space in the fabrication plane of a qubit device for other purposes, such as for additional qubit devices.

[0017] Another embodiment of the invention further includes a dielectric material filled, from the backside, in the space between the surfaces of the via layer. Thus, there is provided one specific manner of forming the partial via.

[0018] The dielectric material may be Silicon oxide (SiO2). Thus, there is provided a specific material for forming one structure of the partial via.

[0019] The dielectric material may be etched such that the dielectric material is removed and the space is occupied by air. Thus, there is provided a process by which another material can be used for forming one structure of the partial via.

[0020] A layer of a second superconducting material may be deposited on the frontside, wherein the layer of second superconducting material is masked and etched to form the superconducting pad on the frontside. Thus, there is provided a structure and a method of forming said structure to capacitively couple with the partial via.

[0021] The layer of second superconducting material may be deposited prior to forming the trench, wherein the layer of second superconducting material is protected by a sacrificial layer. Thus, there is provided one sequence of fabrication operations which forms the structure to capacitively couple with the partial via.

[0022] The extension of the via layer may be electrically coupled with the quantum readout circuit element. Thus, there is provided one structure using which the partial via can be used in a readout circuit.

[0023] The extension of the via layer may be directly electrically coupled with the quantum readout circuit element. Thus, there is provided one method of coupling the partial via with the readout circuit.

[0024] The extension of the via layer may be electrically coupled to a second superconducting pad on the backside, wherein the second superconducting pad couples with the quantum readout circuit element. Thus, there is provided another method of coupling the partial via with the readout circuit.

[0025] An additional set of partial trenches containing superconducting via layers may be included in the device, with these superconducting via layers electrically connected to a ground-plane on the back side of the substrate. These additional vias are positioned to provide a grounding shield between C-couplers vias, to reduce cross-coupling among nearby C-couplers. The additional vias are fabricated simultaneously and identically to the superconducting C-coupler vias.

[0026] An embodiment of the invention includes a fabrication method for fabricating the superconducting device.

[0027] An embodiment of the invention includes a fabrication system for fabricating the superconducting device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] The novel features of the invention are set forth in the appended claims. The invention itself, however, as well as a preferred mode of use, further objectives and advantages thereof, will best be understood by reference to the following detailed description of the illustrative embodiments of the invention when read in conjunction with the accompanying drawings, wherein:

[0029] **Figure 1** depicts a scaled image of qubit with a capacitive coupling to external circuits;

[0030] **Figure 2** depicts a schematic of a superconducting C-coupler used to capacitively couple with a superconducting element of a quantum logic circuit in accordance with an embodiment of the invention;

[0031] **Figure 3** depicts another schematic of a superconducting C-coupler used to capacitively couple with a superconducting element of a quantum logic circuit in accordance with an embodiment of the invention;

[0032] **Figure 4** depicts a block diagram of an example step in a first example fabrication process for fabricating a superconducting C-coupler in accordance with an embodiment of the invention;

[0033] **Figure 5** depicts a block diagram of another example step in the first example fabrication process;

[0034] **Figure 6** depicts a block diagram of another example step in the first example fabrication process;

[0035] **Figure 7** depicts a block diagram of an example step in the first example fabrication process;

[0036] **Figure 8** depicts a block diagram of another example step in the first example fabrication process;

[0037] **Figure 9** depicts a block diagram of another example step in the first example fabrication process;

[0038] **Figure 10** depicts a block diagram of another example step in the first example fabrication process;

[0039] **Figure 11** depicts a block diagram of another example step in the first example fabrication process;

[0040] **Figure 12** depicts a block diagram of another example step in the first example fabrication process;

[0041] **Figure 13** depicts a block diagram of an example step in a second example fabrication process for fabricating a superconducting C-coupler in accordance with an embodiment of the invention;

[0042] **Figure 14** depicts a block diagram of another example step in the second example fabrication process;

[0043] **Figure 15** depicts a block diagram of another example step in the second example fabrication process;

[0044] **Figure 16** depicts a block diagram of another example step in the second example fabrication process;

[0045] **Figure 17** depicts a block diagram of an example step in the second example fabrication process;

[0046] **Figure 18** depicts a block diagram of another example step in the second example fabrication process;

[0047] **Figure 19** depicts a block diagram of another example step in the second example fabrication process;

[0048] **Figure 20** depicts a block diagram of another example step in the second example fabrication process;

[0049] **Figure 21** depicts a block diagram of another example step in the second example fabrication process; and

[0050] **Figure 22** depicts a block diagram of another example step in the second example fabrication process.

DETAILED DESCRIPTION

[0051] The embodiments used to describe the invention generally address and solve the above-described need for superconducting C-coupler. The embodiments of the invention provide a fabrication method for backside coupling with superconducting partial TSV for transmon qubits.

[0052] An embodiment of the invention can be implemented as a superconducting capacitive device for capacitive coupling with a superconducting quantum logic circuit, including but not limited to as a superconducting C-coupler

coupled to a superconducting qubit, in a qubit chip. A fabrication method for superconducting C-couplers can be implemented as a software application. The application implementing an embodiment of the invention can be configured to operate in conjunction with an existing semiconductor/superconductor fabrication system – such as a lithography system.

[0053] For the clarity of the description, and without implying any limitation thereto, embodiments of the invention are described using a simplified diagram of the example superconducting C-coupler in the figures and the illustrative embodiments. In an actual fabrication of a superconducting C-coupler, additional structures that are not shown or described herein, or structures different from those shown and described herein, may be present without departing the scope of the invention. Similarly, within the scope of the invention, a shown or described structure in the example superconducting C-coupler may be fabricated differently to yield a similar operation or result as described herein.

[0054] Differently shaded portions in the two-dimensional drawing of the example structures, layers, and formations are intended to represent different structures, layers, materials, and formations in the example fabrication, as described herein. The different structures, layers, materials, and formations may be fabricated using suitable materials that are known to those of ordinary skill in the art.

[0055] A specific shape, location, position, or dimension of a shape depicted herein is not intended to be limiting on the embodiments of the invention unless such a characteristic is expressly described as a feature of an embodiment of the invention. The shape, location, position, dimension, or some combination thereof, are chosen only for the clarity of the drawings and the description and may have been exaggerated, minimized, or otherwise changed from actual shape, location, position, or dimension that might be used in actual photolithography to achieve an objective according to the embodiments of the invention.

[0056] An embodiment of the invention when implemented in an application causes a fabrication process to perform certain steps as described herein. The steps of the fabrication process are depicted in the several figures. Not all steps may be necessary in a particular fabrication process. Some fabrication processes may implement the steps in different order, combine certain steps, remove or replace certain steps, or perform some combination of these and other manipulations of steps, without departing the scope of the invention.

[0057] Embodiments of the invention are described with respect to certain types of materials, electrical properties, structures, formations, layers orientations, directions, steps, operations, planes, dimensions, numerosity, data processing systems, environments, components, and applications only as examples. Any specific manifestations of these and other similar artifacts are not intended to be limiting to the invention. Any suitable manifestation of these and other similar artifacts can be selected within the scope of the invention.

[0058] Embodiments of the invention are described using specific designs, architectures, layouts, schematics, and tools only as examples and are not limiting to the invention. Embodiments of the invention may be used in conjunction with other comparable or similarly purposed designs, architectures, layouts, schematics, and tools.

[0059] The examples in this disclosure are used only for the clarity of the description and are not limiting to the invention. Any advantages listed herein are only examples and are not intended to be limiting to the invention. Additional or different advantages may be realized by specific embodiments of the invention. Furthermore, a particular embodiment of the invention may have some, all, or none of the advantages listed above.

[0060] A qubit is only used as a non-limiting example superconducting quantum logic circuit in which an embodiment of the invention can be used. From this disclosure, those of ordinary skill in the art will be able to conceive many other superconducting quantum logic circuits in which vertical q-capacitors embodying the invention will be usable, and the same are contemplated within the scope of the invention.

[0061] With reference to **Figure 2**, this figure depicts a schematic of a superconducting C-coupler used to capacitively couple with a superconducting element of a quantum logic circuit in accordance with an embodiment of the invention. In schematic configuration **200**, superconducting C-coupler **202** represents a q-capacitor fabricated in a manner described herein, e.g., usable in place of coupling capacitors **102** in **Figure 1**.

[0062] Substrate **201** is formed of a suitable substrate material, such as, but not limited to, Silicon (Si). Substrate has a frontside and a backside as shown. Superconducting C-coupler **202** is formed partially through substrate **201** as shown. Superconducting C-coupler **202** comprises partial vias **208** which are formed from the backside, in a direction substantially perpendicular to the plane of fabrication of the quantum logic circuit, to wit, the frontside, but not quite reaching the frontside. A thickness “d” of substrate **201** remains between top **208A** of partial vias **208** and the bottom of capacitive pads **206**. In one example, d is of the order of 10-100 microns. Capacitive pads **206** are qubit elements similar to capacitor pads **106** in **Figure 1**.

[0063] Top **208A** of a partial via **208** and a capacitive pad **206** together form capacitive coupling **204**. The substrate remaining in thickness d, e.g., Si of thickness d, forms dielectric **205** in capacitive coupling **204**. In one embodiment, entire partial via **208** and capacitive pad **206** forms capacitive coupling **204**.

[0064] In an additional embodiment of the invention, some of the partial vias 208 may be grounded on the back-side of the wafer in order to form a shield between q-capacitor vias. The grounded partial vias connect to a ground-plane integrated within the resonators and I/O pads 210 on the back-side of the wafer. This ground shield serves the same function as the ground-plane that exists in typical coplanar circuits (figure 1), and reduces cross-coupling among nearby q-capacitor vias.

[0065] Partial via **208** comprises a trench that is lined with a superconducting material (SC2). The superconducting material (SC1) of the capacitive pads **206** and SC2 can be different but need not be different. For example, SC1 may be Niobium (Nb) because Nb is conducive to sputtering method of deposition, and SC2 may be Titanium nitride (TiN) because TiN is more suitable for atomic layer deposition (ALD).

[0066] The trench lining of partial via **208** comprises top portion **208A** of the lining and side layer portions **208B** of the lining. Additionally, in some embodiments of the invention, the lining may extend onto the backside surface in the form of pads **210**. Pads **210** are usable to couple with a readout circuit component, e.g., a resonator or an input/output device/line.

[0067] In this example depiction, a space inside the SC2 lining in the trench of partial via **208** is shown filled with filler **203**. In one example, filler **203** is an oxide, e.g., Silicon-oxide (SiO2). In another example, filler **203** is air, vacuum of a certain degree, or another suitable insulating material.

[0068] With reference to **Figure 3**, this figure depicts another schematic of a superconducting C-coupler used to capacitively couple with a superconducting element of a quantum logic circuit in accordance with an embodiment of the invention. In schematic configuration **300**, superconducting C-coupler **302** represents a q-capacitor fabricated in a manner described herein, e.g., usable in place of coupling capacitors **102** in **Figure 1**. Configuration **300** includes some features that are similar to those described in configuration **200** of **Figure 2**. All reference numerals that are common between **Figure 2** and **Figure 3** represent the features as described with respect to **Figure 2**.

[0069] Partial via **208** may extend on the backside in a variety of ways. One example non-limiting manner of extending the superconducting lining of the trench of partial via **208** was depicted in **Figure 2**. **Figure 3** shows another non-limiting manner of extending the superconducting lining of the trench of partial via **208** on the backside of substrate **201**. Here, one side portion **208B** of the lining of a partial via **208** includes extension **304** on the backside. The other side portion **208B** of the lining in the same partial via **208** terminates at the surface of the backside. Extension **304** connects with superconducting pad **310**. Superconducting pad **310** can be formed using SC1 of pads **206** or another material different from SC2 of the lining of partial vias **208**. Pad **310** is then usable to couple with a readout circuit component, e.g., a resonator, an input/output device/line, or a ground-plane integrated within the resonators and I/O pads **310**. In this way, some of the partial vias **208** may serve as a ground shield between nearby q-capacitor vias.

[0070] Additionally, partial vias **208** are depicted as hollow and open. In other words, where oxide **203** was used as the filler in partial vias **208** in configuration **200**, configuration **300** depicts partial vias **208** filled with filler **303**, which is air, vacuum or partial vacuum, or another suitable insulating material.

[0071] Note that fabrication of the lining of partial vias **208** in the manner of configurations **200** and **300** and the

nature of filler **203** and **303**, respectively therein, are not dependent upon one another. Configuration **200** can be fabricated with air filler and configuration **200** can be fabricated with oxide filler within the scope of the invention.

[0072] Capacitive coupling **204** is communicating the qubit information to the readout circuitry through partial vias **208**. Each partial via **208** comprises a continuous conducting structure. The enclosed area **203** of each partial via **208** does not capacitively interfere with its respective capacitive coupling **204**.

[0073] **Figures 4-12** depict various example steps of one example fabrication process for fabricating a superconducting C-coupler. **Figures 13-22** depict various example steps of a second example fabrication process for fabricating a superconducting C-coupler. The superconducting C-couplers formed by the two example processes are structurally different as described below but are functionally equivalent to be interchangeably usable instead of coupling capacitors **102** in **Figure 1**.

[0074] With reference to **Figure 4**, this figure depicts a block diagram of an example step in the first example fabrication process for fabricating a superconducting C-coupler in accordance with an embodiment of the invention. Substrate **201** is the same as described with respect to **Figures 2-3**.

[0075] In step **400**, layer **402** of superconducting material SC1 is deposited on the frontside of substrate **201**. As a non-limiting example, Nb is sputter-deposited on the frontside to form layer **402**. Other materials having similar superconducting and deposition characteristics as SC1, e.g., for use as pads **206**, may be used and suitably deposited as layer **402** within the scope of the invention.

[0076] With reference to **Figure 5**, this figure depicts a block diagram of another example step in the first example fabrication process. Fabrication continues on the frontside of substrate **201**.

[0077] In step **500**, layer **502** of oxide or other similarly protective material is deposited on superconducting layer **402**. As a non-limiting example, SiO2 may be used in layer **502**.

[0078] With reference to **Figure 6**, this figure depicts a block diagram of another example step in the first example fabrication process. Fabrication step **600** continues on the backside of substrate **201**.

[0079] In fabrication systems that fabricate from only one side, the wafer is turned over such that the fabrication can proceed on the backside. As can be seen in this figure, the wafer of substrate **201** has been flipped to bring the backside up, assuming the fabrication system fabricates from the top. In some fabrication systems the flipping of the wafer may be omitted if the backside can be fabricated without the flip.

[0080] One or more trench **602** is formed using a suitable deep trenching method. Reactive ion etching or Bosch

etching are examples of deep trenching methods that can be used to form trenches **602**. In one example, trench **602** is formed with an aspect ratio of 20:1, i.e., for every 20 microns in depth of trench **602**, opening **602D** of trench **602** expands by 1 micron, giving trench **602** the tapered shape. Essentially, walls **602A** and **602B** of trench **602** are substantially parallel within a tolerance defined by this or similar aspect ratio. In subsequent steps, surface **602C** of trench **602** will form top **208A** as shown in configurations **200** and **300**.

[0081] With reference to **Figure 7**, this figure depicts a block diagram of an example step in the first example fabrication process. Fabrication continues on the backside of substrate **201**.

[0082] In step **700**, layer **702** of superconducting material SC2 is deposited on the backside of substrate **201**. Layer **702** comprises portions **702A**, **702B**, **702C**, and **702D**. One or more instances of portions **702A**, **702B**, **702C**, and **702D** may be present depending upon the number of trenches **602**.

[0083] Portions **702A**, **702B**, **702C** of layer **702** cover surfaces **602A**, **602B**, and **602C**, respectively, of each trench **602**. Additionally, portion **702D** of layer **702** covers an untrenched area adjacent to trench **602** on the backside of substrate **201**. Portion **702D** will form either pad **210** of configuration **200** or extension **304** of configuration **300** as described herein. As a non-limiting example, TiN is deposited using ALD on the backside to form layer **702**. Other materials having similar superconducting and deposition characteristics may be used and suitably deposited as material SC2 of layer **702** within the scope of the invention.

[0084] With reference to **Figure 8**, this figure depicts a block diagram of another example step in the first example fabrication process. Fabrication continues on the backside of substrate **201**.

[0085] In step **800**, layer **802** of oxide or other similarly insulating material is deposited on superconducting layer **702**. The material used to form layer **802** also forms filler **803**, which fills a space remaining inside trench **602** that is lined with layer **702**. As a non-limiting example, SiO2 may be used in layer **802**. At least some portions of layer **802** – e.g., a portion other than portion **803** – serves as a protective layer to protect a portion of layer **702** underneath, and is sacrificial in another step of the fabrication process.

[0086] With reference to **Figure 9**, this figure depicts a block diagram of another example step in the first example fabrication process. Fabrication continues on the backside of substrate **201**.

[0087] In step **900**, one or more portions of layer **802** other than filler portion **803** are removed to reveal layer **702**. For example, a portion of layer **802** that overlies portion **702D** of layer **702** is removed in this step to reveal portion **702D**. The removal process stops at layer **702**. Chemical Mechanical Planarization (CMP) is an example removal method that can be used to remove a portion of layer **802**.

[0088] With reference to **Figure 10**, this figure depicts a block diagram of another example step in the first example fabrication process. Fabrication continues on the backside of substrate **201**.

[0089] In step **1000**, one or more sub-portions of portion(s) **702D** are removed. The removal process of this step masks and etches certain sub-portions which result in one or more etched areas **1002** and pads **210** forming from layer **702D**. The masking and etching process of step **1000** can be implemented using an existing lithography system. This step enables the superconducting partial vias to attach to resonators and I/O pads on the back-side of the wafer, or in some embodiments of the invention for a subset of the superconducting partial vias to connect to resonators and I/O pads while another subset of them connects to a ground-plane on the back-side of the wafer.

[0090] With reference to **Figure 11**, this figure depicts a block diagram of another example step in the first example fabrication process. Fabrication step **1100** continues on the frontside of substrate **201**.

[0091] In fabrication systems that fabricate from only one side, the wafer is turned over such that the fabrication can proceed on the frontside again. As can be seen in this figure, the wafer of substrate **201** has been flipped to bring the frontside up, assuming the fabrication system fabricates from the top. If the wafer was not flipped over in step **600**, then step **1100** may proceed on the frontside without the flip.

[0092] Oxide layer **502**, which was protecting superconducting layer **402** is etched, e.g. using a buffered oxide etch if the material of layer **502** was silicon oxide. The removal of layer **502** exposes layer **402** as shown.

[0093] With reference to **Figure 12**, this figure depicts a block diagram of another example step in the first example fabrication process. Fabrication continues on the frontside of substrate **201**.

[0094] In step **1200**, one or more portions of layer **402** are removed. The removal process of this step masks and etches certain portions, which result in one or more etched areas **1202** and pads **206** forming from layer **402**. Recall from configuration **200** (or **300**) that pads **206** are used as elements of a qubit, e.g., to which a Josephson junction can be coupled or which become parts of a capacitor that drives the Josephson junction. The masking and etching process of step **1200** can be implemented using an existing lithography system. As can be seen, capacitive coupling **204** is now formed using top **208A** or the entirety of partial vias **208** and a pad **206** with intervening dielectric **205** of thickness “d”.

[0095] **Figures 13-22** depict various example steps of a second example fabrication process for fabricating a superconducting C-coupler.

[0096] With reference to **Figure 13**, this figure depicts a block diagram of an example step in the second example fabrication process for fabricating a superconducting C-coupler in accordance with an embodiment of the invention.

Substrate **201** is the same as described with respect to **Figures 2-3**.

[0097] Steps **400** and **500** are performed on substrate **201**, as described with respect to **Figures 4** and **5**.

[0098] Again, the wafer is flipped over in a single direction fabrication system as in **Figure 6**. Essentially, fabrication on the backside is enabled for the fabrication system by making the backside accessible for fabrication.

[0099] In step **1300**, layer **1302** of a superconducting material is deposited on the backside. The superconducting material of layer **1302** can be but need not be the same as the superconducting material of layer **402**. Assuming, as a non-limiting example, that SC1 (Nb) is used for both layers **402** and **1302**, Nb is sputter-deposited on the backside to form layer **1302**. Other materials having similar superconducting and deposition characteristics as SC1 may be used and suitably deposited as layer **1302** within the scope of the invention.

[0100] With reference to **Figure 14**, this figure depicts a block diagram of another example step in the second example fabrication process. Fabrication continues on the backside of substrate **201**.

[0101] In step **1400**, one or more portions of layer **1302** are removed. The removal process of this step masks and etches certain portions, which result in one or more etched areas **1402** and pads **310** forming from layer **1302**. Recall from configuration **300** that pads **310** are used to couple extension **304** of a partial via of a superconducting C-coupler and an external circuit, which may comprise resonators, I/O pads and ground-planes. The masking and etching process of step **1400** can be implemented using an existing lithography system.

[0102] With reference to **Figure 15**, this figure depicts a block diagram of another example step in the second example fabrication process. Fabrication continues on the backside of substrate **201**.

[0103] In step **1500**, layer **1502** of oxide or other similarly protective material is deposited on pads **310**. As a non-limiting example, SiO2 may be used in layer **1502**. Layer **1502** is a protective sacrificial layer. Layer **1502** covers and protects at least pad **310** and can also cover an area of substrate **201** that is exposed around pad **310**.

[0104] With reference to **Figure 16**, this figure depicts a block diagram of another example step in the second example fabrication process. Fabrication continues on the backside of substrate **201**.

[0105] In step **1600**, one or more trench **1602** is formed using a suitable deep trenching method in a manner similar to the manner of forming trench **602** in **Figure 6**. Trench **1602** has characteristics similar to trench **602** with one additional feature. Trench **1602** is formed in such a manner that pad **310** is exposed through a wall of trench **1602** (e.g., wall **1602A** in case of one example trench **1602** as shown, or wall **1602B** in case of the other example trench as shown). Reactive ion etching or Bosch etching are examples of deep trenching methods that can be

used to form trenches **1602**.

[0106] In one embodiment of the invention, trench **1602** is formed with an aspect ratio of 20:1, i.e., for every 20 microns in depth of trench **1602**, opening **1602D** of trench **1602** expands by 1 micron, giving trench **1602** the tapered shape. Essentially, walls **1602A** and **1602B** of trench **1602** are substantially parallel within a tolerance defined by this or similar aspect ratio. In subsequent steps, surface **1602C** of trench **1602** will form top **208A** as shown in configurations **200** and **300**.

[0107] With reference to **Figure 17**, this figure depicts a block diagram of an example step in the second example fabrication process. Fabrication continues on the backside of substrate **201**.

[0108] In step **1700**, layer **1702** of superconducting material SC2 is deposited on the exposed surfaces on the backside. Layer **1702** comprises portions **1702A**, **1702B**, **1702C**, and **1702D**. One or more instances of portions **1702A**, **1702B**, **1702C**, and **1702D** may be present depending upon the number of trenches **1602**.

[0109] Portions **1702A**, **1702B**, **1702C** of layer **1702** cover surfaces **1602A**, **1602B**, and **1602C**, respectively, of each trench **1602**. Additionally, portion **1702D** of layer **1702** establishes an electrical connection with pad **310** as shown. Portion **1702D** will form extension **304** of configuration **300** as described herein. As a non-limiting example, TiN is deposited using ALD on the backside to form layer **1702**. Other materials having similar superconducting and deposition characteristics may be used and suitably deposited as material SC2 of layer **1702** within the scope of the invention.

[0110] With reference to **Figure 18**, this figure depicts a block diagram of another example step in the second example fabrication process. Fabrication continues on the backside of substrate **201**.

[0111] In step **1800**, layer **1802** of oxide or other similarly insulating material is deposited on superconducting layer **1702**. The material used to form layer **1802** also forms filler **1803**, which fills a space remaining inside trench **1602** that is lined with layer **1702**. As a non-limiting example, SiO2 may be used in layer **1802**. At least some portions of layer **1802** – e.g., a portion other than portion **1803** – serves as a protective layer to protect a portion of layer **1702** underneath, and is sacrificial in another step of the fabrication process.

[0112] With reference to **Figure 19**, this figure depicts a block diagram of another example step in the second example fabrication process. Fabrication continues on the backside of substrate **201**.

[0113] In step **1900**, one or more portions of layer **1802** other than filler portion **1803** are removed. The removal step also removes some portions of layer **1702** such that only portions **1702A**, **1702B**, **1702C**, and **1702D** are remaining in the fabricated structure. For example, a portion of layer **1702** that overlies layer **1502** is removed in

this step. The removal process stops at layer **1502**. Chemical Mechanical Planarization (CMP) is an example removal method that can be used to remove a portion of layer **1802**.

[0114] With reference to **Figure 20**, this figure depicts a block diagram of another example step in the second example fabrication process. Fabrication continues on the backside of substrate **201**.

[0115] In fabrication systems that fabricate from only one side, the wafer is turned over such that the fabrication can proceed on the frontside again. As can be seen in this figure, the wafer of substrate **201** has been flipped to bring the frontside up, assuming the fabrication system fabricates from the top. If the wafer was not flipped over in step **1300**, then step **2000** may proceed on the frontside without the flip.

[0116] Oxide layer **502**, which was protecting superconducting layer **402** is etched, e.g. using a buffered oxide etch if the material of layer **502** was silicon oxide. The removal of layer **502** exposes layer **402** as shown.

[0117] With reference to **Figure 21**, this figure depicts a block diagram of another example step in the second example fabrication process. Fabrication continues on the frontside of substrate **201**.

[0118] In step **2100**, one or more portions of layer **402** are removed. The removal process of this step masks and etches certain portions, which result in one or more etched areas **2102** and pads **206** forming from layer **402**. Recall from configuration **200** (or **300**) that pads **206** are used as elements of a qubit, e.g., to which a Josephson junction can be coupled or which become parts of a capacitor that drives the Josephson junction. The masking and etching process of step **2100** can be implemented using an existing lithography system. As can be seen, capacitive coupling **204** is now formed using top **1702A** or the entirety of partial vias **1702** and a pad **206** with intervening dielectric **205** of thickness “d”.

[0119] With reference to **Figure 22**, this figure depicts a block diagram of another example step in the second example fabrication process. Fabrication continues on the backside of substrate **201**.

[0120] The wafer may be flipped to perform the oxide etch. In some cases, etching the oxide from the backside may be performed without flipping the wafer to bring the backside up.

[0121] In step **2200**, one or more portions of layer **1502** are removed. The removal process of this step etches layer **1502** – which in the described example is oxide, and filler **1803** – which in the described example is also oxide. The buffered oxide etching results in one or more etched areas **2202** becoming exposed. The exposed areas include areas of substrate **201** as well as pads **310**. Walls **1702A** and **1702B** and area **1702D** of layer **1702** in each trench **1602** is etched to form extensions **304** and **306**.

[0122] The etching also forms a space between walls **1702A** and **1702B** in deep trenches **1602** such that the space is occupied by air filler in the manner of configuration **300**. In one embodiment of the invention, the etching can be stopped such that filler **1803** is not removed to result in a hybrid of configurations **200** and **300**.

[0123] As can be seen, capacitive coupling **204** is now formed using top **1702A** or the entirety of partial vias **1702** and a pad **206** with intervening dielectric **205** of thickness "d".

[0124] Various embodiments of the present invention are described herein with reference to the related drawings. Alternative embodiments of the invention can be devised without departing from the scope of this invention. Although various connections and positional relationships (e.g., over, below, adjacent, etc.) are set forth between elements in the following description and in the drawings, persons skilled in the art will recognize that many of the positional relationships described herein are orientation-independent when the described functionality is maintained even though the orientation is changed. These connections and/or positional relationships, unless specified otherwise, can be direct or indirect, and the present invention is not intended to be limiting in this respect. Accordingly, a coupling of entities can refer to either a direct or an indirect coupling, and a positional relationship between entities can be a direct or indirect positional relationship. As an example of an indirect positional relationship, references in the present description to forming layer "A" over layer "B" include situations in which one or more intermediate layers (e.g., layer "C") is between layer "A" and layer "B" as long as the relevant characteristics and functionalities of layer "A" and layer "B" are not substantially changed by the intermediate layer(s).

[0125] The following definitions and abbreviations are to be used for the interpretation of the claims and the specification. As used herein, the terms "comprises," "comprising," "includes," "including," "has," "having," "contains" or "containing," or any other variation thereof, are intended to cover a non-exclusive inclusion. For example, a composition, a mixture, process, method, article, or apparatus that comprises a list of elements is not necessarily limited to only those elements but can include other elements not expressly listed or inherent to such composition, mixture, process, method, article, or apparatus.

[0126] Additionally, the term "illustrative" is used herein to mean "serving as an example, instance or illustration." Any embodiment of the invention described herein is not necessarily to be construed as preferred or advantageous over other embodiments of the invention. The terms "at least one" and "one or more" are understood to include any integer number greater than or equal to one, i.e. one, two, three, four, etc. The terms "a plurality" are understood to include any integer number greater than or equal to two, i.e. two, three, four, five, etc. The term "connection" can include an indirect "connection" and a direct "connection."

[0127] References in the specification to "one embodiment," "an embodiment," "an example embodiment," etc., indicate that the embodiment described can include a particular feature, structure, or characteristic, but every

embodiment may or may not include the particular feature, structure, or characteristic. Moreover, such phrases are not necessarily referring to the same embodiment of the invention. Further, when a particular feature, structure, or characteristic is described in connection with an embodiment of the invention, it is submitted that it is within the knowledge of one skilled in the art to affect such feature, structure, or characteristic in connection with other embodiments of the invention whether or not explicitly described.

[0128] The terms “about,” “substantially,” “approximately,” and variations thereof, are intended to include the degree of error associated with measurement of the particular quantity based upon the equipment available at the time of filing the application. For example, “about” can include a range of ± 8% or 5%, or 2% of a given value.

[0129] The descriptions of the various embodiments of the present invention have been presented for purposes of illustration, but are not intended to be exhaustive or limited to the invention. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope of the invention. The terminology used herein was chosen to best explain the principles of the invention, the practical application or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments of the invention described herein.

CLAIMS

1. A capacitive coupling device (superconducting C-coupler) comprising:

a trench through a substrate, from a backside of the substrate, reaching a depth in the substrate, substantially orthogonal to a plane of fabrication on a frontside of the substrate, the depth being less than a thickness of the substrate;

a superconducting material deposited as a via layer in the trench with a space between surfaces of the via layer in the trench remaining accessible from the backside;

a superconducting pad on the frontside, the superconducting pad coupling with a quantum logic circuit element fabricated on the frontside; and

an extension of the via layer on the backside, wherein the extension couples to a quantum readout circuit element fabricated on the backside.

2. The superconducting C-coupler of claim 1, further comprising:

a dielectric material filled, from the backside, in the space between the surfaces of the via layer.

3. The superconducting C-coupler of claim 2, wherein the dielectric material is Silicon oxide (SiO2).

4. The superconducting C-coupler of claim 2,

wherein the dielectric material is etched such that the dielectric material is removed and the space is occupied by air.

5. The superconducting C-coupler of claim 1,

wherein a layer of a second superconducting material is deposited on the frontside, and

wherein the layer of the second superconducting material is masked and etched to form the superconducting pad on the frontside.

6. The superconducting C-coupler of claim 5, wherein the layer of the second superconducting material is deposited prior to forming the trench, and

wherein the layer of the second superconducting material is protected by a sacrificial layer.

7. The superconducting C-coupler of claim 1, wherein the extension of the via layer is electrically coupled with the quantum readout circuit element.

8. The superconducting C-coupler of claim 1, wherein the extension of the via layer is directly electrically coupled with the quantum readout circuit element.

9. The superconducting C-coupler of claim 1, wherein the extension of the via layer is electrically coupled to a second superconducting pad on the backside, and wherein the second superconducting pad couples with the quantum readout circuit element.

10. The superconducting C-coupler of claim 1, wherein the quantum readout circuit element comprises a ground-plane of a circuit, and wherein the C-coupler additionally functions as a grounding shield for other C-couplers coupling with the circuit.

11. A method comprising:

forming, in a capacitive coupling device (superconducting C-coupler), a trench through a substrate, from a backside of the substrate, reaching a depth in the substrate, substantially orthogonal to a plane of fabrication on a frontside of the substrate, the depth being less than a thickness of the substrate;

depositing a superconducting material as a via layer in the trench with a space between surfaces of the via layer in the trench remaining accessible from the backside;

forming a superconducting pad on the frontside, the superconducting pad coupling with a quantum logic circuit element fabricated on the frontside; and

forming an extension of the via layer on the backside, wherein the extension couples to a quantum readout circuit element fabricated on the backside.

12. The method of claim 11, further comprising:

filling a dielectric material, from the backside, in the space between the surfaces of the via layer.

13. The method of claim 12, wherein the dielectric material is Silicon oxide (SiO2).

14. The method of claim 12,

wherein the dielectric material is etched such that the dielectric material is removed and the space is occupied by air.

15. The method of claim 11, further comprising:

depositing a layer of a second superconducting material on the frontside; and

masking and etching the layer of the second superconducting material to form the superconducting pad on the frontside.

16. The method of claim 15, further comprising:

depositing the layer of the second superconducting material prior to forming the trench; and

protecting, using a sacrificial layer, the layer of the second superconducting material.

17. The method of claim 11, further comprising:

electrically coupling the extension of the via layer with the quantum readout circuit element.

18. The method of claim 11, further comprising:

directly electrically coupling the extension of the via layer with the quantum readout circuit element.

19. The method of claim 11, further comprising:

electrically coupling the extension of the via layer to a second superconducting pad on the backside, wherein the second superconducting pad couples with the quantum readout circuit element.

20. The method of claim 11, wherein the quantum readout circuit element comprises a ground-plane of a circuit, and wherein the C-coupler additionally functions as a grounding shield for other C-couplers coupling with the circuit.

21. A superconductor fabrication system comprising a lithography component, the superconductor fabrication system when operated to fabricate a superconducting device performing operations comprising:

forming, in a capacitive coupling device (superconducting C-coupler), a trench through a substrate, from a backside of the substrate, reaching a depth in the substrate, substantially orthogonal to a plane of fabrication on a frontside of the substrate, the depth being less than a thickness of the substrate;

depositing a superconducting material as a via layer in the trench with a space between surfaces of the via layer in the trench remaining accessible from the backside;

forming a superconducting pad on the frontside, the superconducting pad coupling with a quantum logic circuit element fabricated on the frontside; and

forming an extension of the via layer on the backside, wherein the extension couples to a quantum readout circuit element fabricated on the backside.

22. The system of claim 21, further comprising:

filling a dielectric material, from the backside, in the space between the surfaces of the via layer.

23. The system of claim 22, wherein the dielectric material is Silicon oxide (SiO2).

24. The system of claim 22,

wherein the dielectric material is etched such that the dielectric material is removed and the space is occupied by air.

25. The system of claim 21, further comprising:

depositing a layer of a second superconducting material on the frontside; and

masking and etching the layer of the second superconducting material to form the superconducting pad on the frontside.

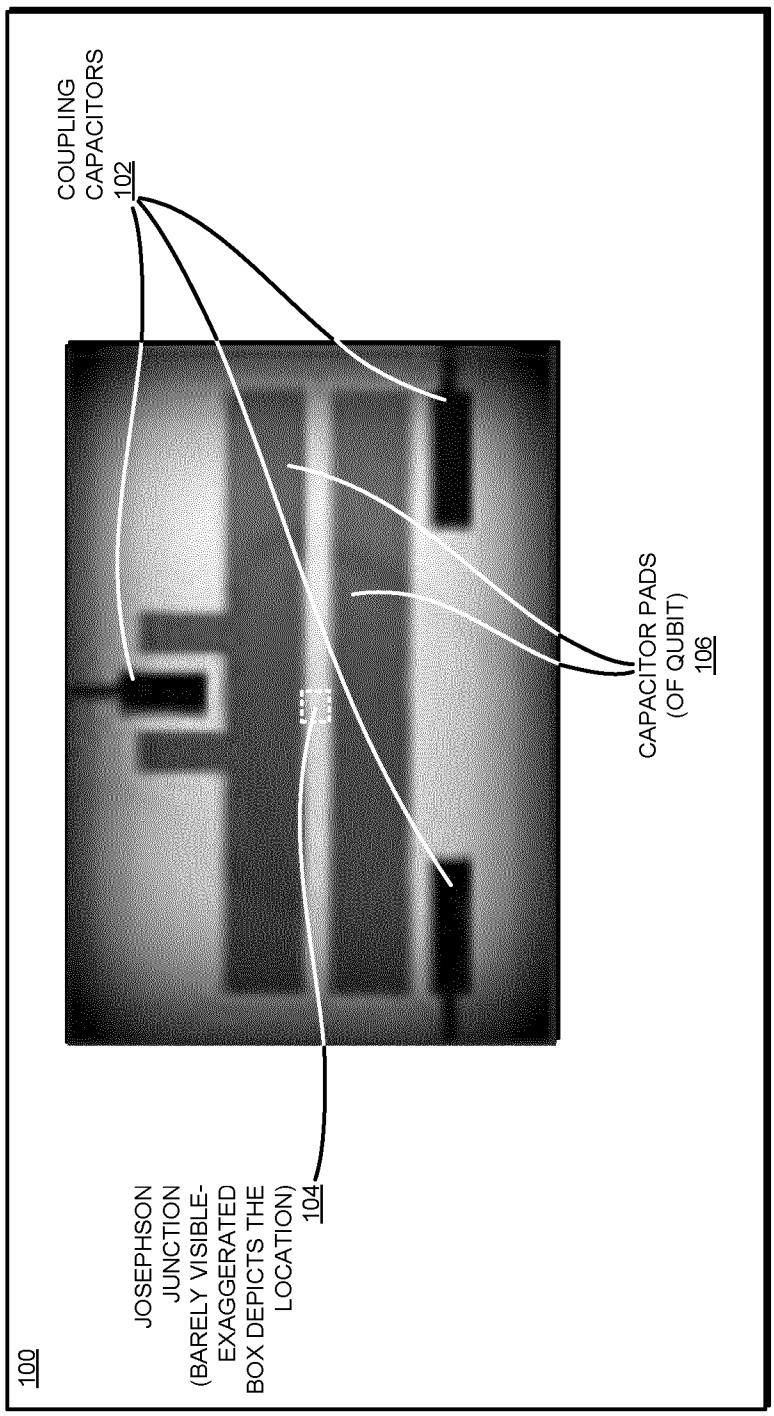
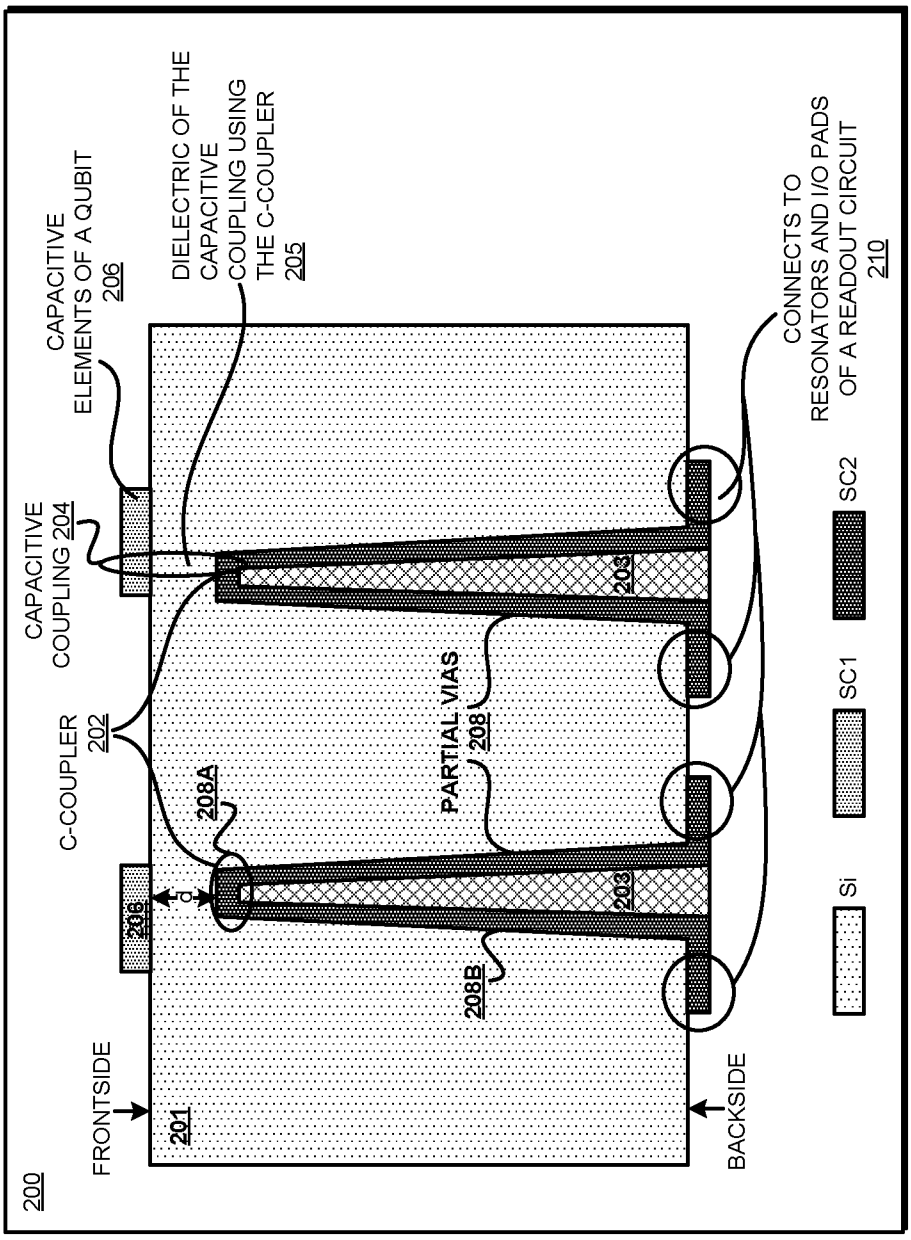


FIGURE 1 (PRIOR-ART)

FIGURE 2


200
FRONTSIDE
201
BACKSIDE
C-COUPLER 202
CAPACITIVE COUPLING 204
CAPACITIVE ELEMENTS OF A QUBIT 206
DIELECTRIC OF THE CAPACITIVE COUPLING USING THE C-COUPLER 205
CONNECTS TO RESONATORS AND I/O PADS OF A READOUT CIRCUIT 210
PARTIAL VIAS 208
208A
208B
206
d
203
Si
SC1
SC2

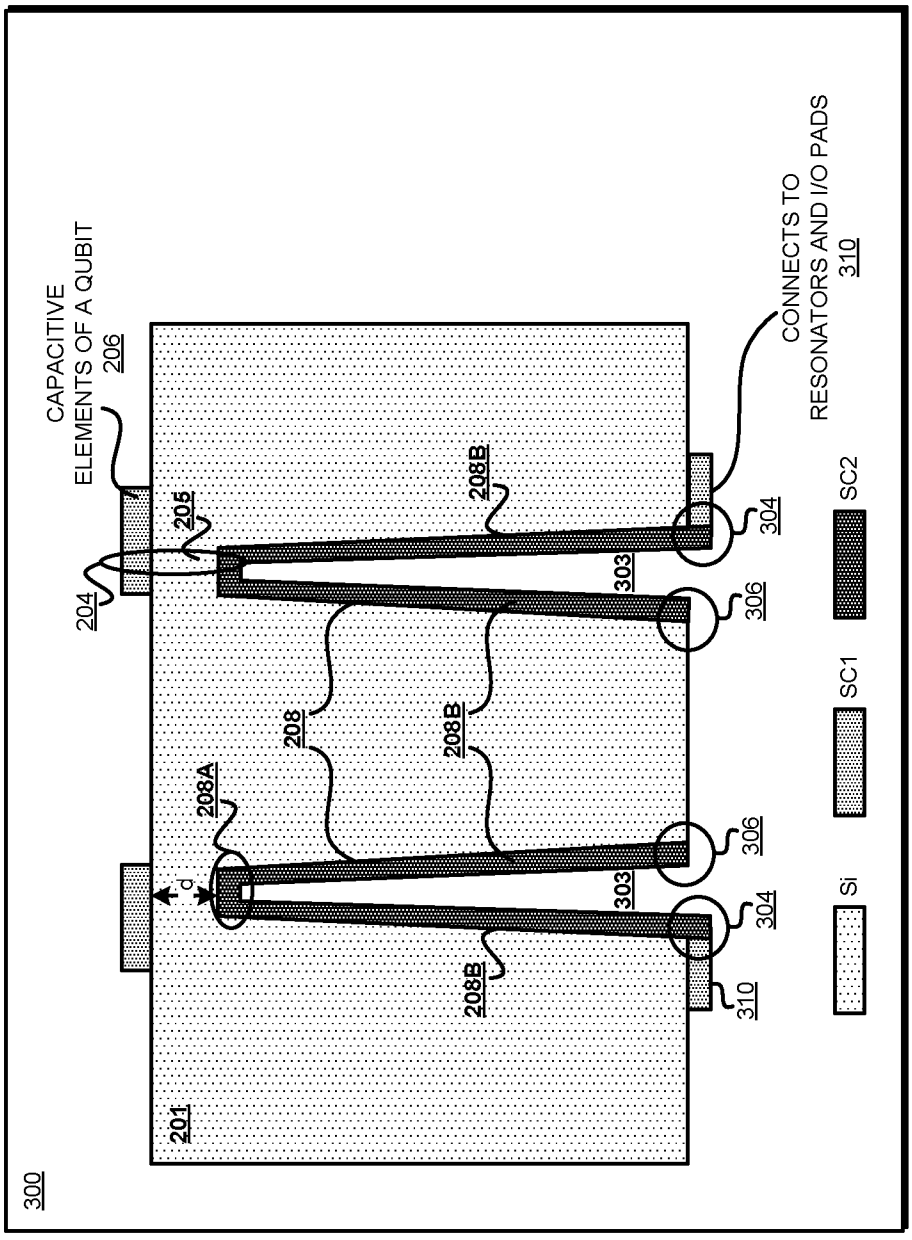

300
201
CAPACITIVE ELEMENTS OF A QUBIT 206
204
205
208
208A
208B
303
304
306
310
d
CONNECTS TO RESONATORS AND I/O PADS 310
SC2
SC1
Si

FIGURE 3

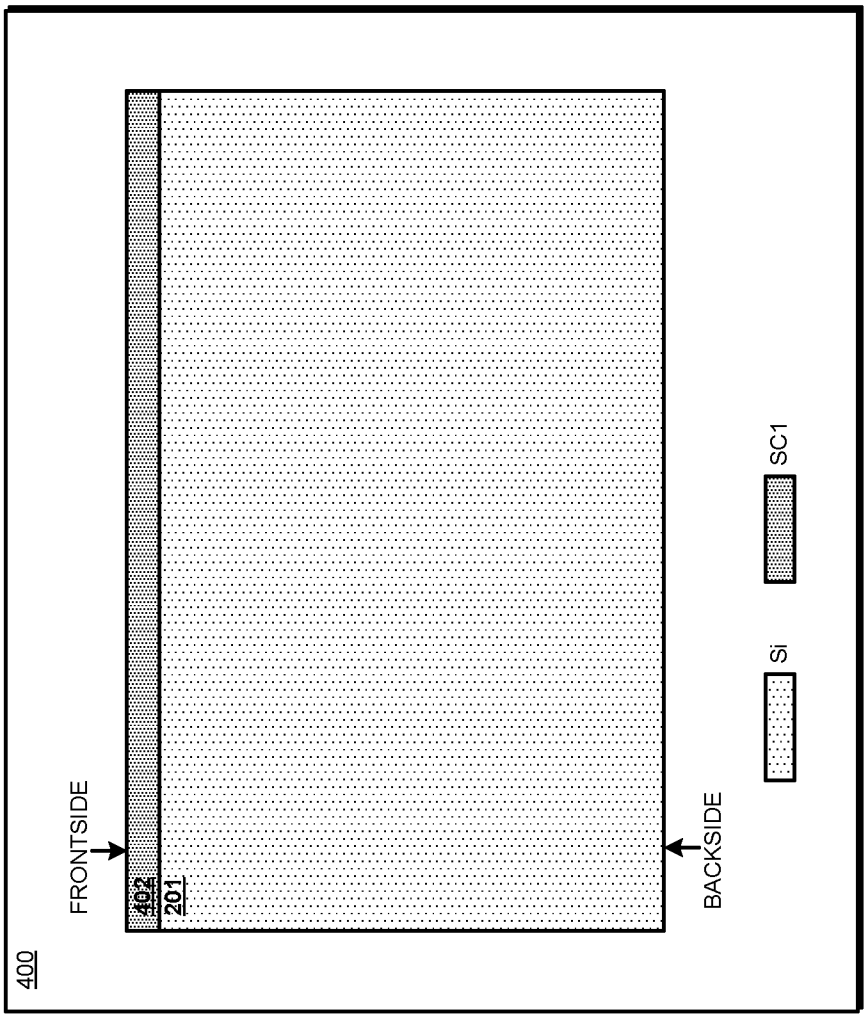


FIGURE 4

FIGURE 5

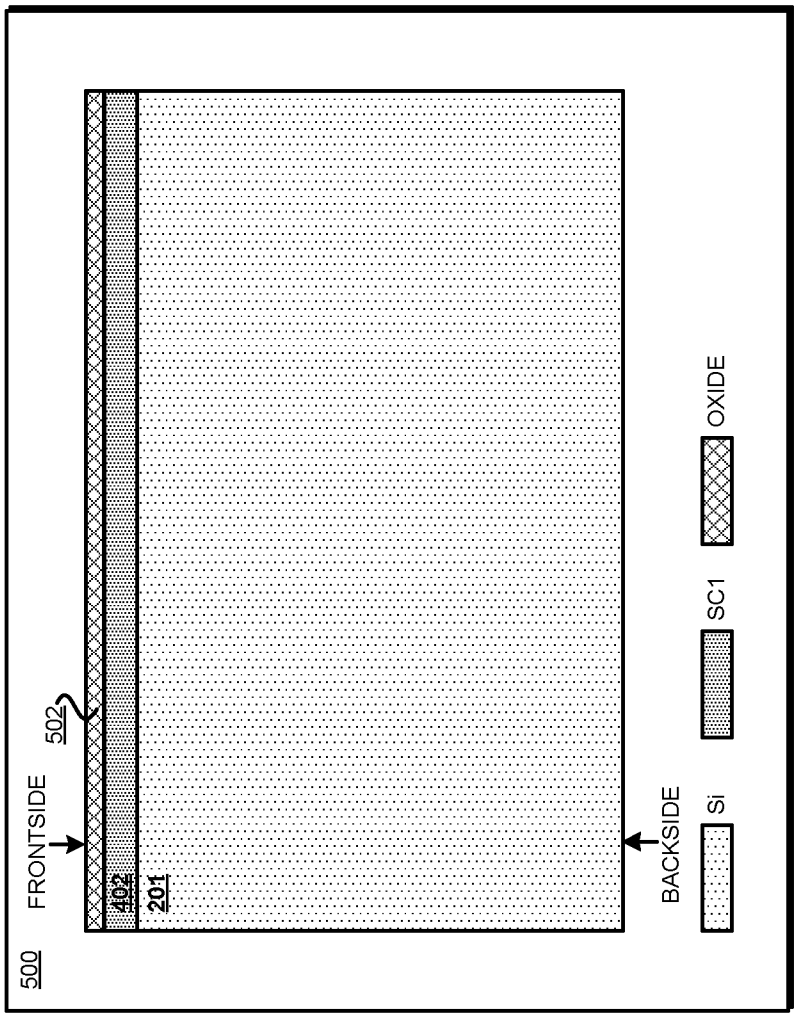
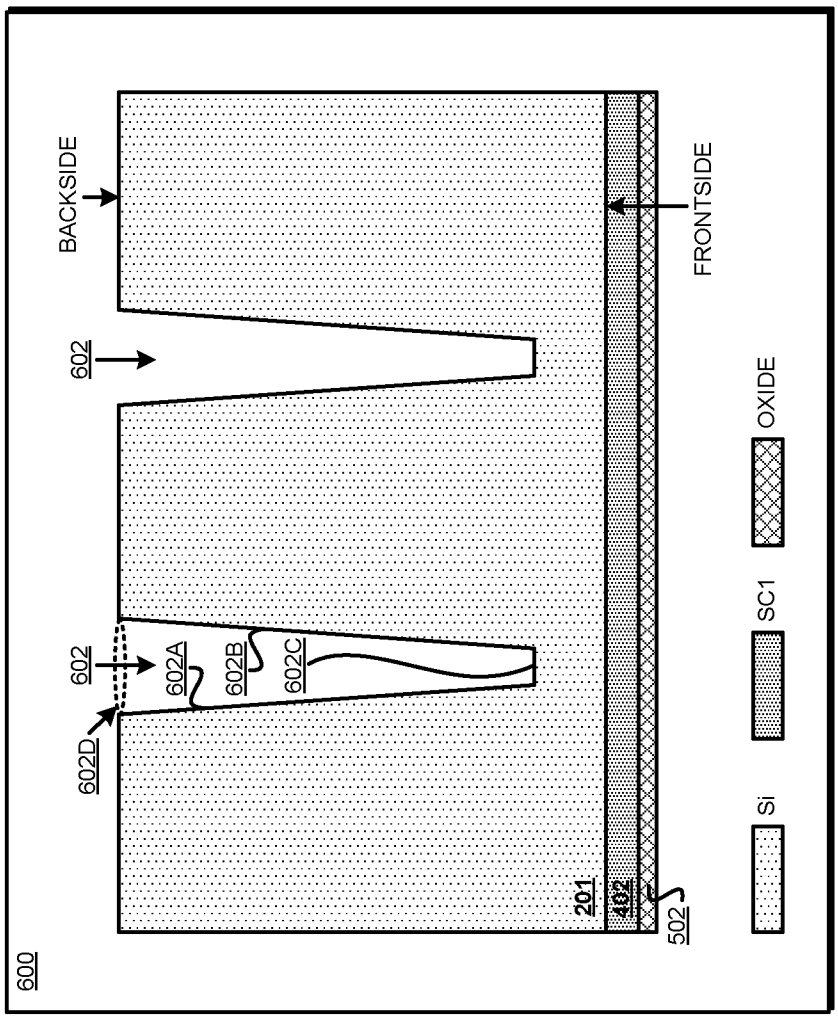


FIGURE 6


600
BACKSIDE
602
602
602A
602B
602C
602D
201
402
502
FRONTSIDE
Si
SC1
OXIDE

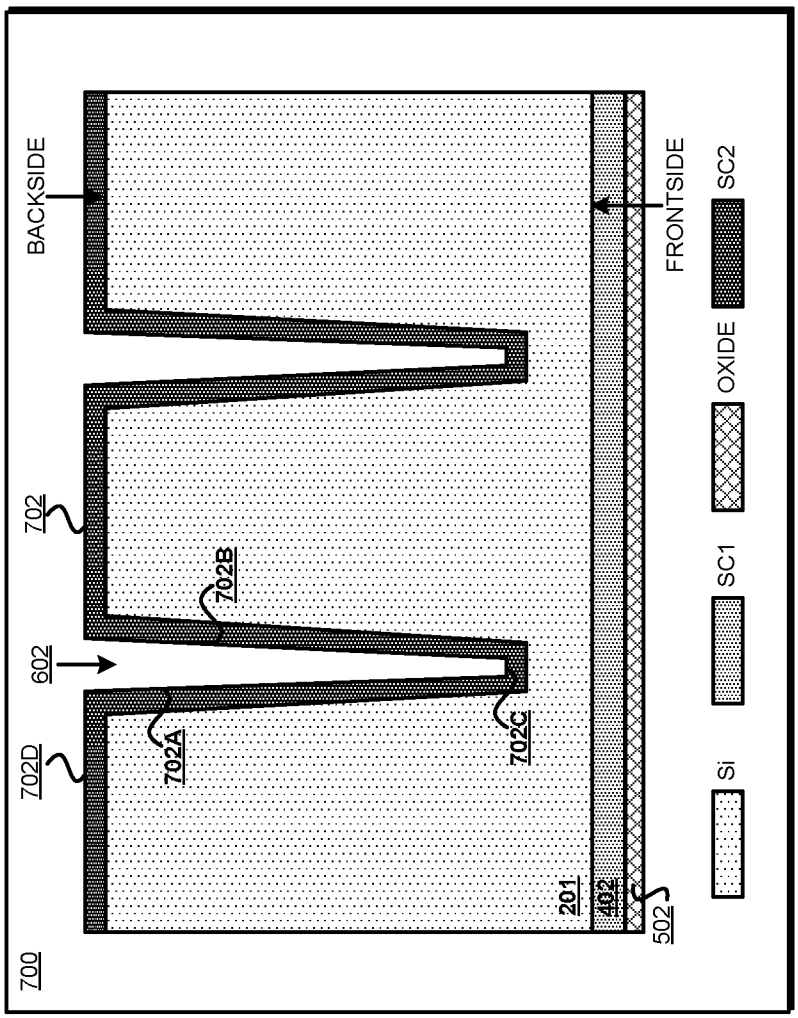

700
BACKSIDE
FRONTSIDE
702
702A
702B
702C
702D
602
201
402
502
Si
SC1
OXIDE
SC2

FIGURE 7

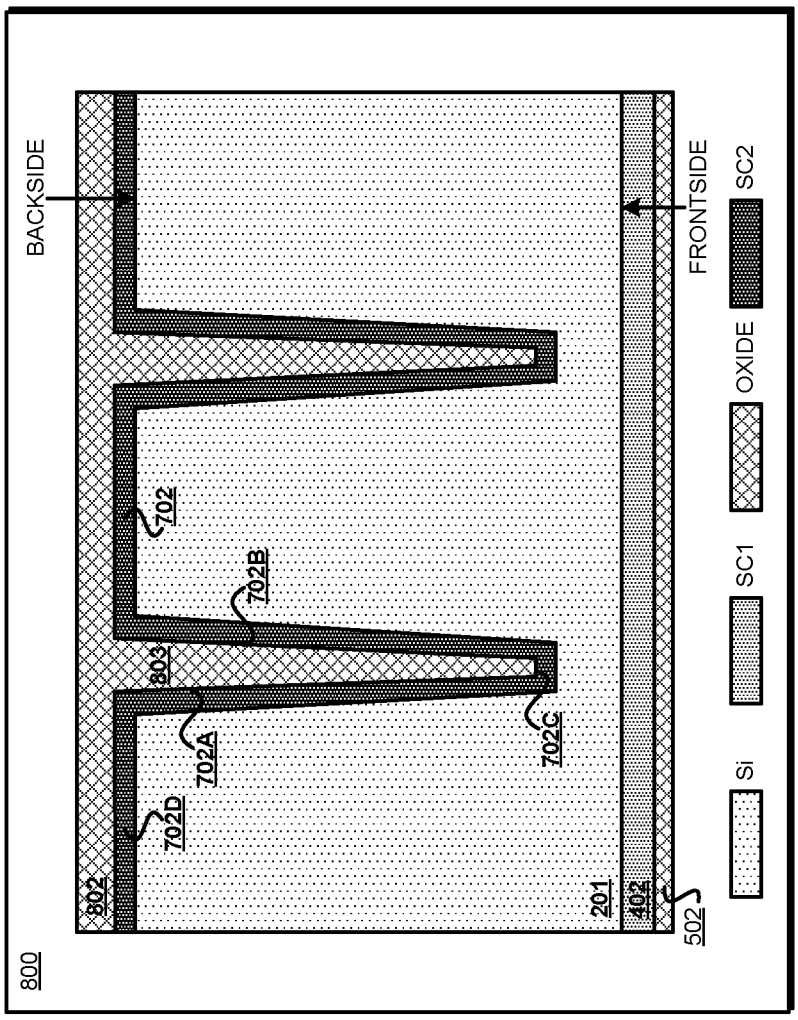

800
BACKSIDE
FRONTSIDE
702
702B
803
702A
702C
702D
802
201
402
502
Si
SC1
OXIDE
SC2

FIGURE 8

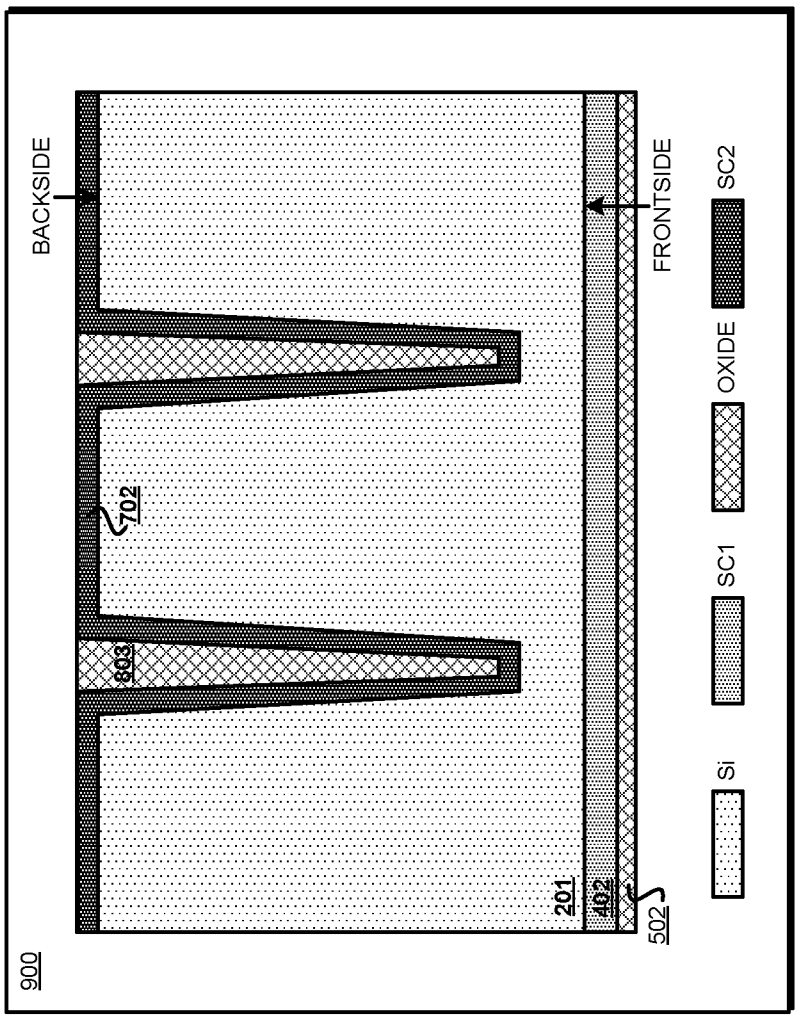


FIGURE 9

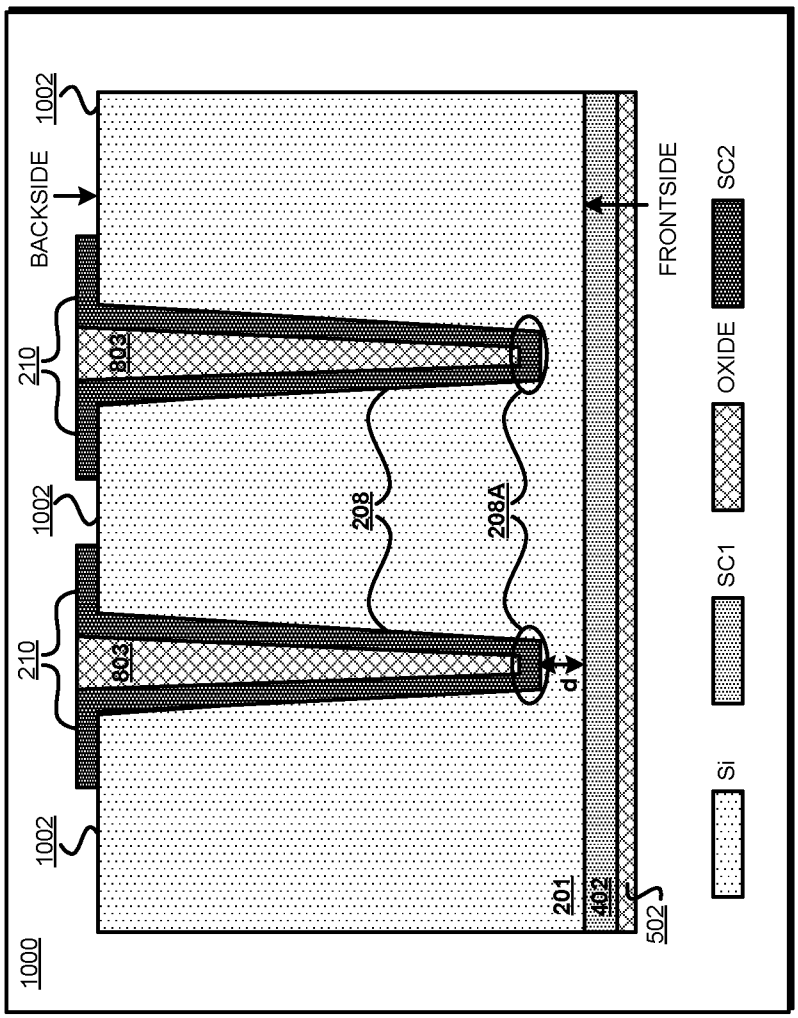

1000
1002
1002
1002
210
210
803
803
208
208A
d
201
402
502
BACKSIDE
FRONTSIDE
Si
SC1
OXIDE
SC2

FIGURE 10

FIGURE 11

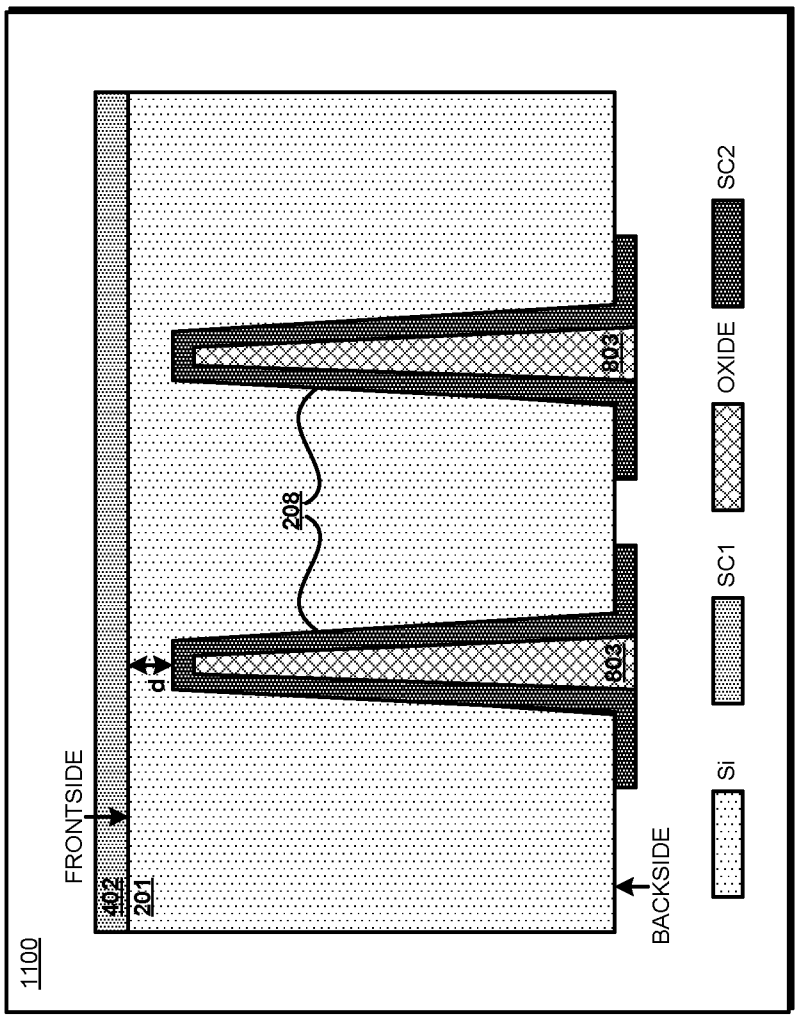

1100
FRONTSIDE
402
201
d
208
803
803
BACKSIDE
Si
SC1
OXIDE
SC2

FIGURE 12

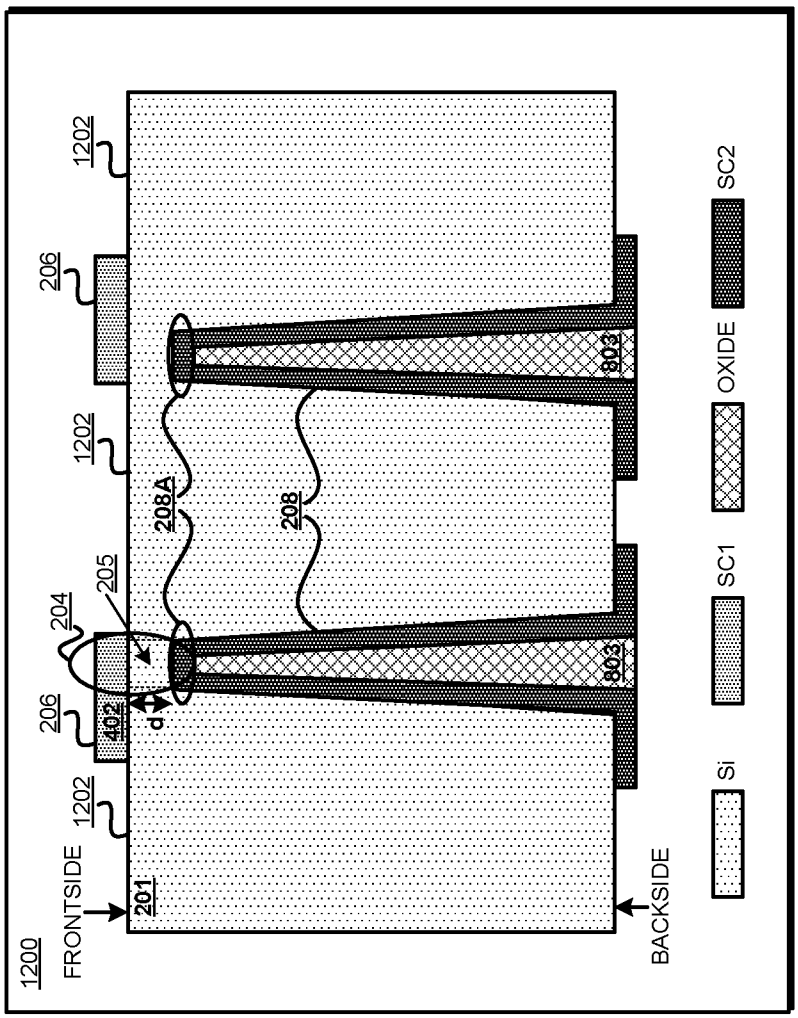

1200
FRONTSIDE
BACKSIDE
201
1202
206
402
d
204
205
208A
208
803
Si
SC1
OXIDE
SC2

FIGURE 13

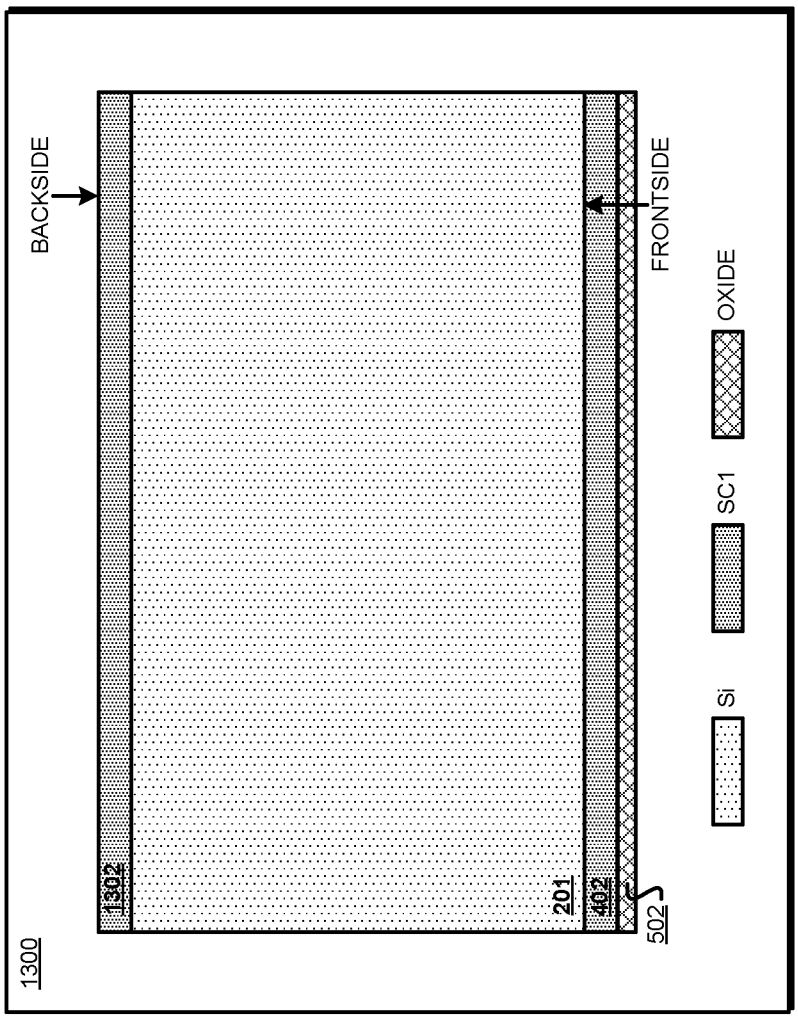


FIGURE 14

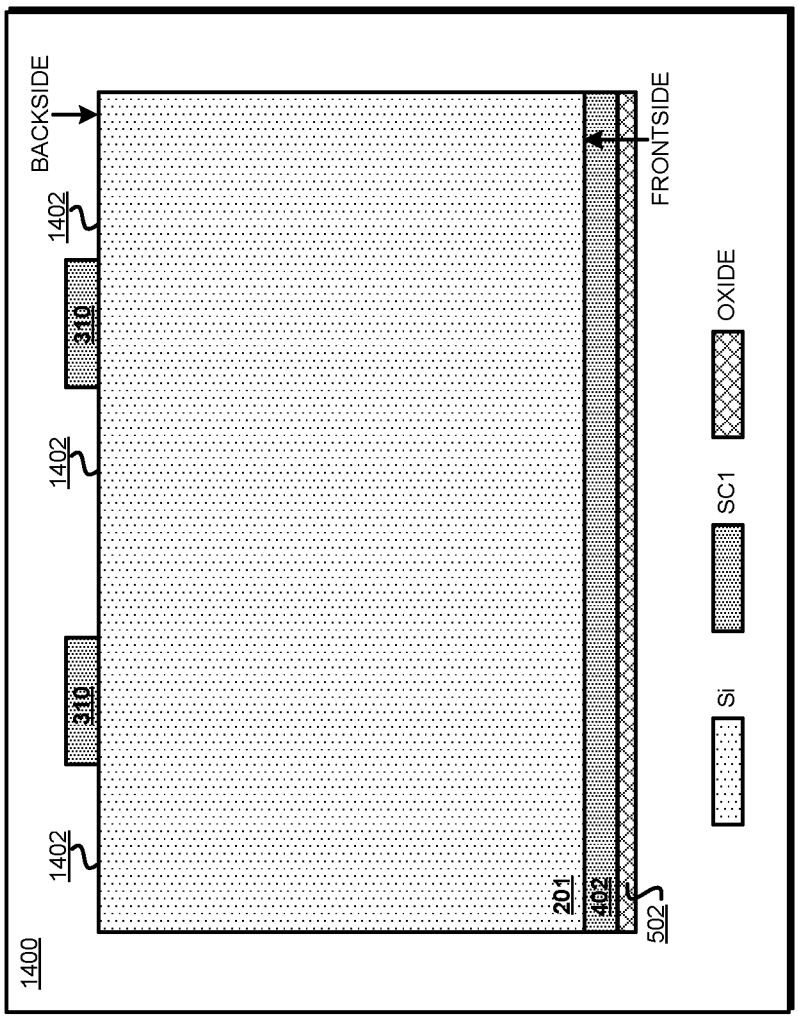
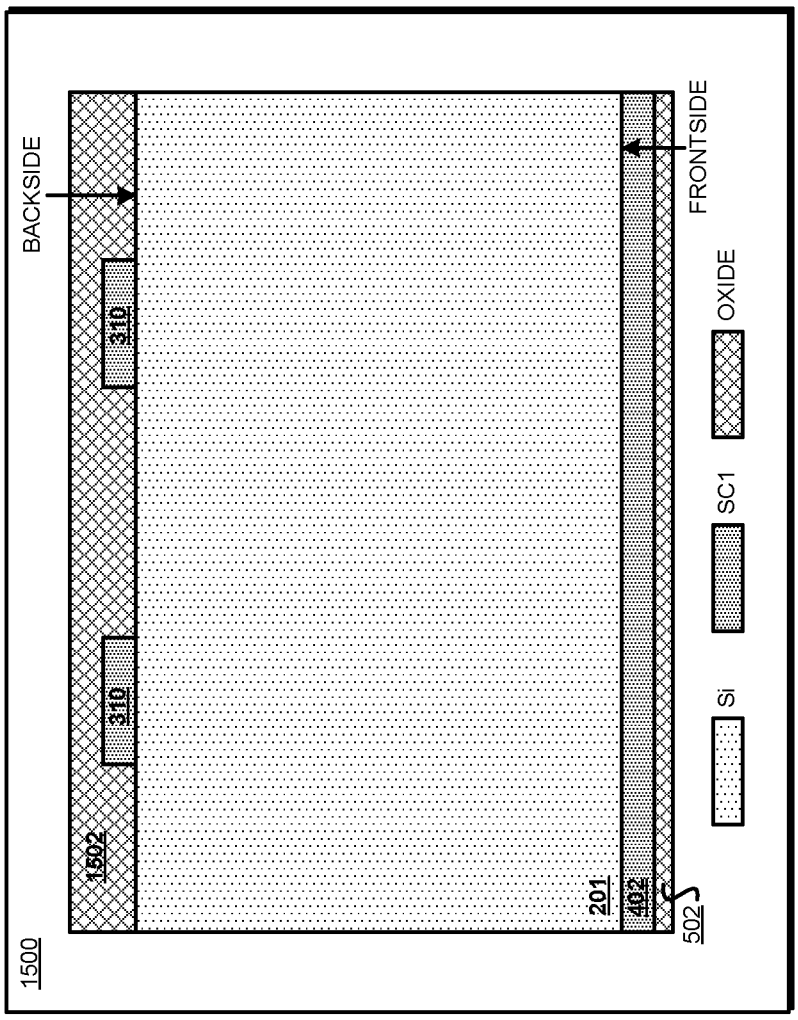
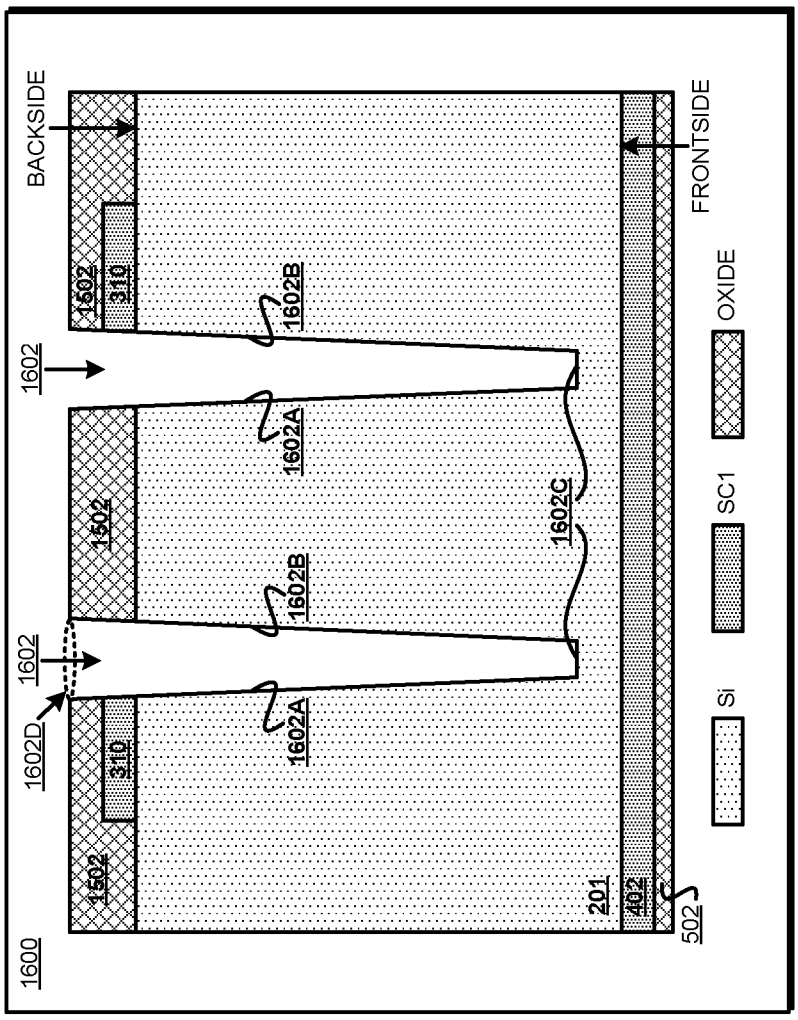

1400
BACKSIDE
FRONTSIDE
1402
1402
1402
319
319
201
402
502
Si
SC1
OXIDE

FIGURE 15


1500
BACKSIDE
FRONTSIDE
310
310
1502
201
402
502
Si
SC1
OXIDE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201
402
502
Si
SC1
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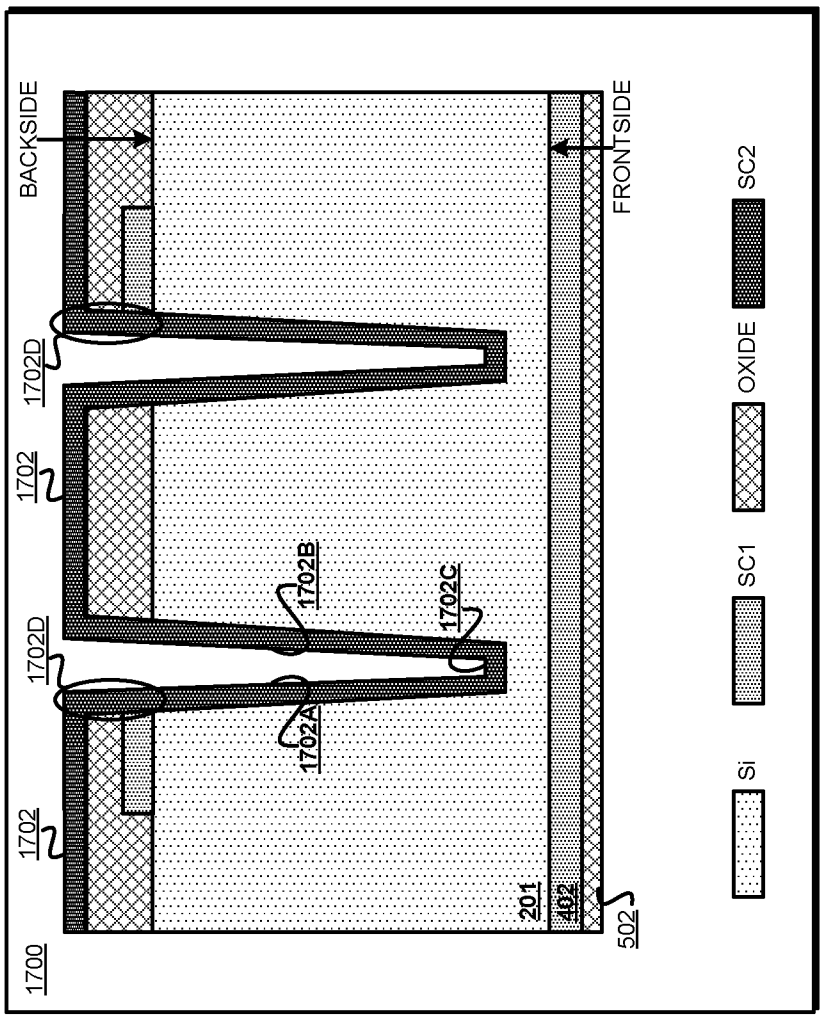
FIGURE 16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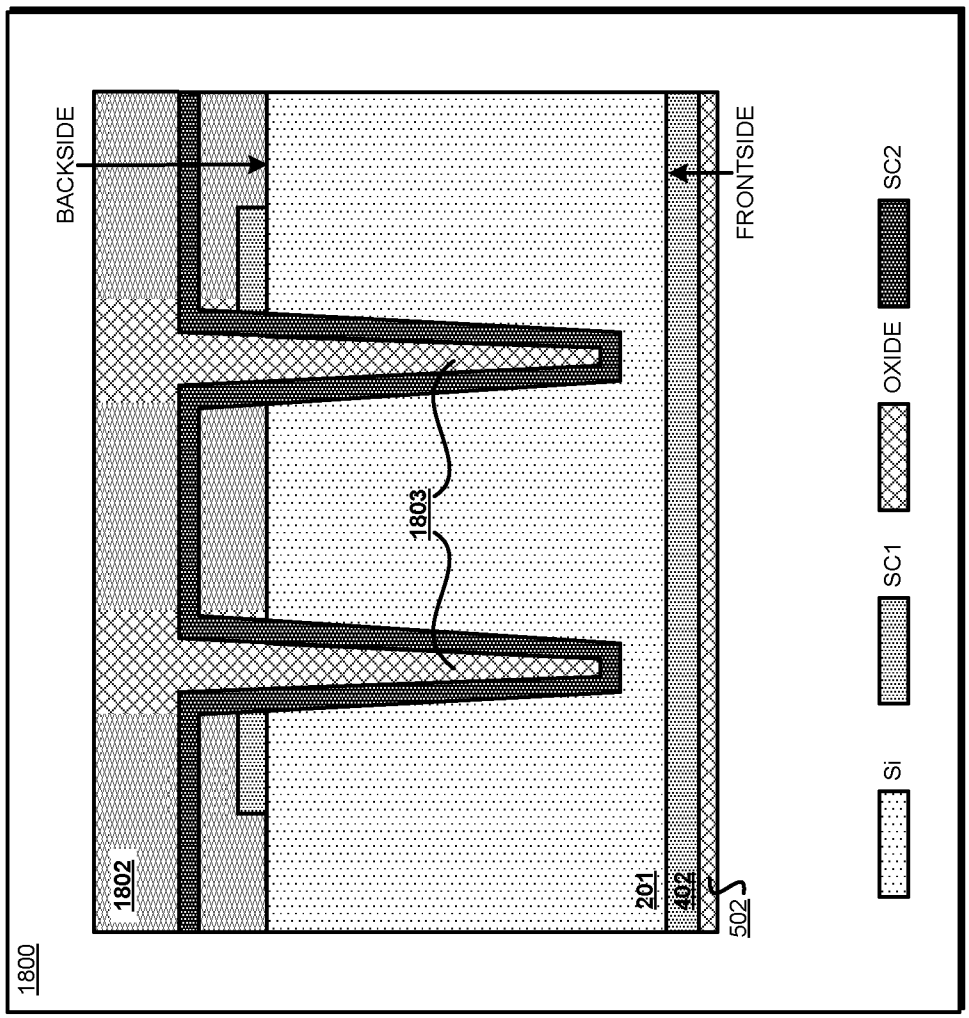
1702B
1702C
201
502
Si
SC1
OXIDE
SC2

FIGURE 17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1803
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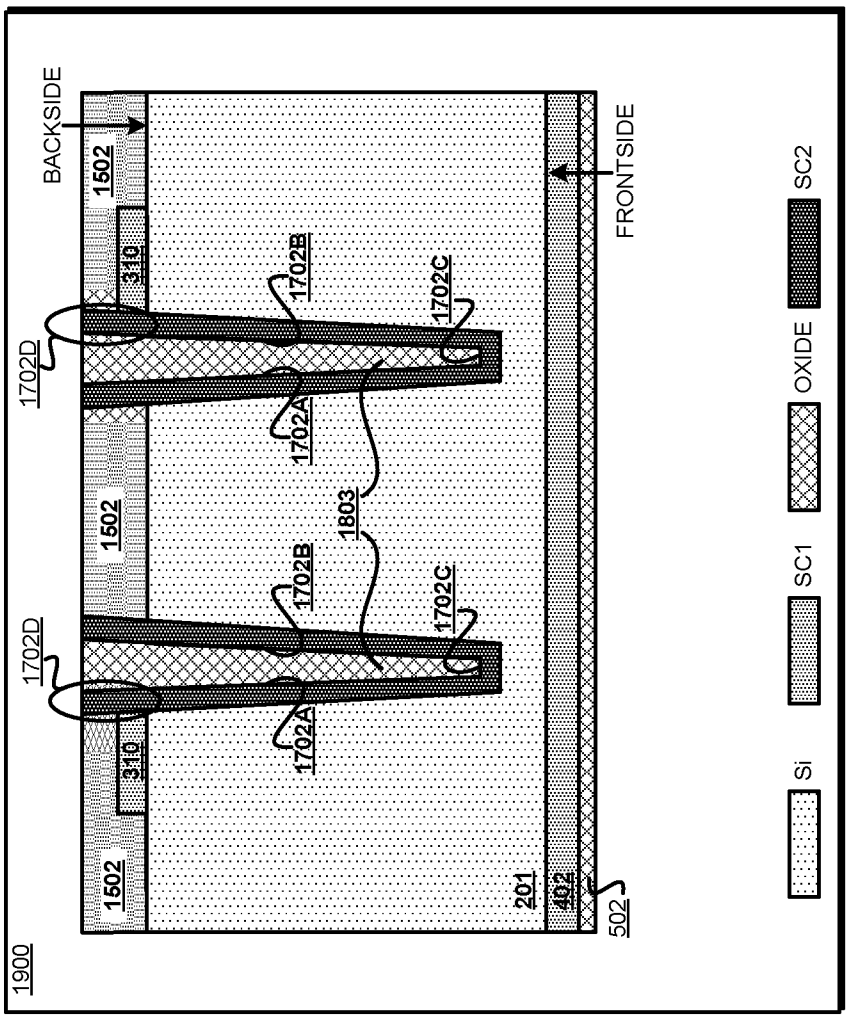
Si
SC1
OXIDE
SC2

FIGURE 18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1803
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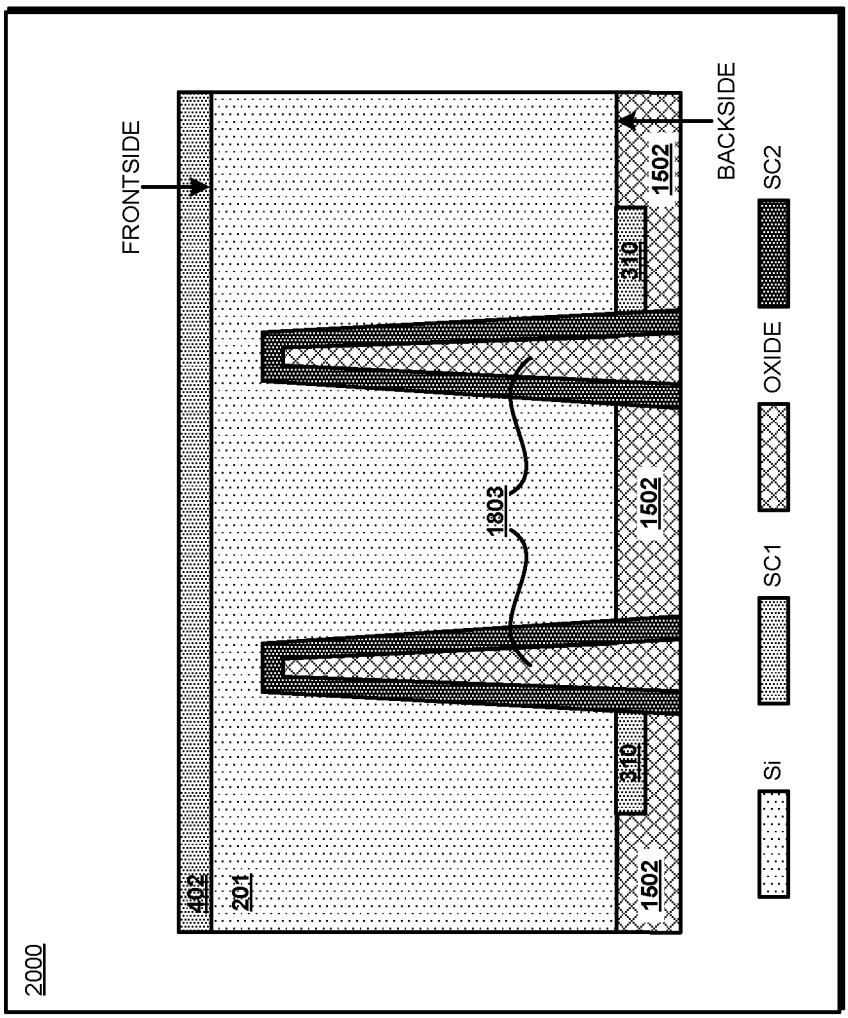
402
502
Si
SC1
OXIDE
SC2

FIGURE 19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201
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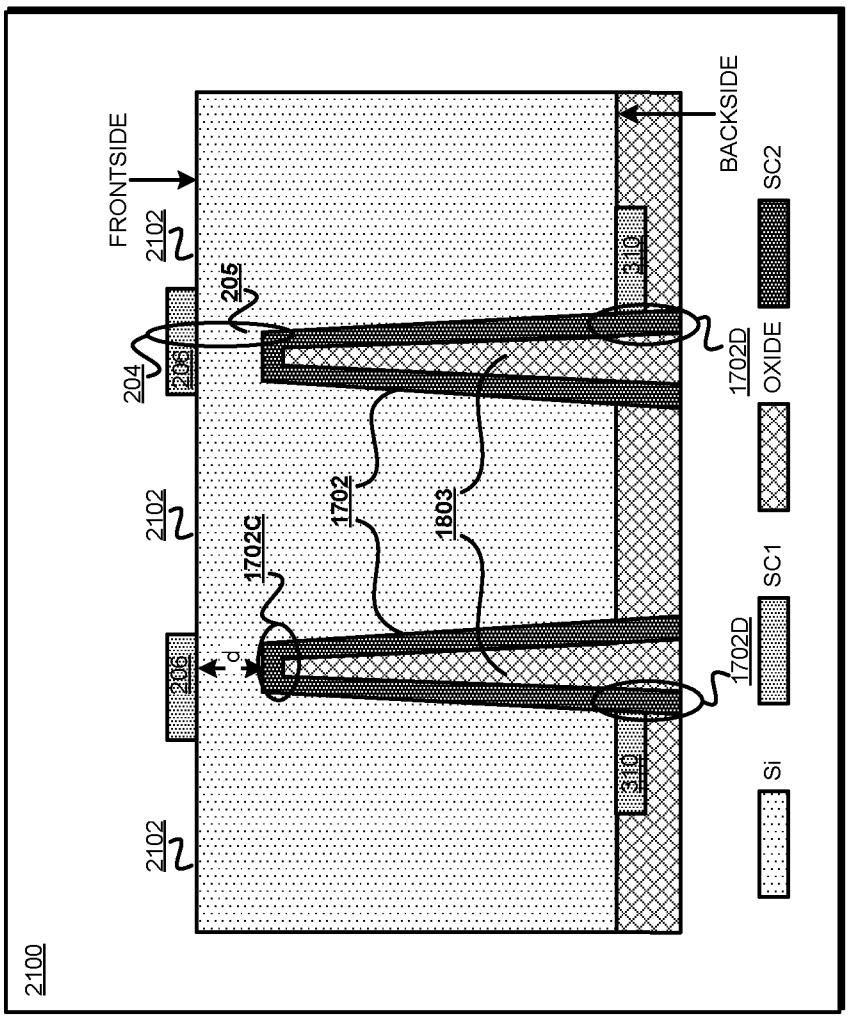
310
1803
FRONTSIDE
BACKSIDE
Si
SC1
OXIDE
SC2

FIGURE 20

FIGURE 21


2100
FRONTSIDE
BACKSIDE
2102
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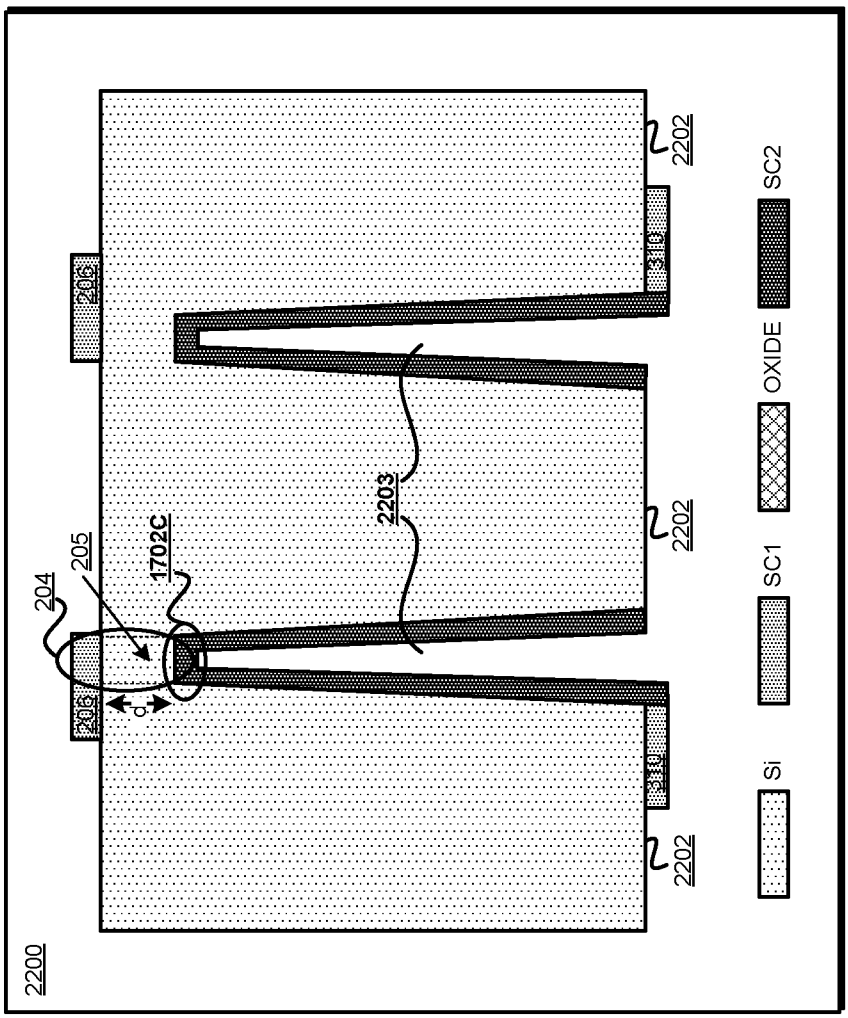
204
206
1702C
1702
1803
d
1702D
310
SC2
OXIDE
SC1
Si

FIGURE 22


2200
2202
2202
2202
2203
206
206
205
204
1702C
d
Si
SC1
OXIDE
SC2

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2018/078707

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06N10/00 H01L27/18 H01L39/02 H01L39/22 H01L39/24
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06N H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2016/148112 A1 (KWON HYEOKSHIN [KR]) 26 May 2016 (2016-05-26) paragraph [0067] - paragraph [0068]; figure 10	1-25

A,P	WO 2018/125026 A1 (INTEL CORP [US]) 5 July 2018 (2018-07-05) paragraph [0074] - paragraph [0086]; figure 4	1-25

A,P	WO 2017/217961 A1 (INTEL CORP [US]) 21 December 2017 (2017-12-21) paragraph [0110] - paragraph [0011]; figures 5F, 5G	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
9 January 2019	18/01/2019

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Angermeier, Detlef

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2018/078707

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2016148112 A1	26-05-2016	KR 20160062569 A	02-06-2016
		US 2016148112 A1	26-05-2016
WO 2018125026 A1	05-07-2018	NONE	
WO 2017217961 A1	21-12-2017	NONE	