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[72] Inventor **Klaus Jörg Hecker**
6242 Schonberg/Uber, Kronberg, Germany

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[54] **METHOD AND SYSTEM FOR CONTROLLING PRINTOUT ELEMENTS IN A PRINTOUT MECHANISM**
8 Claims, 1 Drawing Fig.

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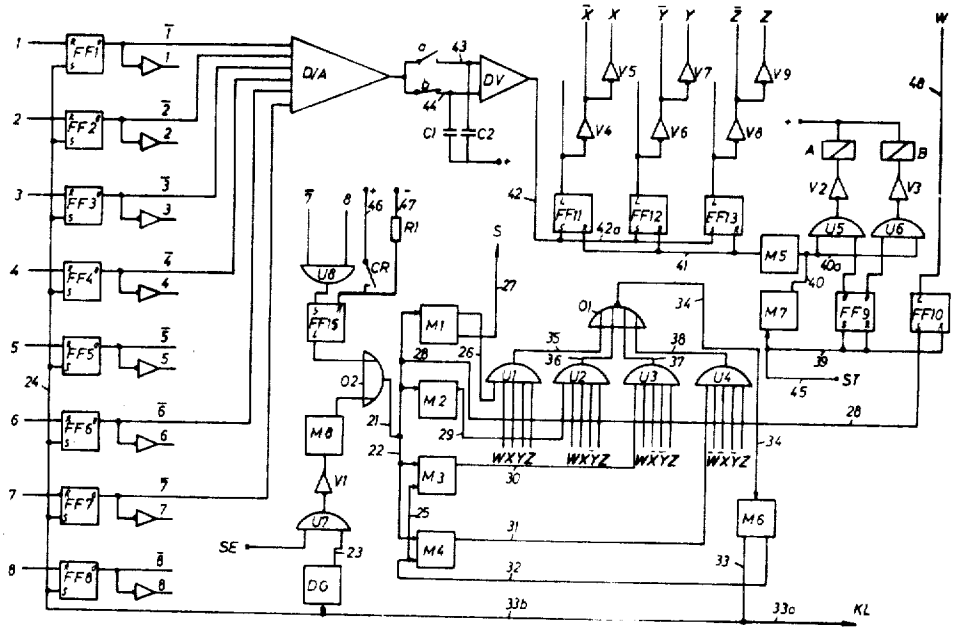
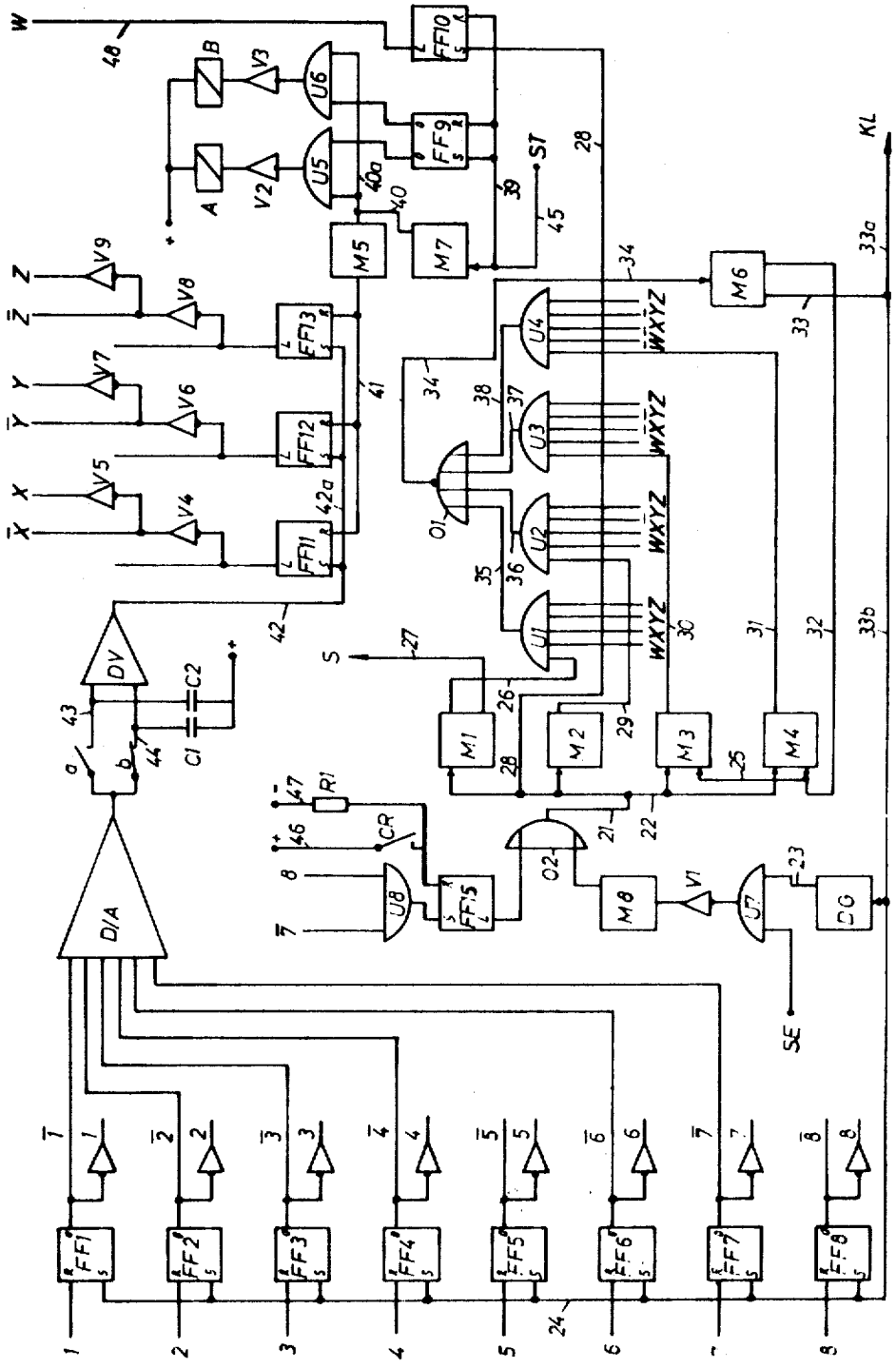
Primary Examiner—Gareth D. Shaw
Assistant Examiner—Jan E. Rhoads
Attorney—Michael S. Striker

ABSTRACT: The printout of a first and second printout element to be activated consecutively is controlled by storing a corresponding first and second location dependent selection signal and obtaining the difference therebetween. The second printout element is then activated after a time period following activation of the first printout element which depends upon this difference in selection signals.





INVENTOR
KLAUS JORG HECKER
By: Richard S. Sheridan
ATTORNEY

METHOD AND SYSTEM FOR CONTROLLING PRINTOUT ELEMENTS IN A PRINTOUT MECHANISM

BACKGROUND OF THE INVENTION

This invention relates to a method and system for controlling the activation of printout elements in data processing installations. In particular the printout elements in data processing arrangements wherein punched tapes are used are covered in this application. In such a machine, for example, data may be supplied by means of a tape which has holes punched therein, such holes representing, in combination, different letters or numbers. Signals scanned or readout from such a tape may then be used to control the operation of a type bar. In such a system each number or letter is associated with a particular one of said code or hole combination.

Because of the arrangement of the type bars in typewriters the time of activation of each of the type bars must be set so that no interference results between consecutively operated type bars. If the type bars lie in a circular arc, these type bars may be divided into different groups according to their position within the arc so that, for example, the time interval between activation of type bars of the same group may be made longer than that between type bars located in different groups. Thus the time interval between the activation of consecutive type bars must vary with the relative location of said type bars, thus, if, for example, the same type bar is to be activated twice in succession, the interval between successive activations must be long, since the type bar must return to its original position prior to the subsequent activation.

Some methods and arrangements are already known for controlling the type bar activation in such a manner that the operating speed of the typewriter or other printout mechanism is increased over that which would result if the maximum interval between successive operations were used throughout. In such known arrangements, which operate using time criteria, either individual-type bar activators or groups of such activators have more or less fixed time intervals assigned between activations.

SUMMARY OF THE INVENTION

It is an object of the invention to furnish a method and arrangement for activation of type bars which permits the use of a minimum time interval between activations in dependence on the relative location of two consecutively activated type bars.

For purposes of this invention, it is assumed that the scanning of the tape or other input means immediately yield, the code of the type bar to be activated, so that the location of the type bar to be activated is determined prior to the actual activation of said bar.

The invention set forth herein is thus a control system for printout mechanisms having printout elements arranged in predetermined locations, the minimum time interval required between activation of two consecutive printout elements depending at least in part on the relative location of said element. The invention comprises a plurality of selection signal generating means which generate a different selection signal depending on the respective location of said printout elements. The selection signals for a first and second printout element to be operated consecutively are stored and compared. A difference signal is generated which depends upon the difference between said selection signals. Further, timing means are provided for furnishing a plurality of timing signals at predetermined time intervals after activation of the first of said two consecutive printout elements. One of said timing signals is then selected in dependence upon said difference signal. The activating means for activating the second printout element are then energized upon receipt of the selected timing signal.

In a particular embodiment of the invention the selection signals may be two voltages which were respectively derived from a digital to analog converter whose inputs were the first and second code combination signals corresponding to the first and second elements to be activated.

The comparator means may be a differential amplifier, while the above-mentioned proportional voltages may be stored on capacitors. The difference signal derived from the differential amplifier may be evaluated by means of a plurality of threshold circuits, each set for a different predetermined value. The timing means may comprise a plurality of monostable multivibrators, each set for a different timing interval, all started upon activation of the first type bar. The selection of the particular timing interval may then take place by means of a plurality of AND gates, each combining one combination condition of the threshold circuit outputs with a corresponding one of the timing signals generated when a particular monostable vibrator changes back to its stable condition.

The novel features which are considered as characteristic for the invention are set forth in particular in the appended claims. The invention itself, however, both as to its construction and its method of operation, together with additional objects and advantages thereof, will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWING

The FIGURE is an overall diagram of the control circuit in accordance with this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The preferred embodiment of this invention will now be discussed in relation to the FIGURE.

It is assumed that the input signals, which signify the type bar to be activated (or character to be printed) are furnished at inputs **1** through **8**, which are respectively connected to the reset inputs of flip-flops FF1 through FF8. The set inputs S of these flip-flops are connected in common to line **24** which is connected to one output of the monostable multivibrator **M6** via lines **33***b* and **33**. The 0 output lines $\overline{1}$, $\overline{2}$, $\overline{3}$, $\overline{4}$, $\overline{6}$ and $\overline{7}$ corresponding to the reset inputs R, are connected in common to the input of a digital analog converter D/A. The outputs of the flip-flops FF1–FF8 which correspond to a set input S, are furnished from the corresponding 0 output lines via an amplifier and inverter.

The digital to analog converter D/A does not necessarily have to perform a correct mathematical conversion. It may be tailored to the particular requirements of the circuit in which such mathematical proportionality is not essential. All the 0 outputs of flip-flops FF1–FF7 are connected to the inputs of this analog to digital converter. The output of the digital to analog converter is connected to the control circuitry, and, in particular to contact pairs *a* and *b* which are relay contacts controlled by relays A and B respectively. Contact *a* is connected, when closed, to line **43**, while contact *b* is connected to line **44** when closed. Lines **43** and **44** are in turn connected to the first and second input of the differential amplifier, denoted by DV in the FIGURE. Lines **43** and **44** are further respectively connected to capacitors C2 and C1 the other terminal of which are connected in common to the positive voltage supply source.

The output of the differential amplifier DV is connected in common to the set inputs S of flip-flops FF1, FF12, and FF13 via line **42***a*. The reset inputs of these flip-flops are connected in common, via line **41** to the output of a multivibrator M5. As per the Figure, the L outputs of flip-flops FF11–FF13 respectively are each connected respectively to the input of an inverter amplifier V4, V6, and V8, which in turn are connected to inverter amplifiers V5, V7, and V9. Obviously the output of inverter amplifiers V4, V6, and V8 constitute the $\overline{X}$, $\overline{Y}$, $\overline{Z}$, outputs of flip-flops FF11, FF12 and FF13 respectively while the outputs V5, V7 and V9 respectively represent the L outputs of FF11–FF13.

Multivibrator M5 is controlled via line **40** from the output of multivibrator M7. Line **40** is also connected to one of the inputs each of AND gates U5 and U6. The second inputs of AND gates U5 and U6 respectively are connected to the 0 outputs of flip-flop FF9. One 0 output is connected with AND

gate U5, while the other is connected to AND gate U6. Flip-flop FF9 is constituted to yield an output at the two 0 outputs alternately, upon receipt of pulses on line 39. One of the 0 outputs controls relay A via amplifier V2 which is preceded by an inverter, while the 0 output of AND gate U6 controls relay B via amplifier V3 and its corresponding inverter, as will be further explained below.

The inputs of monostable multivibrator M7, flip-flop FF9 and one input of flip-flop FF10 are connected in common to line 39. Line 39 is connected to line 45, which receives a signal from the output of the readout arrangement (not shown) over terminal ST, when a code combination of the tape is under the scanning element. This corresponds to the so-called "stop" operation. The output of flip-flop FF10 yields a trigger pulse for AND gates U_1 through U_4 which will be described below. The second input of flip-flop FF10 is connected to line 22 via line 28. Line 22 is connected to the inputs of multivibrator M1–M4. Line 22 is further connected to the output of OR gate O2 via line 21.

OR gate O2 has a first input connected to the output of flip-flop FF15 and a second input connected to the output side of multivibrator M8. Flip-flop FF15 has a set input connected to the input of AND gate U8 which in turn has an input connected to the output of flip-flop FF7 and a second input connected to the output of flip-flop FF8. The other input, namely the reset input of flip-flop FF15 is connected to a carriage return control circuit comprising a line 46 connected to the positive voltage supply and a line 47 connected to the negative voltage supply terminal. Line 46 is connected to a switch whose second contact is connected to the reset input of flip-flop FF15. Line 47 is connected to a relay designated R1 which, on its other side, is also connected to the reset input of flip-flop FF15. The switch in line 46 is labeled CR and is the carriage return switch.

Multivibrator M8 is fed via a two-stage amplifier V1. This amplifier V1 is preceded by an AND gate U7 which has a first input connected to a differentiator DG and a second input connected to receive a signal at the start of operation. The input to the differentiator DG is connected to line 33*b*.

One output of multivibrator M1 is connected to an input of AND gate U1 via line 26. The other output is connected via line 27 to the control system for the readout means and serves to activate said readout means. Line 29 connects the output of the multivibrator M2 with one input of AND gate U2. A similar connection is made via lines 30 and 31 between the outputs of multivibrators M3 and M4, and the inputs of AND gates U3 and U4. The output lines 35, 36, 37 and 38 of AND gates U1, U2, U3 and U4 respectively are connected to the input of OR gate O1 which is followed by an inverter. The output of OR gate O1 is connected to multivibrator M6 via line 34. One output of multivibrator M6 is connected via lines 33 and 33*a* to the type bar activators or the corresponding positions in the decoding matrix, and via lines 33 and 33*b* to the set input S of flip-flops FF1–FF8 connected in common to line 24. The other output of this multivibrator is connected via line 23 with the input of multivibrator 24 and further, via line 25, with one input of multivibrator M3.

The above described circuit operates as follows:

At the beginning of the operation, a start signal is applied at terminal SE, thus fulfilling the necessary conditions to yield an output at AND gate U7, since the voltage at the other input is absent. The output of AND gate U7 in turn causes multivibrator M8, having a time constant of 1 millisecond to be flipped to its unstable state. The output of the multivibrator furnishes the signal to OR gate O2, which in turn furnishes a signal via lines 21 and 22 to multivibrators M1–M4, and via line 28 to set input S of flip-flop FF10. The outputs of multivibrators M1–M4 are of course connected to the first inputs of AND gates U1–U4 via lines 29, 30 and 31. Further the output of multivibrator M1 starts the readout via line 27. It should be noted that multivibrators M1–M4 constitute timing means for furnishing a plurality of timing signals at predetermined time intervals after activation of the previously activated printout element. These multivibrators thus have different time constants as follows:

M1=20.5 ms.
M2=30.5 ms.
M3=41.5 ms.
M4=58.5 ms.
M5=3.0 ms.
M6=25.0 ms.
M7=3.0 ms.
M8=1.0 ms.

The timing signals of course are derived from multivibrators M1–M4. The values of the other multivibrators are furnished here only for later reference.

When the desired code is under the reader, a signal is furnished to terminal ST indicating the so-called "stop" operation. This causes multivibrator M7 to be switched to its unstable state. Simultaneously the applied pulse causes a triggering of flip-flop FF9 and the resetting of flip-flop FF10. This causes either AND gate U5 or AND gate U6 to generate the pulse required for activation of either relay A or relay B respectively. This occurs because the output of multivibrator M7 furnishes the necessary input for the AND gates U5 or U6 which in turn activate relays A and B respectively. Further, the output of multivibrator M5 is applied to the reset inputs R of flip-flops FF11–FF13 via common line 41, thus causing these flip-flops to be reset. If now for example relay A has been activated, contact *a* will be closed. A signal derived from the tape is applied via flip-flops FF1–FF7 to the inputs of the digital to analog converter D/A. The voltage furnished by digital-analog converter D/A in response to this input code signal is then applied to capacitor C2 via this now closed contact *a*. The voltage resulting on capacitor C2 is the selection signal corresponding to the first printout element to be activated. The charging of capacitor C2 continues until the following pulse is received at terminal ST which causes the flip-flop FF9 to flip to its second output causing activation of relay B and deactivation of relay A. Upon deactivation of relay A the voltage stored on capacitor C2 is applied to the differential amplifier DV. The output of differential amplifier DV is applied to the set inputs of flip-flops FF11, FF12, and FF13. Each of these flip-flops is adjusted to set for different threshold values, or different minimum voltages applied to their respective set inputs. It will be noted that different combinations of L or O conditions at the outputs of flip-flops 11–13 are applied to the inputs of AND gates U1, U2, U3, and U4. These different combination conditions furnish inputs of each of the AND gates U1, U2, U3 and U4. The input labeled W on each of the above-mentioned AND gates is furnished by the output L of flip-flop FF10 via line 48 which signals appear in synchronism to the inputs applied via the outputs of flip-flops FF8 to OR gate U8. The fifth input to each of the AND gates U1–U4 is applied, respectively from the output of multivibrators M1–M4. These AND gates thus serve as means for selecting a timing signal as a function of the difference signal which is the output of the differential amplifier DV. The particular selected one of AND gates U1–U4 then furnishes a signal to OR gate O1 which is followed by an inverter and in turn controls multivibrator M6 which has a time constant which is approximately 25 percent greater than that of multivibrator M1. The output signal of M6 then causes the energization of the corresponding position in the decoding matrix for activating the type bars. This pulse controlling the activation of the type bars is applied to the decoding matrix via lines 33 and 33*a*. The timing of the activation of the type bar has thus been made dependent upon the differential amplifier output signal, which in turn depends upon the difference between the selection signals for two type bars to be activated in succession. At the same time at which the signal which causes the activation of the type bars is generated, the differentiator DG is energized via line 33*b* and flip-flops FF1–FF8 are reset via line 24. A further output of multivibrator M6 causes the resetting of multivibrators M3 and M4 which have the largest time constants, in case these have not already reset.

The output of differentiator DG causes the setting of multivibrator M8 via the two stage amplifier V1. The output of multivibrator M8 in turn causes multivibrators M1–M4 to be switched to the unstable state via AND gate O2. The next signal received at terminal ST then again causes a flipping of flip-flop FF9, causing relay B to be deactivated and its contact *b* to be opened. The voltage on condenser C1 is the voltage proportional to the code read from the tape.

It may be seen from the above-described operating cycle that the four monostable multivibrators M1–M4 in connection with the threshold circuits represented by flip-flops FF11–FF13 determine the timing of the activation of the type bar corresponding to the code read out from the tape.

In order to avoid errors during long tape movements or during a corrective punching, the flip-flop FF9 prevents any operation until the signal arrives at terminal ST which indicates that a usable code is being scanned.

During a carriage return the signal for starting the readout means are blocked via contact CR until this contact is again opened. Flip-flop FF15 is flipped for each output of AND gate U8.

While the invention has been illustrated and described as embodied in particular types of logic circuits, it is not intended to be limited thereto since structural and circuit changes may be made without departing in any way from the spirit of the present invention.

What is claimed as new and desired to be protected by Letters Patent is set forth in the appended claims:

1. In a printout mechanism having a plurality of printout elements arranged in predetermined locations, a control system for activating a selected printout element a determined time interval following activation of the last previously selected printout element in dependence on the relative locations of said selected printout element and said last previously selected printout element, comprising, in combination for: storage means storing a first selection signal having an amplitude corresponding to the location of said last previously selected printout element and for storing furnishing a second selection signal having an amplitude corresponding to the location of said selected printout element; said selection signal furnishing means comprising means for generating a code combination signal corresponding to the location of said selected printout element, and digital-to-analog converter means for converting said code combination signal to a corresponding analog signal; comparator means for furnishing a difference signal thus furnishing said selection selection signal, having an amplitude corresponding to the difference in amplitude between said first and second selection signals; timing means for furnishing a plurality of timing signals at predetermined time intervals after said activation of said last previously selected printout element; means for selecting one of said timing signals as a function of the amplitude of said difference signal, thus furnishing a selected timing signal; and activating means for activating said selected printout element in response to said selected timing signal.

2. A system as set forth in claim 1, wherein said storage means comprises first and second capacitive storage means for storing said first and second selection signals second selection signal; further comprising connecting means for alternately connecting said first and second capacitive storage means to the output of said digital-to-analog converter means in such a manner that the voltage on said first and second capacitive storage means respectively constitutes said first and second selection signals.

3. Control system as set forth in claim 2 wherein said comparator means comprise differential amplifier means having a first input connected to said first capacitive storage means and a second input connected to said second capacitive storage means.

4. A system as set forth in claim 3, wherein said means for selecting one of said timing signals comprises a plurality of threshold circuits, each connected to said differential amplifier means, each for generating a corresponding threshold signal when the amplitude of said difference signal exceeds the corresponding associated threshold value; wherein said timing means comprise a plurality of timing circuit means; and wherein said means for selecting one of said timing signals further comprises a plurality of gating means, each connected to a corresponding one of said timing circuits, each adapted to allow transmission of the corresponding timing signal in response to a predetermined combination of said threshold signals.

5. A control system as set forth in claim 4 wherein said gating means comprise AND gates.

6. A control system as set forth in claim 5 wherein each of said timing circuit means comprises a monostable multivibrator.

7. A system as set forth in claim 6, wherein said connecting means for alternately connecting said first and second capacitive storage means to said digital to analog converter means comprises first and second relay means respectively having a first and second pair of relay contacts, said first and second pair of relay contacts, when closed, respectively furnishing the connection between said digital-to-analog converter means and said first and second capacitive storage means; means for furnishing signals signifying the generation of a selection signal; and relay activating means for alternately activating said first and second relays in response to said signals.

8. In a printout mechanism having a plurality of printout elements arranged in predetermined locations, a method for controlling the time interval between activation of a first and second printout element, in dependence on the relative location of said first and second printout elements, comprising, in combination, furnishing a first digital signal corresponding to the location of said first printout element; converting said first digital signal to a first analog signal having an amplitude corresponding to the location of said first printout element; storing said first analog signal; activating said first printout element; furnishing a second digital signal corresponding to the location of said second printout element; converting said second digital signal to a second analog signal having an amplitude corresponding thereto; storing said second analog signal; comparing said first and second analog signals and furnishing a difference signal having an amplitude corresponding to the difference in amplitude between said first and second analog signals; furnishing a plurality of timing signals following activation of said first printout element; selecting one of said timing signals as a function of the amplitude of said difference signal; and activating said second printout element in response to said selected timing signal.

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