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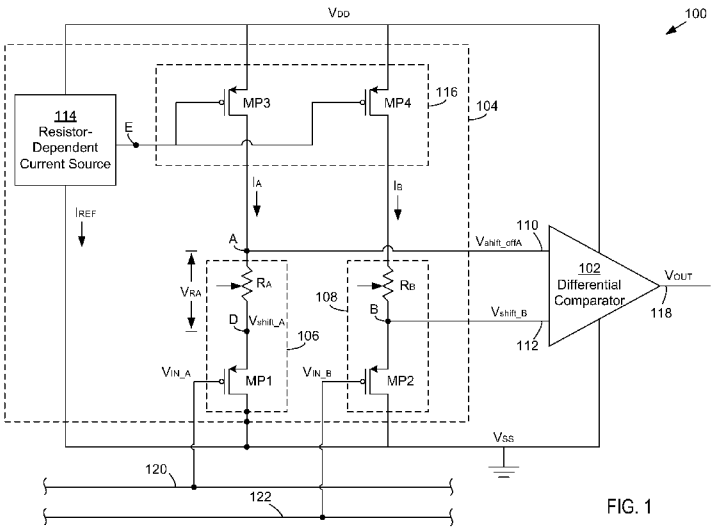

FIG. 1

(57) Abstract: A comparator system (100) may include a comparator circuit (102) and input circuitry (104) coupled to a communication line (120, 122). The circuitry may include resistors (RA, RB) that are used to generate input voltages supplied to input terminals of the comparator. Resistor- dependent currents (Iref, IA, IB) generated from a resistor-dependent current source (114) may be supplied to the resistors of the input circuitry. The resistors of the input circuitry and resistors of the resistor-dependent current source may be of the same type and/ or configured on the same chip to increase stability in the presence of various process-voltage-temperature (PVT) conditions. The comparator system may be implemented as a squelch detector or other signal detection system, such that an output generated by the comparator (Vout) based on the input voltages may indicate presence or absence of a signal.

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Differential Comparator with Stable Offset

Background

[0001] Squelch detectors may be used with communication links to provide an indication of whether a signal is present on a link or communication line. Some squelch detectors may provide the indication based on a voltage difference between two signals. However, if the voltage difference that is generated is not stable due to instability-causing factors such as temperature changes or noise, the indication provided by squelch detector may be false. As such, it may be desirable to generate a voltage difference that is stable in the presence of instability-causing factors so that the output provided by the squelch detector is accurate.

Brief Description of the Drawings

[0002] Figure 1 is a circuit schematic diagram of an example differential comparator system.

[0003] Figure 2 is a circuit schematic diagram of another example differential comparator system.

[0004] Figure 3 is a circuit schematic diagram of an example resistor-dependent current source.

[0005] Figure 4 is a circuit schematic diagram of another example resistor-dependent current source.

[0006] Figure 5 is a flow chart of an example method of detecting a signal communicated on a communication line.

Detailed Description of the Presently Preferred Embodiments

[0007] **Overview**

[0008] By way of introduction, the below embodiments relate to electronic systems and related methods for providing an accurate, stable, and configurable offset across a wide range of fabrication process, voltage, and temperature conditions. In one embodiment, a comparator system may include a comparator circuit, an input circuit, and a resistor-dependent current generation circuit. The comparator circuit may be

configured to receive a first input voltage and a second input voltage, and output an output voltage based on a difference between the first input voltage and the second input voltage. The input circuit may include first resistor circuitry and be circuit configured to: generate the first input voltage based on the first resistor circuitry, and supply the first input voltage to the comparator circuit. The resistor-dependent current generation circuit may include second resistor circuitry and be configured to generate a resistor-dependent current that depends on the second resistor circuitry, and supply the resistor-dependent current to the first resistor circuitry to generate the first input voltage. The first resistor circuitry and the second resistor circuitry may be of the same type.

[0009] In another embodiment, a signal detection system may include a signal detection circuit coupled to a pair of communication lines. The signal detection circuit may include first resistor circuitry, a comparator circuit, and a resistor-dependent generation circuit. The first resistor circuitry may be configured to generate an offset voltage. A comparator circuit may be coupled to the first resistor circuitry and be configured to generate an output voltage at a level that indicates whether a first line voltage on the pair of communication lines exceeds a second line voltage on the pair of communication lines by an amount corresponding to the offset voltage. The resistor-dependent current generation circuit may include second resistor circuitry and be configured to generate a resistor-dependent current that depends on the second resistor circuitry, and supply the resistor-dependent current to the first resistor circuitry to generate the offset voltage. The first resistor circuitry and the second resistor circuitry may be of the same type.

[0010] In yet another embodiment, a method of detecting presence of a signal on a pair of communication lines may be performed. The method may include generating, with resistor-dependent current generation circuitry, a resistor-dependent current that depends on first resistor circuitry; and generating, with second resistor circuitry, an offset voltage in response to the resistor-dependent current. In addition, the method may include generating, with a first input circuit coupled to the pair of communication lines, a first input voltage at a first input terminal of a comparator circuit, where the first input voltage is based on the offset voltage and a first line voltage generated on the pair of communication lines; and generating, with a second input circuit coupled to the pair of

communication lines, a second input voltage at a second input terminal of the comparator circuit, where the second input voltage based on a second line voltage generated on the pair of communication lines. The method may also include outputting, with the comparator circuit, an output voltage based on a difference between the first input voltage and the second input voltage, where a level of the output voltage indicates presence or absence of a signal being communicated on the pair of communication lines.

[0011] In some embodiments, the input circuit and the resistor-dependent current generation circuit may be configured on the same chip.

[0012] In some embodiments, the resistor-dependent current generation circuitry may include a current source circuit and a current mirror circuit. The current source circuit may include the second resistor circuitry and be configured to generate a reference current that depends on the second resistor circuitry. The current mirror circuit may be configured to mirror the reference current to generate the resistor-dependent current, and supply the resistor-dependent current to the first resistor circuitry.

[0013] In some embodiments, a switch may be connected in parallel with the first resistor circuitry, and a feedback connection may couple an output terminal of the comparator circuit with the switch, where a level of the output voltage controls switching of the switch.

[0014] In some embodiments, the first resistor circuitry and the second resistor circuity may have respective temperature coefficient parameters that are within 5% of each other.

[0015] In some embodiments, the first resistor circuitry and the second resistor circuitry may be both polysilicon resistors, P-POLY resistors saliside, P-POLY resistors non-saliside, N-POLY resistors saliside, N-POLY resistors non-saliside, Nwell resistors, or metal resistors.

[0016] Other embodiments may be possible, and each of the embodiments can be used alone or together in combination. Accordingly, various embodiments will now be described with reference to the attached drawings.

[0017] **Exemplary Embodiments**

[0018] The following embodiments can be used to provide an accurate, stable, and configurable offset across a wide range of fabrication process, voltage, and temperature (PVT) conditions. Fig. 1 is a circuit schematic diagram of an example differential

comparator system 100. The differential comparator system 100 may include a differential comparator circuit 102 and comparator input circuitry 104 configured to generate and supply a pair of comparator input voltages, including a first comparator input voltage V_{shift_offA} and a second comparator input voltage V_{shift_B}, to the differential comparator circuit 102. The differential comparator circuit 102 may be configured to generate and output an output voltage V_{OUT} at an output terminal 118 based on a difference of the first comparator input voltage V_{shift_offA} and the second comparator input voltage V_{shift_B}. In particular, the differential comparator circuit 102 may generate the output voltage V_{OUT} at a level that indicates which of the first comparator input voltage V_{shift_offA} and the second comparator input voltage V_{shift_B} is higher than the other. That is, the differential comparator circuit 102 may generate the output voltage V_{OUT} at a first level if the first comparator input voltage V_{shift_offA} is higher than the second comparator input voltage V_{shift_B}, and may generate the output voltage V_{OUT} at a second level if the second comparator input voltage V_{shift_B} is higher than the first comparator input voltage V_{shift_offA}.

[0019] The comparator input circuitry 104 may be configured to receive a pair of input voltages, including a first input voltage V_{IN_A} and a second input voltage V_{IN_B}, and generate the pair of comparator input voltages V_{shift_offA}, V_{shift_B} based on the pair of input voltages V_{IN_A}, V_{IN_B}. The comparator input circuitry 104 may include a first input circuit 106 and a second input circuit 108. The first input circuit 106 may include first resistor circuitry R_A connected in series with a first transistor MP1. The first resistor circuitry R_A may include a potentiometer, although other circuits or circuit configurations that provide a resistance, including a programmable and/or a reconfigurable resistance, may be possible. Additionally, as shown in Fig. 1, the first transistor MP1 may be a p-channel metal-oxide-semiconductor field-effect transistor (PMOS transistor), although other types of transistor or switching circuitry may be possible. The PMOS transistor MP1 may have a gate terminal configured to receive the first input voltage V_{IN_A}. Additionally, the first PMOS transistor MP1 may have a source terminal connected to a first end of the first resistor circuitry R_A at a node D, and a drain terminal connected to a ground reference voltage V_{SS}. A second end of the first resistor circuitry R_A may be connected to a first input terminal 110 of the differential comparator circuit 102 at a node

A at which the first comparator input voltage V_{shift_offA} may be generated. Accordingly, the first comparator input voltage V_{shift_offA} generated at node A with respect to ground may be the sum of a first resistor voltage generated across the first resistor circuitry R_A and a source-to-drain voltage generated across the source and drain terminals of the first PMOS transistor MP1. The source-to-drain voltage, and in turn the first comparator input voltage V_{shift_offA}, may depend on the level of the first input voltage V_{IN_A} applied to the gate terminal of the first PMOS transistor MP1.

[0020] The second input circuitry 108 may include second resistor circuitry R_B connected in series with a second transistor MP2. Like the first input circuitry 106, the second resistor circuitry R_B may include a potentiometer and the second transistor MP2 may be a PMOS transistor, although other types of resistance-providing circuitry and/or switching circuitry may be possible. The second PMOS transistor MP2 may have a gate terminal configured to receive the second input voltage V_{IN_B}. Additionally, the second PMOS transistor MP2 may have a source terminal connected to a first end of the second resistor circuitry R_B at a node B, and a drain terminal connected to the ground reference voltage V_{SS}. The second comparator input voltage V_{shift_B} may be generated at node B, which may be connected to a second input terminal 112 of the differential comparator circuit 102. The second comparator input voltage V_{shift_B} generated at node B with respect to ground may be a source-to-drain voltage generated across the source and drain terminals of the second PMOS transistor MP2, which may depend on the level of the second input voltage V_{IN_B} applied to the gate terminal of the second PMOS transistor MP2.

[0021] The comparator input circuitry 104 my further include current generation circuitry configured to generate and provide currents to each of the first input circuitry 106 and the second input circuitry 108. The current generation circuitry may include a resistor-dependent current source 114 that is configured to generate a reference current I_{REF}, which may be a direct current (DC) current source that is dependent upon a resistance of the resistance-dependent current source 114. The resistance may be a single resistance provided by a single resistor or a plurality of resistances provided by a plurality of resistors. An amount of the reference current I_{REF} generated by the resistor-dependent current source 114 may depend on and/or be determined by the resistance of the resistor-

dependent current source 114. Accordingly, changes in the resistance of the resistor-dependent current source 114 may cause a change in the amount of the reference current I_{REF} that is generated. For some example configurations, there may be an inverse relationship between the resistance of the resistor-dependent current source 114 and the amount of the reference current I_{REF} that is generated. For example, an increase in the resistance may cause a decrease in the amount of the reference current I_{REF}, and vice versa.

[0022] As described in further detail below, the resistors of the resistor-dependent current source 114 may be of the same type or kind as each other as well the same type or kind as the resistors of the first resistor circuitry R_A and the second resistor circuitry R_B. Resistors of the same type or kind may be made of the same material, have the same size, or combinations thereof. As non-limiting examples, the resistors of the resistor-dependent current source 114 and the first and second resistor circuitries R_A, R_B may each be polysilicon resistors, P-POLY resistors saliside, P-POLY resistors non-saliside, N-POLY resistors saliside, N-POLY resistors non-saliside, Nwell resistors, or metal resistors.

[0023] In addition or alternatively, the resistors of the resistor-dependent current source 114 and the first and second resistor circuitries R_A, R_B may be of the same type in that they respond to and/or are affected by one or more process-voltage-temperature (PVT) conditions in the same or similar ways. That is, their respective resistances may respond or vary in the same way or proportional to each other when subjected to the same PVT conditions and/or changes in PCT conditions. One example PVT condition may include temperature (e.g., environmental or surrounding temperature. By being of the same type, the respective resistances of the resistors of the resistor-dependent current source 114 and the first and second resistor circuitries R_A, R_B may have the same or similar temperature coefficient parameters (e.g., within 5% of each other) that indicate how a resistor may response to temperature variation. As a result, the respective resistances of the resistors of the resistor-dependent current source 114 and the first and second resistor circuitries R_A, R_B may change or otherwise respond in the same way or proportional to each other when subjected to a change in temperature of the surrounding environment. Another PVT condition may include process variations.

[0024] In addition, for some example configurations, at least the resistor-dependent current source 114 and the first and second resistor circuitries R_A, R_B may be configured on the same or a single chip or integrated circuit (IC). In particular example configurations, the circuit components of the comparator input circuitry 104; the components of the comparator circuitry 104 and the differential comparator circuit 102; and/or the differential comparator system 100 as a whole may be configured on the same chip or IC. In addition to temperature, another example PVT condition may be process variation. Due to imperfections in fabrication processes, an actual resistance of a resistor may be different that its target or designed-for resistance. Such differences may be referred to as resistance drift or mismatch. However, resistance drift may be much lower among resistors located on the same chip or IC (e.g., less than 1%), compared to resistance drift among resistors located on different chips or ICs (e.g., 5-6%). As such, by being located on the same chip or IC, the resistors of the resistor-dependent current source 114 and the first and second resistor circuitries R_A, R_B may have the same or very similar (e.g., less than 1%) resistance drifts.

[0025] The current generation circuitry may further include current mirror circuitry 116 that is configured to mirror the reference current I_{REF} generated by the resistor-dependent current source 114 to generate a first mirrored current I_A and a second mirrored current I_B. As shown in Fig. 1, the current mirror circuitry 116 may include a third PMOS transistor MP3 that generates the first mirrored current I_A and supplies the first mirrored current I_A to the first input circuitry 106, and a fourth PMOS transistor MP4 that generates the second mirrored current I_B and supplies the second mirrored current I_B to the second input circuitry 108. The third PMOS transistor MP3 may have a source terminal coupled to a supply voltage V_{DD} and a drain terminal coupled to the second end of the first resistor circuitry R_A at node A at which the first comparator input voltage V_{shift_offA} is generated. In addition, the fourth PMOS transistor MP4 may have a source terminal coupled to the supply voltage V_{DD} and a drain terminal coupled to a second end of the second resistor circuitry R_B. Also, in order to mirror the reference current I_{REF}, gate terminals of the third and fourth PMOS transistor MP3, MP4 may each be connected at a node E to a gate terminal of a transistor of the resistor-dependent current source 114 generating the reference current I_{REF}, as described in further detail

below. By being mirrored versions of the reference current I_{REF}, each of the first mirrored current I_A and the second mirrored current I_B may have amounts that are the same as and/or proportional to the amount of the reference current I_{REF}, depending on the respective sizes of the third and fourth PMOS transistors MP3, MP4 in relation to the size of the transistor of the resistor-dependent current source 114 generating the reference current I_{REF}.

[0026] For some example configurations, the third and fourth PMOS transistors MP3 and MP4 may have the same or substantially the same sizes as each other so that the amounts of first and second mirrored currents I_A and I_B are the same or substantially the same as each other. Additionally, the resistances of the resistor circuities R_A and R_B may be the same or substantially the same. As a result, the voltages generated across the resistor circuitries R_A and R_B may be the same or substantially the same as each other.

[0027] Further, the level of the voltage V_{shift_A} generated at node D may be above or shifted up from the level of the first input voltage V_{IN_A}. Similarly, the level of the voltage V_{shift_B} generated at node B may be above or shifted up from the level of the first input voltage V_{IN_B}. In a particular example configuration, the first and second PMOS transistors MP1 and MP2 may be sized, and the amount of the first and second mirrored currents I_A and I_B may be generated such that the amounts that the voltages V_{shift_A} and V_{shift_B} are shifted up may be the threshold voltage V_T of the first and second PMOS transistors MP1 and MP2.

[0028] Additionally, for particular implementations, the first and second input voltages V_{IN_A} and V_{IN_B} may be low enough such that the first and second PMOS transistors MP1 and MP2 remain turned on for varying levels of the first and second input voltages V_{IN_A} and V_{IN_B}. Also, the levels of the voltages V_{shift_A} and V_{shift_B} may vary linearly in proportion to the varying levels of the first and second input voltages V_{IN_A} and V_{IN_B}. The first and second PMOS transistors may have the same or substantially the same size so that when the first and second input voltage V_{IN_A} and V_{IN_B} are at the same level, the voltages V_{shift_A} and V_{shift_B} may also be at the same level. As such, when the first and second input voltage V_{IN_A} and V_{IN_B} are at the same level, the difference between the first comparator input voltage V_{shift_offA} and the second comparator input voltage V_{shift_B} may be the voltage generated across the first resistors circuitry R_A, hereafter referred to as

the first resistor voltage V_{RA}. For some applications, the first resistor voltage V_{RA} may be an offset voltage indicative of an amount that the first comparator input voltage V_{shift_offA} is offset from the second comparator input voltage V_{shiftB}.

[0029] In operation, as long as the difference between the first input voltage V_{IN_A} and the second input voltage V_{IN_B} is less than the first resistor voltage V_{RA} (e.g., the offset voltage) the differential comparator circuit 102 may output the voltage V_{OUT} at a level that indicates that the first comparator input voltage V_{shift_offA} is greater than the second comparator input voltage V_{shift_B}. However, when the second input voltage V_{IN_B} increases above the first input voltage V_{IN_A} by an amount that is greater than or equal to the first resistor voltage V_{RA}, the level of the second comparator input voltage V_{shift_B} may be correspondingly greater than or equal to the level of the first comparator input voltage V_{shift_offA}. When this occurs, the level of the output voltage V_{OUT} may change to indicate that the level of the second comparator input voltage V_{shift_B} is greater than or equal to the level of the first comparator input voltage V_{shift_offA}. Subsequently, if the level of the second input voltage V_{IN_B} falls below the first resistor voltage V_{RA}, the first comparator input voltage V_{shift_offA} may again be correspondingly above the second comparator input voltage V_{shift_offA}, and the level of the output voltage V_{OUT} may switch back to indicate that relationship.

[0030] For some example configurations, the differential comparator system 100 may be implemented as a squelch detector or other signal detection circuit or system that detects a presence or absence of a signal being communicated on a link or communication line. The signal being communicated may be a data signal, a command signal, or other type of signal that may be differentiated from noise. Accordingly, for purposes of the present description, the term "signal" includes any signal carrying data or any other information other than or in addition to noise.

[0031] Fig. 1 shows the gate terminal of the first PMOS transistor MP1 coupled to a first communication line 120 such that the first input voltage V_{IN_A} is proportional to a line voltage being generated on the first communication line 120. Similarly, the gate terminal of the second PMOS transistor MP2 may be coupled to a second communication line 122 such that the second input voltage V_{IN_B} is proportional to a line voltage being generated on the second communication line 122. When implemented as a squelch

detector or other signal detection circuit, the differential comparator system 100 may be configured to detect presence or absence of a signal being communicated on one or both of the communication lines.

[0032] In some example implementations, the signal being communicated on the communication lines 120, 122 may be a differential signal. When no differential signal is being communicated, only noise may be present on the lines 120, 122, and any difference in the voltages generated on the lines 120, 122 from the noise may be small enough (i.e., less the first resistor voltage V_{RA}) such that the resulting first comparator input voltage V_{shift_offA} may be greater than the second comparator input voltage V_{shiftB}. As a result, the level of the output signal V_{OUT} generated by the differential comparator circuit 102 when the first comparator input voltage V_{shift_offA} is greater than the second comparator input voltage V_{shiftB} may indicate that no signal is being communicated on the differential communication lines 120, 122. Alternatively, when a differential signal is being communicated, there may be a time during the communication when a voltage of a signal of the differential pair being communicated on the second communication line 122 may be the same as or exceed a voltage of the other signal of the differential pair being communicated on the first communication line 120 by an amount corresponding to the first resistor voltage V_{RA}. When this occurs, the level of the second comparator input signal V_{shift_B} may be greater than or equal to the level of the first comparator input voltage V_{shift_offA}. As a result, the differential comparator circuit 102 may output the output voltage V_{OUT} at a level indicate the presence of a signal being communicated on the communication lines 120, 122. Subsequently, when communication of the differential signal stops such that there is only noise on the lines 120, 122, the level of the second comparator input voltage V_{shift_B} may again fall below the level of the first comparator input voltage V_{shift_offA}, and in turn, the differential comparator circuit 102 may again output the output voltage V_{OUT} at a level to indicate that no signal is being communicated on the lines 120, 122.

[0033] In other example implementations, the first communication line 120 may be configured to communicate a reference voltage, and the second communication line 122 may be configured to communicate a signal (either a single-ended signal or a signal of a differential pair). When no signal is being communicated on the second communication

line 122, any voltage level generated as a result of noise generated on the second line 122 relative to the reference voltage generated on the first line 120 may be less than the first resistor voltage V_{RA}. As a result, the first comparator input voltage V_{shift_offA} may be greater than the second comparator input voltage V_{shift_B}, and in turn the differential comparator circuit 102 may output the output voltage V_{OUT} at a level that indicates that no signal is being communicated on the second line 122. Alternatively, when a signal is communicated on the second communication line 122, the voltage level on the second line 122 relative to the reference voltage generated on the first line 120 may be greater than or equal to first resistor voltage V_{RA} such that the differential comparator circuit 102 outputs the output voltage V_{OUT} at a level that indicates a signal is being communicated on the second communication line 122.

[0034] For the example differential comparator system 100, if the level of the signal being communicated is relatively small such that the level of the second comparator input voltage V_{shift_B} exceeds the level of the first comparator input voltage V_{shift_offA} by only a small amount, then fluctuations in the signal level may cause the level of the second comparator input voltage V_{shift_B} to fall below the level of the first comparator input voltage V_{shift_offA} which in turn may cause the differential comparator circuit 102 may output the output voltage V_{OUT} at the level indicating that no signal is being communicated even though one still is. To avoid such incorrect indications, the differential comparator system 100 may be modified to include hysteretic functionality such that after the second comparator input voltage V_{shift_B} increases above the first comparator input voltage V_{shift_offA}, the level of the first comparator input voltage V_{shift_offA} drops to increase the amount that level of the second comparator input voltage V_{shift_B} has to drop in order to fall back below the level of the first comparator input voltage V_{shift_offA}.

[0035] Fig. 2 is a circuit schematic diagram of another example differential comparator system 200 that has the hysteretic functionality. The differential comparator system 200 is similar to the differential comparator system 100 except that the differential comparator system 200 further includes a p-channel metal-oxide-semiconductor field-effect transistor (PMOS transistor) MN1 connected in parallel with the first resistor

circuitry R_A, and a feedback connection 202 that connects the output terminal 118 of the differential comparator circuit with a gate terminal of the NMOS transistor.

[0036] The input terminals 110 and 112 of the differential comparator circuit 102 may be configured such that the first input terminal 110 configured to receive the first comparator input voltage V_{shift_offA} may be the negative input terminal and the second input terminal 112 configured to receive the second comparator input voltage V_{shift_B} may be the positive input terminal. As such, when the first comparator input voltage V_{shift_off} is higher than the second comparator input voltage V_{shift_B}, the differential comparator circuit 102 may generate the output voltage V_{OUT} at a low level. This low level, applied to the gate terminal of the NMOS transistor MN1 via the feedback connection 202, may turn off the NMOS transistor MN1 such that NMOS transistor MN1 has a relatively high resistance, functioning substantially as an open circuit. Accordingly, all or substantially all of the first mirrored current I_A may flow through the first resistor circuitry R_A instead of the NMOS transistor MN1. Alternatively, when the second comparator input voltage V_{shift_B} rises above the first comparator input voltage V_{shift_offA}, the differential comparator circuit 102 may generate the output voltage V_{OUT} at a high level. This high level, applied to the gate terminal of the NMOS transistor MN1 via the feedback connection 202, may turn on the NMOS transistor MN1 such that the NMOS transistor MN1 has a relatively low resistance, functioning substantially as a short circuit. Accordingly, most if not all of the first mirrored current I_A may flow through the NMOS transistor MN1 instead of through the first resistor circuitry R_A.

[0037] When the NMOS transistor MN1 is turned off, the first comparator input voltage V_{shift_offA} generated at node A may be at or substantially at the level at which it was generated in the first example differential comparator system 100 of Fig. 1. Accordingly, for the second comparator input voltage V_{shift_B} to rise above the first comparator input voltage V_{shift_offA}, the second input voltage V_{IN_B} may correspondingly rise above the first input voltage V_{IN_A} by an amount greater than the voltage generated across the first resistor circuitry R_A. However, when the second comparator input voltage V_{shift_B} does rise above the first comparator input voltage V_{shift_offA}, the high level of the output voltage V_{OUT} may turn on the NMOS transistor MN1, causing the first comparator input voltage V_{shift_offA} generated at node A to drop to a level slightly above the level of

the voltage V_{shift_A} generated at node D. As a result, the second comparator input voltage V_{shift_B}, and correspondingly the second input voltage V_{IN_B}, has to fall by a greater amount to be below the level of the first comparator input voltage V_{shift_offA} than if the first comparator input voltage V_{shift_offA} remained at its initial level.

[0038] For squelch detector or other signal detection applications, such a hysteretic feature may provide for more accurate signal detection in that the voltage generated on the second communication line 122 has to fall a greater amount than the amount that the second comparator voltage V_{shift_B} increased above the first comparator input voltage V_{shift_A} to initially cause the differential comparator circuit 102 to indicate a presence of a signal. To illustrate, suppose that prior to detection of a signal, the first comparator input voltage V_{shift_offA} generated at node A is 250 mV and the level of the voltage V_{shift_A} generated at node A is 200 mV. In other words, the first resistor voltage V_{RA} is 50mV. Subsequently, suppose a differential signal is communicated on the lines 120, 122, causing the second comparator voltage V_{shift_B} to increase to 255 mV, or 5 mV above the first comparator input voltage V_{shift_offA}. Referring to the first differential comparator system 100, if that signal being communicated has a voltage that fluctuates around 5 mV, the second comparator input voltage V_{shift_B} may drop below the first comparator input voltage V_{shift_offA} of 250 mV, causing the differential comparator circuit 102 to output the output voltage V_{OUT} to indicate that a signal is no longer being communicated on the lines 120, 122. Alternatively, referring to the second differential comparator system 200, when the second comparator input signal V_{shift_B} rises to 255 mV, the differential comparator circuit 102 outputs the output voltage V_{OUT} at a high level, causing the NMOS transistor MN1 to turn on. By turning on, the NMOS transistor MN1 may cause the voltage drop from node A to node D to be only a couple millivolts, such as 2 mV for example. Accordingly, the first comparator input voltage V_{shift_offA} may drop from 250 mV to 202 mV. In turn, the second comparator input voltage V_{shift_B} may have to fall below 202 mV instead of only 250 mV (i.e., 48 more millivolts) in order to cause the differential comparator circuit 102 to output the output voltage V_{OUT} at a level that indicates no signal is being communicated. As a result, small fluctuations in the voltage of the signal being communicated on the signal lines 120, 122 may prevent an incorrect indication provided by the differential comparator circuit 102.

[0039] Fig. 3 shows a circuit schematic diagram of an example resistor-dependent current source 300, which may be used for the resistor-dependent current source 114 of the example differential comparator systems 100 and 200. The resistor-dependent current source 300 may include a plurality of PMOS transistors, including a first PMOS transistor M1, a second PMOS transistor M2, and a third PMOS transistor M3. Source terminals of each of the PMOS transistors M1, M2, M3 may be connected to the supply voltage V_{DD}. In addition, gate terminals of each of the PMOS transistors M1, M2, M3 may be connected to each other and to an output of an analog comparator circuit 302. A drain terminal of the first PMOS transistor M1, a first end of a first resistor R1 and a first end of a second resistor R2 may be connected to a positive input terminal of the analog comparator circuit 302 at a node F. A second end of the first resistor R1 may be connected to an emitter terminal of a first bipolar junction transistor (BJT) Q1. Each of a collector terminal of the first BJT Q1 and a second end of the second resistor R2 may be connected to the ground reference voltage V_{SS}. A drain terminal of the second PMOS transistor M2, an emitter terminal of a second BJT Q2 and a first end of a fourth resistor R4 may be connected to a negative input terminal of the analog comparator circuit 302 at a node G. Each of a collector terminal of the second BJT Q2 and a second end of the fourth resistor R4 may be connected to the ground reference voltage V_{SS}. Additionally, base terminals of the first and second BJTs Q1, Q2 may be tied together and also connected to the ground reference voltage V_{SS}. In addition, as shown in Fig. 3, a drain terminal of the third PMOS transistor M3 may be connected to a first end of a third resistor R3, and a second end of the third resistor R3 may be connected to the ground reference voltage V_{SS}.

[0040] The analog comparator circuit 302 may output an output voltage indicative of the difference between the voltages generated at nodes F and G, and that output voltage may be applied to the gate terminals of the PMOS transistors M1, M2, M3. In response, reference currents I_{REF_M1}, I_{REF_M2}, I_{REF_M3} may flow through first, second, and third PMOS transistors M1, M2, M3, respectively. The reference currents I_{REF_M1}, I_{REF_M2}, I_{REF_M3} may mirrored versions of each other and equal and/or proportional in amount to each other. At node F, a first portion I_{1_M1} of reference current I_{REF_M1} may flow through the first resistor and the first BJT Q1, and a second portion I_{2_M1} may flow through the

second resistor R2. At node G, a first portion I_{1_M2} of reference current I_{REF_M2} may flow through the second BJT Q2, and a second portion I_{2_M2} may flow through the fourth resistor R4.

[0041] Reference current I_{REF_M3} may flow through the third resistor R3. A reference voltage V_{REF} may the voltage generated across the third resistor R3 with respect to the ground reference voltage V_{SS}. Assuming that the second and fourth resistors R2, R4 have the same resistance and that the reference currents I_{REF_M1}, I_{REF_M2}, I_{REF_M3} are equal in amount and denoted by I_{REF}, that amount may be mathematically represented as:

$$I_{REF} = \left(\frac{1}{R_2}\right)\left[V_{EB2} + \left(\frac{R_2}{R_1}\right)\ln(N)\cdot V_T\right],$$

where R_1 represents the resistance of the first resistor R1, R_2 represents the resistance of the second and fourth resistors R2 and R4, V_{EB2} is the emitter-to-base voltage of the second BJT Q2, N represents a size ratio of the BJT channel width while length is the same, and V_T is the threshold voltage of the first and second BJTs Q1, Q2. As indicated by the equation, the amount of the reference current I_{REF} may depend on the resistances of the first and second resistors. Accordingly, as these resistance values change or due to PVT conditions, so will the amount of the reference current I_{REF}.

[0042] The gate terminals of the first, second, and third PMOS transistors M1, M2, M3 are tied together at node E. Referring back to Figs. 1 and 2, the gate terminals of the PMOS transistors MP3 and MP4 are also connected to node E. As such, for configurations of the differential comparator systems 100, 200 that use the configuration 300 for its resistor-dependent current source 114, the gate terminals of the PMOS transistors MP3 and MP3 may be connected to the gate terminals of the PMOS transistors M1, M2, M3 of the example resistor-dependent current source 300. Accordingly, the first and second mirrored current I_A and I_B generated by the current mirror circuitry 116 may also depend on the resistances of the resistors R1 and R2 of the example resistor-dependent current source 300.

[0043] As previously described, whether the differential comparator circuit 102 outputs the output voltage V_{OUT} at one level or another to indicate presence or absence of a signal may depend on the first resistor voltage V_{AR}. However, the more the first resistor voltage V_{AR} varies, the less reliable the indication provided by the differential comparator 102

may be. As such, it may desirable for the first resistor voltage V_{RA} to be as stable as possible. The first and second resistor circuitries R_A and R_B may be subjected to various PVT conditions, including process and temperature as described above, that may cause their resistances to change during operation due to variations in temperature and/or differ from designed-for resistances due to resistance drift. However, by configuring the resistors R1, R2, R3, and R4 on the same chip and to be of the same type, the variations of the first and second resistor circuitries R_A and R_B due to PVT conditions may be offset by the resistors R1, R2, R3, and R4 being subjected to the same PVT conditions, which is manifested in the first and second mirrored currents I_A and I_B being supplied to the first and second resistor circuitries R_A and R_B, respectively, resulting in a stable first resistor voltage V_{RA}.

[0044] Figure 4 is a block diagram of another example resistor-dependent current source 400, which may be used for the resistor-dependent current source 114 for either of the example differential comparator systems 100 or 200. The resistor-dependent current source 400 may be similar to the resistor-dependent current source 300 of Fig. 3, except that the resistor-dependent current source 400 may include additional current mirror circuitry to generate the reference current I_{REF}. The additional current mirror circuitry may include fourth and fifth PMOS transistors M4 and M5, and first and second NMOS transistors M6 and M6.

[0045] In further detail, a gate terminal of the fourth PMOS transistor may be tied to the gate terminals of the first, second, and third PMOS transistors M1, M2, and M3, which are connected to the output of the analog differential comparator 302. In addition, a source terminal of the fourth PMOS transistor M4 may be connected to the supply voltage V_{DD}, and a drain terminal of the fourth PMOS transistor M4 may be connected to a drain terminal of the first NMOS transistor M6. Source terminals of both the first and second NMOS transistors M6, M7 may be connected to the ground reference voltage V_{SS}. A drain terminal of the second NMOS transistor M7 may be connected to a drain terminal of the fifth PMOS transistor M5. A source terminal of the fifth PMOS transistor M5 may be connected to the supply voltage V_{DD}. Additionally, the gate terminal of the first NMOS transistor M6 may be connected to its drain terminal, and the gate terminal of the fifth PMOS transistor M5 may be connected to its drain terminal. As such, reference

current I_{REF_M4} drawn through the fourth PMOS transistor M4 and the first NMOS transistor M6 and reference current I_{REF_M5} drawn through the fifth PMOS transistor M5 and the second NMOS transistor M7 may be mirrored versions of reference currents I_{REF_M1}, I_{REF_M2}, I_{REF_M3}.

[0046] As shown in Fig. 4, the gate terminal of the fifth PMOS transistor M5 is connected to node E. As such, when the example current-dependent current source 400 is used in the example differential comparator systems 100, 200, the first and second mirrored currents I_A and I_B may be mirrored versions of reference current I_{REF_M5}, the amount of which depends on the resistances R1 and R2. As such, for configurations of the example differential comparator systems 100, 200 that use the resistor-dependent current source 400, variations of the resistances of the first and second resistor circuitries R_A and R_B due to PVT conditions may be offset due to the first and second current mirrored currents I_A and I_B being dependent on the resistance R1 and R2.

[0047] The example resistor-dependent current sources 300 and 400 shown in Figs. 3 and 4 respectively are merely exemplary and shown as non-limiting examples. Other resistor-dependent current sources that may include resistors of the same type and/or configured on the same chip or IC as the first and second resistor circuitries R_A and R_B may be used for the resistor-dependent current source 114 of Fig. 1 and/or Fig. 2.

[0048] Fig. 5 shows a flow chart of an example method 500 of detecting presence of a signal on a communication line. At block 502, a reference current may be generated based on a resistance provided by one or more resistors of a resistor-dependent current source. At block 504, the reference current may be mirrored to generate first and second mirrored currents. At block 506, the first and second mirrored currents may be supplied to first and second resistors to respectively generate first and second comparator input voltages. The first and second comparator input voltage may be supplied to first and second input terminals of a differential comparator circuit. The first and second comparator input voltages may be generated such that when no signal is being communicated on the communication line, the first comparator input voltage is greater than the second comparator input voltage. In response, the different comparator circuit may output an output voltage at a level to indicate that no signal is being communicated on the communication line. In addition, the first and second resistors may be of the same

type and located on the same chip as the one or more resistors of the resistor-dependent current source.

[0049] At block 508, a signal may be communicated on the communication line. At block 510, in response to the signal being communicated on the communication line, the level of the second comparator input voltage may increase to above the level of the first comparator input voltage. At block 512, in response to the level of the second comparator input voltage increasing above the level of the first comparator input voltage, the different comparator circuit may change the level of the output voltage to indicate that a signal is being communicated on the communication line. In addition, for some example methods, the output voltage may be fed back to a transistor connected in parallel with the first resistor to turn on the transistor. In response, the level of the first comparator input voltage may drop to a lower level. At block 514, the signal may no longer be communicated on the communication line, and in response, the level of the second comparator input voltage may drop to below the level of the first comparator input voltage. The differential comparator circuit may respond by switching the level of the output voltage back to the initial level to indicate that no signal is being communicated on the communication line.

[0050] One of skill in the art will recognize that this invention is not limited to the two dimensional and three dimensional exemplary structures described but cover all relevant memory structures within the spirit and scope of the invention as described herein and as understood by one of skill in the art.

[0051] It is intended that the foregoing detailed description be understood as an illustration of selected forms that the invention can take and not as a definition of the invention. It is only the following claims, including all equivalents, that are intended to define the scope of the claimed invention. Finally, it should be noted that any aspect of any of the preferred embodiments described herein can be used alone or in combination with one another.

What is claimed is:

1. A comparator system comprising:

a comparator circuit configured to:

receive a first input voltage and a second input voltage; and

output an output voltage based on a difference between the first input voltage and the second input voltage;

an input circuit comprising first resistor circuitry, the input circuit configured to:

generate the first input voltage based on the first resistor circuitry; and

supply the first input voltage to the comparator circuit;

a resistor-dependent current generation circuit comprising second resistor circuitry, the resistor-dependent current generation circuit configured to:

generate a resistor-dependent current that depends on the second resistor circuitry; and

supply the resistor-dependent current to the first resistor circuitry to generate the first input voltage,

wherein the first resistor circuitry and the second resistor circuitry are of the same type.

2. The comparator system of claim 1, wherein the input circuit and the resistor-dependent current generation circuit are configured on the same chip.

3. The comparator system of claim 1, wherein the resistor-dependent current generation circuitry comprises:

a current source circuit that comprises the second resistor circuitry, the current source circuit configured to generate a reference current that depends on the second resistor circuitry; and

a current mirror circuit that is configured to:

mirror the reference current to generate the resistor-dependent current; and

supply the resistor-dependent current to the first resistor circuitry.

4. The comparator system of claim 1, wherein the input circuit comprises a first input circuit, wherein the resistor-dependent current comprises a first resistor-dependent current, and wherein the comparator system further comprises:

a second input circuit comprising third resistor circuitry, the second input circuit configured to generate the second input voltage and supply the second input voltage to the comparator circuit,

wherein the resistor-dependent current generation circuit is further configured to:

generate a second resistor-dependent current that depends on the second resistor circuitry; and

supply the second resistor-dependent current to the third resistor circuitry to generate the second input voltage,

wherein the third resistor circuitry is of the same type as the first and second resistor circuitries.

5. The comparator system of claim 4, wherein the second input circuit is configured on the same chip as the first input circuit and the resistor-dependent current generation circuitry.

6. The comparator system of claim 1, wherein the input circuit comprises a first input circuit, the comparator system further comprising a second input circuit configured to generate the second input voltage,

wherein the first input circuit is coupled to a first communication line and configured to generate the first input voltage based on a first line voltage on the first communication line,

wherein the second input circuit is coupled to a second communication line and configured to generate the second input voltage based on a second line voltage on the second communication line,

wherein the output voltage is indicative of a difference in voltage levels between the first line voltage and the second line voltage.

7. The comparator system of claim 6, wherein the first input circuit further comprises a first transistor connected in series with the first resistor circuitry and coupled to the first communication line,

wherein the second input circuit comprises third resistor circuitry connected in series with a second transistor, the second transistor coupled to the second communication line.

8. The comparator system of claim 1, further comprising:

a switch connected in parallel with the first resistor circuitry; and

a feedback connection coupling an output terminal of the comparator circuit with the switch,

wherein a level of the output voltage controls switching of the switch.

9. The comparator system of claim 8, wherein the comparator circuit is configured to output the output voltage such that the level of the output voltage opens the switch when the first input voltage exceeds the second input voltage and closes the switch when the second input voltage exceeds the first input voltage.

10. The comparator system of claim 1, wherein the first resistor circuitry and the second resistor circuity have respective temperature coefficient parameters that are within 5% of each other.

11. The comparator system of claim 1, wherein the first resistor circuitry and the second resistor circuitry are both polysilicon resistors, P-POLY resistors saliside, P-POLY resistors non-saliside, N-POLY resistors saliside, N-POLY resistors non-saliside, Nwell resistors, or metal resistors.

12. A signal detection system comprising:

a signal detection circuit coupled to a pair of communication lines, the signal detection circuit comprising:

first resistor circuitry configured to generate an offset voltage;

a comparator circuit coupled to the first resistor circuitry, the comparator configured to generate an output voltage at a level that indicates whether a first line voltage on the pair of communication lines exceeds a second line voltage on the pair of communication lines by an amount corresponding to the offset voltage; and

a resistor-dependent current generation circuit comprising second resistor circuitry, the resistor-dependent current generation circuit configured to:

generate a resistor-dependent current that depends on the second resistor circuitry; and

supply the resistor-dependent current to the first resistor circuitry to generate the offset voltage,

wherein the first resistor circuitry and the second resistor circuitry are of the same type.

13. The signal detection system of claim 12, wherein the first resistor circuitry and the second resistor circuitry are configured on the same chip.

14. The signal detection system of claim 12, further comprising:

a first input circuit that comprises the first resistor circuitry, the first input circuit configured to generate a first comparator input voltage to the comparator circuit, the first comparator input voltage based on the offset voltage and the first line voltage; and

a second input circuit that comprises third resistor circuity, the second input circuit configured to generate a second comparator input voltage to the comparator circuit, the second input voltage based on the second line voltage.

15. The signal detection system of claim 14, wherein the resistor-dependent current comprises a first resistor-dependent current,

wherein the resistor-dependent current generation circuit comprises:

a current source circuit that comprises the second resistor circuitry, the current source circuit configured to generate a reference current that depends on the second resistor circuitry; and

a current mirror circuit that is configured to:

mirror the reference current to generate the first resistor-dependent current and a second resistor-dependent current that depends on the second resistor circuitry;

supply the first resistor-dependent current to the first resistor circuitry; and

supply the second resistor-dependent current to the third resistor circuitry.

16. The signal detection system of claim 14, wherein the second input circuitry is configured to generate the second comparator input voltage at a level that is greater than a level of the first comparator input voltage in response to the first line voltage and the second line voltage corresponding present of a differential signal on the pair of communication lines.

17. The signal detection system of claim 12, further comprising:

a switch connected in parallel with the first resistor circuitry; and

a feedback connection coupling an output terminal of the comparator circuit with the switch,

wherein a level of the output voltage controls switching of the switch.

18. A method of detecting presence of a signal on a pair of communication lines, the method comprising:

generating, with resistor-dependent current generation circuitry, a resistor-dependent current that depends on first resistor circuitry;

generating, with second resistor circuitry; an offset voltage in response to the resistor-dependent current;

generating, with a first input circuit coupled to the pair of communication lines, a first input voltage at a first input terminal of a comparator circuit, the first input voltage based on the offset voltage and a first line voltage generated on the pair of communication lines;

generating, with a second input circuit coupled to the pair of communication lines, a second input voltage at a second input terminal of the comparator circuit, the second input voltage based on a second line voltage generated on the pair of communication lines; and

outputting, with the comparator circuit, an output voltage based on a difference between the first input voltage and the second input voltage, wherein a level of the output voltage indicates presence or absence of a signal being communicated on the pair of communication lines.

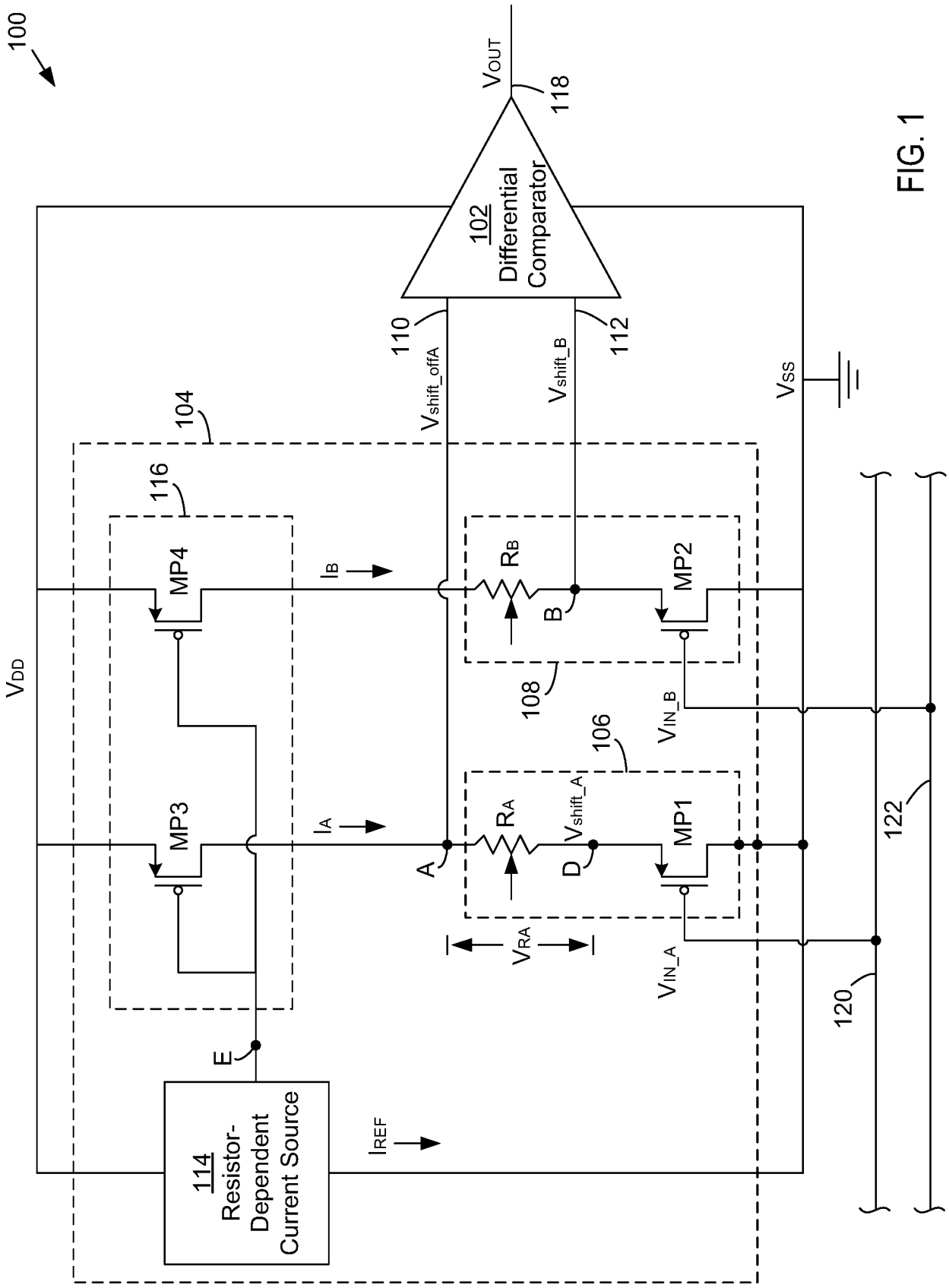
19. The method of claim 18, further comprising:

applying, with a feedback connection, the output voltage to a switch connected in parallel with the second resistor circuitry;

when the second input voltage exceeds the first input voltage, outputting the output voltage at a level that turns on the switch; and

reducing, with the switch, the first input voltage level in response to turning on.

20. The method of claim 18, wherein the first resistor circuity and the second resistor circuitry are at least one of: the same type or configured on the same chip.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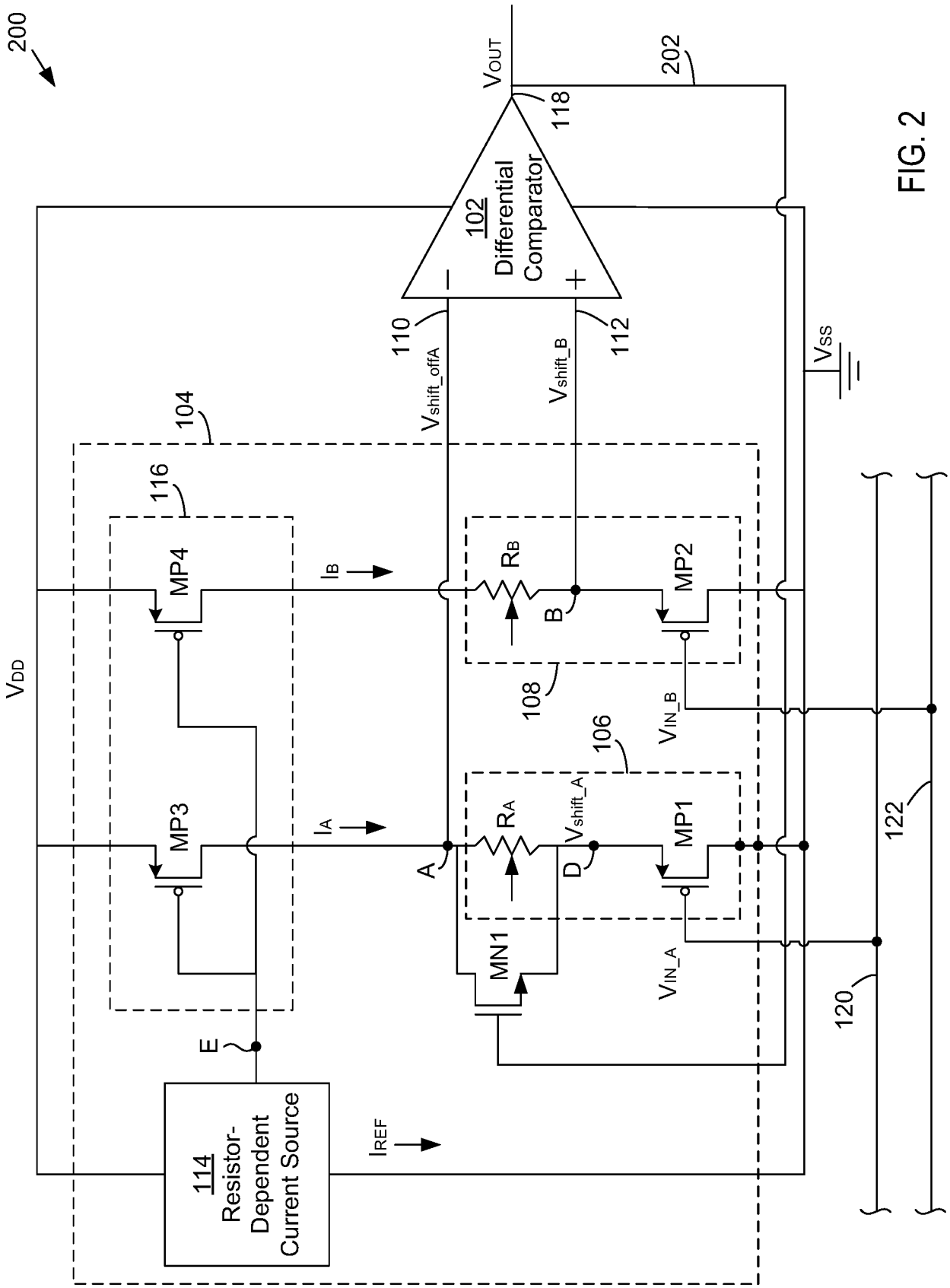
VOUT
118
102
Differential
Comparator
110
Vshift_offA
Vshift_B
112
VSS
104
116
MP4
IB
RB
MP2
B
VDD
108
VIN_B
106
MP3
IA
RA
Vshift_A
MP1
A
D
VRA
VIN_A
122
120
E
114
Resistor-
Dependent
Current Source
IREF

FIG. 1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VOUT
202
118
102
Differential
Comparator
110
Vshift_offA
Vshift_B
112
VSS
104
116
MP4
IB
RB
MP2
B
108
VIN_B
106
MP3
IA
RA
Vshift_A
MP1
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MN1
VIN_A
122
120
E
114
Resistor-
Dependent
Current Source
IREF
VDD

FIG. 2

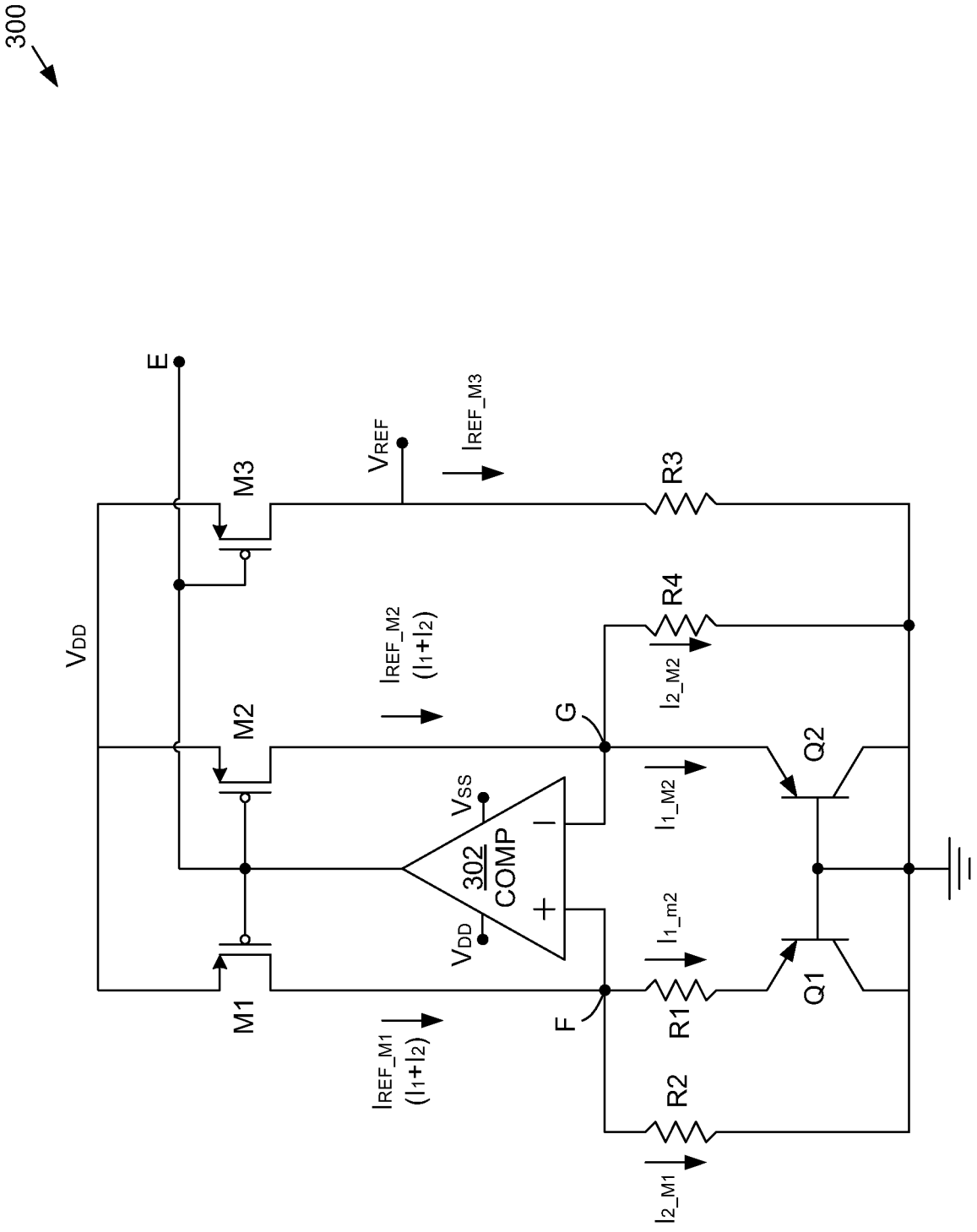
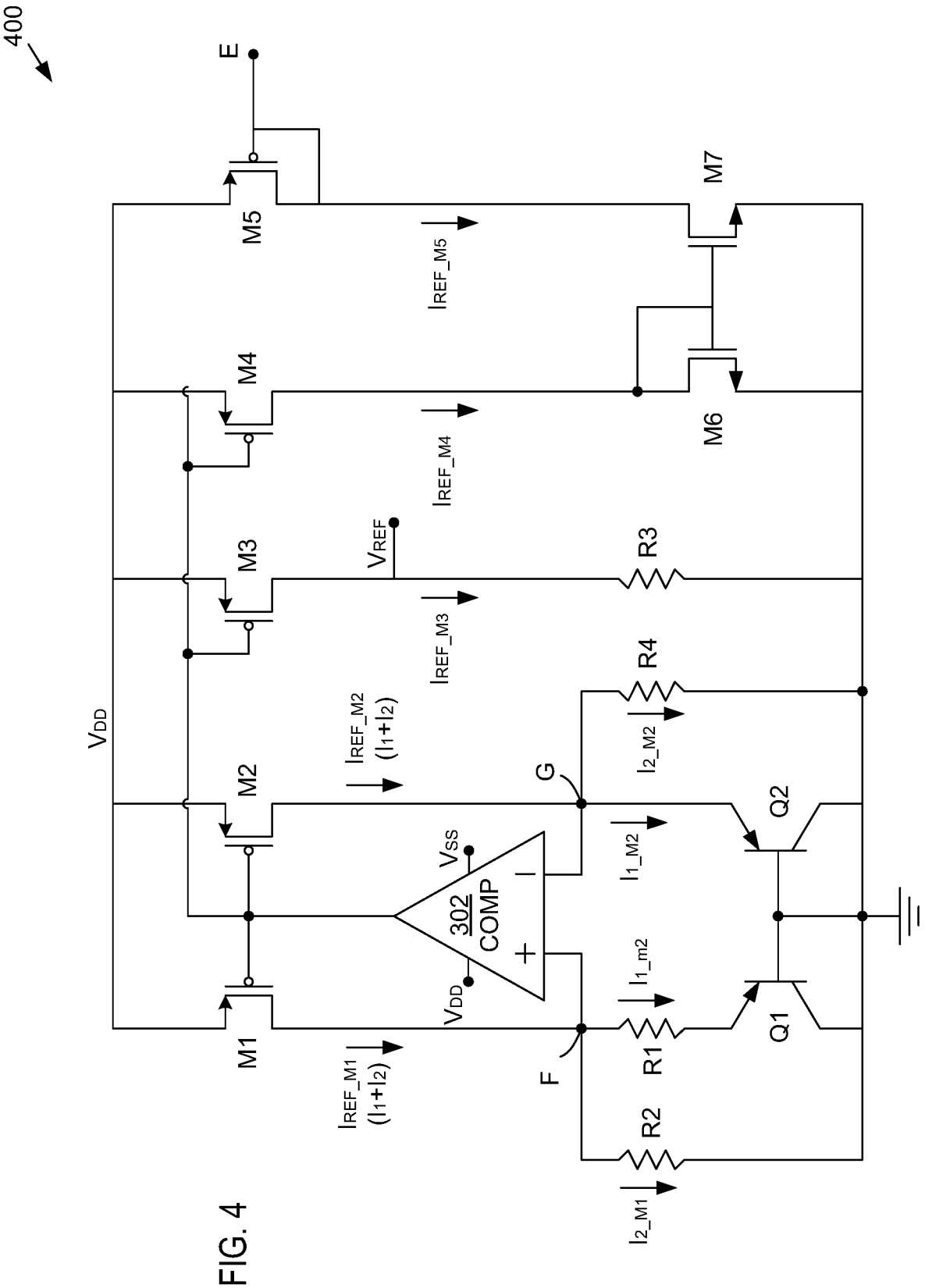

300
E
M3
M2
M1
VDD
VREF
IREF_M3
IREF_M2
(I1+I2)
IREF_M1
(I1+I2)
R3
R4
R2
R1
G
F
Q2
Q1
I2_M2
I1_M2
I1_m2
I2_M1
VSS
VDD
302
COMP
+
-

FIG. 3


400
E
M5
M7
IREF_M5
M4
M6
IREF_M4
VREF
M3
R3
IREF_M3
R4
VDD
IREF_M2
(I1+I2)
I2_M2
G
M2
Q2
VSS
I1_M2
302
COMP
I1_m2
VDD
M1
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Q1
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(I1+I2)
F
R2
I2_M1

FIG. 4

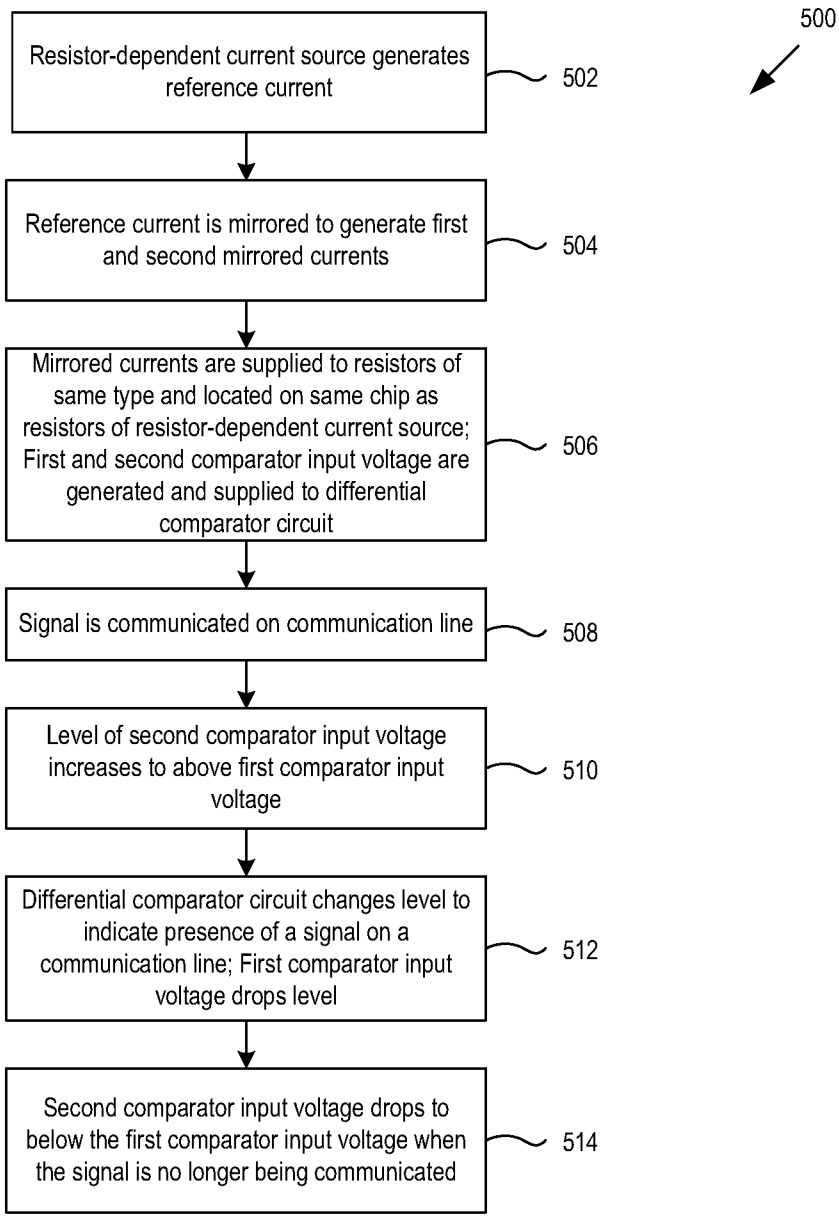
500
Resistor-dependent current source generates reference current
502
Reference current is mirrored to generate first and second mirrored currents
504
Mirrored currents are supplied to resistors of same type and located on same chip as resistors of resistor-dependent current source; First and second comparator input voltage are generated and supplied to differential comparator circuit
506
Signal is communicated on communication line
508
Level of second comparator input voltage increases to above first comparator input voltage
510
Differential comparator circuit changes level to indicate presence of a signal on a communication line; First comparator input voltage drops level
512
Second comparator input voltage drops to below the first comparator input voltage when the signal is no longer being communicated
514

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2016/029969

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K5/24 H04L25/06
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2004 194124 A (ASAHI CHEMICAL MICRO SYST) 8 July 2004 (2004-07-08)	1-6, 8-13, 15-20
A	abstract; figures 1,2,3	7,14
X	US 5 408 694 A (TRAN TOAN V [US]) 18 April 1995 (1995-04-18)	1-7, 10-16, 18,20
	abstract; figure 2 column 2, line 15 - column 3, line 28	
X	US 2009/206806 A1 (KAMATANI TOMOHIKO [JP]) 20 August 2009 (2009-08-20)	1-6, 8-13, 15-20
A	abstract; figures 6,10 paragraphs [0002], [0008], [0037], [0038], [0044], [0046], [0063], [0065]	7,14

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 July 2016	22/07/2016

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Mesic, Maté

1

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2016/029969

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011/057686 A1 (UEDA YASUO [JP]) 10 March 2011 (2011-03-10)	1-6, 10-13, 15,16, 18,20
A	abstract; figures 2,3,4	7,14

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2016/029969

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