A gate driving circuit includes several driving circuit units and several switch units. Each driving circuit unit outputs several driving signals to several scan lines sequentially. One of the switch units is respectively disposed between two adjacent driving circuit units and conducts or blocks a first and a second clock signal transmitted to driving circuit units.
Fig. 1
(PRIOR ART)
Fig. 2
Fig. 4
Fig. 5
Fig. 6
bias

input signal

Switch unit

output signal

Fig. 7A

trigger signal

stop signal

Fig. 7B
trigger signal

stop signal

$V_{bias}$

S1

S2

S3

M1

M2

M3

M4

M5

M6

VSS

VSS

Fig. 8
Fig. 10
GATE DRIVING CIRCUIT OF LIQUID CRYSTAL DISPLAY

RELATED APPLICATIONS

[0001] The present invention is a division of U.S. application Ser. No. 11/674,691, filed Feb. 14, 2007, which claims priority to Taiwan Patent Application Serial Number 95141587, filed Nov. 9, 2006, the disclosure of which is hereby incorporated by reference herein in its entirety.

BACKGROUND

[0002] 1. Field of Invention
[0003] The present invention relates to a gate driving circuit of a liquid crystal display.

[0004] 2. Description of Related Art
[0005] In a conventional liquid crystal display, the driving circuit development is usually one of the key technologies and also the most important factor for the quality and the production cost of the liquid crystal display. FIG. 1 shows a gate driving circuit of the conventional liquid crystal display. The gate driving circuit 100 includes driving signal output circuits 102. Each of the driving signal output circuits 102 is controlled by clock signals CK1 and CK2 with opposite phases, and outputs a driving signal to a corresponding scan line.

[0006] In the gate driving circuit 100, the driving signal outputted from the previous driving signal output circuit 102 is transmitted to the next driving signal output circuit 102, so as to trigger the next driving signal output circuit 102 to output the driving signal. However, the clock signals CK1 and CK2 are continuously transmitted to each of the driving signal output circuits 102 during the operation of the gate driving circuit 100, so that the driving signal output circuits 102, disposed at the latter part of the gate driving circuit 100 and not being driven yet, also receives the clock signals CK1 and CK2 and causes unnecessary losses.

[0007] For the foregoing reasons, there is a need for a gate driving circuit capable of reducing the circuit losses.

SUMMARY

[0008] In accordance with one embodiment of the present invention, a gate driving circuit is provided. The gate driving circuit includes driving circuit units and switch units. Each of the driving circuit units sequentially outputs driving signals to scan lines. Each of the switch units is disposed between two adjacent driving circuit units and conducts or blocks a first clock signal and a second clock signal transmitted to the driving circuit units. Each of the switch units is turned on by receiving one of the driving signals outputted from a previous driving circuit unit, so as to allow a next driving circuit unit to receive the first clock signal and the second clock signal.

[0009] In accordance with another embodiment of the present invention, a gate driving circuit of a liquid crystal display is provided. The gate driving circuit includes driving circuit units, a timing controller, a clock signal generator and switch units. Each of the driving circuit units sequentially outputs one of driving signals to a corresponding scan line of the liquid crystal display. The timing controller generates a reference clock signal. The clock signal generator receives the reference clock signal and outputs a first clock signal and a second clock signal to the driving circuit units according to the reference clock signal. Further, each of the switch units is disposed between two adjacent driving circuit units for conducting or blocking the first clock signal and the second clock signal outputted from the clock signal generator.

[0010] In accordance with yet another embodiment of the present invention, a gate driving circuit is provided. The gate driving circuit includes driving circuit units and a clock output unit. Each of the driving circuit units sequentially outputs driving signals and the driving signals are sequentially transmitted to corresponding scan lines. The clock signal output unit transmits clock signals respectively to one of the driving circuit units to sequentially control the driving circuit units. The clock signal output unit transmits only one of the clock signals to one of the driving circuit units at a time.

[0011] In accordance with yet another embodiment of the present invention, a switch unit is provided. The switch unit includes a switch and a flip-flop circuit. The switch conducts or blocks a transmission signal. The flip-flop circuit is controlled with a bias and electrically couples to the switch, and receives a trigger signal to turn the switch to conduct the transmission signal or receives a stop signal to turn off the switch to block the transmission signal. The flip-flop circuit includes an input unit, an assistant output unit and an output unit. The input unit couples to the bias and receives the trigger signal or the stop signal to output a first signal. The assistant output unit couples to the bias and the input unit and receives the first signal to output a second signal. The output unit couples to the bias, the assistant output unit and the switch and receives the second signal to output a third signal to control the switch.

[0012] It is to be understood that both the foregoing general description and the following detailed description are by examples, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The invention can be more fully understood by reading the following detailed description of the preferred embodiment, with reference made to the accompanying drawings as follows:

[0014] FIG. 1 shows a gate driving circuit of the conventional liquid crystal display; and
[0015] FIG. 2 shows a gate driving circuit according to the first embodiment of the present invention; and
[0016] FIG. 3 is a clock diagram showing the transmission condition of the clock signals; and
[0017] FIG. 4 shows the switch unit in FIG. 2; and
[0018] FIG. 5 shows a gate driving circuit according to the second embodiment of the present invention; and
[0019] FIG. 6 shows a gate driving circuit according to the third embodiment of the present invention; and
[0020] FIG. 7A shows the switch unit in FIG. 6; and
[0021] FIG. 7B shows the switch unit in FIG. 7A; and
[0022] FIG. 8 shows the flip-flop circuit in FIG. 7B; and
[0023] FIG. 9 shows a gate driving circuit according to the fourth embodiment of the present invention; and
[0024] FIG. 10 shows a gate driving circuit according to the fifth embodiment of the present invention; and
[0025] FIG. 11 is another clock diagram showing the transmission condition of the clock signals.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0026] Detailed illustrative embodiments of the present invention are disclosed herein. However, specific details dis-
closed herein are merely representative for purposes of describing exemplary embodiments of the present invention. This invention may, however, be embodied in many alternate forms and should not be construed as limited to the embodiments set forth herein.

[0027] FIG. 2 shows a gate driving circuit according to the first embodiment of the present invention. The gate driving circuit 200 includes driving circuit units 210 and switch units 230a. Four driving circuit units 210 are taken for example herein in order to be easily described, and each of the driving circuit units 210 is assumed to output N driving signals.

[0028] In the gate driving circuit 200, each of the driving circuit unit 210 includes N driving signal output circuits (not shown) for sequentially outputting N driving signals to N scan lines. The switch units 230a are respectively disposed between two adjacent driving circuit units 210 and conduct or block first clock signal CK1 and a second clock signal CK2 transmitted to the driving circuit units 210. Each of the switch units 230a is turned on by receiving one of the driving signals outputted from the previous driving circuit unit 210, so as to allow the next driving circuit unit 210 to receive the first clock signal and the second clock signal.

[0029] Besides, the gate driving circuit 200 can further include a clock signal output unit 220 to transmit the clock signals CK1 and CK2 to the driving circuit units 210, and the clock signal output unit 220 can further include a timing controller 222 and a clock signal generator 224a. The timing controller 222 generates a reference clock signal. The clock signal generator 224a receives the reference clock signal and generates the clock signals CK1 and CK2 according to the reference clock signal.

[0030] Furthermore, a gate driving circuit of a liquid crystal display is provided according to another embodiment of the present invention. The gate driving circuit includes driving circuit units 210, a timing controller 222, a clock signal generator 224a and switch units 230a. Each of the driving circuit units 210 includes driving signal output circuits (not shown) which sequentially output one of driving signals to a corresponding scan line of the liquid crystal display. The timing controller 222 generates a reference clock signal. The clock signal generator 224a receives the reference clock signal and outputs the first clock signal CK1 and the second clock signal CK2 to the driving circuit units 210 according to the reference clock signal. The timing controller 222 and the clock signal generator 224a can be disposed on a printed circuit board assembly or a substrate. Besides, the switch units 230a are respectively disposed between two adjacent driving circuit units 210 to conduct or block the clock signals CK1 and CK2 outputted from the clock signal generator 224a.

[0031] An operation of the gate driving circuit 200 is described as follows with an embodiment. First of all, the clock signals CK1 and CK2 control the first driving circuit unit 210. Then, when the clock signal generator 224a transmits a start signal ST to the first driving circuit unit 210, the first driving circuit unit 210 is triggered and sequentially outputs the driving signals G1, . . . , Gx, to the scan lines, and transmits the last driving signal Gx to the second driving circuit unit 210, so as to trigger the second driving circuit unit 210.

[0032] Therefore, the switch unit 230a, disposed between the first and the second driving circuit units 210, is turned on because the switch unit 230a receives one of the driving signals outputted from the first driving circuit unit 210, such as Gx-2, so that the second driving circuit unit 210 can receive the clock signals CK1 and CK2. Then, after the second driving circuit unit 210 is triggered by the driving signal Gx, the second driving circuit unit 210 sequentially outputs the driving signals Gx+1, . . . , GxN, to the scan lines and transmits the last driving signal GxN to the third driving circuit unit 210, so as to trigger the third driving circuit unit 210. The third and the fourth driving circuit units 210 then sequentially output the driving signals G2N+1, . . . , G3N, and the driving signals G3N+1, . . . , G4N, respectively, in the same way.

[0033] After the last driving circuit unit 210 outputs the last driving signal G4N, the last driving circuit unit 210 transmits the driving signal GxN back to the clock signal generator 224a, so as to stop the clock signal generator 224a transmitting the clock signals CK1 and CK2, and the clock signals CK1 and CK2 are outputted from the clock signal generator 224a again until the next operation.

[0034] FIG. 3 is a clock diagram showing the transmission condition of the clock signals. Referring to FIG. 2 and FIG. 3 and taking the transmission condition of the first clock signal CK1 for example, at first, the clock signal generator 224a transmits the first clock signal CK1 to the first driving circuit unit 210. Therefore, the first switch unit 230a is still turned off, so the first clock signal CK1 only passes nodes A and does not pass nodes B, C and D. Then, after the first switch unit 230a is turned on because of receiving one of the driving signals outputted from the first driving circuit unit 210, such as Gx-2, the first clock signal CK1 passes the nodes A and B; that is, the first clock signal CK1 is transmitted to the second driving circuit unit 210 through the first switch unit 230a. Therefore, the second switch unit 230a is still turned off, so the first clock signal CK1 does not pass the nodes C and D. Each of the switch units 230a is sequentially conducted as mentioned to pass on the first clock signal CK1 to the latter driving circuit units 210.

[0035] FIG. 4 shows the switch unit in FIG. 2. The switch unit 230a is controlled with the bias Vbias and receives a trigger signal to turn on, so that the input signal can be transmitted through the switch unit 230a. In this embodiment, the trigger signal is one of the driving signals outputted from the previous driving circuit unit 210, and the input and output signals are clock signals CK1 and CK2, respectively.

[0036] FIG. 5 shows a gate driving circuit according to the second embodiment of the present invention. Comparing FIG. 5 and FIG. 2, the gate driving circuit 500 further includes compensation circuits 510. Each of the compensation circuits 510 is disposed before one of the driving circuit units 210 for compensating the clock signals CK1 and CK2, and transmits the compensated clock signals CK1 and CK2 to the corresponding driving circuit unit 210, so as to prevent the clock signals CK1 and CK2 from gradually decaying and not being transmitted normally when the clock signals CK1 and CK2 is transmitted to the latter part of the gate driving circuit 500.

[0037] FIG. 6 shows a gate driving circuit according to the third embodiment of the present invention. Comparing FIG. 6 and FIG. 2, the last driving circuit unit 210 transmits the last driving signal G4N back to the switch units 230b, so that the switch units 230b are accordingly turned off to block the clock signals CK1 and CK2.

[0038] FIG. 7A shows the switch unit in FIG. 6. Comparing the switch unit 230b and the switch unit 230a in FIG. 4, the switch unit 230b can further receive a stop signal, so that the switch unit 230b can be turned off to block the clock signals CK1 and CK2 because of receiving the stop signal.
FIG. 7B shows the switch unit in FIG. 7A. The switch unit 230b includes a switch 700 and a flip-flop circuit 702. The switch 700 conducts or blocks the transmission signals, and the switch 700 can be a NAND gate or a transmission gate. The flip-flop circuit 702 is controlled with the bias $V_{bias}$ and electrically couples to the switch 700, and receives a trigger signal to turn on the switch 700 which conducts the transmission signals or receives a stop signal to turn off the switch 700 which blocks the transmission signals. In FIG. 7B, the trigger signal is one of the driving signals outputted from the previous driving circuit unit 210, and the stop signal is the last driving signal outputted from the last driving circuit unit 210, and the input and output signals are the clock signals CK1 and CK2, respectively.

FIG. 8 shows the flip-flop circuit in FIG. 7B. The flip-flop circuit 702 includes an input unit 802, an assistant output unit 804 and an output unit 806. The input unit 802 couples to the bias $V_{bias}$ and receives the trigger signal or the stop signal to output a first signal $S_1$. The assistant output unit 804 couples to the bias $V_{bias}$ and the input unit 802 and receives the first signal $S_1$ to output a second signal $S_2$. The output unit 806 couples to the bias $V_{bias}$, the assistant output unit 804 and the switch unit 700 and receives the second signal $S_2$ to output a third signal $S_3$ to control the switch unit 700.

The input unit 802 includes a transistor M1 and a transistor M2. The gate electrode of the transistor M1 receives the trigger signal, and the first source/drain electrode of the transistor M1 couples to the bias $V_{bias}$, and the second source/drain electrode of the transistor M1 outputs the first signal $S_1$. Further, the gate electrode of the transistor M2 receives the stop signal, and the first source/drain electrode of the transistor M2 couples to the second source/drain electrode of the transistor M1 and outputs the first signal $S_1$, and the second source/drain electrode of the transistor M2 couples to a power voltage VSS.

The assistant output unit 804 includes a transistor M3 and a transistor M4. The gate electrode and the first source/drain electrode of the transistor M3 couples to the bias $V_{bias}$, and the second source/drain electrode of the transistor M3 outputs the second signal $S_2$. Further, the gate electrode of the transistor M4 receives the first signal $S_1$, and the first source/drain electrode of the transistor M4 couples to the second source/drain electrode of the transistor M3 and outputs the second signal $S_2$, and the second source/drain electrode of the transistor M4 couples to the power voltage VSS.

Besides, the output unit 806 includes a transistor M5 and a transistor M6. The gate electrode and the first source/drain electrode of the transistor M5 couples to the bias $V_{bias}$, and the second source/drain electrode of the transistor M5 outputs the third signal $S_3$ to control the switch 700. Further, the gate electrode of the transistor M6 receives the second signal $S_2$, and the first source/drain electrode of the transistor M6 outputs the third signal $S_3$, and the second source/drain electrode of the transistor M6 couples to the power voltage VSS.

An operation of the flip-flop circuit 702 is described as following with an embodiment. When the flip-flop circuit 702 receives the trigger signal, the transistor M1 is turned on and the transistor M2 is turned off, so that the outputted first signal $S_1$ is at the high-level state. At this time, the transistors M3 and M4 are both turned on, so that the outputted second signal $S_2$ is at the low-level state. Then, the transistor M6 is turned off and the transistor M5 is turned on, so the outputted third signal $S_3$ is at the high-level state and the switch 700 is accordingly turned on. After the flip-flop circuit 702 receives the trigger signal, the flip-flop circuit 702 receives no signals. The transistors M1 and M2 are therefore turned off and the second signal $S_2$ is at the low-level state, so that the transistor M6 is turned off and the transistor M5 is turned on, and the third signal $S_3$ is therefore at the high-level state. Then, when the flip-flop circuit 702 receives the stop signal, the transistor M2 is turned on and the transistor M1 is turned off, so that the first signal $S_1$ is at the low-level state. Then, the transistor M3 is turned on and the transistor M4 is turned off, so that the second signal $S_2$ is at the high-level state. The transistor M6 is therefore turned on and the transistor M5 is turned on, so that the third signal $S_3$ is at the low-level state and the switch unit 700 is therefore turned off. So, the output of the flip-flop circuit 702 can be determined by the trigger signal or the stop signal, and the turn-on or turn-off state of the switch unit 230b can be determined as well.

FIG. 9 shows a gate driving circuit according to the fourth embodiment of the present invention. Comparing FIG. 9 and FIG. 6, the clock signal generator 224c transmits a stop signal to each of the switch units 230c to turn off the switch units 230c to block the clock signals CK1 and CK2 after the last driving circuit unit 210 outputs the last driving signal $G_{AN}$. Further, the clock signal generator 224c can also stop transmitting the clock signals CK1 and CK2 after the last driving circuit unit 210 outputs the last driving signal $G_{AN}$.

FIG. 10 shows a gate driving circuit according to the fifth embodiment of the present invention. The gate driving circuit 900 includes driving circuit units 910 and a clock signal output unit 920. Four driving circuit units 910 are similarly taken for example herein in order to be easily described, and each of the driving circuit units 910 is similarly assumed to output N driving signals.

In the gate driving circuit 900, each of the driving circuit units 910 includes N driving signal output circuit (not shown) for outputting N driving signals, and each of the driving signals is sequentially transmitted to a corresponding scan line. Besides, the clock signal output unit 920 transmits clock signals CK1, CK2, CK3 and CK4 respectively to the corresponding driving circuit units 910 to sequentially control the driving circuit units 910, and the clock signal output unit 920 transmits only one of the clock signals to one of the corresponding driving circuit units 910 at a time.

Further, the clock signal output unit 920 can also include a timing controller 922 and a clock signal generator 924. The timing controller 922 generates a reference clock signal. The clock signal generator 924 receives the reference clock signal and outputs the clock signals CK1, CK2, CK3 and CK4 according to the reference clock signal. An operation of the gate driving circuit 900 is described as following with an embodiment. First of all, the clock signal generator 924 outputs only the clock signal CK1 to control the first driving circuit unit 910. Then, when the clock signal generator 924 transmits a start signal ST to the first driving circuit unit 910, the first driving circuit unit 910 is triggered and sequentially outputs the driving signals $G_{s_1}$ to the scan lines, and transmits the last driving signal $G_{AN}$ to the second driving circuit unit 910, so as to trigger the second driving circuit unit 910.

At this time, the clock signal generator 924 is turned into outputting only the clock signal CK2, so as to control the second driving circuit unit 910. After the second driving circuit unit 910 is triggered, the second driving circuit unit
910 sequentially outputs the driving signals $G_{2N+1} \ldots G_{3N}$ to the scan lines and outputs the last driving signal $G_{2N}$ to the third driving circuit unit 910, so as to control the third driving circuit unit 910. The third and fourth driving circuit unit 910 sequentially output the driving signals $G_{3N+1} \ldots G_{3N}$ and the driving signals $G_{4N+1} \ldots G_{4N}$ respectively, in the same way.

As is understood by a person skilled in the art, the foregoing preferred embodiments of the present invention are illustrated of the present invention rather than limiting of the present invention. It is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims, the scope of which should be accorded the broadest interpretation so as to encompass all such modifications and similar structures.

What is claimed is:

1. A gate driving circuit, comprising:
   a plurality of driving circuit units, wherein each of the driving circuit units sequentially outputs a plurality of driving signals and the driving signals are sequentially transmitted to corresponding scan lines; and
   a clock signal output unit transmitting clock signals respectively to one of the driving circuit units to sequentially control the driving circuit units;
   wherein the clock signal output unit transmits only one of the clock signals to one of the driving circuit units at a time.

2. The gate driving circuit of claim 1, wherein the clock signal output unit further comprises:
   a timing controller generating a reference clock signal; and
   a clock signal generator receiving the reference clock signal and outputting the clock signals according to the reference clock signal.

3. The gate driving circuit of claim 1, wherein the gate driving circuit is fabricated on a glass substrate.

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