US 20060051922A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2006/0051922 A1**

Huang et al. (43) **Pub. Date: Mar. 9, 2006**

(54) **STRAINED SILICON DEVICE MANUFACTURING METHOD**

(75) Inventors: **Chien-Chao Huang**, Hsin-Chu (TW); **Cheng-Chuan Huang**, Taipei (TW); **Fu-Liang Yang**, Hsin-Chu City (TW)

Correspondence Address:
HAYNES AND BOONE, LLP
901 MAIN STREET, SUITE 3100
DALLAS, TX 75202 (US)

(73) Assignee: **Taiwan Semiconductor Manufacturing Company, Ltd.**, Hsin-Chu (TW)

(21) Appl. No.: **10/937,722**

(22) Filed: **Sep. 9, 2004**

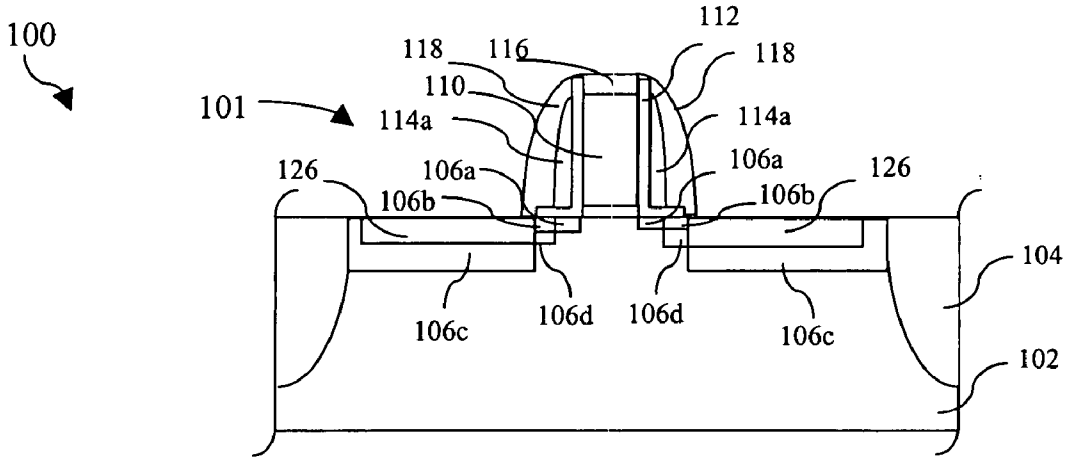
Publication Classification

(51) **Int. Cl.**
H01L 21/336 (2006.01)

(52) **U.S. Cl.** **438/282**

(57) **ABSTRACT**

A method of manufacturing a microelectronic device includes forming a p-channel transistor on a silicon substrate by forming a poly gate structure over the substrate and forming a lightly doped source/drain region in the substrate. An oxide liner and nitride spacer are formed adjacent to opposing side walls of the poly gate structure and a recess is etched in the semiconductor substrate on opposing sides of the oxide liner. Raised SiGe source/drain regions are formed on either side of the oxide liner and slim spacers are formed over the oxide liner. A hard mask over the poly gate structure is used to protect the poly gate structure during the formation of the raised SiGe source/drain regions. A source/drain dopant is then implanted into the substrate including the SiGe regions.



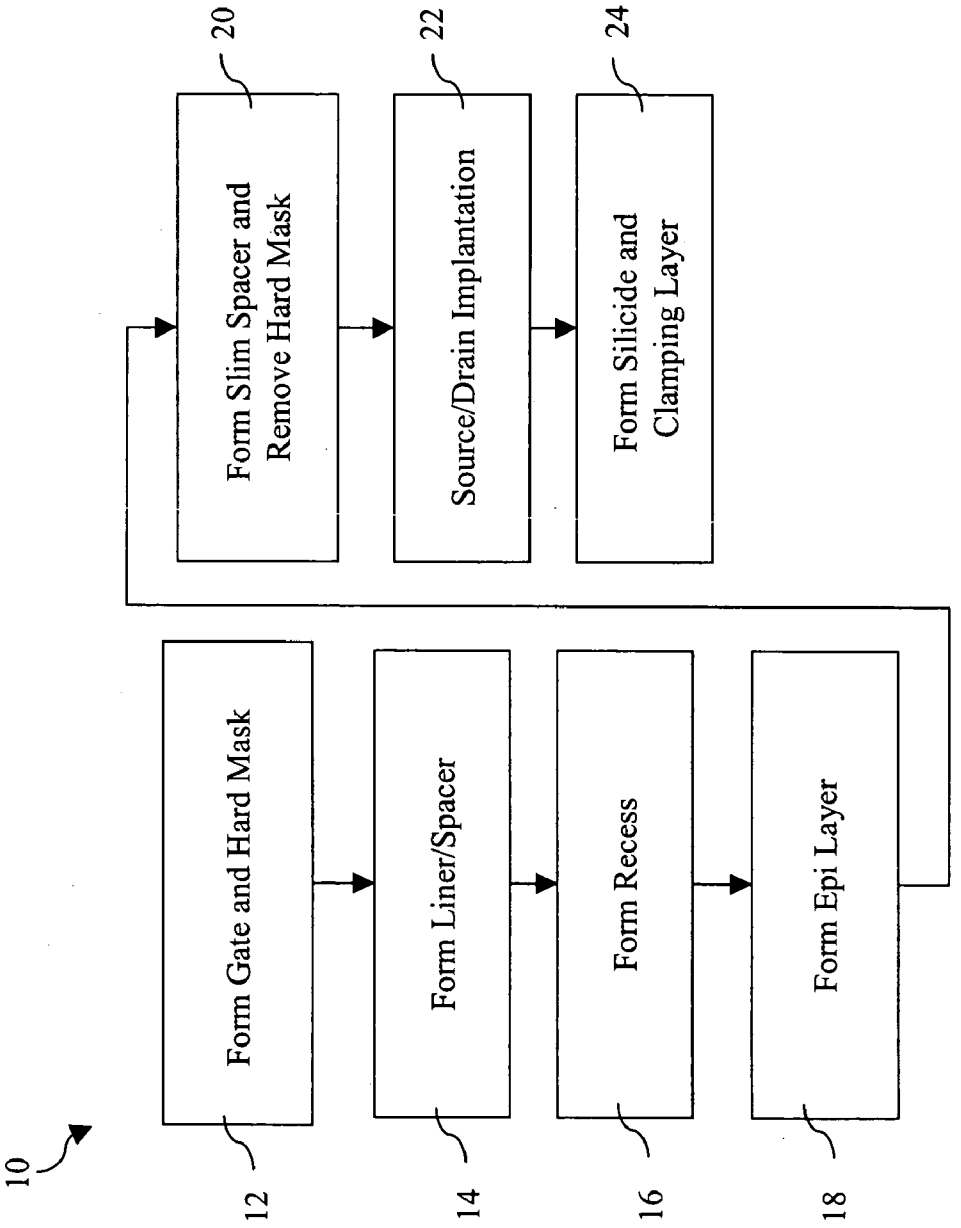

10
12
Form Gate and Hard Mask
14
Form Liner/Spacer
16
Form Recess
18
Form Epi Layer
20
Form Slim Spacer and Remove Hard Mask
22
Source/Drain Implantation
24
Form Silicide and Clamping Layer

Fig. 1

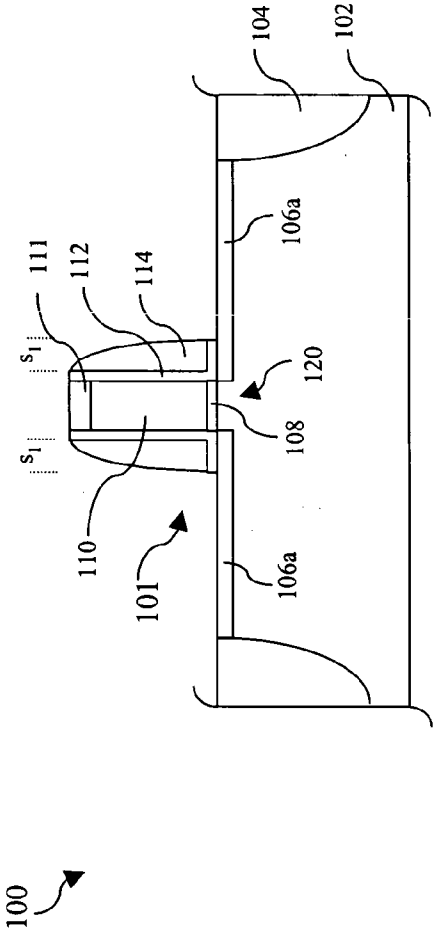

104
102
106a
111
112
114
s_1
s_1
120
108
110
101
106a
100

Fig. 2

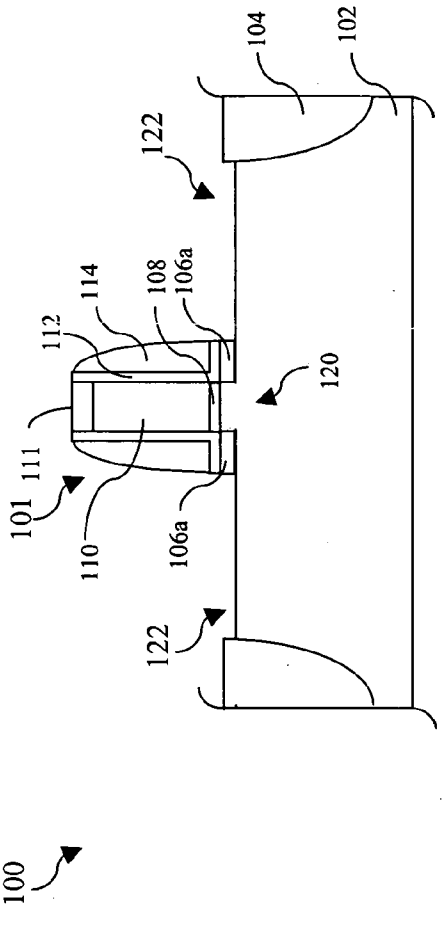

104
102
122
114
108
106a
112
120
111
101
110
106a
122
100

Fig. 3

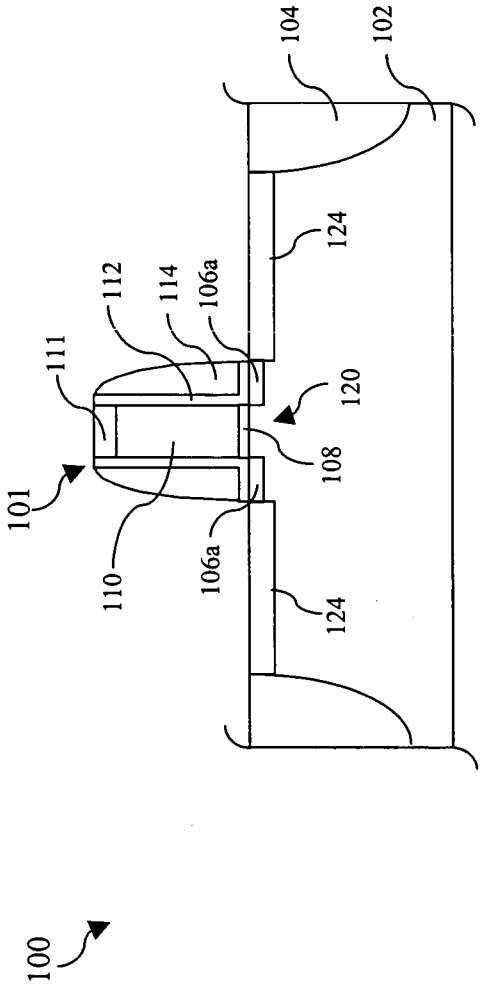

104
102
124
112
114
106a
111
120
108
101
110
106a
124
100

Fig. 4

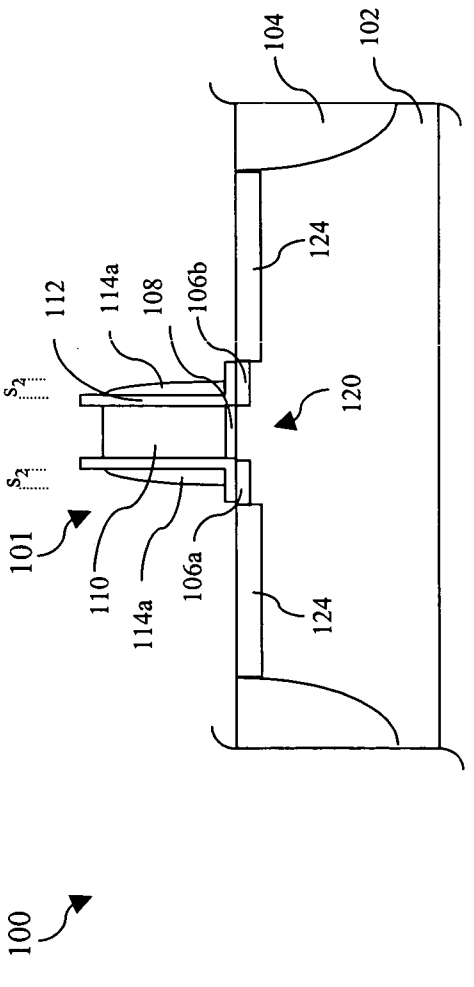

104
102
124
112
114a
108
106b
S_2
120
S_2
101
110
114a
106a
124
100

Fig. 5

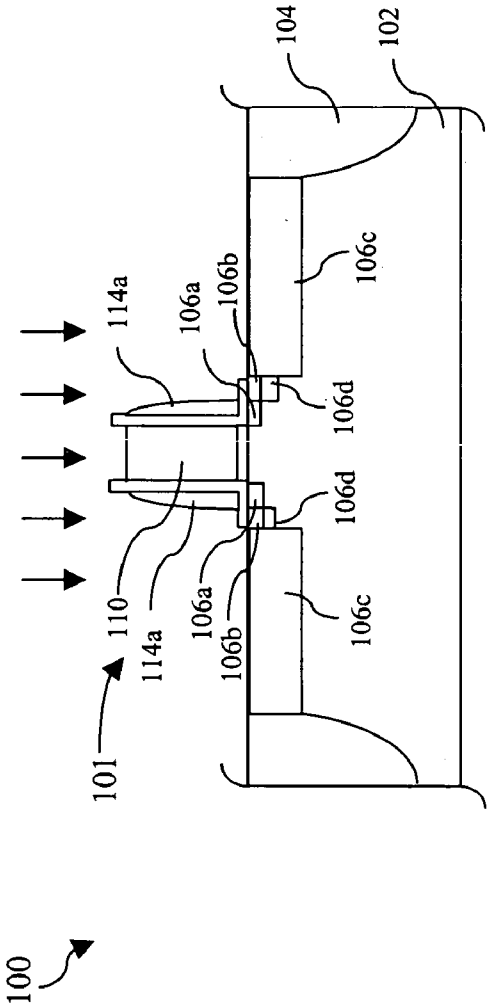

204
104
102
114a
106a
106b
106c
106d
110
114a
106a
106b
106d
106c
101
100

Fig. 6

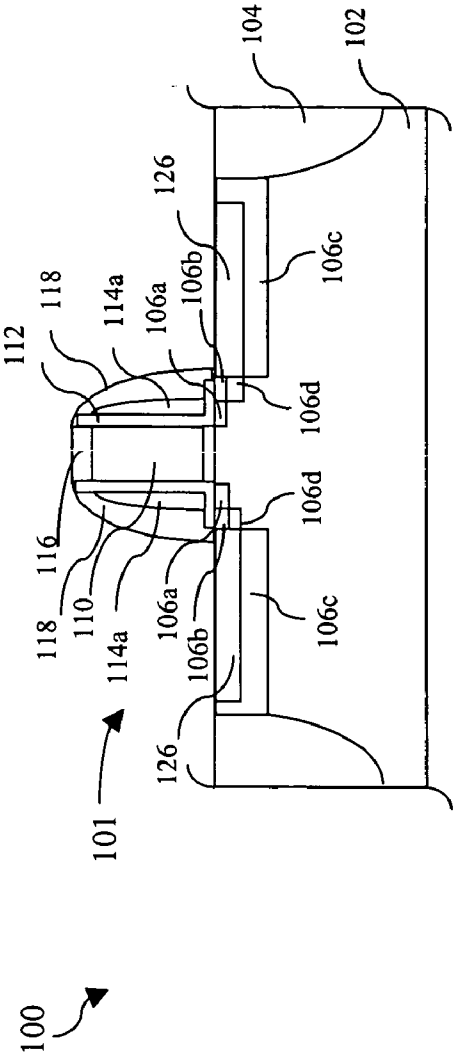

104
102
126
106b
106c
112
118
114a
106a
106d
116
118
110
114a
106a
106b
106d
106c
126
101
100

Fig. 7

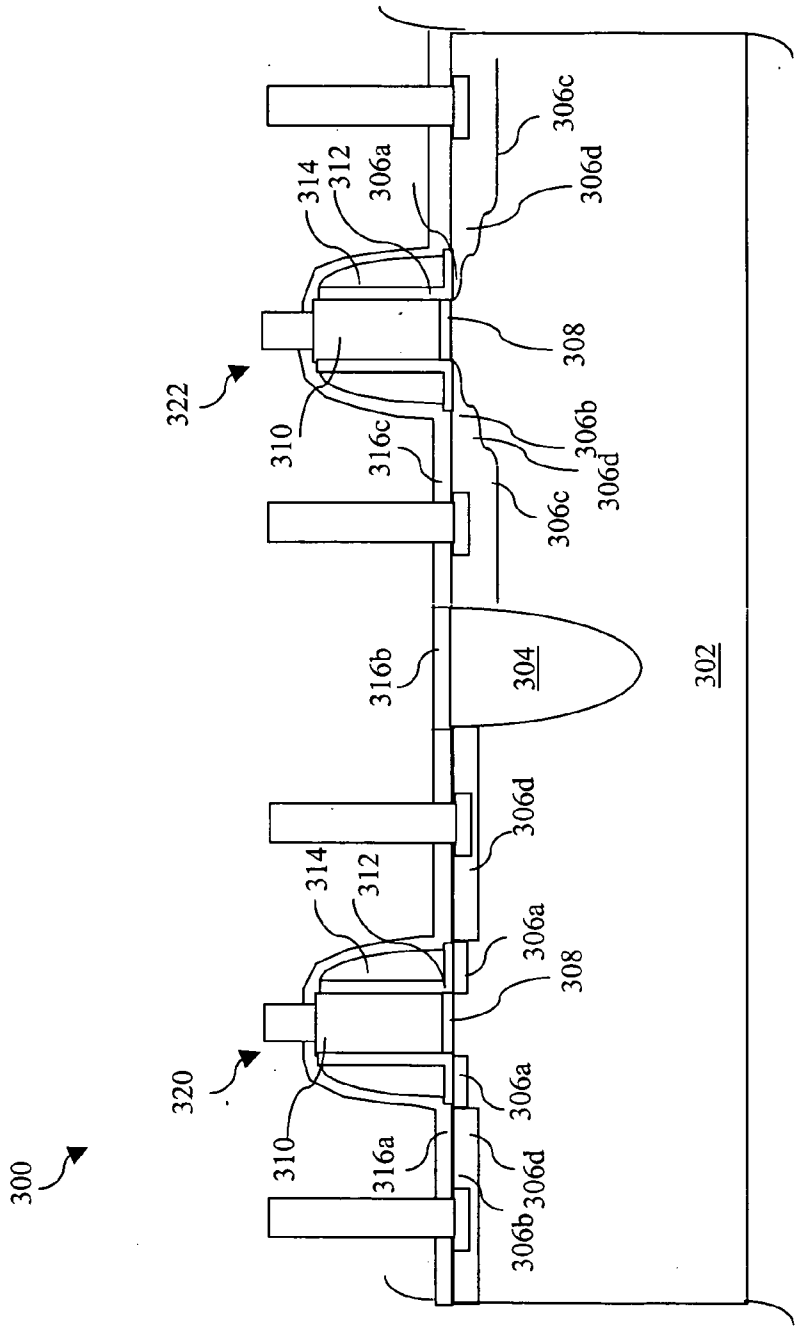

300
320
322
302
304
306a
306b
306c
306d
308
310
312
314
316a
316b
316c

Fig. 8

STRAINED SILICON DEVICE MANUFACTURING METHOD

CROSS-REFERENCE

[0001] This application is related to U.S. patent Ser. No. 10/810,950, filed Mar. 25, 2004, the disclosure of which is hereby incorporated by reference.

BACKGROUND

[0002] An integrated circuit (IC) is formed by creating one or more devices (e.g., circuit components) on a semiconductor substrate using a fabrication process. As fabrication processes and materials improve, semiconductor device geometries continue to decrease in size since such devices were first introduced several decades ago. For example, current fabrication processes are producing devices having geometry sizes (e.g., the smallest component (or line) that may be created using the process) of less than 90 nm. However, the reduction in size of device geometries frequently introduces new challenges that need to be overcome.

[0003] As microelectronic device geometries are scaled below 65 nm, electrical efficiency becomes an issue that impacts device performance. Microelectronic device performance such as current gain can be significantly affected by the configuration and materials incorporated into microelectronic devices. Therefore, there is an inherent conflict with the configuration and/or the materials used in many of today's microelectronic devices.

[0004] Accordingly, what is needed in the art is a microelectronic device and method of manufacture that addresses the above discussed issues.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0006] **FIG. 1** is a flowchart of one embodiment of a method for performing one or more embodiments of the present disclosure.

[0007] **FIGS. 2-7** are sectional views of a portion of a microelectronic device constructed according to the method of **FIG. 1**.

[0008] **FIG. 8** is a sectional view of one embodiment of a microelectronic integrated circuit constructed according to aspects of the present disclosure.

DETAILED DESCRIPTION

[0009] It is to be understood that the following disclosure provides many different embodiments, or examples, for implementing different features of the present invention. Specific components and arrangements are described below to simplify the present disclosure by way of example, and are not intended to be limiting. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed, nor does it dictate that the referenced component is identical to others with the same reference numeral. Moreover, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed interposing the first and second features, such that the first and second features may not be in direct contact.

[0010] Referring to **FIG. 1**, a method **10** can be used for manufacturing a microelectronic device according to one or more embodiments of the present invention. For the sake of example, the method **10** will be described with reference to the manufacture of a semiconductor integrated circuit **100**, illustrated in **FIGS. 2-8**. The manufacturing method **10** can be used for the formation of a "graded junction" source/drain doped region in a semiconductor microelectronic device such as a transistor. It is understood that the method **10** can represent only a portion of a process flow, and it is further understood that in some embodiments, certain steps of the method may be rearranged or not performed altogether.

[0011] Referring also to **FIG. 2**, in the present example, the method **10** begins at step **12** for creating a microelectronics device **101**. The device **101** includes a substrate **102**, isolation regions **104**, a gate layer **108**, an electrode **110**, and a hard mask **111**.

[0012] The substrate **102** may be a semiconductor substrate, such as one including silicon. The isolation regions **104** may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon carbide (SiC), low-k dielectric, and/or other materials. In one embodiment, the isolation regions **104** may be created by etching or otherwise forming a recess in the substrate **102** and subsequently filling with one or more layers of a dielectric.

[0013] The gate layer **108**, which may be gate oxide, is formed followed by the formation of the bulk gate electrode **110**, which may include a layer of polysilicon. In the present example, a hard mask layer **111** resides over the gate electrode **110**. The hard mask layer **111** is about 250 Angstroms in thickness (height, as shown in **FIG. 2**), and may include silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), photoresist, and/or other materials.

[0014] At step **14**, doped regions **106***a* are formed in the substrate **102**. In the present embodiment, the doped regions **106***a* are lightly doped drain/source (LDD) regions that are implanted relatively shallow into the substrate **102**. The LDD regions **106***a* can be created by CVD, PECVD, ALD, ion implantation, and/or other processing techniques. For example, the doped regions **106***a* may be formed by growing a sacrificial oxide on the substrate **102**, opening a pattern for the location of the doped regions **106***a* and then using a chained-implantation procedure. Alternatively, the doped regions **106***a* may be formed by selective epitaxial growth (SEG).

[0015] For the sake of example, the doped regions **106***a* include P-type impurities such as boron, boron fluoride, indium, and/or other materials. Formation of the P-type doped regions may include one or more diffusion, annealing, and/or electrical activation processes. A channel region **120**

is thereby formed between the two doped regions **106***a*. Continuing with the present example, the channel region **120** is a P-channel.

[**0016**] Liners **112** are then formed on the vertical (as illustrated in **FIG. 2**) sides of the gate electrode **110**. In the present embodiment, the liners **112** are L-shaped and include an oxide dielectric layer formed by CVD, PVD, ALD, PECVD, SEG, and/or other processing techniques. Spacers **114** are then formed on the sidewalls of the liners **112**. In the present embodiment, the spacers **114** are nitrogen based insulators, such as silicon nitride (Si_xN_y). In alternate embodiments, the spacers **114** may include silicon oxide (SiO_2), photoresist, and/or other polymers. In the present embodiment, the spacers **114** and the lower portion of the liners **112** are relatively wide, with a width s_1 of about 650 Angstroms.

[**0017**] Referring also to **FIG. 3**, at step **16** (of **FIG. 1**), silicon recesses **122** are formed on either side of the spacers **114**. In the present example, selected portions of the doped regions **106***a* are removed. The portions of the doped regions **106***a* located under the liners **112** and spacers **114** remain following the removal of the exposed portions of the doped regions **106***a*. The exposed portions of the doped regions **106***a* may be removed by silicon etch, chemical etch, plasma etch, or other appropriate method.

[**0018**] Referring also to **FIG. 4**, at step **18** (of **FIG. 1**), an epi layer **124** is formed in the recesses **122** of **FIG. 3** between the doped regions **106***a* and the isolation regions **104**. The epi layer **124** may include silicon germanium (SiGe). Other embodiments include silicon carbide (SiC), and/or other epi materials. It is noted that in the present embodiment, SiGe does not accumulate on the hard mask **111** or on the spacers **114**. The epi layer **124** is used to make the microelectronic device **101** a "strained silicon" device.

[**0019**] Referring also to **FIG. 5**, at step **20** (of **FIG. 1**), the spacers **114** are partially etched, forming "slim" spacers herein designated with the reference numeral **114***a*. The slim spacers **114***a* are shown having a width s_2, which is less than the width s_1 (**FIG. 2**). The width s_2 of the slim spacers **114***a* may be on the order of about 350 Angstroms. As a result, the lower portion of the liners **112** extend about 300 Angstroms (650−350=300 Angstroms) beyond the slim spacers **114***a*. The slim spacers **114***a* may be formed by chemical etch, dry etch, plasma etch, and/or other processing techniques. In one embodiment, the slim spacers **114***a* are formed by a wet etch of phosphoric acid (H_3PO_4).

[**0020**] The hard mask **111** is also removed, either at the same time that the slim spacers **114***a* are formed, or at a different time. The hard mask **111** may be removed by chemical etch, plasma etch, and/or other techniques. For example, the hard mask **111** may be removed by plasma etch, which may include an environment having reactants such as hydrochloric acid (HCl), hydrogen bromide (HBr), sulfur dioxide (SO_2), sulfur hexafluoride (SF_6), perfluorocarbons, and/or other gases.

[**0021**] Referring also to **FIG. 6**, at step **22** (of **FIG. 1**), the doped regions **106***b* are treated by a source drain implant **204**. The implant **204** may include ion implantation by conventional ion beam, plasma source ion immersion, plasma source ion implantation, and/or other processing techniques. In the present embodiment, the implant **204** may include P-type impurities. In other embodiments, the implant **204** may include impurities such as phosphorous, boron, antimony, arsenic, carbon, germanium, and/or other materials. In furtherance of the present example, the implant is heavier doped than the implant used to create the doped regions **106***a*. It is understood that different dopants and/or different dopant concentrations can be used, as desired. Alternatively, the implant **204** may utilize thermal diffusion and/or formation of the doped regions **106***c* by SEG, CVD, PVD, ALD, and/or other processing techniques.

[**0022**] The implant **204** is used to form a graded junction, which is illustrated by the creation of doped regions **106***a*, **106***b*, **106***c* and **106***d*. The doped region **106***b* is a combination of the prior process used to create doped region **106***a* and the implant **204**. If the prior process and the implant **204** use similar dopants, the doped region **106***b* can be comparatively heavier doped than the region **106***a*. If dissimilar dopants are used, the doped region **106***b* can have a unique combination from the two process steps.

[**0023**] The doped region **106***d*, in the present example, is deeper than the previous doped region **106***a* of **FIG. 5**. In one embodiment, the implant **204** uses similar dopants of the prior process used to create doped region **106***a*. In this embodiment, the doped region **106***d* provides a deeper grading affect. It is understood that although the grading effect is shown as a stair step in **FIG. 6**, in actuality the grading effect may be more gradual, or smoothed, as shown in **FIG. 8**.

[**0024**] The doped region **106***c* is created by the implant **204** on the epi layer **124**. In the present example, the SiGe layer **124** allows the implant **204** to go deeper than that of the doped region **106***d*. Furthermore, the resulting properties of the implant **204** on the SiGe layer **124** may be different than those on the Si substrate **102** used for the doped region **102***d*. It is understood that in some embodiments, a portion of the implant **204** may extend beyond the epi layer **124** and further into the substrate **102**, or in the alternative, may not completely diffuse into the epi layer. It is further understood that although the grading effect is shown as a stair step in **FIG. 6**, in actuality the grading effect may be more gradual, or smoothed, as shown in **FIG. 8**.

[**0025**] Referring also to **FIG. 7**, at step **24** (of **FIG. 1**) connections are provided to the gate, source, and drain of the transistor device **101**, and a clamping layer **118** is formed. In the present embodiment, the connections are made through a gate contact **116** and source/drain contacts **126**. The gate contact **116** may include a metal silicide such as cobalt silicide ($CoSi_x$), molybdenum silicide ($MoSi_x$), nickel silicide ($NiSi_x$), titanium silicide ($TiSi_x$), and/or other materials. The gate contact **116** may be formed by lithography, chemical etch, plasma etch, CVD, PECVD, ALD, PVD, and/or other processing techniques. Similarly, the source/drain contacts **126** may be include silicide formed in and/or over the doped region **106***c*. The formation of the gate contact **116** and/or source/drain contacts **126** may also include an anneal process step.

[**0026**] The clamping layer **118** or "contact etch stop layer (CES)" may include openings positioned for the gate contact **116**. The clamping layer **118** may include silicon nitride (Si_xN_y), silicon dioxide (SiO_2), silicon oxy-nitride (SiON), silicon oxy-carbide (SiOC), silicon carbide (SiC), and/or other materials. In some embodiments, the clamping layer

118 may be located over the doped regions **106***b* and **106***c* and include openings positioned for the source/drain contacts **126**.

[**0027**] The clamping layer **118** may also provide tensile stress and/or compressive stress which may influence the crystalline stress of the channel region **120**. The tensile stress of the clamping layer **118** may be controlled by the process parameters during the formation of the clamping layer **118**. Compressive stress may be induced into the clamping layer **118** and may also be controlled by the process parameters. In one embodiment, the clamping layer **118** compressive and/or tensile stress may also be adjusted by temperature, process gas flows, nitrogen content, and/or other process related parameters.

[**0028**] Upon completion of step **24** (of **FIG. 1**), subsequent processing may be performed to form other features located over the gate contact **116** and the doped regions **106***c,* which may include the formation of a metal silicide, a barrier layer such as tantalum nitride (TaN) or silicon oxy-carbide (SiOC), interconnects having copper (Cu) or aluminum (Al), low-k dielectric layers, and or other layers. In one embodiment, the microelectronic device **101** may be annealed thereby forming the "graded junction" between the doped regions **106***b,* **106***a,* and **106***c* (similar to that shown in **FIG. 8**). The anneal may provide a smooth transition between the impurities of the doped regions **106***b,* **106***a,* and **106***c.*

[**0029**] Referring to **FIG. 8**, in another embodiment, a complementary microelectronic circuit **300** (also referred to as complementary metal oxide semiconductor (CMOS) circuit) includes a substrate **302**, an isolation region **304**, microelectronic devices **320** and **322**, and clamping layers **316***a,* **316***b,* and **316***c.* The CMOS circuit **300** can by created, in part, by using one or more steps of the method **10** of **FIG. 1**. It is understood that other steps and/or layers may be created as needed, such is as well known to those of ordinary skill in the art.

[**0030**] The substrate **302** may include one or more of silicon, gallium arsenide, gallium nitride, strained silicon, silicon germanium, silicon carbide, carbide, diamond, and/or other materials. The substrate **102** may also include a silicon-on-insulator (SOI) substrate, such as a silicon-on-sapphire substrate, a silicon germanium-on-insulator substrate, or another substrate including an epitaxial semiconductor layer on an insulator layer. The substrate **302** may further include a fully depleted SOI substrate wherein the device active silicon thickness may range between about 200 nm and about 5 nm in one embodiment. In another embodiment, the substrate **302** may include an air gap to provide insulation for the microelectronic device **300**. For example, a "silicon-on-nothing" (SON) structure may be employed wherein the microelectronic device **300** includes a thin insulation layer formed by air and/or other insulator.

[**0031**] The isolation regions **304** may include shallow trench isolation (STI), local oxidation of silicon (LOCOS), and/or other electrical isolation features. The isolation regions **104** may include silicon dioxide (SiO_2), silicon nitride (Si_xN_y), silicon carbide (SiC), low-k dielectric, and/or other materials. In one embodiment, the isolation region(s) **104** may by etching or otherwise forming a recess in the substrate **302** and subsequently filling with one or more layers of a dielectric.

[**0032**] The microelectronic device devices **320**, **322** may also include one or more layers or other features contemplated by the microelectronic circuit **300** within the scope of the present disclosure, and may be formed by immersion photolithography, maskless lithography, imprint lithography, SEG, CVD, PVD, PECVD, ALD, Langmuir-Blodgett (LB) molecular assembly, chemical mechanical polishing or chemical mechanical planarization (hereafter referred to as CMP), and/or other processing techniques. Conventional and/or future-developed lithographic, etching and/or other processes may be employed to form the microelectronic device **100**.

[**0033**] The microelectronic devices **320** and/or **322** may include an N-type metal oxide semiconductor (NMOS) device and/or P-type metal oxide semiconductor (PMOS) device, respectively. The microelectronic devices **320** and **322** may include portions substantially similar to the discussions above with respect to the microelectronic device **100**. For example, gate layer **308**, liners **312**, spacers **314**, and bulk gate electrode **310** may be substantially similar in composition to the gate layer **108**, liners **112**, spacers **114***a,* and the bulk gate electrode **110** discussed above.

[**0034**] In the present example, the device **322** was formed using an epi layer at the source/drain region, as is discussed above with reference to **FIGS. 4-6**. In contrast, the device **320** was not formed using an epi layer as described above. As a result, the device **322** includes a three-step graded formation of the dopant regions **306***a,* **306***b,* **306***c,* and **306***d,* while the device **320** includes a two-step graded formation of the dopant regions **306***a,* **306***b,* and **306***d.* It is understood that since the devices **320**, **322** are not of the same type, different dopants can be used to form the layers **306***a*-**306***d,* such selection of dopants being well understood by those of ordinary skill in the art.

[**0035**] It is generally understood that different embodiments will see different benefits. For example, in some embodiments, a significant current gain will be observed over prior art devices, as well as a lower junction capacitance. Some prior art devices can only provide higher drive current with a higher junction capacitance. This improvement can occur, in some embodiments, without a significant change in threshold voltage.

[**0036**] The foregoing has outlined features of several embodiments according to aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. For example, there are many know ways to form a layer or structure, including deposition, diffusion, implantation, etching, growing, and so forth. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A method of manufacturing a microelectronic device, comprising:

forming a gate upon a substrate;

forming an epi layer on the substrate proximate to the gate;

forming a slim spacer proximate to the gate; and

forming a source/drain region in the substrate, including in the epi layer.

2. The method of claim 1 further comprising:

forming a hard mask on a top surface of the gate prior to forming the epi layer; and

removing the hard mask from the top surface of the gate after forming the epi layer.

3. The method of claim 1 further comprising:

forming a thick spacer on a side surface of the gate prior to forming the epi layer.

4. The method of claim 3 wherein the step of forming the slim spacer includes etching the thick spacer after forming the epi layer.

5. The method of claim 3 wherein the step of forming the slim spacer includes etching the thick spacer after forming the epi layer and prior to forming the source/drain region.

6. The method of claim 5 further comprising:

forming a clamping layer located substantially over the spacers and the substrate.

7. The method of claim 3 further comprising:

implanting a first dopant prior to forming the thick spacer.

8. The method of claim 3 further comprising:

forming an oxide liner prior to forming the thick spacer; and

leaving the oxide liner approximately the same width when forming the slim spacer.

9. The method of claim 1 wherein the device is a p-channel transistor and the epi layer is SiGe or Si.

10. The method of claim 1 wherein the slim spacer has a thickness less than 500 Angstroms.

11. A microelectronic device comprising:

a gate structure overlying a semiconductor substrate and for selectively operating a strained p-channel in the semiconductor substrate;

source and drain regions, each comprising:

a first doped region located adjacent to the channel and extending a first depth into the semiconductor substrate,

a second doped region located adjacent to the first doped region and extending a second depth into the semiconductor substrate greater than the first depth, and

a third doped region located adjacent to the second doped region and extending a third depth into the semiconductor substrate greater than the second depth.

12. The device of claim 11 wherein the source and drain regions are annealed following the formation of the third doped regions.

13. The device of claim 11 wherein the third doped region includes a SiGe doped portion.

14. The device of claim 11 wherein the gate structure includes a silicide contact.

15. The device of claim 11 further comprising:

a clamping layer surrounding at least a portion of the gate structure.

16. The device of claim 11 wherein the first regions are lightly doped source/drain regions.

17. The device of claim 11 further comprising:

an L-shaped liner having a first portion abutting a sidewall of the gate structure and a second portion extending over the second doped region.

18. The device of claim 17 further comprising a relatively thin spacer extending over the first doped region.

19. The device of claim 18 wherein the relatively thin spacer has a width of about 350 Angstroms and wherein the second doped region has a width of 300 Angstroms extending from an outer edge of the relatively thin spacer.

20. A method of forming a p-channel transistor on a silicon substrate, comprising:

forming a poly gate structure over the substrate;

forming a lightly doped source/drain region in the substrate;

forming an oxide liner adjacent to opposing side walls of the poly gate structure;

etching a recess in the semiconductor substrate on opposing sides of the oxide liner;

forming raised SiGe source/drain regions on either side of the oxide liner;

forming a slim spacer over the oxide liner;

implanting a source/drain dopant into the substrate including the SiGe regions; and

providing a silicide region in the implanted SiGe regions.

21. The method of claim 20 further comprising:

forming a hard mask over the poly gate structure prior to forming the raised SiGe source/drain regions; and

removing the hard mask after the raised SiGe regions are formed;

22. The method of claim 21 wherein the hard mask is about 250 Angstroms in thickness.

23. The method of claim 20 wherein the implanted SiGe regions are deeper than an implanted region of the substrate that is between the slim spacer and the SiGe regions, and wherein the implanted SiGe regions are deeper than the lightly doped source/drain regions under the slim spacer

24. The method of claim 20 further comprising:

forming a nitride spacer over the oxide liner; and

wherein the slim spacer is formed by etching the nitride spacer.

25. The method of claim 24 wherein the nitride spacer is about 650 Angstroms in width.

26. The method of claim 20 wherein the slim spacer is about 350 Angstroms in width.

27. The method of claim 20 wherein the oxide liner is about 650 Angstroms in width.

28. The method of claim 20 further comprising:

forming a clamping layer over the transistor.

* * * * *