United States Patent

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[73] Assignee **General Electric Company**

[54] **FLUERIC LAG-LEAD CIRCUIT**
7 Claims, 7 Drawing Figs.

[52] **U.S. Cl.** **137/81.5**
[51] **Int. Cl.** **F15c 1/14**
[50] **Field of Search** ..... 137/81.5; 235/201 (m.e., p.f.,sens.,gen.), 200 (gen.,anal.,etc.)

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ABSTRACT: A push-pull flueric lag-lead circuit is disclosed which incorporates a fluid amplifier in its forward loop and a pair of positive feedback paths from the output of the fluid amplifier to the control port. The positive feedback path comprises a pair of flow resistances in series with each other and with a volume which provides a capacitance to ground.

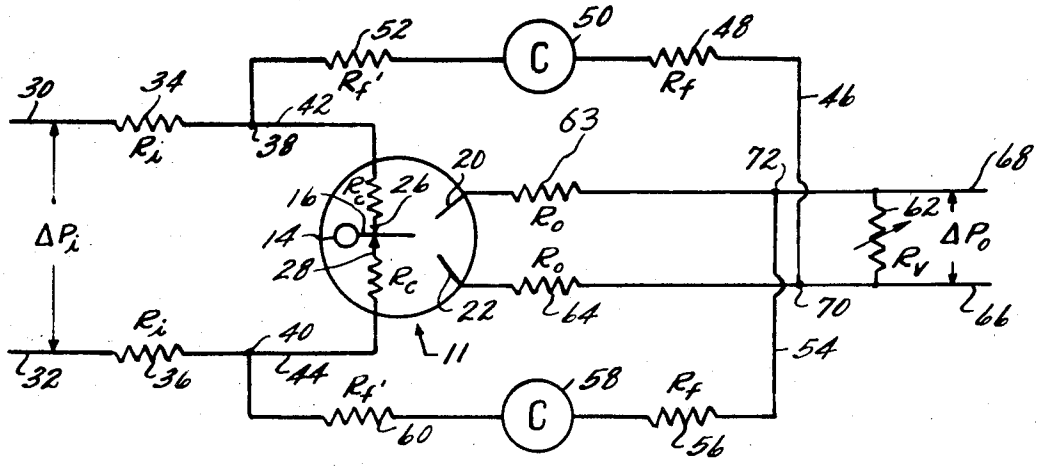

Fig 1

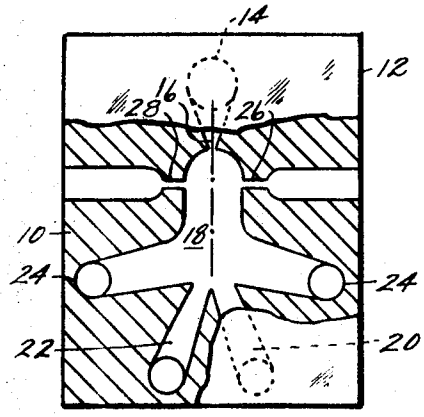

Fig 2

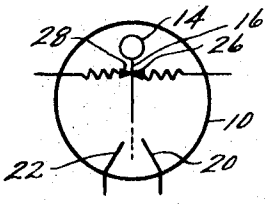

Fig 3

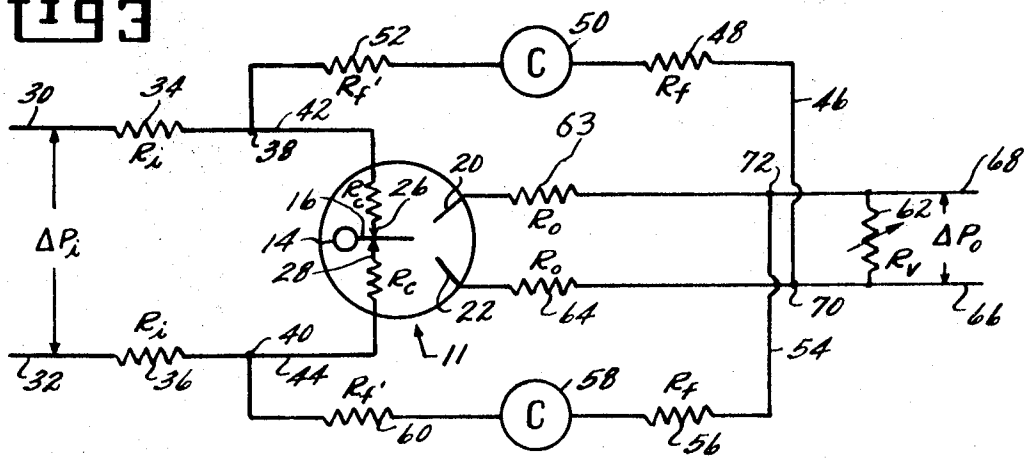

Fig 4

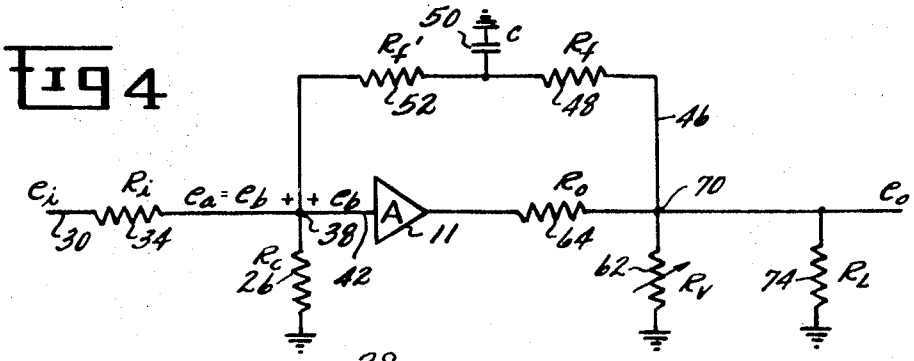

Fig 5

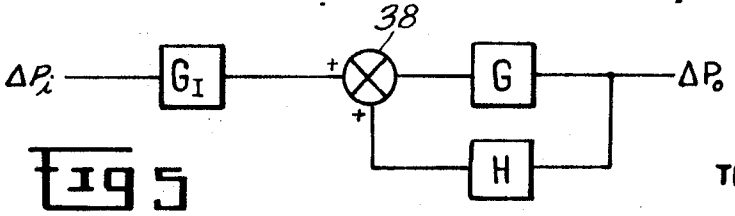

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FIG 6

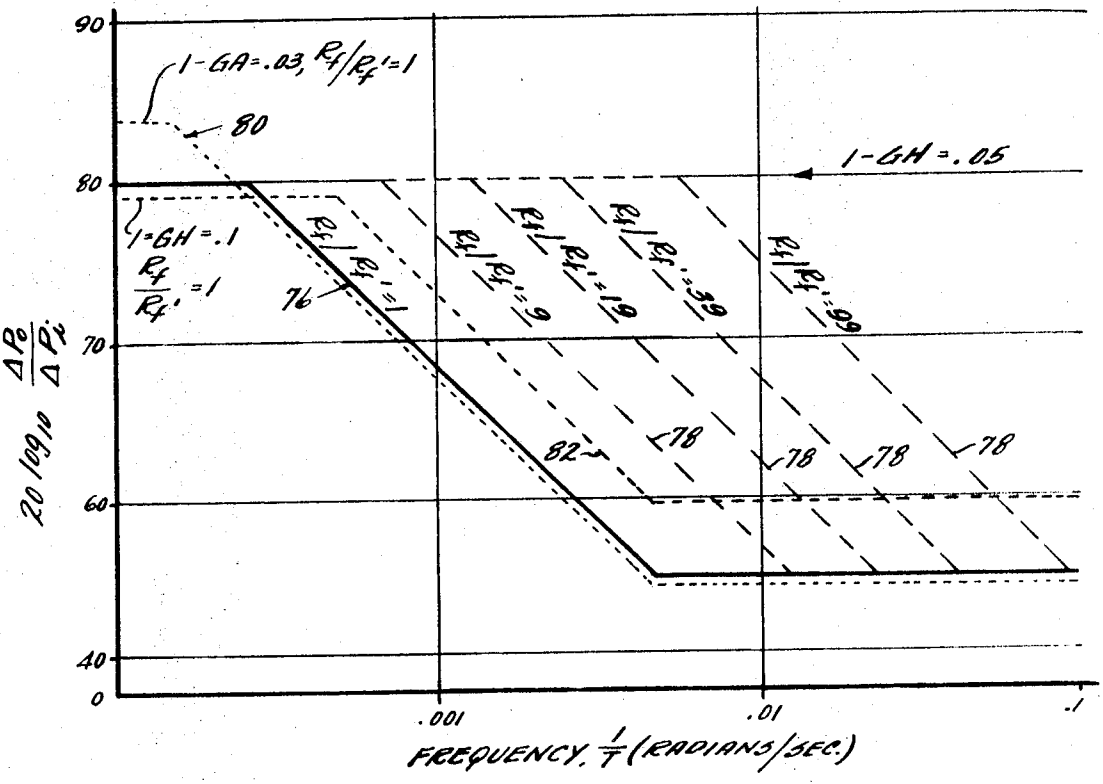
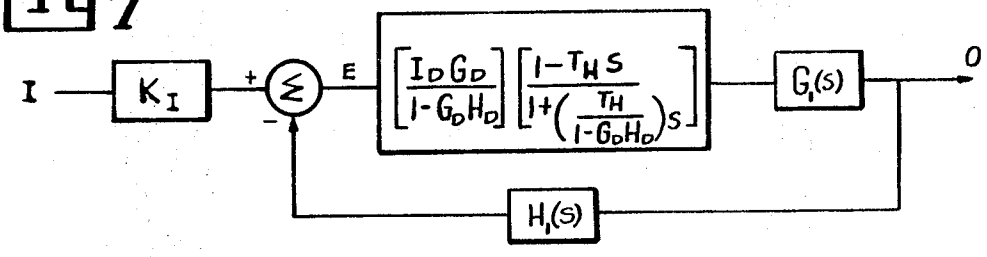


FIG 7



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FLUERIC LAG-LEAD CIRCUIT

BACKGROUND OF THE INVENTION

This invention relates to servomechanism systems and more particularly to a flueric lag-lead network for incorporation in such systems.

In synthesizing servomechanism designs it is often necessary to provide dynamic compensation means in a closed loop control system to render it stable, allow higher control amplification factors while maintaining stability, or provide a desired time response characteristic to a varying control input. One such compensating network is the lag-lead circuit which, when placed in series with the controlled system and its control elements, will insert into the overall system a lead time constant and a somewhat longer lag time constant. If the controlled system contains a lag having a long time constant, the compensating lag-lead usually must have an even longer lag time constant. Inasmuch as the time constant is defined by the product of a resistance and capacitance it is readily apparent that a trade off exists between the two. If the time constant generating resistance is in a series path with the input, which is a common prior art practice, the choices available are to (1) use a large series resistance with a practical size volume or capacitance which concommitantly results in a sacrifice of forward gain of the overall control loop, or (2) size the resistance to maintain the loop gain and use an exceedingly large volume to provide the capacitance required to generate a large lag time constant.

A further problem which can arise when a series means for generating the lag-lead function is used and the series resistance of the function generator is maintained at a relatively low level is that the lag-lead circuit can affect the characteristic of the control device which drives it. One method of minimizing the secondary effect on the driving device is to place a resistor between the output of the driver and the input to the lag-lead circuit to effectively isolate the two from each other. However, if this is done with a lag-lead circuit in which the time constant is generated in the forward path, an added detriment to the forward gain of the control loop results.

OBJECTS OF THE INVENTION

In view of the foregoing problems associated with providing a lag-lead function in the forward path of a control loop, it is an object of this invention to provide a lag-lead circuit which can generate long lag time constants without a corresponding detriment to the overall forward gain of the control system.

A further object of this invention is to provide a lag-lead circuit in which the circuit dynamics can be isolated from the input thereto without adversely affecting the forward gain of the overall control loop in which the circuit is incorporated.

BRIEF SUMMARY OF THE INVENTION

Briefly stated, the invention is a lag-lead circuit comprising an operational amplifier having input and output means connected thereto and positive feedback means connecting the output means to the input means, the feedback means comprising at least two feedback resistors connected in series and a grounded capacitor connected to a point intermediate the two resistors.

DESCRIPTION OF THE DRAWING

While the specification concludes with claims particularly pointing out and distinctly claiming the subject matter of this invention, the invention will be more readily understood by reference to the discussion below and the accompanying drawing in which:

FIG. 1 is a partially fragmented section view of a typical fluid amplifier;

FIG. 2 is a schematic representation of the amplifier shown in FIG. 1;

FIG. 3 is a schematic drawing of the flueric lag-lead circuit of this invention;

FIG. 4 is an electrical schematic showing the electrical analog of the flueric circuit of FIG. 3;

FIG. 5 is a functional block diagram of the circuits shown in FIGS. 3 and 4;

FIG. 6 is a diagram showing the attenuation versus frequency characteristics of the lag-lead circuit of this invention; and

FIG. 7 is a functional block diagram of a process or apparatus control system in which the flueric lag-lead circuit of this invention is incorporated.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring first to FIG. 1, a typical single stage fluid amplifier is shown which can be constructed in a well-known manner. The amplifier comprises a base member **10** in which are formed the several passageways and cavities described below and a cover member **12** which is secured to base member **10** by adhesives, screws or other means so as to enclose the passageways and cavities in base member **10** and seal them from each other. Base member **10** includes an inlet port **14** for supplying pressurized motive fluid, a power nozzle **16**, an interaction chamber **18** at the discharge of power nozzle **16**, control ports **26** and **28** disposed slightly downstream of power nozzle **16** and oppositely directed toward the power nozzle centerline, vent ports **24**, and receivers **20** and **22**. Thus, absent a signal pressure differential across control ports **26, 28** a stream of fluid discharged from power nozzle **16** will be recovered in equal proportions by receivers **20, 22**. If, however, a differential pressure exists between ports **26** and **28**, the power stream will be deflected so as to provide a larger pressure recovery in one of ports **20, 22** than in the other of the ports, the pressure differential between the receivers **20, 22** being proportional to the pressure differential between the control ports **26** and **28**. In this way, a small pressure differential between the control ports **26** and **28** may be amplified into a larger differential pressure between receivers **20** and **22**. Devices such as that shown in FIG. **1** may be used alone for such amplification or may be staged in series relationship wherein the pressure differential between the receivers **20, 22** of one stage provides the input to the control ports **26, 28** of a succeeding stage.

FIG. **2** is a schematic illustration of the fluid amplifier shown in FIG. **1**. The elements of the schematic illustration are numbered to correspond to the same physical elements shown in FIG. **1**. In FIG. **2** the control ports **26** and **28** are shown as resistors to represent the flow resistance of the actual physical control ports, the reason for which will become obvious from the discussion below.

FIG. **3** illustrates the flueric lag-lead circuit of this invention which incorporates the fluid amplifier **11** described above. (Although only a single stage of fluid amplification is shown in FIG. **3**, the amplifier portion of the lag-lead circuit could comprise a multistage gain block which is constructed by cascading several amplifiers **11** as described above). The circuit additionally comprises input resistors **34** and **36** which are interposed in input conduits **30** and **32**, summing junctions **38** and **40** which combine the input fluid flows with the feedback fluid flows from conduits **46** and **54**, conduits **42** and **44** which pass the combined input and feedback fluid flows to the control ports **26** and **28** of fluid amplifier **11**, output conduits **66** and **68** which are connected to receivers **20** and **22** of fluid amplifier **11**, feedback conduits **46** and **54** which were mentioned above, feedback resistors **48** and **52** interposed in conduit **46** and feedback resistors **56** and **60** interposed in conduit **54**, capacitances or volumes **50** and **58** interposed in conduit **46** between resistors **48** and **52** and interposed in conduit **54** between resistors **56** and **60** (an equivalent capacitance connection is a deadheaded volume connected by a conduit to a point intermediate resistors **56** and **60**), and a trimming resistor **62** which connects output conduit **68** with output conduit **66**. Also shown schematically are resistors **63** and **64**, which represent the fluid flow resistance of receivers **20** and **22**.

Resistors **34, 36, 48, 52, 56,** and **60** are preferably laminar flow resistors which have a very nearly linear pressure drop versus flow characteristic, and may each consist of a long thin passageway such as a capillary tube or a small cross section rectangular passage through a block of material such as plastic or metal. However, orifice-type resistors may also be used.

Resistors **34, 36** are sized to have a value dependent upon several factors, among which are the degree to which it is desired to isolate the output of the device which drives the lag-lead circuit from the dynamics of the circuit itself and the steady stage gain desired.

Resistors **48, 56** are sized to have equal resistances which are somewhat large compared to the resistance R_c of control ports **26, 28** and the resistance R_o of the resistors designated **63, 64**. Thus the positive feedback to the control ports, which is apparent from the connection of conduit **46** to output conduit **66** at its one end and to control port **26** via conduit **42** at its other end and the similar connection of conduit **54**, is limited to a smaller quantity than that of the input fluid flow through conduits **30, 32** and the output fluid flow through conduits **66, 68**. Resistors **52, 60** have resistance values R_f' which are equal to each other and may be larger or smaller than the resistance R_f of resistors **48** and **56**. Capacitors **50, 58** have equal capacitances C and can be constructed merely by providing substantial cross-sectional enlargement in conduits **46, 54**.

Resistance R_r of variable resistor **62** may be provided, for example, by a parallel group of laminar flow fixed resistors and means for selectively including or excluding any group or several of these resistors in the parallel circuit. The range of resistance for variable resistor **62** is chosen so that the lag-lead circuit may be matched within limits to the impedance of the load connected to output conduits **66, 68**. Considerations required for such matching are developed below.

Operation of the invention can be understood by reverence to FIGS. **4—6**. Referring first to FIG. **4**, the analogous electrical circuit for one side of the FIG. **3** flueric circuit is shown (the FIG. **3** circuit is a push-pull arrangement and can be analyzed by analysis of only one side). In FIG. **4** the elements (resistances, capacitances, summing points, and leads) are numbered to correspond to their FIG. **3** analogs, and FIG. **4** additionally includes a resistor **74** (denoted R_L) to represent the output load on the circuit.

The FIG. **4** circuit may be defined functionally by the schematic diagram shown in FIG. **5** wherein the summing point shown corresponds to summing point **38** and wherein G_f, G and H are defined by

$G_f=e_a$

$G=e_o/e_b$

$H=e_a/e_0$

$e_a=e_b$,

or, obtaining the Laplace transform of the parameters to place them in operational form;

$G_1(S)=E_a(S)/E_i(S)$

$G(S)=E_o(S)/E_b(S)$

$H(S)=E_a(S)/E_o(S)$

The term H(S) may be expressed as the product of a steady state term and a transient term wherein the steady state term is the DC gain of the element and the transient term takes the form $(1+T_1S)/(1+T_2S)$.

Referring again to FIG. **4**, each of the terms G_1, G, and H can be derived by considering the impedance to ground for each of input signal e_i, error signal e_b, and output signal e_o. The path to ground for e_i is through resistor **34** and then through the parallel paths comprising resistor **26** on one side and resistors **48, 52** and capacitor **50** on the other side [point **70** is considered ground with respect to e_i for purposes of analysis inasmuch as R_o which leads back to interaction chamber **18** (see FIG. **1**) and resistance R_L are in a real fluidic system much smaller than series resistance R_f]. By parity of reasoning, the path to ground for e_b comprises amplifier **11**, fluid amplifier output resistance R_o (resistor **64**) and the parallel path comprising resistances R_L and R_r on one side and the feedback path comprising resistances R_f, R_f', and capacitance C on the other side. Similarly the path to ground for e_o comprises resistances R_o, R_r, and R_L in parallel with each other and with the feedback path comprising resistances R_f, R_f' and capacitance C. Considering for the present that the path provided by resistor **62** (resistance R_r) is open circuited (the function and effect of resistor **62** is explained later herein), expressions for G_f, G, and H can thus be derived wherein,

(1) $$G_1(S)=\left[\frac{1}{1+\frac{R_i}{R_c}+\frac{R_i}{R_f+R_{f'}}}\right],$$

(2) $$G(S)=\frac{A}{1+\frac{R_o}{R_f+R_{f'}}+\frac{R_o}{R_L}},$$

(3) $$H(s)=\left[\frac{1}{1+\frac{(R_f+R_f')(R_i+R_c)}{R_iR_c}}\right]\left[\frac{1}{1+T_HS}\right],$$

(4) $$T_H\cong\frac{R_f'}{R_f+R_f'}(R_fC),$$

Equation (4) assumes a real flueric system wherein $R_f+R_f' \gg R_c$ or R_L or R_0.

Referring again to FIG. **5**, wherein the terms ΔPo, ΔPi, are substituted for their electrical analogs Eo(S), Ei(S), $\Delta Po/\Delta Pi$ is determined to have the relation,

$$\frac{\Delta P_o}{\Delta P_i}=\frac{I(S)G(S)}{1-G(S)H(S)}$$

which, by dividing each of the terms into its steady state factors I_D, G_D, H_D and transient factors I_r, G_r, H_r can be reduced to,

(5) $$\frac{\Delta P_o}{\Delta P_i}=\left[\frac{I_DG_D}{1-G_DH_D}\right]\left[\frac{1+T_HS}{1+\left(\frac{T_H}{1-G_DH_D}\right)S}\right]$$

which contains lead and lag terms whose time constants depend on the relationships described by equation (4) above.

To illustrate the effect of different R_f:R_f' ratios and GH factors, values of resistance and capacitance which represent real flueric devices are listed below.

$$R_c=2\frac{\#\ \text{Sec}}{\text{in.}^5}$$

$$R_i=2\frac{\#\ \text{Sec}}{\text{in.}^5}$$

$$R_f+R_f'=1{,}000\frac{\#\ \text{Sec}}{\text{in.}^5}$$

$$R_L=2\frac{\#\ \text{Sec}}{\text{in.}^5}$$

$$C=.8\frac{\text{in.}^5}{\#}$$

Using these values, the Bode plot of FIG. **6** can be constructed wherein the ordinate is frequency (the inverse of the time constant) and the abscissa is $\Delta P_o/\Delta P_i$ in decibels

$$\left(1\ \text{db}=20\ \log_{10}\frac{\Delta P_o}{\Delta P_i}\right).$$

The solid frequency response or attenuation line **76** represents the case where R_f/R_f' and 1—GH=0.05, attenuation curves shown by line **78**, represent cases $R_f/R_f'>1$ and 1—GH=0.05, and the attenuation curves shown by lines **80, 82** represent cases where $R_f/R_f'=1$ and 1—GH=0.03 and 0.1 respectively. From FIG. **6** it can be seen that for a given circuit frequency at which the respective lag and lead breaks occur can be varied by varying the ratio between R_f and R_f', and the frequency spread between the lag and lead break and be varied by varying the GH factor. Referring to equation (2) above, the GH factor can be varied by varying the amplification factor A, as by varying the number of fluid amplifier stages and/or inserting additional resistances in series with resistors **62, 64**.

FIG. 7 is included to illustrate use of the invention and facilitate explanation of its several advantages. It is a schematic representation of a feedback system for controlling a process or machine. The letter I denotes an input representing the desired value of a controlled variable, letter O denotes the controlled variable, and E denotes the signal representative of the error in the controlled variable. The block labeled $G_1(S)$ represents the transfer function of the control hardware and response of the controlled system to corrective action and includes both steady state and transient terms, and the block containing the defined transfer function represents the lag-lead circuit of this invention. An input steady stage gain labeled K_I and a feedback gain $H_1(S)$ are also included.

The system to be controlled may have a characteristic such that the product $[G_1(S)]$ $[H_1(S)]$ contains transient terms which will make it necessary to provide a compensating circuit to render closed loop control of the system stable at useful low frequency forward gains. In many situations a lag-lead network such as that described and claimed herein can provide the necessary compensation in series with the remainder of the system. Also, the lead-lag is utilized to increase the low frequency open loop gain, thus greatly improving the closed loop steady stage accuracy. If the controlled system contains a lag having a long time constant, the compensating lag-lead circuit usually has an even longer lag time constant. Inasmuch as the time constant is defined by the product of a resistance and a capacitance it is readily apparent that a tradeoff exists between the two. If the time constant generating resistance is in a series path with the input, the choices available are to (1) use a large series resistance with a practical size volume or capacitance, which concommitantly results in a sacrifice of forward gain in the control loop, or (2) size the resistance to maintain an acceptable loop gain and use an exceedingly large volume to provide the capacitance required to generate a large lag time constant. Applicant's invention avoids this tradeoff by generating the time constant in a positive feedback path where a large resistance can be used without reducing the steady state gain of the loop in which the lag-lead circuit is inserted and thus allows use of a reasonably sized volume for a capacitor. Analysis has shown that for comparable types and numbers of components, equivalent circuit impedances, the same time constants and ratios between the lead and lag time constants, Applicant's invention offers a 4800:1 capacitance volume advantage. Additionally, as can be seen by reference to equation (5) above, Applicant's circuit can amplify its input signal while providing a very large time constant by means of varying factors G_DH_D and I_D (see equations 1—3 above).

Additional advantage to Applicant's circuit is derived from the amplification of the input signal according to the term $I_DG_D/1\text{a}\text{E}G_DH_D$. As can be seen equation (1) above, I_D is an inverse function of R_i, the resistance of the input resistors **34, 36**. The designer therefore has the option of increasing R_i at the expense of I_D, and thus at the expense of the gain $I_DG_D/1-G_DH_D$ of the lag-lead circuit, to more effectively isolate the device which drives the lag-lead circuit from the dynamics of the lag-lead circuit and from the lag-lead circuit's positive feedback path. This technique of course requires some sacrifice in gain of the circuit; however, if the sacrifice is detrimental to overall system performance it can be compensated for by adjusting the gain K_I of FIG. 7 or manipulation of the $1-G_DH_D$ factor where system dynamics permit. For equivalent closed loop lag-lead circuit gains and circuit time constants by other known lag-lead methods, the invention offers a 100:1 increase in input resistance R_i.

Referring back to equation (2), the purpose and effect of variable resistor **62** will now be developed. In equation (2), the term R_o/R_f+R_f' is small compared to unity because in a real system R_f is made considerably larger than R_o. Thus equation (2) approximates

$$G(S)=\frac{A}{1+\frac{R_o}{R_L}} \tag{6}$$

Depending upon the load experienced by the lag-lead circuit of FIG. 3, the term R_o/R_L may have a value much smaller than unity, which results in a value of G(S) which approaches A. R_o/R_L could also have a value equal to or larger than unity, which results in G(S) having a value substantially less than A. As can be seen by reference to equation (5) negative time constant, $T_H/1-G_DH_D$ could result if the circuit is applied to a load which differs very much from the load for which it was designed, resulting in unstable operation of the overall control loop depicted by FIG. 7. Because in practice it is not always possible to accurately predict the load impedance on a circuit, or one may want to use the circuit with a load for which it was not designed, it is desirable to provide means of matching the circuit thereto.

When equation (6) is amended to include the effect of resistor **62**, it approximates

$$G(S)=\frac{A}{1+\frac{R_o}{R_L}+\frac{R_o}{R_V}}$$

The circuit can thus be designed to operate with R_o/R_L at a particular value which represents a safe underestimate of load resistance R_L, and if R_L proves to be higher than estimated, the value of G(S) can be tuned to the load by reducing R_V, thereby increasing R_o/R_V, to a value sufficient to correct for the error in estimating R_L and maintaining operation of the overall control loop at the design value for G(S). Thus, only simple adjustment or tuning is required.

I claim:

1. A lag-lead circuit comprising:

an operational amplifier, said amplifier having inherent internal impedance reflect at its input connection;

input means connected to the amplifier input connection;

output means connected to the output of said amplifier; and

positive feedback means connecting said output means to said input means, said feedback means comprising a grounded capacitor whose ungrounded terminal is connected to said output means through a first resistor and to said input means through a second resistor, said second resistor having a resistance larger than said amplifier internal impedance and thereby isolating the said capacitor from both said input means and said input connection to provide a circuit having both lag and lead terms.

2. The circuit recited in claim **1** wherein;

said operational amplifier comprises fluid amplifier means having at least one stage of amplification, said internal impedance comprising the resistance to fluid flow of the control ports of the first stage of amplification, said input connection comprising a connection to said control ports;

said input means comprise a pair of input conduits, each of which is connected to a said input connection and is adapted for connection to an external fluid source;

said output means comprise a pair of conduits; each of which is connected to an output receiver of said fluid amplifier means and is adapted for connection to an external load device; and

said feedback means comprises a feedback conduit connecting each said output conduit with its corresponding input conduit to provide a positive feedback, each said feedback conduit including a said first and second resistor and a said grounded capacitor connected to a point intermediate said first and second resistors.

3. The circuit recited in claim **2** wherein said capacitor to ground comprises a deadheaded volume and a conduit connecting said volume to said feedback conduit at a point intermediate said resistors, each said capacitor having the same capacitance.

4. The circuit recited in claim **2** wherein each said capacitor comprises a volume interposed in each feedback conduit between said resistors.

5. The circuit recited in claim **4** wherein said input means includes a fluid input resistor interposed in each said input conduit upstream of the connection between said input conduit and said feedback conduit, the resistors having equal flow resistances.

6. The circuit recited in claim **5** wherein said input resistors and said feedback resistors are laminar flow devices.

7. The circuit recited in claim **6** wherein a variable trimming resistor is connected between said output conduits.