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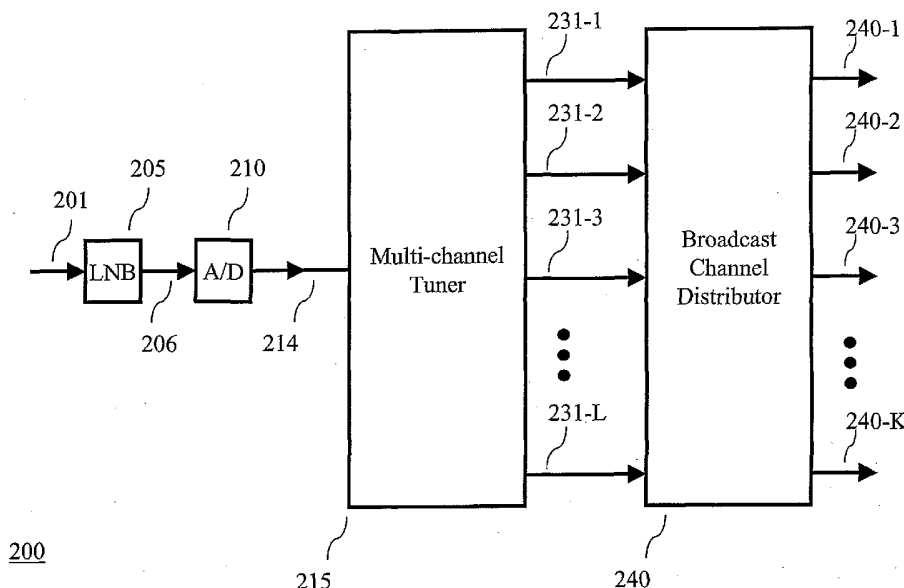
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(54) Title: A MULTI-CHANNEL TUNER USING A DISCRETE COSINE TRANSFORM



(57) Abstract: A satellite receiver includes a multi-channel tuner for processing a plurality of different transponder signals to simultaneously provide a plurality of different bit streams from at least two of the transponder signals. The multi-channel tuner includes (a) a demultiplexer for demultiplexing a received signal representing the plurality of transponder signals into a plurality of sample signals, each transponder signal conveying a bit stream, (b) a plurality of bifurcated filters operative on the plurality of sample signals for providing a plurality of filtered signals, and (c) a discrete cosine transform element operative on the plurality of filtered signals for simultaneously providing at least two of the bitstreams.

WO 2004/100433 A2



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A MULTI-CHANNEL TUNER USING A DISCRETE COSINE TRANSFORM

BACKGROUND OF THE INVENTION

[0001] The present invention generally relates to signal receiving devices, and more particularly, to a multi-channel satellite signal receiver.

[0002] A conventional satellite receiving device, such as a direct broadcast satellite (DBS) receiver, can tune to any one of a number of satellite transponders, each transponder transmitting a downlink signal in a particular frequency band. The transponder downlink signal typically represents a bit stream in a packet format, the packets conveying data, such as audio, video, programming information, etc., associated with one or more broadcast channels or services. In this regard, each transponder is typically associated with a different set of broadcast channels. As such, a desired sports program may be found on one of the broadcast channels associated with one transponder while a movie may be found on one of the broadcast channels associated with a different transponder.

[0003] Unfortunately, as noted above, such a conventional satellite receiving device only tunes to one downlink signal from one transponder at a time. This leads to a number of problems. For example, "channel surfing," i.e., switching from one broadcast channel to another, may entail switching transponders, which causes additional processing delays — delays that slow down the channel surfing process. Further, in households that desire to simultaneously watch, or listen, to programs associated with different transponders — those households must spend more money to purchase, or lease, multiple conventional satellite receiving devices.

SUMMARY OF THE INVENTION

[0004] Therefore, and in accordance with the principles of the invention, a receiving device includes a multi-channel tuner for simultaneously processing a plurality of received signals, each received signal corresponding to a bit stream. The receiver includes a receiver section for providing a signal having a plurality of different frequency channels, each frequency channel conveying a different bit stream and a multi-channel signal tuner operative on the signal for recovering the different bit streams from at least two of the plurality of different frequency channels and for simultaneously providing the recovered different bit streams, wherein the multi-channel signal tuner utilizes a discrete cosine transformation (DCT).

[0005] In one embodiment of the invention, the receiving device is a satellite receiver. The satellite receiver comprises a multi-channel tuner that includes (a) a demultiplexer for demultiplexing a received signal representing a plurality of transponder signals into a plurality of sample signals, each transponder signal conveying a bit stream, (b) a plurality of bifurcated
5 filters operative on the plurality of sample signals for providing a plurality of filtered signals, and (c) a discrete cosine transform element operative on the plurality of filtered signals for simultaneously providing signals representing at least two of the bitstreams.

[0006] In another embodiment of the invention, an integrated circuit includes a transform element for receiving a plurality of signals. The transform element is operative on the
10 received plurality of signals using a discrete cosine transform to simultaneously provide signals representing at least two bit streams, each bit stream associated with a different transmission frequency band. Illustratively, each frequency band is associated with a different transponder of a satellite cable distribution network.

[0007] In another embodiment of the invention, the receiving device is a satellite receiver.
15 The satellite receiver performs a multi-channel tuning method that includes (a) demultiplexing a received signal representing a plurality of transponder signals into a plurality of signals, each transponder signal conveying a bit stream, (b) filtering the plurality of signals to provide a plurality of filtered signals, and (c) transforming the plurality of filtered signals in accordance with a discrete cosine transform for simultaneously providing signals representing
20 at least two of the bitstreams.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1 illustrates an embodiment of a multi-channel tuner;

[0009] FIG. 2 shows an illustrative frequency spectrum for a signal representing 16
25 transponder channels;

[0010] FIG. 3 shows an illustrative filter for use in the multi-channel tuner of FIG. 1;

[0011] FIG. 4 illustrates the relationship between a carrier set and a type 4 discrete carrier transform in accordance with the principles of the invention;

[0012] FIG. 5 is an illustrative block-level diagram of a receiver embodying the principles
30 of the invention;

[0013] FIG. 6 is an illustrative embodiment of a multi-channel tuner in accordance with the principles of the invention;

[0014] FIG. 7 shows an illustrative embodiment of a bifurcated filter in accordance with the principles of the invention;

[0015] FIG. 8 shows an illustrative bifurcated filter bank in accordance with the principles of the invention;

5 [0016] FIGs. 9 – 16 show illustrative matrix values for use in transform element 330 of FIG. 6;

[0017] FIG. 17 is an illustrative block diagram of a demodulator for use in the embodiment of FIG. 6; and

10 [0018] FIG. 18 is another illustrative embodiment in accordance with the principles of the invention.

DETAILED DESCRIPTION

[0019] Other than the inventive concept, the elements shown in the figures are well known and will not be described in detail. Also, familiarity with satellite-based program distribution is assumed and is not described in detail herein. For example, other than the inventive concept, satellite transponders, downlink signals, a radio-frequency (rf) front-end, or receiver section, such as a low noise block, and formatting and encoding methods (such as Moving Picture Expert Group (MPEG)-2 Systems Standard (ISO/IEC 13818-1)) for generating transport bit streams are well-known and not described herein. In addition, the inventive concept may be implemented using conventional programming techniques, which, as such, will not be described herein. Finally, like-numbers on the figures represent similar elements.

[0020] An embodiment of a multi-channel receiver 100 is illustrated in FIG. 1. Receiver 100 includes a low noise block (LNB) 205, an analog-to-digital (A/D) converter 210, and a bank of tuning elements 140-1 through 140-N. One or more satellites (not shown) transmit a plurality of downlink radio frequency (RF) signals 201 in different frequency bands (or frequency channels) associated with different transponders at the same polarization. Each transponder-specific RF signal represents a different transport bit stream encoded, e.g., in accordance with the above-mentioned MPEG2. The RF signals 201 may, e.g., be in the frequency range of 17 GHz (giga-hertz). Illustratively, RF signals 201 includes N adjacent frequency channels, whose center frequencies are F_0 to F_{N-1} , respectively. The channel spacing, F_S , is illustratively uniform and equal to the separation between adjacent center frequencies, e.g., $F_S = F_2 - F_1$. As such, the total bandwidth of all frequency bands, F_{total} ,

equals NF_s . Each frequency channel contains a modulation on its center frequency (carrier) of bandwidth F_{bw} and has an excess bandwidth of $x\%$ and a guard band F_{gb} , where $F_{gb} = (F_s - (F_{bw}[(100+x)/100]))$. For purposes of illustration, it is assumed that $N = 16$, and $F_s = 29.164$ MHz, which is also illustrative of a sixteen transponder digital satellite system (DSS).

5 [0021] The RF signals 201 are received by one or more antennas (not shown) of receiver 100 for application to low noise block (LNB) 205. The latter down shifts and filters the received RF signals 201 and provides a signal 206, which is a near base-band signal having a total bandwidth across all channels of F_{total} . For example, the lowest frequency channel (e.g., channel 0) has a carrier $F_0 = F_s/2$. This is further illustrated in FIG. 2, which shows the
10 spectrum of the near base-band signal 206 for the 16 DSS channels. Returning to FIG. 1, signal 206 is converted from the analog domain to the digital domain via A/D converter 210, which samples signal 206 at a sampling rate, F_{samp} , equal to or greater than the Nyquist rate for signal 206. Illustratively, $F_{samp} = 2F_{total}$, i.e., the sampling rate is twice the total bandwidth across all frequency channels, i.e., $F_{samp} = 2NF_s$. In this example, $F_{samp} = 933.12$ MHz. A/D
15 210 provides a signal 214, which is a discrete time sequence of samples representing the plurality of transponder channels at the sample rate, F_{samp} .

[0022] Signal 214 is applied to the bank of tuning elements 140-1 to 140-N. Each tuning element filters signal 214 at a particular one of the N transponder channels to simultaneously provide a respective inphase/quadrature (IQ) baseband signal representing the associated
20 transport bit stream. For example, tuning element 140-1 includes a bandpass filter 145-1, a decimate by N element 150-1 and a demodulator 155-1. Bandpass filter 145-1 has a passband centered by F_0 , and a stop band that attenuates the remaining transponder channels. As such, bandpass filter 145-1 filters signal 214 to provide a filtered signal 146-1 that represents only channel 0 (Ch0). An illustrative block diagram of a representative filter 145, which provides
25 an output signal 146, is shown in FIG. 3. Filter 145, e.g., illustratively includes 256 tap coefficients as represented by tap coefficient 165, delay elements Z^{-1} as represented by delay element 160, each of which provide a time delay equal to $\frac{1}{2}(NF_s)$, and adders as represented by adder 170. The sample data impulse response of bandpass filter 145 is the sample impulse data response of a low-pass filter (not shown) modulated by a sample data representation of a
30 cosine wave at the carrier frequency of the transponder channel to be received. The phase of this cosine wave is so arranged that zero degrees aligns with the center of the linear phase low pass sample data impulse response. Since signal 146 is a sequence of samples that only represents those samples associated with a particular transponder channel, this signal is now

over-sampled at F_{smp} . This means that relative to a single received transponder channel the sample rate is much greater than required. As such, and returning to FIG. 1, signal 146-1 is now decimated by N (where N , again, is the number of transponder channels) via element 150-1 to provide a sequence of samples at $1/N$ th the sample rate, i.e., $2F_s$, to demodulator 155-1. The latter includes a half-channel spacing sine/cosine generator for demodulation at the associated transponder frequency, e.g., F_0 . Demodulator 155-1 provides an inphase/quadrature baseband signal representing the associated transport bit stream.

[0023] It can be observed from FIG. 1, that N tuning elements are required to simultaneously provide N transport bit streams. In addition, the filtering process of each bandpass filter 145, must run at a very high clock rate. For example, the symbol rate of signal 214 is close to 1 GHz (giga-hertz). However, and in accordance with the principles of the invention, it is possible to transform the architecture of receiver 100 into an architecture such that the high speed pipelined calculations followed by a decimation operation as illustrated in receiver 100 are replaced with a number of lower speed parallel calculations, which are then summed together.

[0024] In particular, assume that $N = 16$ DSS transponder channels as illustrated in FIG. 2. Illustratively, A/D 210 samples signal 206 (described earlier) at the Nyquist rate equal to $2NF_s$. Each transponder channel carrier frequency, F_{ch} , is located in the middle of the corresponding frequency channel. As such, for N channels, numbered 0 to $N - 1$:

$$F_{CH} = ch \cdot F_s + \frac{F_s}{2}, \quad (1)$$

where $0 \leq ch \leq N - 1$. The transponder carrier channel frequencies can be normalized to the sampling rate $2NF_s$. In this case, equation (1) becomes:

$$F_{CHN} = \frac{(2 \cdot ch + 1)}{4 \cdot N}, \quad (2)$$

where F_{CHN} represents the normalized transponder carrier frequency for a particular channel, ch , where, again, $0 \leq ch \leq N - 1$. The set of normalized transponder carrier frequencies is referred to as a carrier set. For $N = 16$ transponder channels, there are 16 normalized transponder carrier frequencies in the carrier set. In accordance with an aspect of the invention, I have observed that this carrier set corresponds to a variant of the type 4 Discrete Cosine Transform. Application of the type 4 DCT in this application for complex

modulations has an advantage in that the IQ (in-phase/quadrature) modulation is maintained as a real near base band signal for down stream conventional near base band demodulation.

[0025] The equation for a N point type 4 (or IV) DCT is shown below:

$$DCT_N^{IV}(i, j) = \sqrt{\frac{2}{N}} \cdot \cos\left(2\pi \cdot \frac{2j+1}{4N} \cdot \frac{2i+1}{2N}\right), \quad (3)$$

5 where i is the time index and $0 \leq i \leq N - 1$; and j is the frequency index (frequency channel number) and $0 \leq j \leq N - 1$, and N is the number of frequency channels. The relationship between the type 4 DCT and the carrier set is illustrated in FIG. 4 for $N = 16$. In FIG. 4, it is assumed that the A/D converter (e.g., A/D 210) samples at 32 times the channel spacing so that 16 channels are equally spaced between 0 and the Nyquist folding
10 frequency. Continuous Cosines at F_{ch} of each frequency channel (Ch0 to Ch15) are illustrated in FIG. 4. A sample data representation of each cosine carrier at the A/D sample rate is represented by the black dots on the continuous cosines shown in FIG. 4. Along the axis labeled "Time in A/D Samples", the relationship between the carrier set and the type 4 DCT is noted. In the first 16 samples (1 - 16), each carrier is exactly equal to a 16 point type 4 DCT,
15 as signified by the axis label "DCT_{IV}." In the next set of 16 samples (17 - 32), each carrier is minus the time flipped 16 point type 4 DCT, as signified by the axis label "-Time Flipped DCT_{IV}." The third set of samples (33 - 48) is exactly equal to minus the type 4 DCT, as signified by the axis label "-DCT_{IV}." The final set of 16 samples (49 - 64) is exactly equal to the time flipped type 4 DCT, as signified by the axis label "Time Flipped DCT_{IV}." The
20 aforementioned pattern of sign changes and time order flips continuously repeats for any desired length of carrier set. This generalizes to any number of channels N and any order DCT. Another way to look at FIG. 4 is to view the axis labels as identifying the operations required to be performed on a cosine carrier for the cosine carrier to match a type 4 DCT. For example, for time samples 49 - 64, the cosine carrier must be "time flipped" to match a 16
25 point type 4 DCT. Therefore, and in accordance with another aspect of the invention, the earlier described filter 145 can be used as the basis for exploiting the symmetries of a type 4 Discrete Cosine Transform.

[0026] Now, assume a single low pass finite impulse response (FIR) filter for processing the multi-channel transponder signal. Let a sample data impulse response (in the z-domain) of
30 the FIR filter be:

$$H_{LPF}(z) = \sum_{I=0}^{k-N-1} A_I \cdot z^{-I}, \quad (4)$$

where A_I are the filter tap coefficients, z^{-I} are delay elements, k is the number of filter taps, $0 \leq I \leq N-1$, and N is the number of frequency channels. In accordance with an aspect of the invention, the architectural trick for using a DCT is to divide each filter such that different subsets of the taps are separately accumulated to provide partial results that match the symmetry of a DCT. In this example, the division of the filter is a bifurcation such that the odd and even tap coefficients are separately accumulated thus providing partial results that match the symmetry of the DCT type 4 as illustrated in FIG. 4. (It should be noted that the inventive concept is not limited to a bifurcation.) In addition, the tap coefficients, A_I , will be distributed among different ones of the bifurcated filters.

[0027] Turning now to FIG. 5, an illustrative receiver 200 in accordance with the principles of the invention is shown. Receiver 200 includes a low noise block (LNB) 205, an analog-to-digital (A/D) converter 210, a multi-channel tuner 215 and a broadcast channel distributor 240. As described above, one or more satellites (not shown) transmit a plurality of downlink radio frequency (RF) signals 201 in different frequency bands (or frequency channels) associated with different transponders at the same polarization. RF signals 201 are processed by LNB 205 to provide signal 206, which is a near base-band signal having a total bandwidth across all channels of F_{total} . (Again, this is illustrated in FIG. 2 for 16 DSS channels.) Signal 206 is converted from the analog domain to the digital domain via A/D converter 210, which samples signal 206 at a sampling rate, $F_{samp} = 2NF_s$, to provide signal 214, which is a discrete time sequence of samples representing the plurality of transponder channels. Signal 214 is applied to multi-channel tuner 215 (described below), which, in accordance with the principles of the invention, processes signal 214 to provide a number of simultaneous bit streams from two or more transponder channels as represented by bit streams 231-1 through 231-L, where $I < L \leq N$. It should be noted that these simultaneous bit streams are applied to broadcast channel distributor 240, which processes each of the bit streams to provide data associated with virtual channels 240-1 through 240-K, where $K > 1$. For example, broadcast channel distributor 240 decodes each of the bit streams encoded, e.g., in accordance with the earlier-mentioned MPEG-2 Systems Standard ISO/IEC 13818-1. As such, each of these virtual channels represents content and/or services, for example, audio, video (e.g., a selected movie), electronic programming guide etc. It should be realized the

although shown as separate signals 240-1 through 240-K, one, or more, of these signals may be multiplexed together for transmission on a broadcast medium, e.g., a cable, or via wireless (such as Wi-Fi (Wireless Fidelity)). For simplicity, other input signals to broadcast channel distributor 240 specifying selection of content and/or services has not been shown. Likewise,
5 other circuitry for delivering the content/services, which may, or may not, be a part of receiver 200 also not been shown.

[0028] An illustrative embodiment of a multi-channel tuner 215 in accordance with the principles of the invention is shown in FIG. 6. Multi-channel tuner 215 includes demultiplexer (demux) 220, bifurcated filter bank 325, transform element 330 and
10 demodulators 335-1 to 335-L. Demux 220 samples signal 214 at a demultiplexer sampling rate, F_F , (or post-decimation sampling rate) to provide a number of decimated sample streams, 221-1 to 221-N, where N is the number of transponder channels, to bifurcated filter bank 325 (described further below). As such, $F_F = 2F_S$. The bifurcated filter bank 325 forms a filter input vector to transform element 330 (described below), which recovers therefrom, via
15 demodulators 335, a number of simultaneous bit streams from two or more transponder channels as represented by bit streams 231-1 through 231-L, where $I < L \leq N$.

[0029] In this illustrative embodiment, transform element 330 uses a type 4 Discrete Cosine Transform (DCT) for processing the filter input vector. The output vector from transform element 330 is further processed by a respective demodulator, 335- i , at each of the
20 transponder carrier frequencies.

[0030] Bifurcated filter bank 325 includes a number of bifurcated filters, 325- i , where $I \leq i \leq N$, i.e., one bifurcated filter for a respective one of the N decimated streams from demux 220. Since all the bifurcated filters have a similar structure, only one bifurcated filter is described in detail herein. An illustrative bifurcated filter 325-1 in accordance with the
25 principles of the invention is shown in FIG. 7. Bifurcated filter 325-1 receives decimated stream 221-1 from demux 220 and provides two output signals: signal 506, also designated as the even output signal (E), and signal 507, also designated as the odd output signal (O). Bifurcated filter 325-1 includes a number of delay elements as represented by delay element 515, a number of coefficient multipliers as represented by coefficient multiplier 520 (also
30 referred to as tap coefficient 520) having a coefficient value of A_0 , and two summing networks 505 and 510. The time delay elements, e.g., time delay element 515, delay the signal by an amount of time equal to the inverse of the demux sampling rate, i.e., $1/F_F$. As can be observed from FIG. 7, summing network 505 adds together those values from the even

coefficient multipliers to form the even output signal. Similarly, summing network 510 adds together those values from the odd coefficient multipliers to form the odd output signal. It can be further observed that each summing network 505 and 510 alternates the sign of the value from alternate coefficient multipliers. For example, the value from the coefficient multiplier 525 is inverted by summing network 505. In other words, the coefficients for the even output signal are the even numbered decimations by $2N$ alternated in sign, while the coefficients for the odd output signal are the odd numbered decimations by $2N$. This alternating in sign implements the required inversions in sign required at points in time as illustrated by the axis of the graph in FIG. 4 for matching a type 4 DCT. This bifurcating filter structure shown in FIG. 7 results in the even tap partial sum being modulated by a direct type 4 DCT, while the odd tap partial sum is always modulated by a time reversed type 4 DCT. This can be realized with a single N point type 4 DCT by summing the vector of even taps partial sum to the vector of odd taps partial sum in reverse time order. In addition, it should be observed that in this example there are $k = N$ tap coefficients per bifurcated filter, i.e., $k = 16$, with respect to equation (4). As such, the total number of tap coefficients in this example is 256, which are spread among the 16 bifurcated filters as indicated in FIG. 7. In particular, bifurcated filter 325-1 illustratively includes the 16 tap coefficients: $A_0, A_{16}, A_{32}, A_{48}, A_{64}, \dots, A_{208}, A_{224},$ and A_{240} , arranged as shown. Similarly, bifurcated filter 325-2 (not shown) includes the 16 tap coefficients: $A_1, A_{17}, A_{33}, A_{49}, A_{65}, \dots, A_{209}, A_{225},$ and A_{241} . This pattern continues, such that the last bifurcated filter 325- N (not shown) includes the 16 tap coefficients: $A_{15}, A_{31}, A_{47}, A_{63}, A_{79}, \dots, A_{223}, A_{239},$ and A_{255} . (Referring briefly back to FIG. 3, it could be observed that the taps of filter 145 are divided among the N bifurcated filters.)

[0031] It should also be noted that the effective N , or, e.g., 16, bifurcated filter responses have the same delay such that transform element 330 processes N decimated samples at the same time. In other words, at a particular time, t_P , a filter input vector is formed for application to transform element 330. This filter input vector includes one sample from each of the decimated sample streams at a particular sampling time. Turning back briefly to FIG. 6, the filter input vector comprises samples F1 through FN.

[0032] An illustrative bifurcated filter bank is shown in FIG. 8. The latter illustrates the combination of the even signals and odd signals from each of the N bifurcated filters via N adders 345- i , $1 \leq i \leq N$, to complete the match to the symmetry of a DCT. For example, the even signal from bifurcated filter 325-1 is combined with the odd signal from bifurcated filter 325- N via adder 345-1. This provides the above-noted required time reversal illustrated in

FIG. 4. As a result, bifurcated filter bank 325 provides the filter input vector [F1, F2, ..., FN] to transform element 330 as illustrated in FIG. 6.

[0033] Having matched the symmetry of a type 4 DCT with the use of the above-described bifurcated filter bank 325, transform element 330 provides a DCT_{IV} transformation of the filter input vector, where:

$$O_C = DCT_{IV}F, \quad (5)$$

where F is the filter input vector, O_C is an output vector, the elements of which represents each of the N transponder channels, and DCT_{IV} is an implantation of an N -point type DCT. One illustrative implementation of transform element 330 is simply the implementation of equation (3), shown above. Indeed, in accordance with an aspect of the invention, any of the known algorithms to realize a type 4 DCT may be used, each having different computational efficiencies. However, for the high sampling rate applications targeted, a sparse factoring of the DCT IV matrix by exploiting relationships to the Discrete Fourier Transform (DFT) is preferred. One illustrative sparse factoring of an $N=16$ point DFT IV is provided below. In particular, DCT_{IV} is:

$$DCT_{IV} = CF \cdot CE \cdot CDFT0 \cdot CDFT1 \cdot CDFT2 \cdot CDFT3 \cdot CDFT4 \cdot CDFT5 \cdot CD \cdot CC. \quad (6)$$

This factorization requires 62 additions and 46 multiplications. If all 16 transponder channels are simultaneously received this corresponds to 3.875 adds and 2.875 multiplies per channel per near base band sample (the demultiplexer sample rate is $2F_S$ in Hz)). The matrices shown in equation (6) are illustrated in FIGs. 9-16. It should be noted that the notation $C(x)$ or $S(x)$ illustrated in these figures represents the operations cosine(x) and sine(x), respectively. Further, where clearly identifiable portions of a matrix are equal to zero, a single "0" is entered on that portion of the matrix, as illustrated in matrix CD of FIG. 10.

[0034] As noted above, an advantage of the use of a type 4 DCT is that the elements of the output vector represent each of the transponder channels wherein the IQ modulation is maintained as a real near base band signal for down stream conventional near base band demodulation. As such, each element of the output vector from transform element 330 is further processed by a respective demodulator, 335-i, at each of the transponder carrier frequencies. An illustrative demodulator is shown in FIG. 17 for processing an output signal from transform element 330 into a baseband IQ signal for a respective transponder channel. In this illustrative embodiment, one demodulator of the form illustrated in FIG. 17 is required for each desired transponder channel.

[0035] As described above, receiver 200 enables a plurality of frequency channels to be simultaneously tuned such that broadcast channel programs included within different frequency channels may be simultaneously accessed. In addition, and in accordance with an aspect of the invention, the amount of hardware and processing required to implement a multi-channel tuner is simplified by use of a single computation element as represented by transform element 330. For example, now all calculations are performed at a convenient rate, e.g., F_F .

[0036] As noted above, the transform element may be implemented in an integrated circuit such as an FPGA. As such, as shown in FIG. 18, a single-chip solution is possible for simultaneously providing content from different transponder channels. Illustratively, an integrated circuit 400 may include at least a transform element, such as represented by transform element 330, described above, to provide therefrom a plurality of virtual channels 240-1 to 240-K, where at least some of the content of these virtual channels are simultaneously provided from different transponder channels. As required, the integrated circuit 400 may include demodulators (DM), as described above.

[0037] It should be noted that other forms of LNB processing may also be used. For example, LNB 205 may perform a filtering operation to a relaxed specification with a broad transition band of width (PF_S) above and below the N channel band to reach acceptable stop band attenuation, where P is an integer. Moreover, the LNB may spectrally move the lowest frequency channel so that the corresponding carrier F_0 is equal to $[F_S/2 + (PF_S)]$. With this variation, the A/D converter 210 is clocked at the sampling rate $[2(N+(2P))F_S]$, and the number of demultiplexer parallel paths used for signal tuning is $N+(2P)$. This variation may allow LNB 205 to utilize smaller, lower performance filters, rather than physically larger and lossy SAW filters.

[0038] Similarly, LNB 205 may provide signal 206 such that the frequency of the highest frequency channel (i.e., F_N) is arranged to fall on an even folding frequency of the demultiplexer sampling rate, F_F . This technique may be used for those highest frequency channels that satisfy:

$$F_F = 2 \left[\frac{F_N + \frac{F_S}{2}}{2NF_S} \right], \quad (7)$$

30 when sampling A/D 210 at $2NF_S$, or

$$F_F = \left[\frac{F_N + F_S(P+.5)}{2(N+2P)F_S} \right], \quad (8)$$

when sampling A/D 210 at $[2(N+(2P))F_S]$.

[0039] Likewise, LNB 205 may provide signal 206 such that the frequency of the lowest frequency channel (i.e., F_l) is arranged to fall on an even folding frequency of the demultiplexer sampling rate, F_F . This technique may be used for those lowest frequency channels that satisfy:

$$F_F = 2 \left[\frac{\frac{F_l - F_S}{2}}{2NF_S} \right], \quad (9)$$

when sampling A/D 210 at $2NF_S$, or

$$F_F = \left[\frac{F_l - F_S(P+.5)}{2(N+2P)F_S} \right], \quad (10)$$

10 when sampling A/D 210 at $[2(N+(2P))F_S]$.

[0040] It should also be noted that constraints on the clock rate of A/D 210 can be relaxed somewhat by inclusion of a sample rate converter. The latter representing a calculated sequence derived from some sampling (uniform or non-uniform) not conforming to the desired sample spacing T . In addition, it should be noted that other types of DCTs may be also be used in accordance with the inventive concept, e.g., type 2, type 3, etc. However, mismatches of boundary conditions in time and frequency entail a hardware and circuit complexity penalty for using these types of DCTs and, as such, are not described further herein.

[0041] Further, it should be noted that although described in the context of a satellite distribution, the inventive concept is not so limited and also applies to other distribution mechanisms whether wireless and/or wired. For example, the invention is applicable to cable, terrestrial or other networks (such as broadcast and/or commercial networks).

[0042] As such, the foregoing merely illustrates the principles of the invention and it will thus be appreciated that those skilled in the art will be able to devise numerous alternative arrangements which, although not explicitly described herein, embody the principles of the invention and are within its spirit and scope. For example, although illustrated in the context of separate functional elements, these functional elements may be embodied on one or more integrated circuits (ICs). Similarly, although shown as a separate elements, any or all of the

elements of FIGs. 10 and 12 (e.g., 215 and/or 240) may be implemented in a stored-program-controlled processor. It is therefore to be understood that numerous modifications may be made to the illustrative embodiments and that other arrangements may be devised without departing from the spirit and scope of the present invention as defined by the appended

5 claims.

CLAIMS

1. A receiver comprising:

a receiver section for providing a signal having a plurality of different frequency channels, each frequency channel conveying a different bit stream; and

5 a multi-channel signal tuner operative on the signal for recovering the different bit streams from at least two of the plurality of different frequency channels and for simultaneously providing the recovered different bits streams, wherein the multi-channel signal tuner utilizes a discrete cosine transformation (DCT).

10 2. The receiver of claim 1, wherein the multi-channel signal tuner comprises:

a sampler for sampling the signal to provide a number of decimated sample streams;

a transform element operative on the number of decimated sample streams to provide transform output signals wherein the transform element utilizes the DCT; and

15 a number of demodulators operative on the transform output signals to provide the recovered different bit streams.

3. The receiver of claim 2, wherein the sampler includes:

a demultiplexer for demultiplexing the signal into the number of decimated sample streams; and

20 a divided filter bank for processing the number of decimated sample streams for matching the DCT utilized by the transform element.

4. The receiver of claim 3, wherein the divided filter bank includes a bank of bifurcated filters and the DCT is an N-point type IV DCT.

25

5. The receiver of claim 4, wherein the transform element performs matrix-based processing on the number of decimated sample streams using a sparse matrix factorization of the N-point type IV DCT.

30 6. The receiver of claim 1, further comprising a broadcast channel distributor for providing a number of virtual channels from the recovered different bit streams.

7. A satellite receiver comprising:

a low-noise block for receiving a signal representing a plurality of different transponder channels and an analog-to-digital converter for providing therefrom a data signal
5 representing a sequence of samples occurring at a sample rate greater than, or equal to, a Nyquist rate related to a total bandwidth of the plurality of different transponder channels, each transponder channel conveying a bit stream;

a sampler for sampling the data signal for providing N decimated data streams, where
10 $N > 1$;

a transform element operative on the N decimated data streams for simultaneously providing at least two transform output signals from at least two of the plurality of different transponder channels, wherein the transform element utilizes a discrete cosine transformation (DCT); and

at least two demodulators operative on the at least two transform output signals to
15 provide at least two bit streams from the plurality of different transponder channels.

8. The satellite receiver of claim 7, wherein the sampler includes:

a demultiplexer for demultiplexing the signal into the number of decimated data streams; and

20 a divided filter bank for processing the number of decimated sample streams for matching the DCT utilized by the transform element.

9. The satellite receiver of claim 7, wherein the divided filter bank includes a bank of bifurcated filters and the DCT is an N -point type IV DCT.

25

10. The satellite receiver of claim 9, wherein the transform element performs matrix-based processing on the number of decimated data streams using sparse matrix factorization.

11. The satellite receiver of claim 7, further comprising a broadcast channel distributor
30 for providing a number of virtual channels from the at least two bit streams.

12. An integrated circuit for use in a satellite receiver, which receives signals from a plurality of transponder channels, the integrated circuit comprising:

5 a transform element operative on a plurality of data streams for simultaneously providing at least two transform output signals, each of the data streams conveying samples of the plurality of transponder channels, wherein the transform element utilizes a discrete cosine transform (DCT);

10 at least two demodulators operative on the at least two transform output signals for simultaneously providing two bit streams from at least two of the plurality of transponder channels; and

a broadcast channel distributor for providing a number of virtual channels from the at least two bit streams.

15 13. The integrated circuit of claim 12, wherein the DCT is an N-point type IV DCT.

14. The integrated circuit of claim 13, wherein the transform element performs matrix-based processing on the plurality of data streams using sparse matrix factorization.

15. A multi-channel tuner comprising:

20 a sampler for sampling a signal representing a plurality of different frequency channels to provide a plurality of sample streams, each frequency channel conveying a transport bit stream;

a bank of filters for filtering the plurality of sample streams to provide a plurality of filtered sample streams;

25 a discrete cosine based transform element operative on the plurality of filtered sample streams to provide a plurality of data signals, each data signal associated with one of the different frequency channels; and

a plurality of demodulators for demodulating each of the plurality of data signals to simultaneously provide the transport bit streams.

30

16. The multi-channel tuner of claim 1 wherein the plurality of data signals is at least two.

17. The multi-channel tuner of claim 1, wherein the bank of filters include a plurality of bifurcated filters and the discrete cosine based transform element uses a type IV discrete cosine transform.

5 18. A method for use in a receiver comprising:
providing a signal having a plurality of different frequency channels, each frequency channel conveying a different bit stream; and
performing multi-channel signal tuning on the signal for recovering the different bit streams from at least two of the plurality of different frequency channels; and
10 simultaneously providing the recovered different bits streams,
wherein the step of multi-channel signal tuning utilizes a discrete cosine transformation (DCT).

19. The method of claim 18, wherein the multi-channel signal tuning step comprises:
15 sampling the signal to provide a number of decimated sample streams;
performing transform-based processing on the number of decimated sample streams to provide transform output signals wherein the transform based processing utilizes the DCT;
and
demodulating the transform output signals to provide the recovered different bit
20 streams.

20. The method claim 19, wherein the sampling step includes:
demultiplexing the signal into the number of decimated sample streams; and
processing the number of decimated sample streams with a divided filter bank for
25 matching the DCT utilized by the transform element.

21. The method of claim 20, wherein the divided filter bank includes a bank of bifurcated filters and the DCT is an N-point type IV DCT.

30 22. The method of claim 19, wherein the performing transform-based processing step performs matrix-based processing on the number of decimated sample steams using a sparse matrix factorization of the N-point type IV DCT.

23. The method of claim 18, further comprising the step of providing a number of virtual channels from the recovered different bit streams.

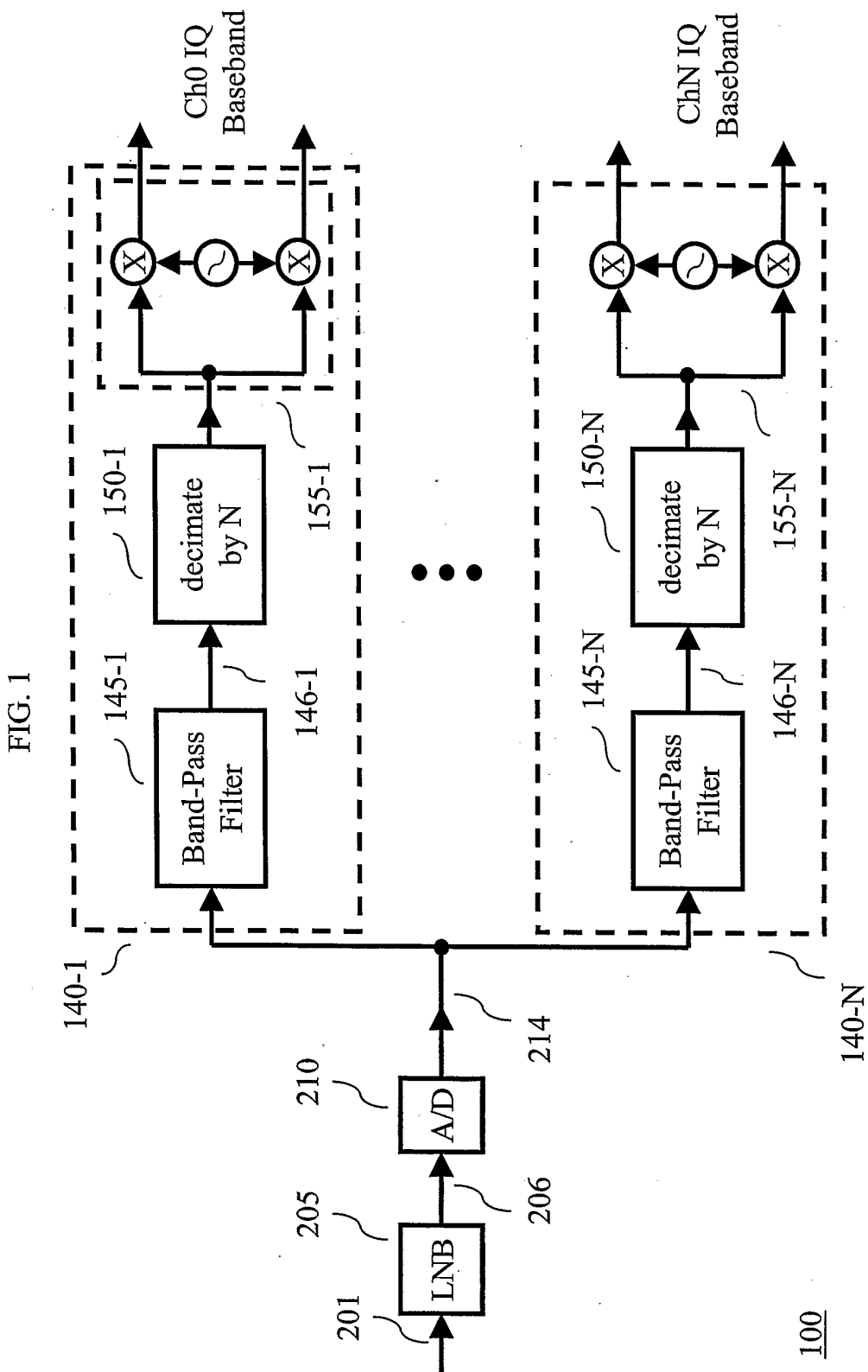


FIG. 2

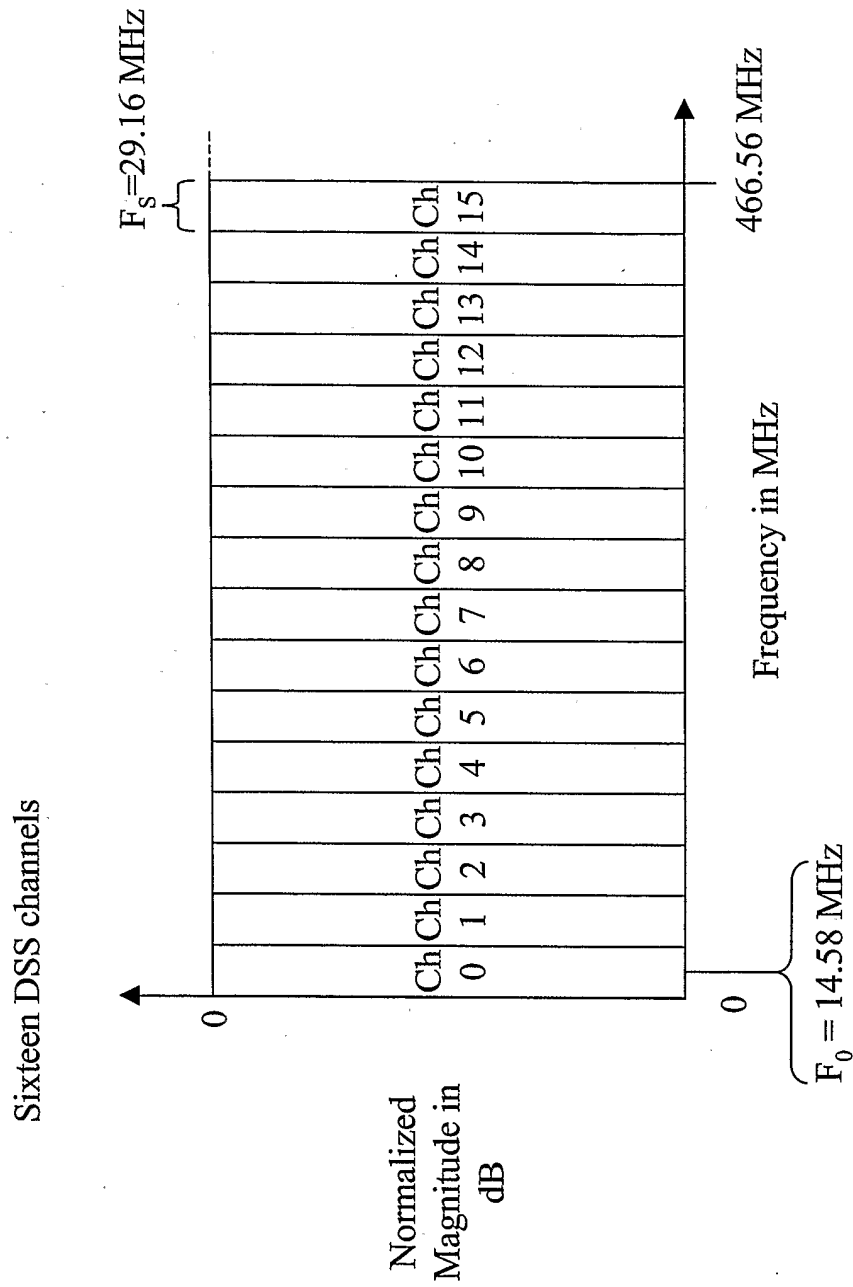
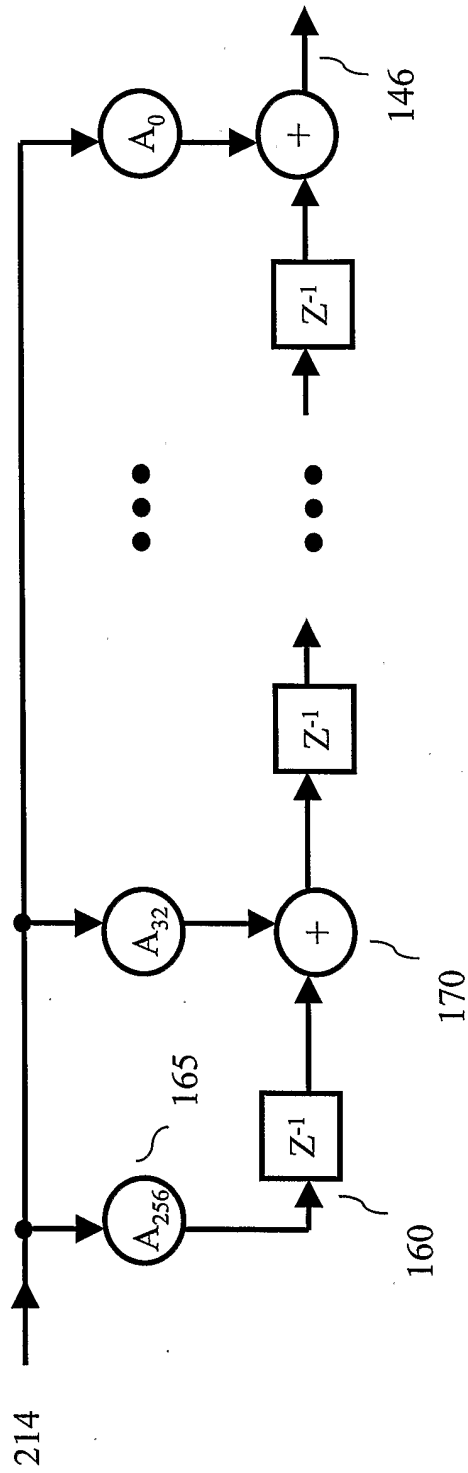
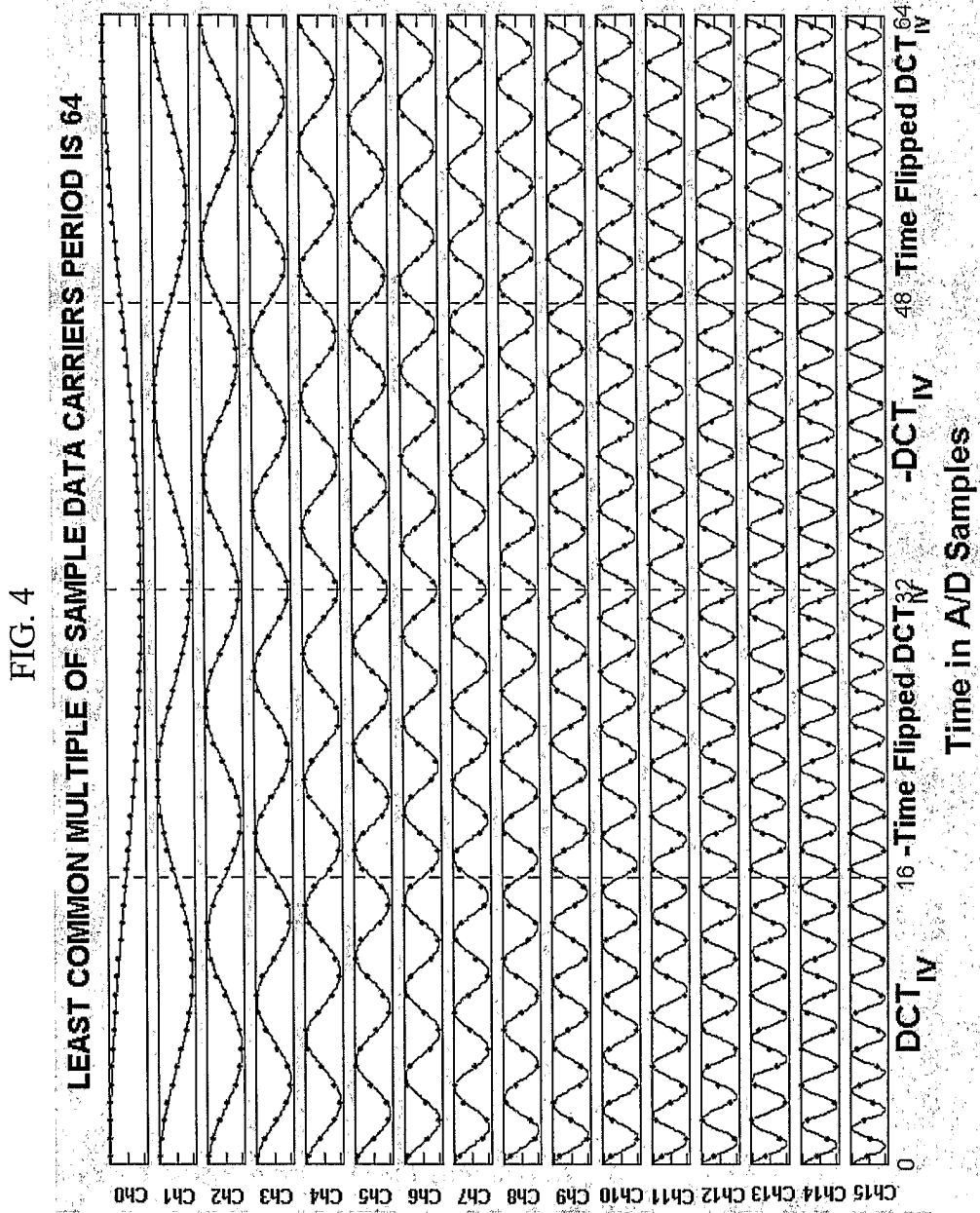
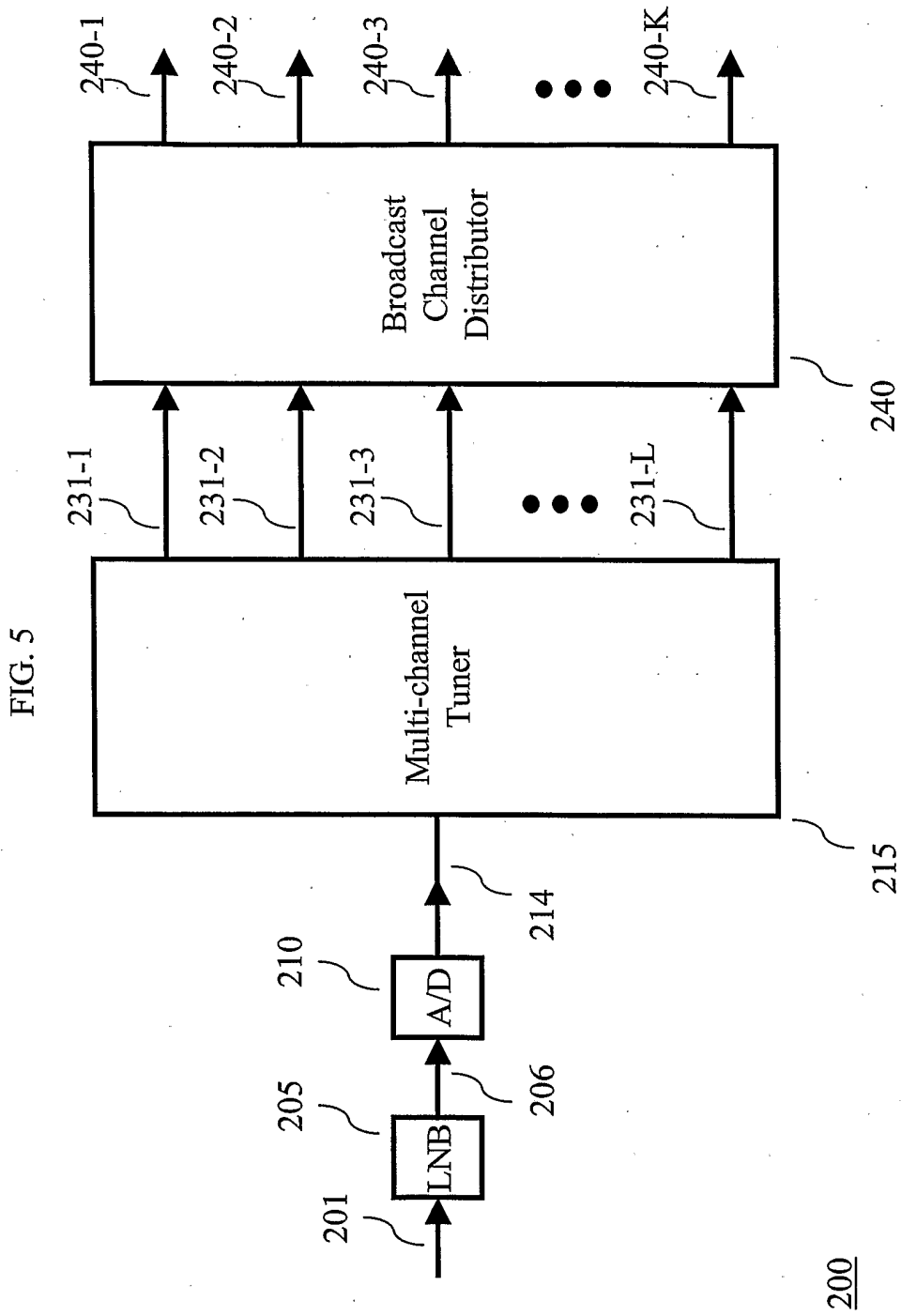


FIG. 3

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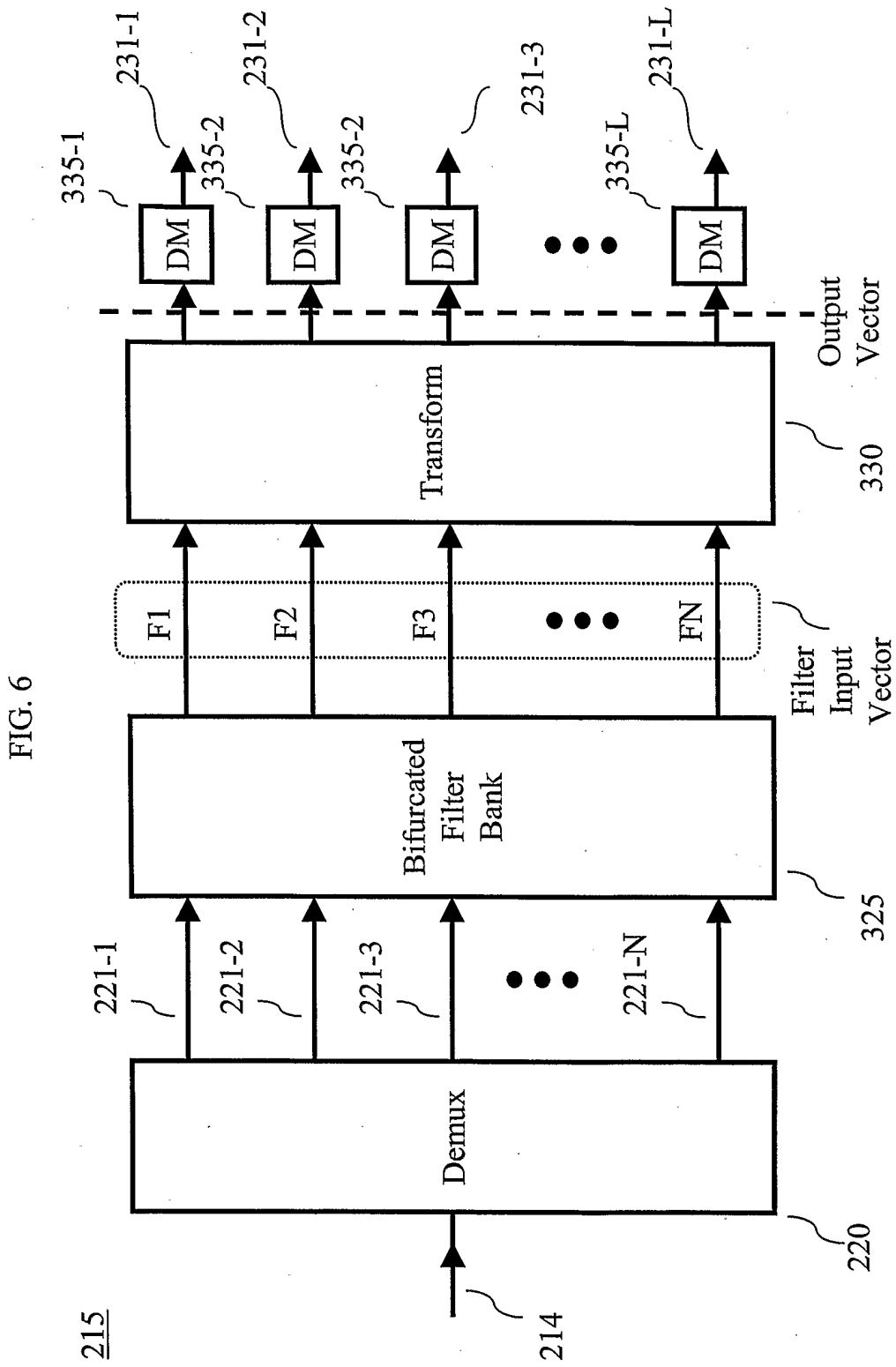


FIG. 6

215

214

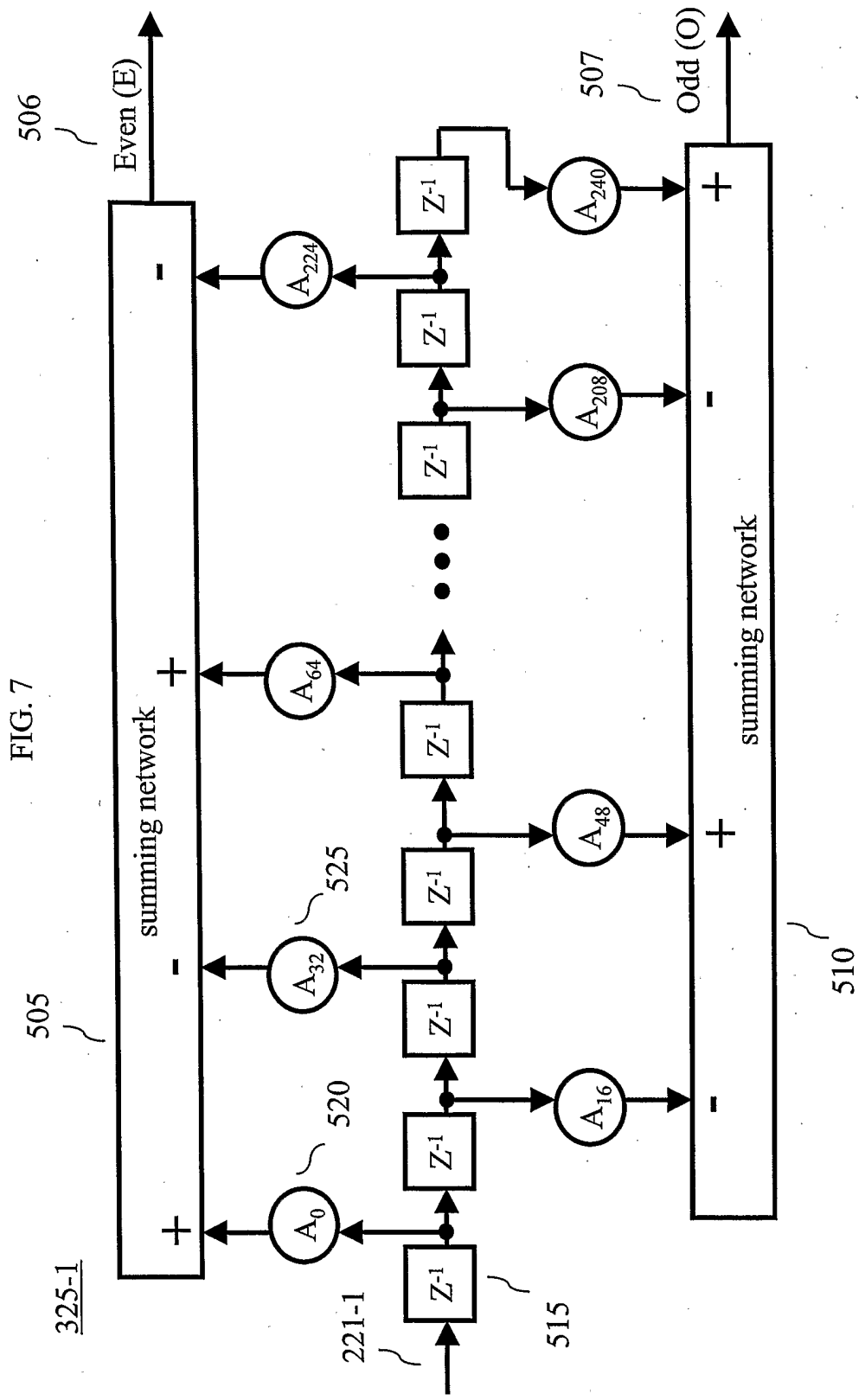


FIG. 7

325-1

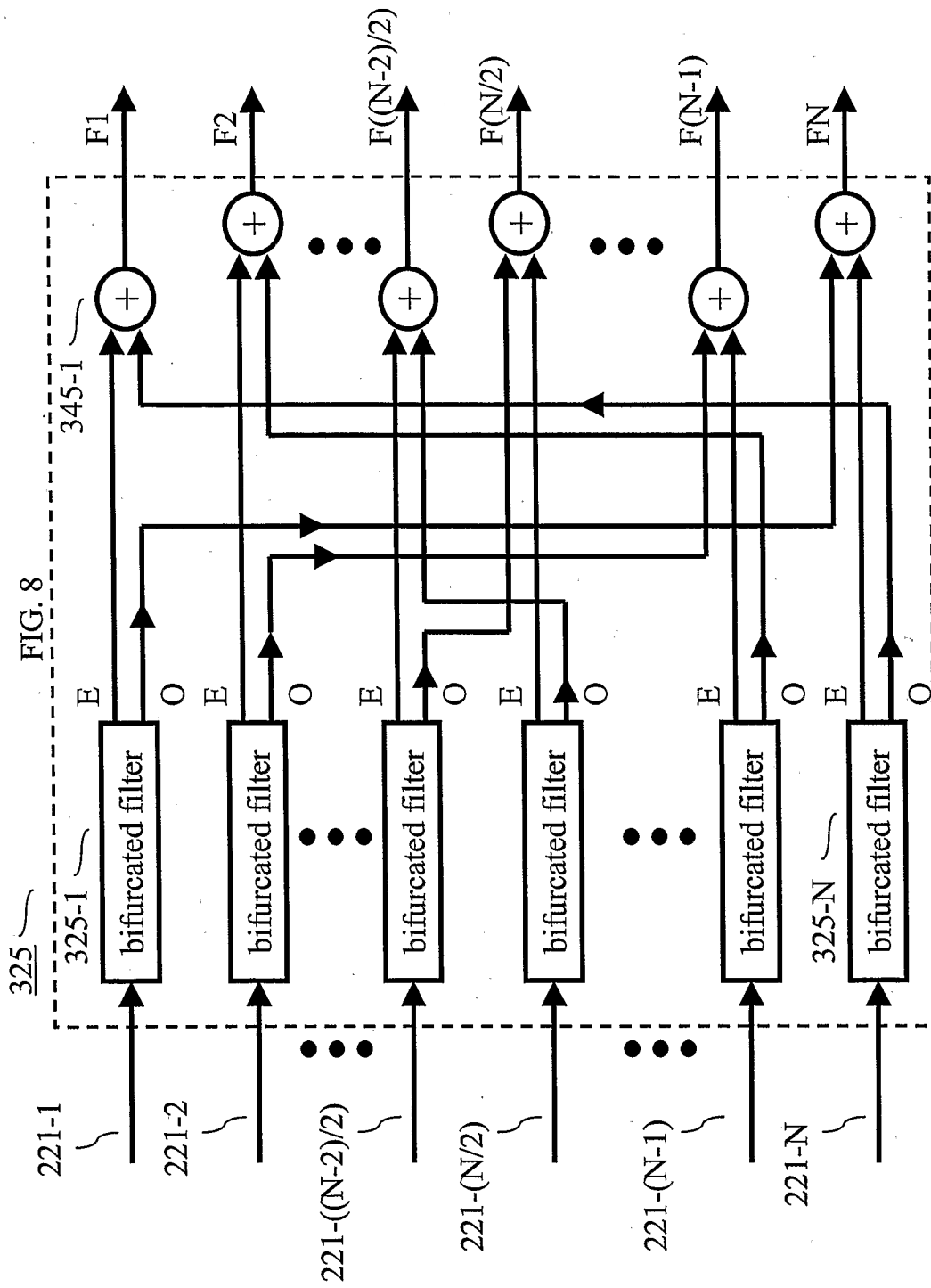


FIG. 11

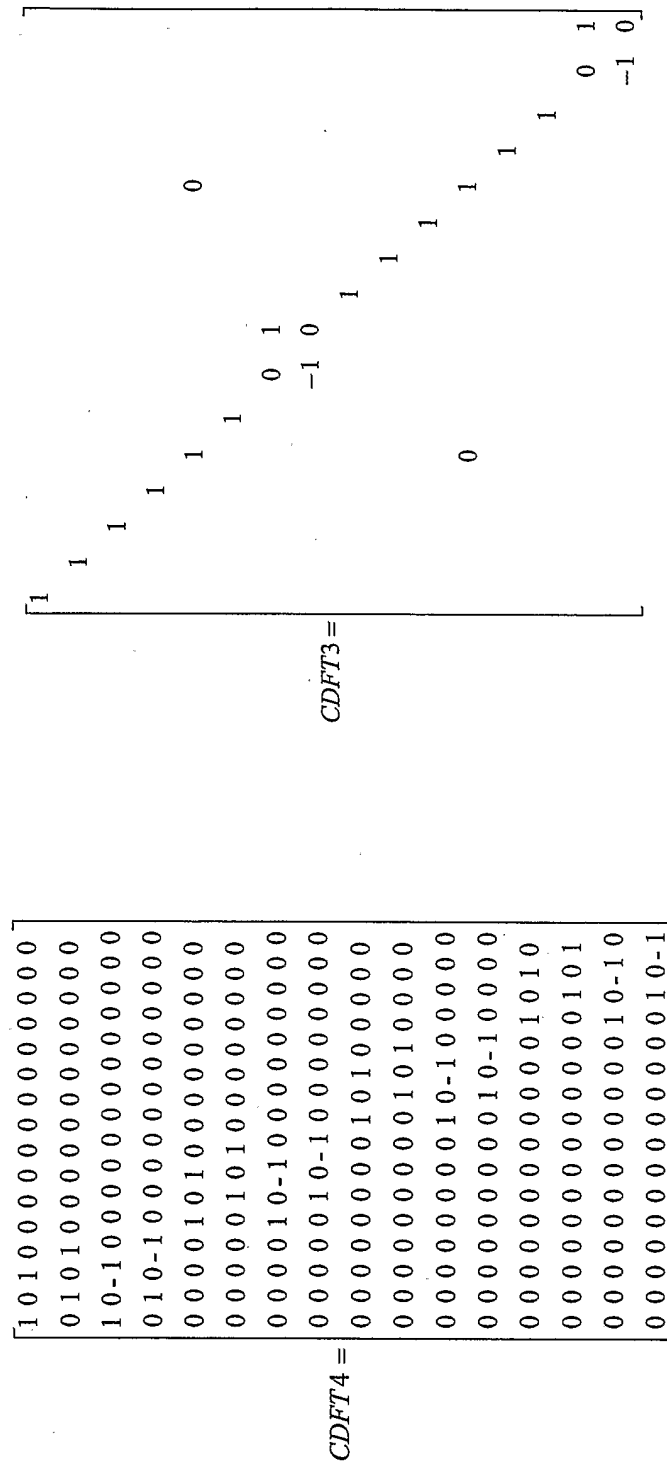


FIG. 12

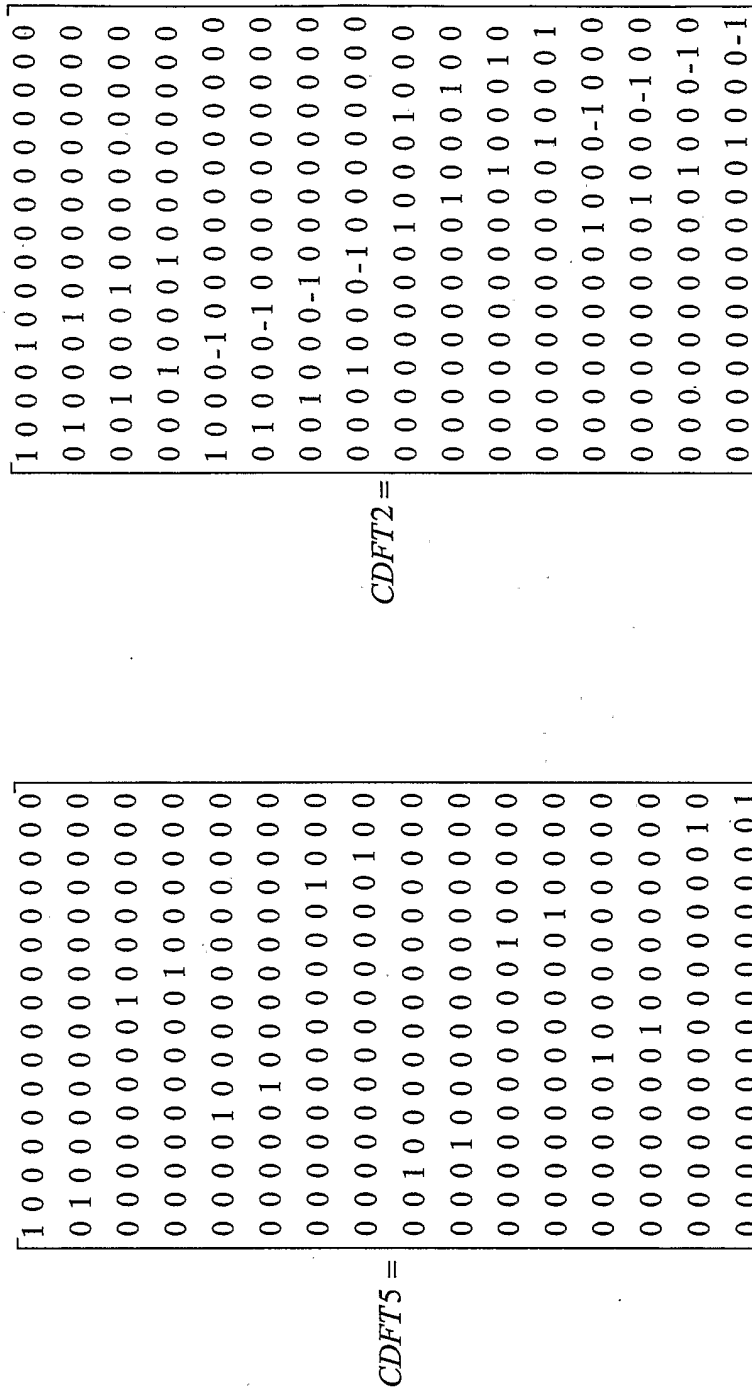


FIG. 15

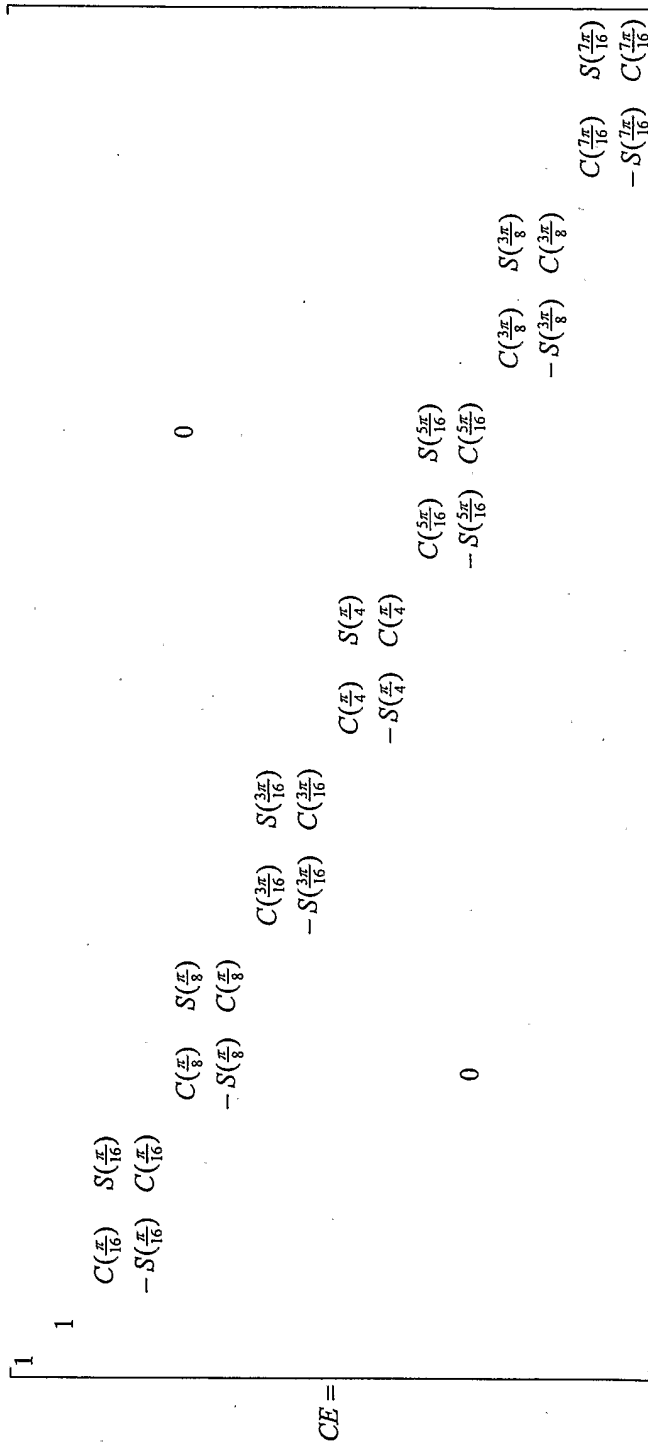


FIG. 17

