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PATENT SPECIFICATION (11) 1 572 878

(21) Application No. 7963/77 (22) Filed 24 Feb. 1977
(31) Convention Application No. 7605585
(32) Filed 27 Feb. 1976 in
(33) France (FR)
(44) Complete Specification published 6 Aug. 1980
(51) INT CL³ H03K 19/08
(52) Index at acceptance
H3T 2T2X 3C1 3J 4D 4S 5E HM
H1K 11A3 11B3 11C1A 11C4 11D 1AA1 1AA9 1BD 4C11 4C1R 9D1 9E 9R2 GAH

(19)

(54) A COMPONENT FOR LOGIC CIRCUITS AND LOGIC CIRCUITS EQUIPPED WITH THIS COMPONENT

(71) We, THOMSON—CSF, a French Body Corporate, of 173, Boulevard Haussmann—75008 Paris—France—do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a new component for logic circuits and to the circuits equipped with this component.

It is known that the qualities required of a component for logic circuits are, on the one hand, its energy consumption and, on the other hand, its switching speed from the conductive state to the blocked state and vice versa.

In the majority of circuits based on bipolar transistors, the transistors are close to saturation when they are conductive.

Their switching time from the conductive state to the blocked state is increased, because the minority electrical charges stored in certain regions of the structure take a certain time to disappear.

According to the present invention there is provided a solid-state two-state logic circuit inverter component comprising in combination a first and a second complementary transistor forming a pnpn or an npnp structure, the base of said first transistor being the emitter of the second, the collector of said first transistor, being the base of the second, the whole being integrated upon the same semiconductor substrate, a two terminal element having a first terminal connected to said base of said second transistor and a second terminal to the collector of said second transistor, and capable of establishing between said terminals, a fixed difference of potential lower than that of said second transistor base-emitter voltage when the corresponding junction is conducting, a supply of constant d.c. current being connected to said base of said first transistor, the emitter of the last mentioned transistor being grounded.

The invention will be better understood from the following description in conjunction with the accompanying drawings, wherein:

Figure 1 shows the basic circuit of the component according to the invention;

Figure 2 diagrammatically illustrates one embodiment of a logic inverter comprising an element according to the invention;

Figure 3 is a cross-section through the logic inverter illustrated in Figure 2 integrated on a single substrate.

Figure 1 is the basic circuit diagram of the component according to the invention.

The Component shown in Figure 1 comprises two complementary npn and pnp transistors, namely the two transistors T_1 and T_2.

The emitter of the transistor T_1 is connected to ground terminal E, its base is connected to the *p*-type emitter of the transistor T_2 and its collector is connected to the *n*-type base of the transistor T_2. A Schottky diode DS is connected between the base of the transistor T_2 and its collector.

The base of the transistor T_1 and the emitter of the transistor T_2 are connected to a constant current supply which supplies a current I.

When the structure is conductive, the current I divides into two parts I_1 and I_2, with $I=I_1+I_2$.

The current I_1 is injected into the base of the transistor T_1 and renders it conductive.

The result of this is that the collector of the transistor T_1 is connected to earth.

The same applied to the base of the transistor T_2. In this transistor, the p-n base emitter junction is thus unblocked.

The potential of the emitter of this transistor is substantially equal to 0.7 volt.

Since the base of the transistor T_2 is connected to earth, this transistor is also unblocked and the Schottky diode is

conductive. Now, it is known that when a Schottky diode is conductive, there is a potential difference of 0.3 volt, i.e. less than 0.7 volt, between its terminals.

The transistor T_2 is the seat of a current I_2 of which the object is to accelerate the desaturation of the transistor T_1. Since the sum $I=I_1+I_2$ is constant, if I_1 increases, I_2 decreases and vice versa.

A structure such as this may be used in the inverter illustrated in Figure 2.

Figure 2 again shows the two transistors T_1 and T_2 and the Schottky diode DS connected in the same way as in the preceding Figure.

The base of the transistor T_1 is connected to the input B of the structure. The constant current source CC is connected to the point B through a transistor T_3 of which the *p*-type emitter is connected to one terminal of this source, its base to the base of the transistor T_2 and its collector to the point B, i.e. to the base of the transistor T_1.

The current arriving at the collector of transistor T_3 is α I, α being the gain of the transistor T_3.

If the point B is at a voltage Level termed "1", for example 0.7 volt, the transistor T_1 is conductive. Its collector is connected to earth as is the base of the transistor T_2.

There are two possible outputs, the output C_1 on the collector of the transistor T_1, which is then at the level "0" (earth potential). Since the Schottky diode is then also conductive, the collector of the transistor T_2 will be at 0.3 volt, i.e. the output C_2.

If B, state "0", is at the potential or below the potential of 0.3 volt, the transistor T_1 is blocked by its base. C_1 is disconnected from earth and is at the potential of the base of the transistor T_3. This corresponds to the state "1" of the output C_1. The output C_2 will also be at the potential of 0.7 volt due to the blocking of the transistor T_2 of which the base will be at 0.7 volt because it is connected to the base of the transistor T_3 which is conductive. The current I is entirely directed to point B (potential near to 0).

Figure 3 shows how the structure illustrated in Figure 2 may be integrated on one and the same substrate.

The structure is integrated on a *p*-type substrate 1.

An *n*-type layer 2 has been deposited onto this substrate for example by epitaxial growth. Two *n*+-type buried layers 3 and 4 have been diffused by known means at the interface of the two *n*-type and *p*-type layers 1 and 2. Finally, three *p*+-type insulating pits 5 have been diffused from the free surface of the *n*-type layer 2 to the layer 1 so as to form two compartments insulated from one another in the structure.

The whole has been covered with a layer of oxide for example by oxidation "in situ". If the substrate is of silicon, the layer 10 may be a layer of the oxide SiO_2, i.e. silica. The left-hand compartment contains the elements enabling the constant current source to be formed. The right-hand compartment contains the component according to the invention.

It is this latter structure which will be described first.

Three regions 6, 7, 8 and 9, respectively of p-type conductivity (regions 6, 7 and 8) and of n+-type conductivity (region 9), are diffused or implanted in this compartment.

In the layer of silica 10, which can have been deposited after the operations of diffusion or implantation, there have been opened the contact S on the layer 6, the contact B on the layer 7, the contact C_2 on the layer 8 and on the layer 2 and the contact C_1 on the layer 9.

In the p-type layer 7, there has been implanted or diffused an n-type region 11 in which a contact E has been opened. The layer 11 again contains the emitter of the transistor T_1, the layer 7 its base and the layer 9 its collector with one of the output contacts C_1 on the system.

The contact C_2 on the layer 8 and 2 is the Schottky contact of Figure 2.

The structure is therefore very easy to integrate and has low speed and consumption.

WHAT WE CLAIM IS:—

1. A solid-state two-state logic circuit inverter component comprising in combination a first and a second complementary transistor forming a pnpn or an npnp structure, the base of said first transistor being the emitter of the second, the collector of said first transistor, being the base of the second, the whole being integrated upon the same semiconductor substrate, a two terminal element having a first terminal connected to said base of said second transistor and a second terminal to the collector of said second transistor, and capable of establishing between said terminals, a fixed difference of potential lower than that of said second transistor base-emitter voltage when the corresponding junction is conducting, a supply of constant d.c. current being connected to said base of said first transistor, the emitter of the last mentioned transistor being grounded.

2. A component as claimed in claim 1, wherein, in the first transistor, the current flows perpendicularly of the faces of the

substrate and, in the second transistor, parallel to those faces.

3. An element as claimed in claim 1, wherein the constant current source comprises a transistor having a base connected to said base of the second transistor and a collector to said base of the first transistor.

4. A solid state two-state component for logic circuit, substantially as hereinbefore described with reference to Figure 1, or Figures 1 and 2, or Figures 1 to 3 of the accompanying drawings.

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Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1980
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

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Sheet 1

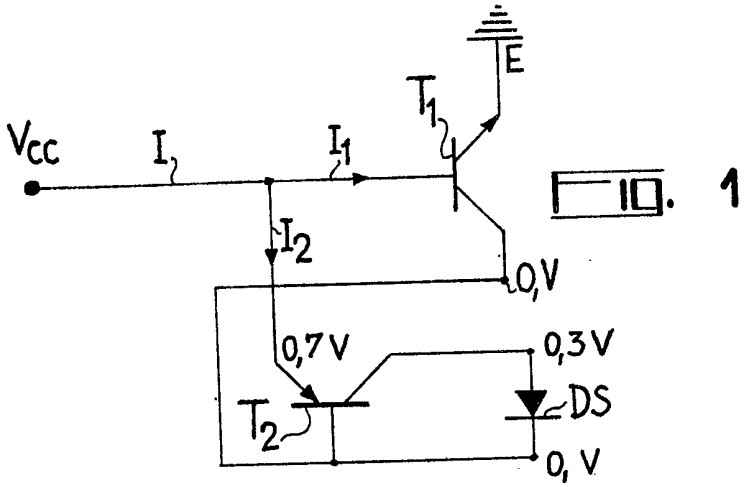

FIG. 1

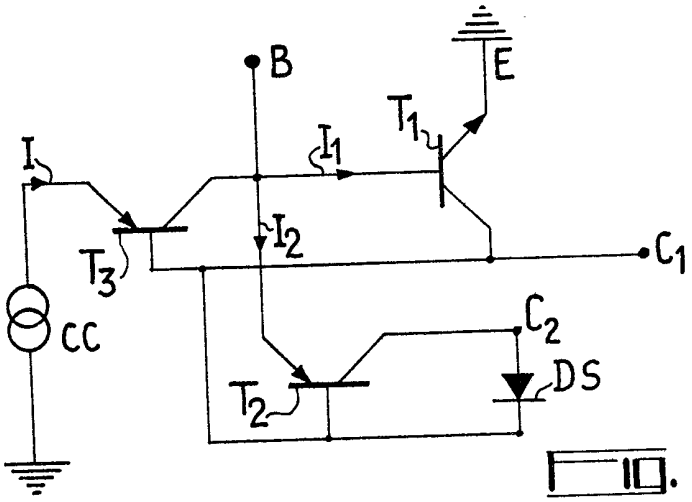

FIG. 2

1572878 COMPLETE SPECIFICATION

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Sheet 2

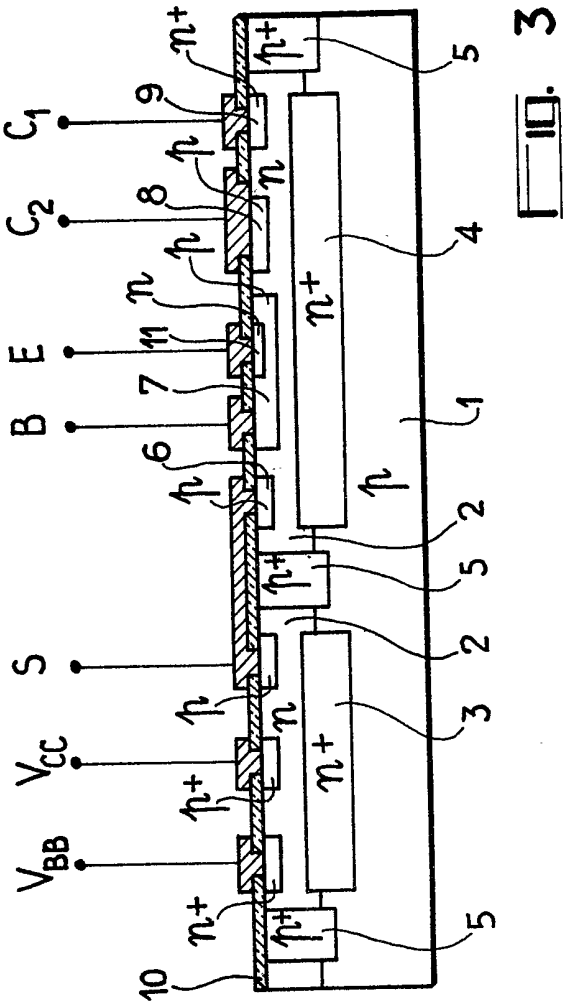

FIG. 3