



(51) International Patent Classification:

H01L 33/48 (2010.01) *H01L 33/62* (2010.01)
H01L 33/56 (2010.01)

(21) International Application Number:

PCT/EP2016/073301

(22) International Filing Date:

29 September 2016 (29.09.2016)

(25) Filing Language:

English

(26) Publication Language:

English

(71) Applicant: **OSRAM OPTO SEMICONDUCTORS GMBH** [DE/DE]; Leibnizstr. 4, 93055 Regensburg (DE).

(72) Inventors: **LIM, Choo Kean**; E-Park, 2C-24-07, Jalan Batu Uban, Penang, 11700 (MY). **NENG, Siang Min**; 50B-26-06, Persiaran Minden 1, U-Garden, Gelugor, Penang, 11700 (MY). **OR, Choon Keat**; Block 11-9-6, Lintang Paya Terubong 4, Ayer Itam, Penang, 11060 (MY). **KOAY, Seong Tak**; 19, Jalan Ismail Cik Mat, Georgetown, Penang, 10460 (MY).

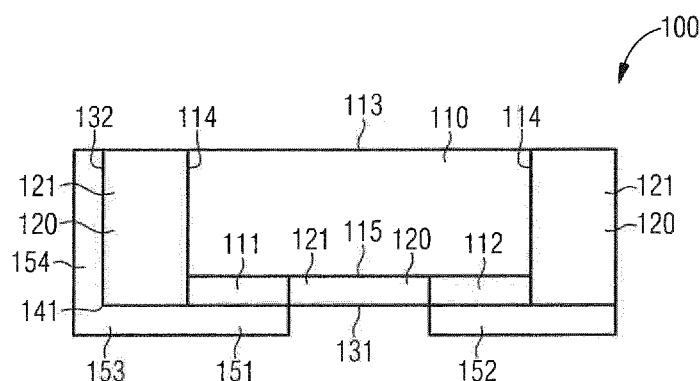
(74) Agent: **PATENT ATTORNEYS WILHELM & BECK**; Prinzenstr. 13, 80639 Munich (DE).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

(54) Title: OPTOELECTRONIC SEMICONDUCTOR CHIP PACKAGE AND MANUFACTURING METHOD THEREOF

FIG 1



(57) Abstract: The scope of the invention is an optoelectronic semiconductor package, comprising an optoelectronic semiconductor chip, which comprises a first contact pad and a second contact pad for applying an electric voltage to the optoelectronic semiconductor chip and a light emitting face. The optoelectronic package further comprises an isolating material adjacent to the optoelectronic semiconductor chip forming a housing of the optoelectronic semiconductor chip. The housing comprises walls. The light emitting face of the optoelectronic semiconductor chip is uncovered by the isolating material. A part of the first contact pad and a part of the second contact pad are free from the isolating material. The first contact pad is arranged at a first wall of the housing, which is opposite to the emitting face. The optoelectronic package further comprises a first contact layer in electrical contact with the first contact pad, which is arranged at the first wall and at a second wall of the housing, extending over a first edge between the first and the second wall of the housing. A second contact layer is in electrical contact with the second contact pad and arranged at a wall of the housing.

Published:

— *with international search report (Art. 21(3))*

OPTOELECTRONIC SEMICONDUCTOR CHIP PACKAGE AND MANUFACTURING METHOD
THEREOF

DESCRIPTION

5 The invention refers to an optoelectronic semiconductor chip package. Optoelectronic semiconductor chip packages may be implemented with small dimensions of the package compared to the semiconductor chip size. For electrical connection of the semiconductor chip, usually lead frames are used. A main dis-
10 advantage of the approach of using lead frames in such optoelectronic semiconductor chip packages is that these packages only allow for a bottom soldering, but not side soldering.

An assignment of the invention is to provide an improved op-
15 toelectronic semiconductor chip package. Another assignment of the invention is to provide a fabrication method of such an optoelectronic semiconductor chip package.

The solution of these assignments is disclosed in the inde-
20 pendent claims of this invention. Preferred embodiments are disclosed in the dependent claims.

An optoelectronic semiconductor package comprises an optoelectronic semiconductor chip. The optoelectronic semiconductor chip comprises a first contact pad and a second contact pad for applying an electric voltage to the optoelectronic semiconductor chip. Additionally, the optoelectronic semiconductor chip comprises a light emitting face. The optoelectronic semiconductor package further comprises an isolating
25 material adjacent to the optoelectronic semiconductor chip forming a housing of the optoelectronic semiconductor chip. The housing comprises walls. The light emitting face of the optoelectronic semiconductor chip is uncovered by the isolating material. A part of the first contact pad and a part of
30 the second contact pad are free from the isolating material to allow for electrical contacting of the contact pads. The first contact pad is arranged at a first wall of the housing opposite to the emitting face of the optoelectronic semicon-
35

ductor chip. The optoelectronic semiconductor package further comprises a first contact layer in electrical contact with the first contact pad. The first contact layer is arranged at the first wall and at a second wall of the housing and extends over a first edge between the first wall and the second wall of the housing. Additionally, the optoelectronic semiconductor package comprises a second contact layer in electrical contact with the second contact pad, which is arranged on a wall of the housing. The second contact layer may be arranged at the first wall of the housing or at another wall of the housing. As the first contact layer of the optoelectronic semiconductor package extends over the first edge between the first and the second wall of the housing, the first contact layer extends to a side wall of the housing. Therefore, side soldering of said optoelectronic semiconductor package is possible. This allows for a greater variety of applications of such an optoelectronic semiconductor package.

In one embodiment of the invention, the housing comprises a first lug extending from the second wall of the housing. The first lug may be adjacent to the light emitting face of the optoelectronic semiconductor chip or at another place of the second wall. The first contact layer is arranged on the first lug and extends over a second edge between the first lug and the second wall. Therefore, the first contact layer extends over the first edge and the second edge, thus forming a shape which allows for easy aligning of the optoelectronic semiconductor package.

In one embodiment of the invention, the second contact pad is arranged at the first wall of the housing and the second contact layer is arranged on the first and a third wall of the housing. The second contact layer extends over a third edge between the first and the third wall of the housing. This allows for side soldering of the second contact layer as well.

In one embodiment, the housing comprises a second lug extending from the third wall of the housing. The second contact

layer is arranged on the second lug and extends over a fourth edge between the second lug and the third wall.

5 In one embodiment, the second wall and the third wall are on opposite sides of the housing. If the second wall and the third wall are on opposite sides of the housing, the side soldering parts of the first contact layer and the second contact layer are on opposite sides of the housing as well. Therefore, several such optoelectronic semiconductor packages
10 can be arranged right next to each other and can be connected from the side.

In one embodiment of the invention, the first contact layer and/or the second contact layer comprise galvanically deposited metal. Galvanic deposition of metal is suitable for
15 forming contact layers, which can easily be extended over edges, as during the galvanic deposition the deposited metal follows the shape of the underlying housing.

20 In one embodiment of the invention, the first contact layer and/or the second contact layer comprise copper. Copper is a metal, which can be easily galvanically deposited and which allows for good electrical connectivity. Therefore, copper is a very suitable material for an optoelectronic semiconductor
25 package with contact layers that are suited for side soldering.

In one embodiment of the invention, the housing is formed by a mold process. Mold processes are easily performed. There-
30 fore, the forming of the housing using a mold process allows for easy implementation and cheap production of the chip scaled optoelectronic semiconductor package.

In one embodiment of the invention, the isolating material
35 forming the housing comprises a silicone compound and/or titanium dioxide. Silicone compounds can be easily molded and are therefore suitable for the housing. Titan dioxide, in the form of titan dioxide powder, can be applied to the silicone

compound or to another mold material and therefore lead to a white appearance of the housing, which is favorable for optoelectronic semiconductor devices.

- 5 A method of producing the optoelectronic semiconductor package comprises the steps:
- Providing a light emitting optoelectronic semiconductor chip with a light emitting face, a first contact pad and a second contact pad;
 - 10 - Embedding the optoelectronic semiconductor chip in an isolating material. The isolating material forms a housing with walls. The first contact pad is arranged at a first wall of the housing. The light emitting face of the optoelectronic semiconductor chip is uncovered by the isolating material;
 - 15 - Deposition of a first contact layer, which is in electrical contact with the first contact pad and arranged on the first wall and a second wall of the housing. The first contact layer extends over a first edge between the first and the second wall of the housing;
 - 20 - Deposition of a second contact layer, which is in electrical contact with the second contact pad.

In one embodiment, the deposition of the contact layers comprises the steps:

- 25 - Sputtering of a first metal layer on the contact pads and the isolating material, covering at least two external walls of the housing extending over an edge between two external walls of the housing. The first metal layer may extend over the first edge between the first and the second wall of the
- 30 housing;
- Structuration of the first metal layer to electrically disconnect the contact pads from each other;
 - Galvanic deposition of a second metal layer on top of the first metal layer, forming two contact layers.

35

As the first metal layer extends over an edge of the housing, the galvanically deposited second metal layer on top of the first metal layer extends over said edge as well.

In one embodiment of the invention, the structuration of the first metal layer is performed before the galvanic deposition of the second metal layer is performed and comprises the

5 steps:

- depositing of a photo-resist on top of the first metal layer;

- partially illuminating of the photo-resist;

- developing of the photo-resist, forming dissolvable and
10 non-dissolvable parts of the photo-resist regarding a first solvent;

- dissolving the dissolvable parts of the photo-resist using the first solvent;

- applying of an etchant to the first metal layer at loca-
15 tions where the photo-resist has been dissolved;

- removing of the remaining photo-resist using a second solvent.

With these intermediate steps, the first metal layer can be
20 structured in at least two parts, therefore breaking the connection between the first and the second contact pad and thus allowing for electric isolation of the two contact pads from each other. Afterwards, the galvanic deposition is performed in a way that the contact layers remain isolated from each
25 other as well.

In one embodiment of the invention, the deposition of the second metal layer is performed in between the process steps leading to the structuration of the first metal layer. The
30 galvanic deposition and the structuration comprise the steps:

- depositing of a photo-resist on top of the first metal layer;

- partially illuminating of the photo-resist;

- developing of the photo-resist, forming dissolvable and
35 non-dissolvable parts of the photo-resist regarding a first solvent;

- dissolving the dissolvable parts of the photo-resist using the first solvent;

- galvanic deposition of the second metal layer, wherein areas of the first metal layer covered with remaining photo-resist are kept free from the second metal layer. The thickness of the second metal layer is larger than the thickness of the first metal layer;
- removing of the remaining photo-resist using a second solvent;
- applying of an etchant to the first metal layer and the second metal layer in a way, that the first metal layer is completely removed in the areas previously covered with the non-dissolvable parts of the photo-resist regarding the first solvent.

With this approach, the remaining photo-resist after dissolving the dissolvable parts of the photo-resist functions as a barrier for the second metal layer during the galvanic process. After the galvanic process the first contact layer and the second contact layer are still in electrical contact with each other through the first metal layer. With a subsequently performed etching process, the connection of the first contact layer and the second contact layer can be removed by removing the first contact layer in the areas previously covered with the non-dissolvable parts of the photo-resist. During this process, parts of the second metal layer are also removed, but as the second metal layer has a larger thickness as the first metal layer, the contact layers stay intact.

In one embodiment, the contact pads of the optoelectronic semiconductor chip are covered by the isolating material during the embedding process. Afterwards, in an additional step, parts of the isolating material are removed to expose the contact pads.

In one embodiment of the invention, the embedding of the optoelectronic semiconductor chip within the isolating material is performed as mold process.

The above described properties, features and advantages of this invention as well as the method of obtaining them, will be more clearly and obviously understandable in the context of the following description of the embodiments, which are explained in more detail in the context of the figures.

In schematic illustration show

Figs. 1 - 8 cross sections and top views of different embodiments an optoelectronic semiconductor chip package; and

Figs. 9 - 20 intermediate steps during the fabrication process.

Fig. 1 shows a cross section of an optoelectronic semiconductor package 100. The optoelectronic semiconductor package 100 comprises an optoelectronic semiconductor chip 110. The optoelectronic semiconductor chip 110 comprises a first contact pad 111 and a second contact pad 112, wherein both contact pads 111, 112 are located on a bottom face 115 of the optoelectronic semiconductor chip 110. Opposite to the bottom face 115, the optoelectronic semiconductor chip 110 comprises a light emitting face 113. Thus, the light emitting face 113 is a top face of the optoelectronic semiconductor chip 110. A voltage applied to the contact pads 111, 112 leads to light emitting through the light emitting face 113 of the optoelectronic semiconductor chip 110. Adjacent to the optoelectronic semiconductor chip 110 an isolating material 120 forms a housing 121. The housing 121 is located at side faces 114 of the optoelectronic semiconductor chip 110 and in between the contact pads 111, 112 on the bottom face 115 of the optoelectronic semiconductor chip 110. The side faces 114 of the optoelectronic semiconductor chip 110 are the faces that are neither the light emitting face 113 nor the bottom face 115. The light emitting face 113 is uncovered by the isolating material 120. The contact pads 111, 112 are free from the isolating material 120 on the bottom face 115. Therefore, the

contact pads 111, 112 are freely accessible from the bottom of the optoelectronic semiconductor chip package 100. The first contact pad 111 is arranged at a first wall 131 of the housing 121. The first wall 131 is a bottom wall of the housing 121, located at the same side of the optoelectronic semiconductor chip 110 than the bottom face 115. The optoelectronic semiconductor package 100 further comprises a first contact layer 151 that is in electrical contact with the first contact pad 111. The first contact layer 151 is arranged at the first wall 131 and at a second wall 132 of the housing 121. In between the first wall 131 and the second wall 132, the housing 121 comprises a first edge 141. The first contact layer 151 comprises a first section 153 located at the first wall 131 and a second section 154 located at the second wall 132, thus extending over the first edge 141 between the first wall 131 and the second wall 132 of the housing 121. The second section 154 of the first contact layer 151 covers the second wall 132 completely. It is also possible to arrange the second section 154 of the first contact layer 151 in a way that only a part of the second wall 133 is covered. The first section 153 and the second section 154 of the first contact layer 151 are perpendicular to each other in the embodiment of fig. 1. Other angles between the first section 153 and the second section 154 of the first contact layer 151 are also possible though.

A second contact layer 152 is in electrical contact with the second contact pad 112 and arranged on the first wall 131 of the housing 121. The second contact pad 112 and the second contact layer 152 may be arranged at another location of the optoelectronic semiconductor chip 110, for example at a side face 114 of the optoelectronic semiconductor chip 110.

Fig. 2 shows a top view of the optoelectronic semiconductor chip package 100 of fig. 1. The rectangular light emitting face 113 of the optoelectronic semiconductor chip 110 is encircled by the isolating material 120 forming the housing 121 adjacent to the side faces 114 of the optoelectronic semicon-

ductor chip 110. At the second wall 132 of the housing facing one of the side faces 114, the second section 154 of the first contact layer 151 is arranged and visible from the top. The first wall 131 of the housing 121 with the first section 153 of the first contact layer 151 is located on the in fig. 2 not visible bottom side of the optoelectronic semiconductor chip package 100.

Fig. 3 shows a cross section of an optoelectronic semiconductor package 100, which essentially corresponds to the optoelectronic semiconductor package 100 of Fig. 1. The housing 121 further comprises a first lug 161 extending from the second wall 132. The first lug 161 is in line with the light emitting face 113 of the optoelectronic semiconductor chip 110. A second edge 142 is arranged between the second wall 132 and the first lug 161. The first contact layer 151 extends over the first edge 141 and the second edge 142, thus the first section 153 of the first contact layer 151 touches the first contact pad 111 and the first wall 131. The second section 154 of the first contact layer 151 touches the second wall 132. A third section 155 of the first contact layer 151 touches the first lug 161. The first section 153 and the third section 155 are parallel to each other, the second section 154 is perpendicular to the first section 153 and the third section 155. Other angles between the sections 153, 154, 155 of the first contact layer 151 are also possible though.

Fig. 4 shows a top view of the optoelectronic semiconductor package 100 of fig. 3. The first lug 161 extends the housing 121 over the (not visible) second wall 132 of the housing 121. The partial area of the light emitting face 113 compared to the total area of the optoelectronic semiconductor package is thus smaller than in fig. 2. The first lug 161 exhibits the same width than the second wall 132. It is also possible, that the first lug 161 has a lower width. The width of the first lug 161 may be similar to the size of the light emitting face 113 of the optoelectronic semiconductor chip.

Fig. 5 shows another cross section through an optoelectronic semiconductor package 100 which is essentially similar to the previous described embodiments. The housing 121 comprises a first lug 161 as described in Fig. 3. A third edge 143 is located between the first wall 131 and a third wall 133, wherein the third wall 133 is opposite to the second wall 132 of the housing 121. The second contact layer 152 extends over the third edge 143, thus touching the second contact pad 112, the first wall 131 and the third wall 133. A first section 153 of the second contact layer 152 is arranged at the first wall 131, whereas a second section 154 of the second contact layer 152 is arranged at the third wall 133. The first section 153 and the second section 154 are perpendicular, other angles are possible as well though.

The second wall 132 and the third wall 133 may be walls of the housing 121 that are not on opposite sides of the housing 121 as well.

Fig. 6 shows another embodiment of an optoelectronic semiconductor package 100 with essentially the same features as the optoelectronic semiconductor package of Fig. 5. The housing 121 comprises a second lug 162 extending from the third wall 133 of the housing. In between the third wall 133 and the second lug 162, the housing 121 comprises a fourth edge 144. The second contact layer 152 extends over the third edge 143 and the fourth edge 144, thus touching the second contact pad 112, the first wall 131, the third wall 133 and the second lug 162. The second contact layer 152 comprises three sections, a first section 153 touching the second contact pad 112 and the first wall 133, a second section 154 touching the third wall 133 and a third section 155 touching the second lug 162. The first section 153 of the second contact layer 152 and the third section 155 of the second contact layer 152 are parallel to each other, the second section 154 of the second contact layer 152 is perpendicular to the first section 153 of the second contact layer 152 and the third sec-

tion 155 of the second contact layer 152. Other angles between the sections 153, 154, 155 of the second contact layer 152 are also possible though.

5 For the embodiments of the Figs. 3 to 6 the first lug 161 and/or the second lug 162 may be arranged at another position of the second wall 132 and the third wall 133 respectively. In the embodiments of figs. 5 or 6, the third wall 133 is arranged opposite to the second wall 132 of the housing 122. It
10 is also possible, to arrange the third wall 133 at another side wall of the housing 121, not opposite to the second wall 132.

The optoelectronic semiconductor chip package 100 may com-
15 prise a first contact layer 151 similar to fig. 1 and a second contact layer 152 similar to fig. 5, thus omitting the first lug 161 in fig. 5.

The optoelectronic semiconductor chip 110 and the housing 121
20 are of a cuboid shape. Other shapes, particularly for the housing 121 are also possible, for example prisms like cylinders or a prism with a hexagonal base.

Fig. 7 shows another cross section of an optoelectronic semiconductor package 100. The optoelectronic semiconductor package 100 comprises an optoelectronic semiconductor chip 110
25 with a first contact pad 111, a second contact pad 112, both arranged at a bottom face 115 of the optoelectronic semiconductor chip 110 and a light emitting face 113 opposite of the bottom face 115. An isolating material 120 forms a housing of
30 the optoelectronic semiconductor chip 110. The housing 122 comprises a first lug 161 and a second lug 162. The bottom face 115 of the semiconductor chip 110 is above a bottom side 163 of the first lug 161 and a bottom side 163 of the second
35 lug 162. Thus, the optoelectronic semiconductor chip 110 is embedded in the part of the housing 121 that is formed by the first lug 161 and the second lug 162. To allow for the embedding, the thickness of the first lug 161 and the second lug

162 is larger than thickness of the optoelectronic semiconductor chip 110, relatively to a direction parallel to a connecting line extending from the bottom face 115 to the light emitting face 113 of the optoelectronic semiconductor chip 110. In a middle part 127 of the housing 121, the housing 121 is thicker than in the outer parts of the housing 121, formed by the lugs 161, 162. A first wall 131 is arranged at the housing 121 in the middle part 127 of the housing 121, thus forming a protrusion with the first wall 131 as a bottom wall of the housing 121. The first wall and the bottom sides 163 of the lugs 161, 162 in parallel to each other. A first inner connector 123 is located within the housing 121 and adjacent to the first connector pad 111. A second inner connector 124 is also located within the housing 121 and electrically connected to the second contact pad 112. The inner connectors 123, 124 may be regarded as parts of the first contact pad 111 and the second contact pad 112 respectively. A second wall 132 is located in between the first wall 131 and the bottom side 163 of the first lug 161. In between the first wall 131 and the second wall 132 a first edge 141 is located. Between the second wall 132 and the first lug 161 a second edge 142 is located. The first contact layer 151 extends over the first edge 141 and the second edge 142. The first contact layer 151 comprises a first section 153 adjacent to the first wall 131, a second section 154 adjacent to the second wall 132 and a third section 155 adjacent to the bottom side 163 of the first lug 161. The second contact layer 152 is arranged extending over a third edge 143 in between the first wall 131 and a third wall 133 and a fourth edge 144 in between the third wall 133 and the second lug 162, symmetrically arranged at an opposite side of the optoelectronic semiconductor device 100. The second contact layer 152 comprises a first section 153 adjacent to the first wall 131, a second section 154 adjacent to the third wall 133 and a third section 155 adjacent to the bottom side 163 of the second lug 162.

The first section 153 and the third section 155 of both contact layers 151, 152 are parallel to each other, the second section 154 is perpendicular to the first section 153 and the third section 155 of both contact layers 151, 152. Other angles between the sections 153, 154, 155 of the first contact layer 151 and the second contact layer 152 are also possible though.

Fig. 8 shows a top view of the optoelectronic semiconductor chip package 100 of fig. 7 with the housing 121 consisting of the isolating material 120. The isolating material is arranged circumventing the light emitting face 113 of the rectangular optoelectronic semiconductor chip 110.

In one embodiment of the invention, the first contact layer 151 and/or the second contact layer 152 comprise galvanically deposited metal.

The optoelectronic semiconductor chip 110 may be square with a side length of 1 mm. The optoelectronic package 100 can may be square with a side length of 1.4 mm. The thickness of the housing 121 thus is 0.2 mm. Another possibility for the optoelectronic semiconductor chip 110 is a rectangular shape of 0.2 x 1.2 mm, with a size of the rectangular optoelectronic semiconductor package of 0.3 x 1.8 mm. The second set of sizes is particularly applicable to the embodiment of Figs. 7 and 8.

In one embodiment, the first contact layer 151 and/or the second contact layer 152 comprise copper. In one embodiment, the housing 121 is formed by a mold process. In one embodiment, the isolating material 120 forming the housing 121 comprises a silicone compound and/or titan dioxide. The titan dioxide may be applied in the form of a titan dioxide powder mixed into the isolating material 121.

Figs. 9 to 19 show intermediate products during a fabrication of an optoelectronic semiconductor package according to the

invention. Figs. 9 to 15 relate to a first production method, whereas after the intermediate product of fig. 11 is achieved, a second production method can be implemented as well. The further steps of the second production method explained in figs. 16 to 19.

Fig. 9 shows a cross section of an optoelectronic semiconductor chip 110 with a first contact pad 111 and a second contact pad 112 arranged at a bottom face 115 of the optoelectronic semiconductor chip 110. A light emitting face 113 is arranged opposite of the bottom face 115. The optoelectronic semiconductor chip 110 is comparable to one of the optoelectronic semiconductor chips 110 of Figs. 1 to 8. The optoelectronic semiconductor chip 110 is of cuboid shape, but may comprise another shape like a hexagonal prism as well.

After the optoelectronic semiconductor chip 110 is provided, it is embedded into an isolating material 120. The isolating material 120 forms a housing 121 of the optoelectronic semiconductor chip. The housing is arranged at the bottom face 115 as well as side faces 114 of the optoelectronic semiconductor chip 110. The contact pads 111, 112 are arranged at a first wall 131 of the housing 121 and at least partially free of the isolating material 120. The light emitting face 113 is also uncovered by the isolating material 120. On top of the side faces 114 of the optoelectronic semiconductor chip 100 the housing 121 forms a second wall 132 and a third wall 133. A first edge 141 is located in between the first wall 131 and the second wall 132. A third edge 143 is located in between the first wall 131 and the third wall 133. The isolating material 121 comprises a cuboid shape, but may also be a cylinder or a hexagonal prism. The isolating material 120 in which the optoelectronic semiconductor chip 110 is embedded, may comprise first and/or second lugs 161, 162 according to the figs. 3 to 8.

In a subsequent process step, a first contact layer 151 is deposited in a way, that it is arranged on the first wall

131, the second wall 132 and in electrical contact with the first contact pad 111. Therefore, the first contact layer 151 extends over the first edge 141. A second contact layer 152 is deposited onto the first wall 131 and in electrical contact with the second contact pad 112. The optoelectronic semiconductor package 100 then is similar to the package shown in figs. 1 to 6.

Fig. 11 shows a cross section of the optoelectronic semiconductor chip 110 with the housing 120 after a first metal layer 170 has been sputtered on the contact pads 111, 112 and the housing 121. The first metal layer 170 covers the first wall 131, the second wall 132 and the third wall 133. The first metal layer 170 may cover just the first wall 131 and the second wall 132, not covering the third wall 133.

After the sputtering of the first metal layer 170 the first metal layer 170 is structured to electrically disconnect the first contact pad 111 from the second contact pad 112. Another process step is a galvanic deposition of a second metal layer on top of the first metal layer 170 thus forming the first contact layer 151 and the second contact layer 152. The first production method relates to the structuration of the first metal layer 170 before the galvanic deposition of the second metal layer takes place. The second production method relates to a structuration of the first metal layer 170 after the galvanic deposition of the second metal layer takes place.

A possibility for the structuration of the first metal layer 170 is shown in Fig. 12, which shows a cross section of the optoelectronic semiconductor chip 110 after the subsequent process step of depositing a photo-resist 180 on top of the first metal layer 170 adjacent to the bottom face 113. The photo-resist 180 is then partially illuminated, shown in Fig. 12 by arrows representing the illuminating light and a mask 190 blocking part of the light illuminating the photo-resist 180. The photo-resist can therefore be separated in a first

part 181 illuminated by the light and a second part 182, not illuminated by the light. After the illumination of the photo-resist 180 the photo-resist 180 is developed, therefore forming dissolvable and non-dissolvable parts of the photo-resist 180 regarding a first solvent. In the example of Fig. 12, the second part 182 of the photo-resist, which is not illuminated by the light, is dissolvable regarding a first solvent, whereas the first parts 181 are not dissolvable due to the illumination. The mask 190 and therefore the second part 182 of the photo-resist 180 is located in between the first contact pad 111 and the second contact pad 112.

After developing the photo-resist 180 and the removing of the second part 182 of the photo-resist 180, an intermediate product shown in Fig. 13 is achieved. The first parts 181 of the photo-resist 180 cover the first metal layer 170 in areas adjacent to the contact pads 111, 112. In between the contact pads 111, 112, the first metal layer 170 is not covered by the photo resist 180 anymore.

Fig. 14 shows the optoelectronic semiconductor chip 110 and the intermediate product after a next process step, in which the first metal layer 170 in between the first contact pad 111 and the second contact pad 112 has been etched using an etchant. Therefore the first contact pad 111 and the second contact pad 112 are not in electrical contact anymore as the first metal layer 170 connecting these two contact pads 111, 112 has been removed. Subsequently, the remaining first parts 181 of the photo-resist 180 are removed using a second solvent which is capable of dissolving these first parts 181 of the photo-resist 180.

In a final process step, a second metal layer forming a first contact layer 151 and a second contact layer 152 is deposited galvanically on top of the remaining parts of the first metal layer 170 and thus forming the contact layers 151 and 152. The product after this final process step is shown in fig. 15. Using all these described process steps from Fig. 9 to

Fig. 15, an optoelectronic semiconductor package 100 is achieved.

It is also possible to use a photo-resist 180 which is dissolvable for the first solvent after illumination and non-dissolvable, if the photo-resist 180 has not been illuminated by light. For the process step described in Fig. 12, a different mask 190 may then be used, to achieve the dissolvable and non-dissolvable parts of the photo-resist 180 according to Fig. 13.

Figs. 16 to 19 describe another method of fabrication of an optoelectronic semiconductor package according to the invention. The first steps of this process are similar to the Figs. 9 to 11. After the deposition of the photo-resist 180 on top of the first metal layer 170, the photo-resist 180 is partially illuminated. In this case, as shown in Fig. 16, the non-dissolvable first parts 181 of the photo-resist 180 are in between the first contact pad 111 and the second contact pad 112.

Fig. 17 shows an intermediate product after a next process step, in which a second metal layer has been galvanically deposited on top of the first metal layer 170, thus forming the first contact layer 151 and the second contact layer 152. In between the first contact pad 111 and the second contact pad 112 the photo-resist 180 has covered a first metal layer 170 thus not allowing for the galvanic deposition to take place in between the first contact pad 111 and the second contact pad 112, as the photo-resist 180 blocks the galvanic deposition.

Fig. 18 shows a cross section to an intermediate product after the next process step of removing the remaining photo-resist using a second solvent. The first metal layer 170 still connects the first contact pad 111 and the second contact pad 112. The second metal layer forming the first con-

tact layer 151 and the second contact layer 152 has a larger thickness than the first metal layer 170.

In a subsequent step, the optoelectronic semiconductor package 100 is exposed to an etchant in a way that the first metal layer 170 is completely removed in the area previously covered with the non-dissolvable first part 181 of the photoresist 180. Some minor parts of the second metal layer are thereby removed by the etchant as well. Due to this etching step, the first contact pad and the second contact pad are electrically isolated from each other. The optoelectronic semiconductor chip package after the etching process is shown in fig. 19.

In one embodiment of the invention, the isolating material 120 and thus the housing 121 is formed using a mold process.

The first metal layer 170 may be used as a seed layer for the subsequent galvanic deposition of the second metal layer.

Both metal layers may consist of the same metal. Therefore, the first metal layer 170 and the first contact layer 151 as well as the second contact layer 152 consist of the same metal and the boundary between the first metal layer 170 and the first contact layer 151 as well as the second contact layer 152 may not be determinable.

Fig. 20 shows another intermediate product during the process step. In this intermediate step, the optoelectronic semiconductor chip 110 has been embedded within an isolating material 120 forming a housing 121. During the embedding process, the first contact pad 111 and the second contact pad 112 have been covered by the isolating material 120 as well. In a subsequent step, lower parts 125 of the isolating material can be removed. Upper parts 126 of the isolating material 120 remain adjacent to the optoelectronic semiconductor chip 110. With a dash line the boundary between the upper part 126 and the lower part 125 is indicated in Fig. 20. After removing the lower part 125 of the isolating material, the first con-

tact pad 111 and the second contact pad 112 are exposed. After the removal of the lower parts 125 of the isolating material, the intermediate product looks similar to the one in Fig. 10.

5

With the process steps described in figs. 9 to 20, the various embodiments shown in figs. 1 to 8 can be achieved.

10 The optoelectronic semiconductor chip 110 may be embodied as a light emitting diode or a laser diode.

15 Although the invention was described and illustrated in more detail using preferred embodiments, the invention is not limited to these. Variants of the invention may be derived by a person skilled in the art from the described embodiments without leaving the scope of the invention.

REFERENCE NUMERALS

	100	optoelectronic semiconductor package
	110	optoelectronic semiconductor chip
5	111	first contact pad
	112	second contact pad
	113	light emitting face
	114	side face
	115	bottom face
10	120	isolating material
	121	housing
	123	first inner connector
	124	second inner connector
	125	lower part
15	126	upper part
	127	middle part
	131	first wall
	132	second wall
	133	third wall
20	141	first edge
	142	second edge
	143	third edge
	144	fourth edge
	151	first contact layer
25	152	second contact layer
	153	first section
	154	second section
	155	third section
	161	first lug
30	162	second lug
	163	bottom side
	170	first metal layer
	180	photo-resist
	181	first part
35	182	second part
	190	mask

CLAIMS

1. An optoelectronic semiconductor package (100), comprising:

5

an optoelectronic semiconductor chip (110), wherein the optoelectronic semiconductor chip (110) comprises a first contact pad (111) and a second contact pad (112) for applying an electric voltage to the optoelectronic semiconductor chip (110) and wherein the optoelectronic semiconductor chip (110) comprises a light emitting face (113);

10

15

an isolating material (120) adjacent to the optoelectronic semiconductor chip (110) forming a housing (121) of the optoelectronic semiconductor chip (110), wherein the housing (121) comprises walls (131, 132, 133), wherein the light emitting face (113) of the optoelectronic semiconductor chip (110) is uncovered by the isolating material (120), wherein a part of the first contact pad (111) and a part of the second contact pad (112) are free from the isolating material (120), wherein the first contact pad (111) is arranged at a first wall (131) of the housing (121), wherein the first wall (131) is opposite to the light emitting face (113);

20

25

a first contact layer (151) in electrical contact with the first contact pad (111), wherein the first contact layer (151) is arranged at the first wall (131) and at a second wall (132) of the housing (121), wherein the first contact layer (151) extends over a first edge (141) between the first and the second wall (132) of the housing (121)

30

35

and a second contact layer (152) in electrical contact with the second contact pad (112) and arranged at a wall of the housing (121).

2. The optoelectronic semiconductor package (100) according to claim 1, wherein the housing (121) comprises a first lug (161) extending from the second wall (132) of the housing (121), wherein the first contact layer (151) is arranged on the first lug (161) and wherein the first contact layer (151) extends over a second edge (142) between the first lug (161) and the second wall (132).

3. The optoelectronic semiconductor package (100) according to any of the claims 1 or 2, wherein the second contact pad (112) is arranged at the first wall (131) of the housing (121), wherein the second contact layer (152) is arranged on the first wall (131) and a third wall (133) of the housing (121), wherein the second contact layer (152) extends over a third edge (143) between the first and the third wall (133) of the housing (121).

4. The optoelectronic semiconductor package (100) according to claim 3, wherein the housing (121) comprises a second lug (162) extending from the third wall (133) of the housing (121), wherein the second contact layer (152) is arranged on the second lug (162) and wherein the second contact layer (152) extends over a fourth edge (144) between the second lug (162) and the third wall (133).

5. The optoelectronic semiconductor package (100) according to claims 3 or 4, wherein the second wall (132) and the third wall (133) are on opposite sides of the housing (121).

6. The optoelectronic semiconductor package (100) according to any of the claims 1 to 5, wherein the first contact layer (151) and/or the second contact layer (152) comprise galvanically deposited metal.

7. The optoelectronic semiconductor package (100) according to any of the claims 1 to 6, wherein the first contact

layer (151) and/or the second contact layer (152) comprise copper.

8. The optoelectronic semiconductor package (100) according to any of the claims 1 to 7, wherein the housing (121) is formed by a mold process.

9. The optoelectronic semiconductor package according (100) to any of the claims 1 to 8, wherein the isolating material (120) comprises a silicone compound and/or titan dioxide.

10. A method of producing the optoelectronic semiconductor package according to any of the claims 1 to 9, with the steps:

- Providing a light emitting optoelectronic semiconductor chip with a light emitting face, a first contact pad and a second contact pad;
- Embedding the optoelectronic semiconductor chip in an isolating material, wherein the light emitting face is uncovered by the isolating material, thus forming a housing composed of the isolating material with walls, wherein the first contact pad is arranged at a first wall of the housing;
- Deposition of a first contact layer, wherein the first contact layer is in electrical contact with the first contact pad and wherein the first contact layer is arranged on the first wall and a second wall of the housing, wherein the first contact layer extends over a first edge between the first and the second wall of the housing;
- Deposition of a second contact layer, wherein the second contact layer is in electrical contact with the second contact pad.

11. The method according to claim 10, wherein the contact pads are covered by the isolating material during the embedding process and removing, with an additional step,

parts of the isolating material to expose the contact pads.

12. The method according to any of the claims 10 or 11,
5 wherein the embedding of the optoelectronic semiconductor chip within the isolating material is performed as a mold process.

13. The method according to any of the claims 10 to 12,
10 wherein the deposition of the contact layers comprises the steps:

- Sputtering of a first metal layer on the contact pads and the isolating material, covering at least two external walls of the housing extending over an
15 edge between two external walls of the housing;
- Structuration of the first metal layer to electrically disconnect the contact pads from each other;
- Galvanic deposition of a second metal layer on top of the first metal layer, forming two contact layers.
20

14. The method according to claim 13, wherein the structuration of the first metal layer is performed before the galvanic deposition of the second metal layer is performed and comprises the steps:

- Depositing of a photo-resist on top of the first metal layer;
- Partially illuminating of the photo-resist;
- Developing of the photo-resist, forming dissolvable and non-dissolvable parts of the photo-resist regarding a first solvent;
30
- Dissolving the dissolvable parts of the photo-resist using the first solvent;
- Applying of an etchant to the first metal layer at locations where the photo-resist has been dissolved;
35
- Removing the remaining photo-resist using a second solvent.

15. The method according to claim 13, wherein the galvanic deposition of the second metal layer is performed in between process steps leading to the structuration of the first metal layer, wherein the galvanic deposition and the structuration comprise the steps:

- Depositing of a photo-resist on top of the first metal layer;
- Partially illuminating of the photo-resist;
- Developing of the photo-resist, forming dissolvable and non-dissolvable parts of the photo-resist regarding a first solvent;
- Dissolving the dissolvable parts of the photo-resist using the first solvent;
- Galvanic deposition of the second metal layer, wherein areas of the first metal layer covered with remaining photo-resist are kept free from the second metal layer, wherein the thickness of the second metal layer is larger than the thickness of the first metal layer;
- Removing of the remaining photo-resist using a second solvent;
- Applying of an etchant to the first metal layer and the second metal layer in a way that the first metal layer is completely removed in the areas previously covered with the non-dissolvable parts of the photo-resist regarding the first solvent.

FIG 1

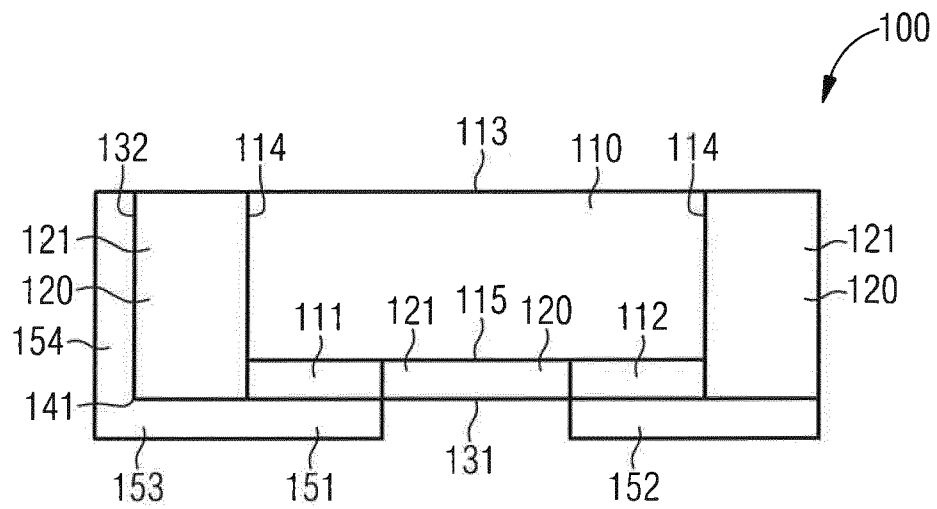
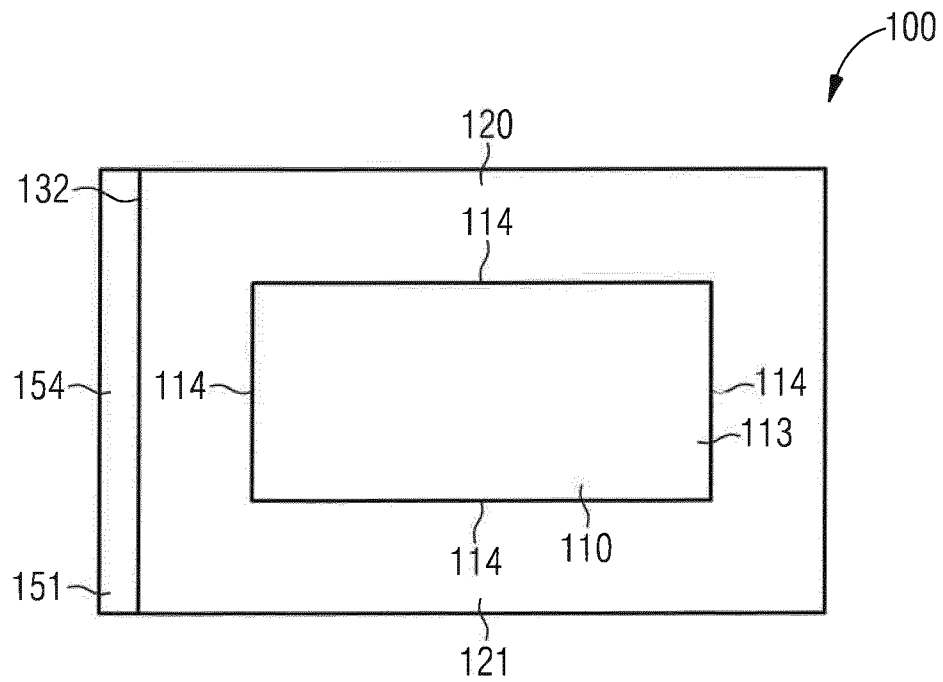


FIG 2



2/10

FIG 3

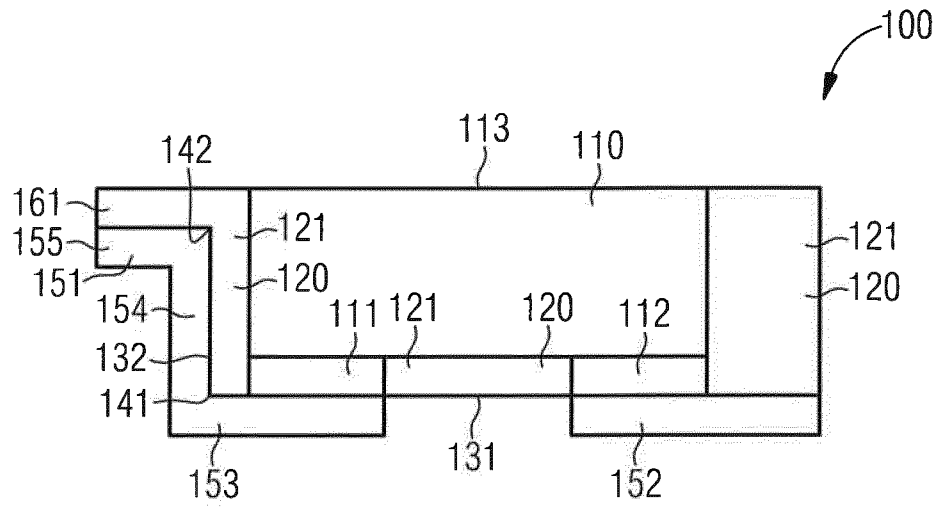
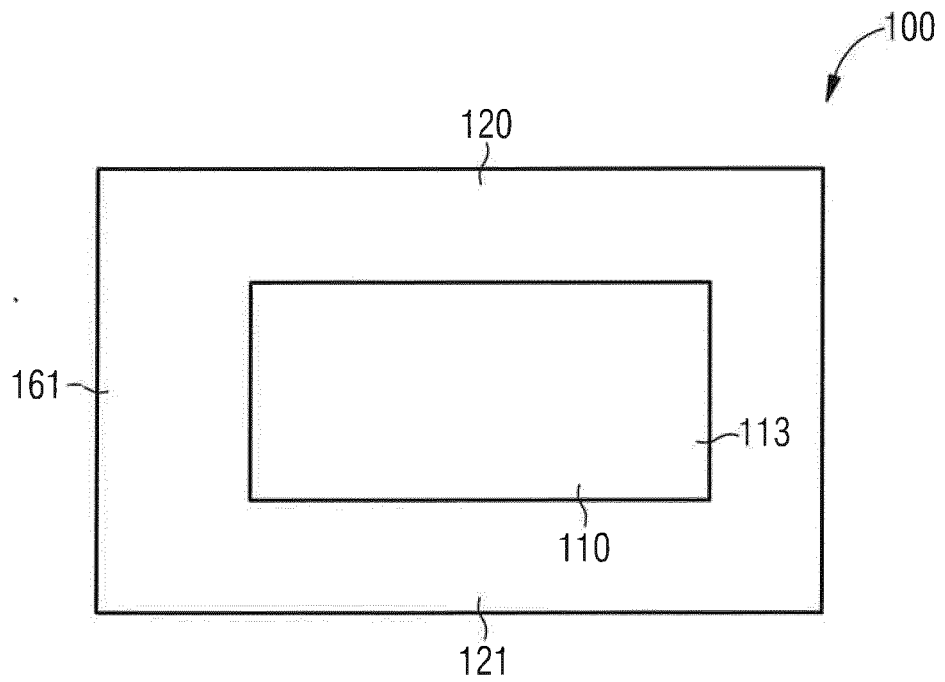


FIG 4



3/10

FIG 5

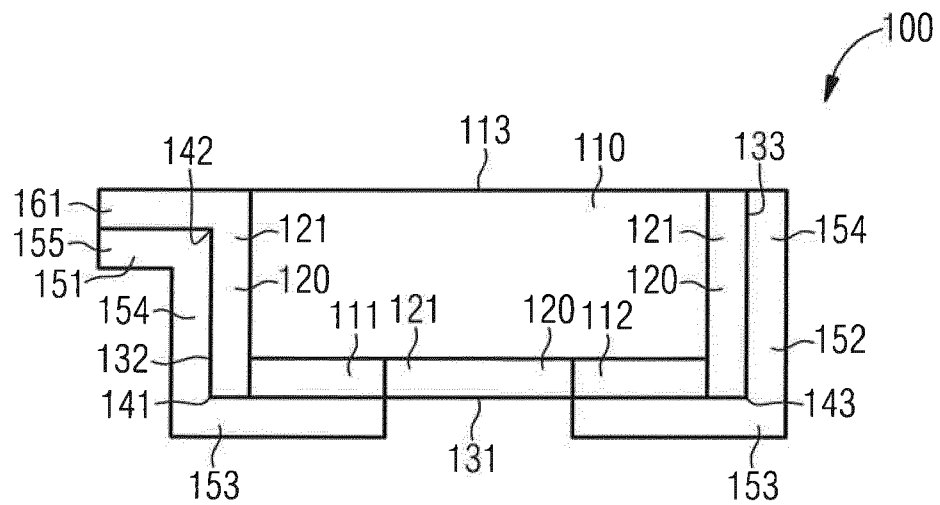
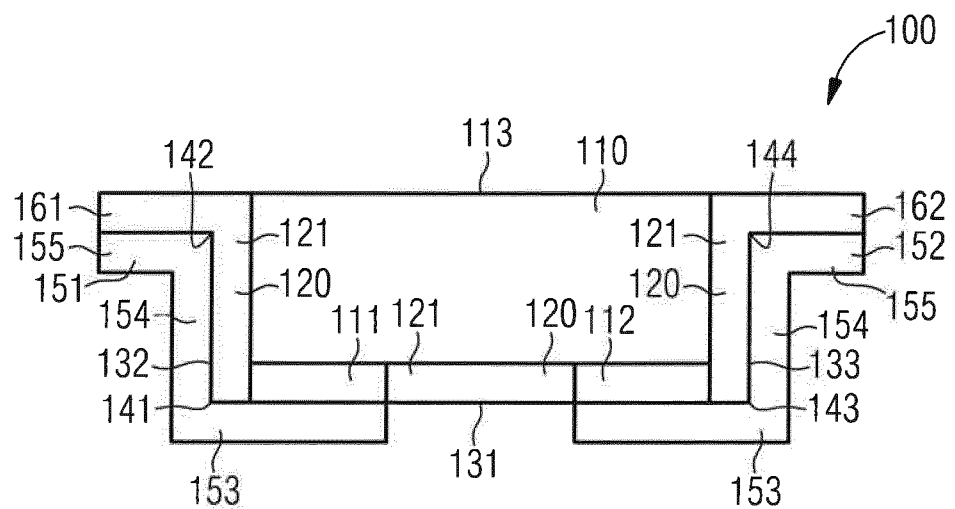


FIG 6



4/10

FIG 7

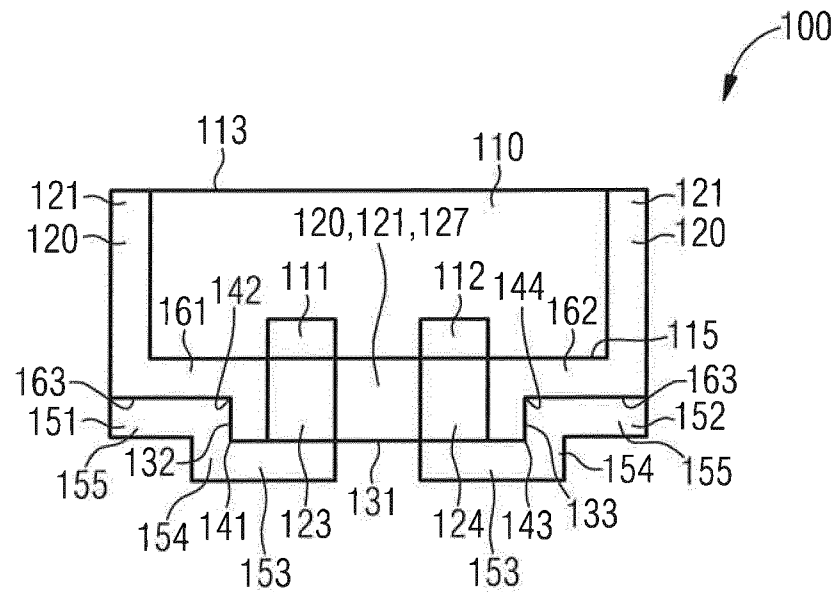
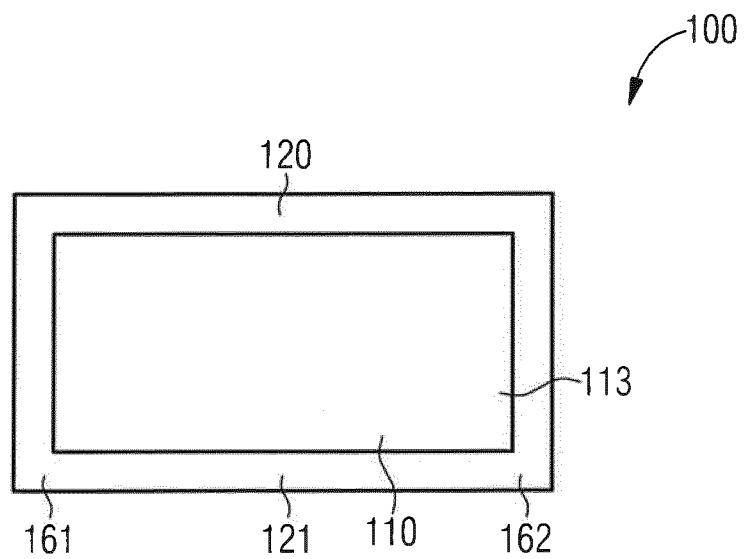


FIG 8



5/10

FIG 9

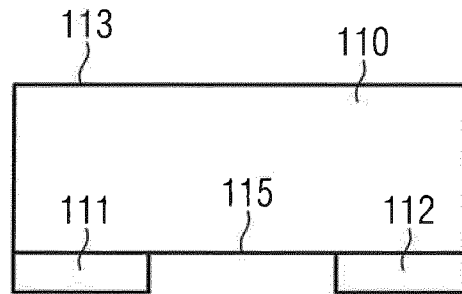
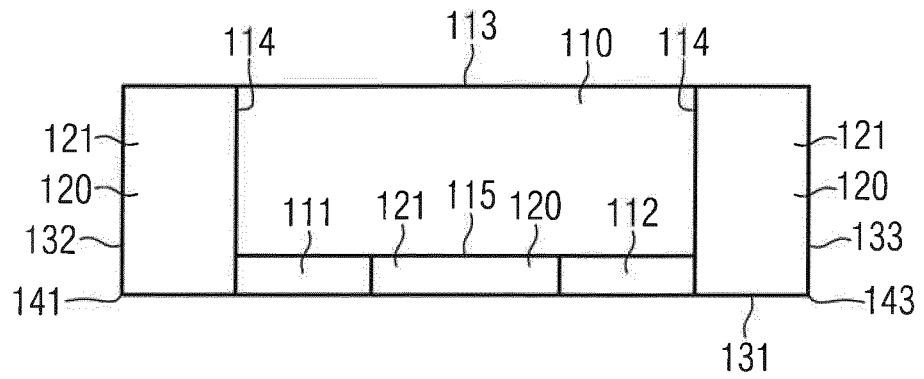


FIG 10



6/10

FIG 11

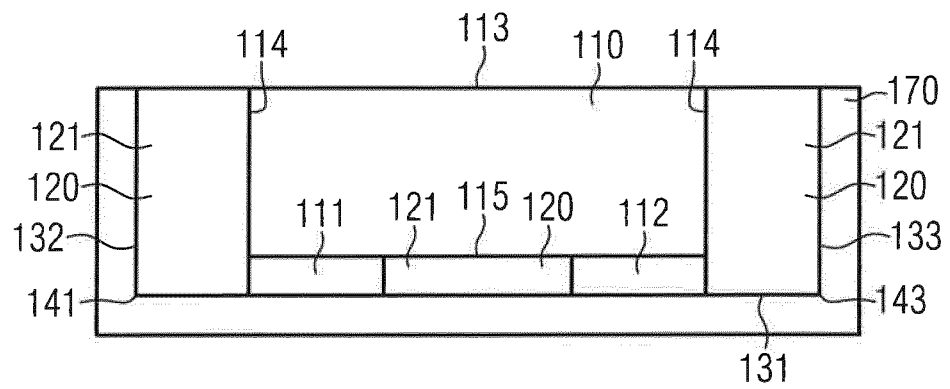
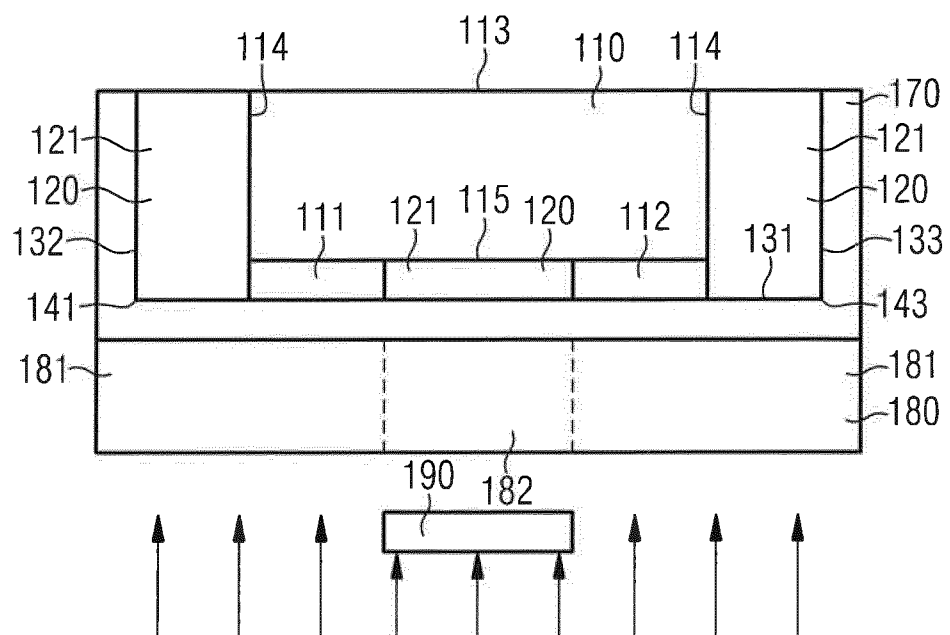


FIG 12



7/10

FIG 13

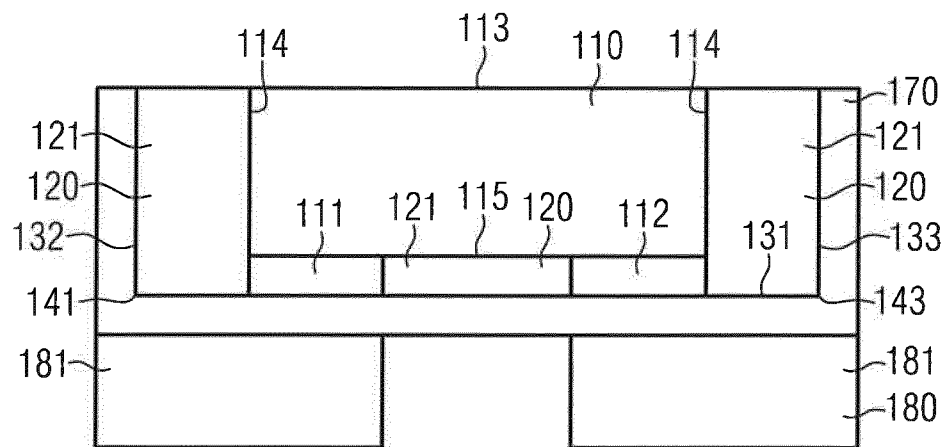
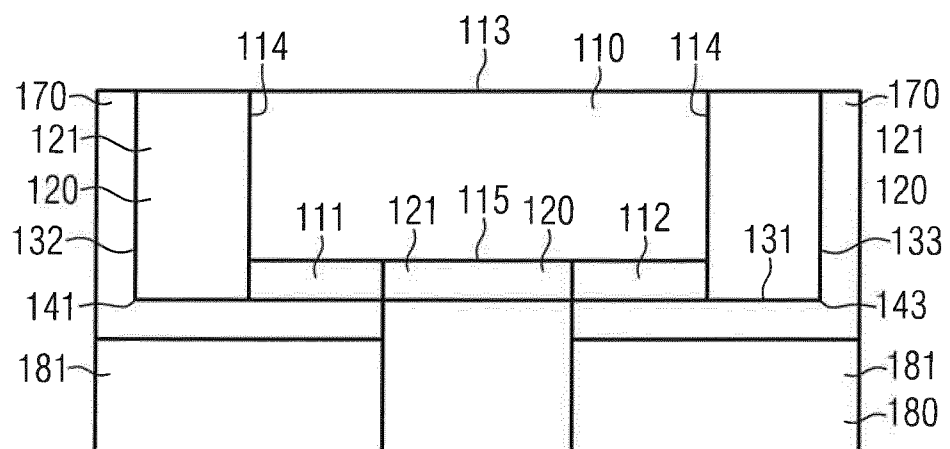


FIG 14



8/10

FIG 15

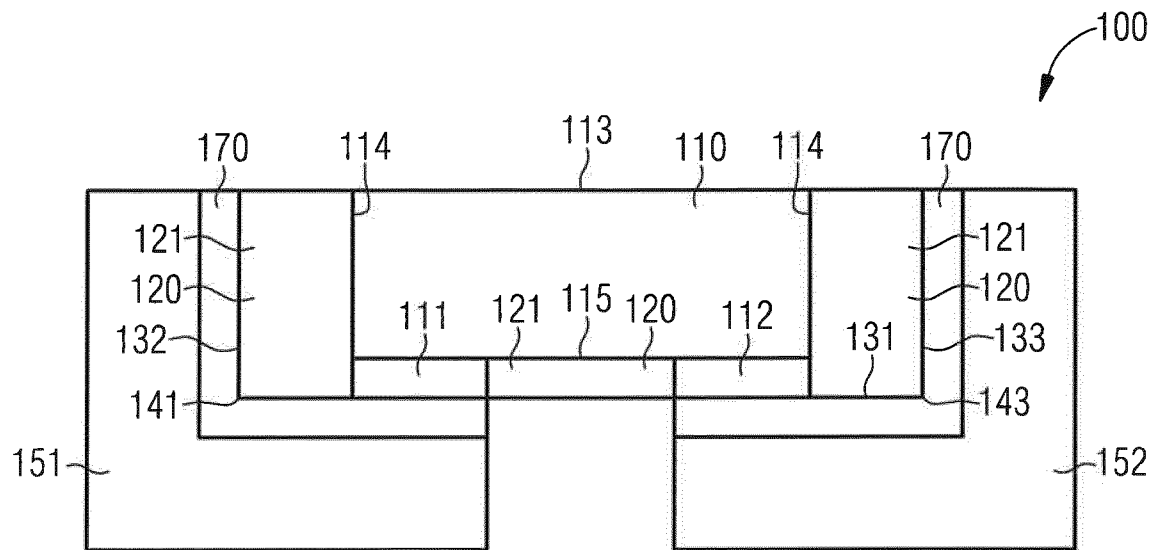
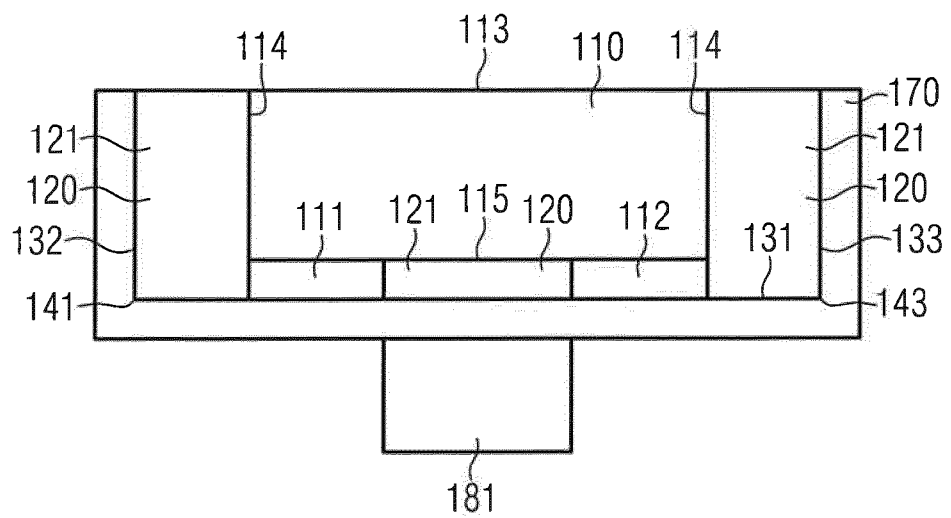


FIG 16



10/10

FIG 19

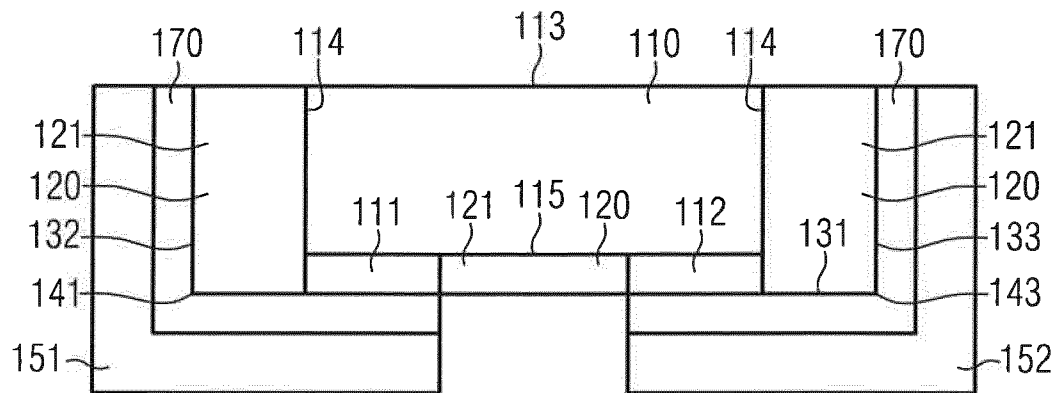
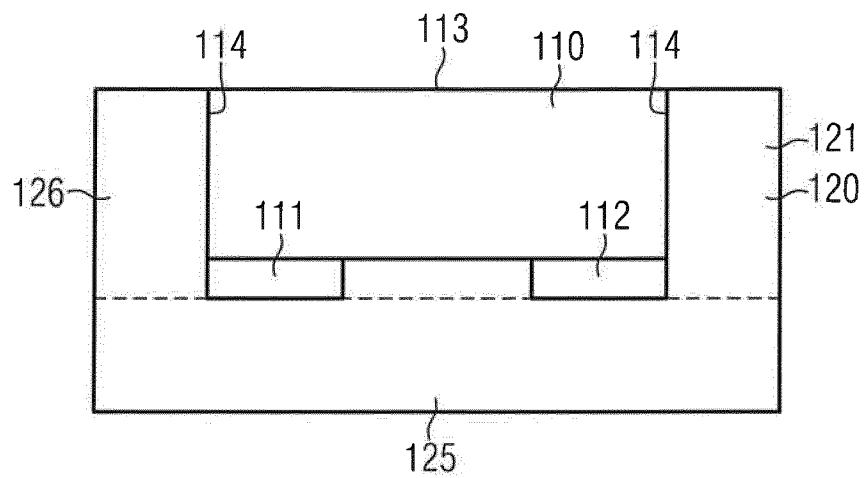


FIG 20



INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2016/073301

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L33/48 H01L33/56 H01L33/62
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 2 642 535 A2 (TOSHIBA KK [JP]) 25 September 2013 (2013-09-25) paragraphs [0010], [0020], [0021], [0064] - [0072]; figures 3b,3c,6c,6b -----	1-15
A	US 2016/141476 A1 (LING PEICHING [US] ET AL) 19 May 2016 (2016-05-19) paragraphs [0047] - [0051]; figures 3a-3c -----	1,10
A	DE 10 2015 100578 A1 (OSRAM OPTO SEMICONDUCTORS GMBH [DE]) 21 July 2016 (2016-07-21) paragraph [0019]; figures 1-3 -----	6
A	US 2016/056344 A1 (REILL JOACHIM [DE] ET AL) 25 February 2016 (2016-02-25) paragraph [0083]; figures 3-6 ----- -/-	13-15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

27 February 2017

Date of mailing of the international search report

03/03/2017

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Chin, Patrick

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2016/073301

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2002/079837 A1 (OKAZAKI JUN [JP]) 27 June 2002 (2002-06-27) figure 15	2,4
A	----- US 2015/221830 A1 (KIM GI CHERL [KR] ET AL) 6 August 2015 (2015-08-06) figure 14 -----	2,4

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2016/073301

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
EP 2642535	A2	25-09-2013	CN	103325933 A	25-09-2013
			EP	2642535 A2	25-09-2013
			JP	5684751 B2	18-03-2015
			JP	2013201273 A	03-10-2013
			KR	20130108119 A	02-10-2013
			TW	201340402 A	01-10-2013
			US	2013248910 A1	26-09-2013
			US	2015008469 A1	08-01-2015

US 2016141476	A1	19-05-2016	KR	20160059451 A	26-05-2016
			US	2016141476 A1	19-05-2016

DE 102015100578	A1	21-07-2016	DE	102015100578 A1	21-07-2016
			WO	2016113032 A1	21-07-2016

US 2016056344	A1	25-02-2016	CN	105103314 A	25-11-2015
			DE	102013103226 A1	02-10-2014
			DE	112014001665 A5	10-12-2015
			JP	2016515762 A	30-05-2016
			KR	20150135299 A	02-12-2015
			US	2016056344 A1	25-02-2016
			WO	2014154632 A1	02-10-2014

US 2002079837	A1	27-06-2002	JP	3614776 B2	26-01-2005
			JP	2002185046 A	28-06-2002
			US	2002079837 A1	27-06-2002
			US	2004036081 A1	26-02-2004

US 2015221830	A1	06-08-2015	CN	104821358 A	05-08-2015
			JP	2015149471 A	20-08-2015
			KR	20150092423 A	13-08-2015
			US	2015221830 A1	06-08-2015
			US	2016118549 A1	28-04-2016
