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RESISTIVE RANDOM ACCESS MEMORY DEVICES

Background

[0001] A non-volatile random access memory (NVRAM) device is a memory device that retains its data in the absence of supplied power. Flash memory is an example of an existing NVRAM technology, but flash memory may be limited in its speed and lifetime.

Brief Description of the Drawings

[0002] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0003] FIG. 1 is a cross-sectional view of an example electronic device including a memory cell having a resistive random access memory (RRAM) device coupled to a transistor, in accordance with various embodiments.

[0004] FIG. 2 is a schematic illustration of the memory cell of FIG. 1 with an n-type metal oxide semiconductor (NMOS) transistor, in accordance with various embodiments.

[0005] FIG. 3 is a detailed view of an embodiment of the RRAM device of FIG. 1.

[0006] FIGS. 4-8 illustrate various example stages in the manufacture of the RRAM device of FIG. 3, in accordance with various embodiments.

[0007] FIG. 9 is a flow diagram of an illustrative method of manufacturing an RRAM device, in accordance with various embodiments.

[0008] FIGS. 10A and 10B are top views of a wafer and dies that may include any of the RRAM devices disclosed herein.

[0009] FIG. 11 is a cross-sectional side view of a device assembly that may include any of the RRAM devices disclosed herein.

[0010] FIG. 12 is a block diagram of an example computing device that may include any of the RRAM devices disclosed herein, in accordance with various embodiments.

Detailed Description

[0011] Disclosed herein are resistive random access memory (RRAM) devices, and related memory cells and electronic devices. In some embodiments, an RRAM device may include a bottom electrode, an oxygen exchange layer (OEL), and an oxide layer. The bottom electrode may be disposed between the OEL and a substrate, and the OEL may be disposed between the oxide layer and the bottom electrode.

[0012] In the following detailed description, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, embodiments that may be

practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0013] Various operations may be described as multiple discrete actions or operations in turn in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be performed, and/or described operations may be omitted in additional embodiments.

[0014] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C). The term "between," when used with reference to measurement ranges, is inclusive of the ends of the measurement ranges. As used herein, the notation "A/B/C" means (A), (B), and/or (C).

[0015] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. The disclosure may use perspective-based descriptions such as "above," "below," "top," "bottom," and "side"; such descriptions are used to facilitate the discussion and are not intended to restrict the application of disclosed embodiments. The disclosure may use the singular term "layer," but the term "layer" should be understood to refer to assemblies that may include multiple different material layers. The accompanying drawings are not necessarily drawn to scale.

[0016] FIG. 1 is a side cross-sectional view of an example electronic device 150 including a memory cell 160 having a resistive random access memory (RRAM) device 100 coupled to a transistor 110, in accordance with various embodiments. As discussed in detail below, during operation, the RRAM device 100 may switch between two different non-volatile states: a high resistance state (HRS) and a low resistance state (LRS). The state of the RRAM device 100 may be used to represent a data bit (e.g., a "1" for HRS and a "0" for LRS, or vice versa). The transistor 110 may help control the current provided to the RRAM device 100 during use, as discussed below.

[0017] The electronic device 150 may be formed on a substrate 152 (e.g., the wafer 450 of FIG. 10A, discussed below) and may be included in a die (e.g., the die 452 of FIG. 10B, discussed below). The substrate 152 may be a semiconductor substrate composed of semiconductor material systems including, for example, n-type or p-type materials systems. The substrate 152 may include, for

example, a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In some embodiments, the semiconductor substrate 152 may be formed using alternative materials, which may or may not be combined with silicon, that include, but are not limited to, germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or gallium antimonide. Further materials classified as group II-VI, III-V, or IV may also be used to form the substrate 152. Although a few examples of materials from which the substrate 152 may be formed are described here, any material that may serve as a foundation for an electronic device 150 may be used. The substrate 152 may be part of a singulated die (e.g., the dies 452 of FIG. 10B) or a wafer (e.g., the wafer 450 of FIG. 10A).

[0018] The electronic device 150 may include one or more device layers 154 disposed on the substrate 152. The device layer 154 may include features of one or more transistors 110 (e.g., metal oxide semiconductor field-effect transistors (MOSFETs)) formed on the substrate 152. The device layer 154 may include, for example, one or more source and/or drain (S/D) regions 118, a gate 116 to control current flow in the channel 120 of the transistors 110 between the S/D regions 118, and one or more S/D contacts 156 (which may take the form of conductive vias) to route electrical signals to/from the S/D regions 118. Adjacent transistors 110 may be isolated from each other by a shallow trench isolation (STI) insulating material 122, in some embodiments. The transistors 110 may include additional features not depicted for the sake of clarity, such as device isolation regions, gate contacts, and the like. The transistors 110 are not limited to the type and configuration depicted in FIG. 1 and may include a wide variety of other types and configurations such as, for example, planar transistors, non-planar transistors, or a combination of both. Non-planar transistors may include FinFET transistors, such as double-gate transistors or tri-gate transistors, and wrap-around or all-around gate transistors, such as nanoribbon and nanowire transistors.

[0019] Each transistor 110 may include a gate 116 formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate electrode layer may include at least one p-type work function metal or n-type work function metal, depending on whether the transistor 110 is to be included in a p-type metal oxide semiconductor (PMOS) transistor or an n-type metal oxide semiconductor (NMOS) transistor. For a PMOS transistor, metals that may be used for the gate electrode layer may include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides (e.g., ruthenium oxide). For an NMOS transistor, metals that may be used for the gate electrode layer include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals (e.g., hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide). In some embodiments, the gate electrode layer may consist of a stack of two or more metal layers, where

one or more metal layers are work function metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as to act as a barrier layer. The gate dielectric layer may be, for example, silicon oxide, aluminum oxide, or a high-k dielectric, such as hafnium oxide. More generally, the gate dielectric layer may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of materials that may be used in the gate dielectric layer may include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, tantalum oxide, tantalum silicon oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric layer to improve the quality of the gate dielectric layer.

[0020] In some embodiments, when viewed as a cross section of the transistor 110 along the source-channel-drain direction, the gate electrode may consist of a U-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In other embodiments, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In other embodiments, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers. In some embodiments, the gate electrode may consist of a V-shaped structure.

[0021] In some embodiments, a pair of sidewall spacers 126 may be formed on opposing sides of the gate 116 to bracket the gate stack. The sidewall spacers 126 may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers 126 are well known in the art and generally include deposition and etching process steps. In some embodiments, multiple pairs of sidewall spacers 126 may be used; for instance, two pairs, three pairs, or four pairs of sidewall spacers 126 may be formed on opposing sides of the gate stack.

[0022] The S/D regions 118 may be formed within the substrate 152 adjacent to the gate 116 of each transistor 110. For example, the S/D regions 118 may be formed using either an implantation/diffusion process or a deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate 152

to form the S/D regions 118. An annealing process that activates the dopants and causes them to diffuse farther into the substrate 152 may follow the ion implantation process. In the latter process, an epitaxial deposition process may provide material that is used to fabricate the S/D regions 118. In some implementations, the S/D regions 118 may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some embodiments, the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In some embodiments, the S/D regions 118 may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. In further embodiments, one or more layers of metal and/or metal alloys may be used to form the S/D regions 118. In some embodiments, an etch process may be performed before the epitaxial deposition to create recesses in the substrate 152 in which the material for the S/D regions 118 is deposited.

[0023] Electrical signals, such as power and/or input/output (I/O) signals, may be routed to and/or from the transistors 110 of the device layer 154 through one or more interconnect layers disposed on the device layer 154 (illustrated in FIG. 1 as interconnect layers 158 and 162). For example, electrically conductive features of the device layer 154 (e.g., the gate 116 and the S/D contacts 156) may be electrically coupled with the interconnect structures including conductive vias 112 and/or conductive lines 114 of the interconnect layers 158 and 162. The one or more interconnect layers 158 and 162 may form an interlayer dielectric (ILD) stack of the electronic device 150.

[0024] The interconnect structures may be arranged within the interconnect layers 158 and 162 to route electrical signals according to a wide variety of designs (in particular, the arrangement is not limited to the particular configuration of interconnect structures depicted in FIG. 1). Although a particular number of interconnect layers is depicted in FIG. 1, embodiments of the present disclosure include electronic devices having more or fewer interconnect layers than depicted.

[0025] In some embodiments, the interconnect structures may include conductive lines 114 (sometimes referred to as "trench structures") and/or conductive vias 112 (sometimes referred to as "holes") filled with an electrically conductive material such as a metal. The conductive lines 114 may be arranged to route electrical signals in a direction of a plane that is substantially parallel with a surface of the substrate 152 upon which the device layer 154 is formed. For example, the conductive lines 114 may route electrical signals in a direction in and out of the page from the perspective of FIG. 1. The conductive vias 112 may be arranged to route electrical signals in a direction of a plane that is substantially perpendicular to the surface of the substrate 152 upon which the device layer 154 is formed. In some embodiments, the conductive vias 112 may electrically couple conductive lines 114 of different interconnect layers 158 and 162 together.

[0026] The interconnect layers 158 and 162 may include a dielectric material 124 disposed between the interconnect structures, as shown in FIG. 1. In some embodiments, the dielectric material 124 disposed between the interconnect structures in different ones of the interconnect layers 158 and 162 may have different compositions; in other embodiments, the composition of the dielectric material 124 between different interconnect layers 158 and 162 may be the same.

[0027] A first interconnect layer 158 (referred to as Metal 1 or "M1") may be formed directly on the device layer 154. In some embodiments, the first interconnect layer 158 may include conductive lines 114 and/or conductive vias 112, as shown. The conductive lines 114 of the first interconnect layer 158 may be coupled with contacts (e.g., the S/D contacts 156) of the device layer 154.

[0028] A second interconnect layer 162 (referred to as Metal 2 or "M2") may be formed directly on the first interconnect layer 158. In some embodiments, the second interconnect layer 162 may include conductive vias 112 to couple the conductive lines 114 of the second interconnect layer 162 with the conductive lines 114 of the first interconnect layer 158. Although the conductive lines 114 and the conductive vias 112 are structurally delineated with a line within each interconnect layer (e.g., within the second interconnect layer 162) for the sake of clarity, the conductive lines 114 and the conductive vias 112 may be structurally and/or materially contiguous (e.g., simultaneously filled during a dual-damascene process) in some embodiments.

[0029] Additional interconnect layers may be formed in succession on the second interconnect layer 162 according to similar techniques and configurations described in connection with the first interconnect layer 158 or the second interconnect layer 162.

[0030] The electronic device 150 may include a solder resist material 164 (e.g., polyimide or similar material) and one or more bond pads 166 formed on the interconnect layers. The bond pads 166 may be electrically coupled with the interconnect structures and may route the electrical signals of the memory cell 160 to other external devices. For example, solder bonds may be formed on the one or more bond pads 166 to mechanically and/or electrically couple a chip including the electronic device 150 with another component (e.g., a circuit board). The electronic device 150 may include other structures to route the electrical signals from the interconnect layers than depicted in other embodiments. For example, the bond pads 166 may be replaced by or may further include other analogous features (e.g., posts) that route electrical signals to external components.

[0031] As noted above, the electronic device 150 may include an RRAM device 100 electrically coupled to a transistor 110, forming a memory cell 160. The RRAM device 100 is illustrated as being included in the interconnect layer 162, but the RRAM device 100 may be located in any suitable interconnect layer or other portion of the electronic device 150.

[0032] The RRAM device 100 may include a bottom electrode 102, an oxygen exchange layer (OEL) 104, an oxide layer 106, and a top electrode 108. The OEL 104 may be disposed between the bottom electrode 102 and the oxide layer 106, and the oxide layer 106 may be disposed between the OEL 104 and the top electrode 108. The components of the RRAM device 100 are discussed in further detail below with reference to FIG. 3. The bottom electrode 102 may be electrically coupled to an S/D region 118 of the transistor 110 (e.g., through one or more conductive vias 112, conductive lines 114, and S/D contacts 156). Thus, the bottom electrode 102 of the RRAM device 100 may be electrically coupled between the transistor 110 and the top electrode 108 of the RRAM device 100.

[0033] FIG. 2 is a schematic illustration of the memory cell 160 of FIG. 1 with an NMOS transistor 110, in accordance with various embodiments. In particular, FIG. 2 illustrates the transistor 110, its gate node G (corresponding to the gate 116), its drain node D (corresponding to the S/D region 118a), and its source node S (corresponding to the S/D region 118b). FIG. 2 also illustrates the RRAM device 100 (using a variable resistor circuit symbol), its top electrode node TE (corresponding to the top electrode 108) and its bottom electrode node BE (corresponding to the bottom electrode 102).

[0034] An amply negative voltage applied to the RRAM device 100 (e.g., applied between the TE node and the BE node) may cause oxygen atoms in the oxide layer 106 to migrate toward the OEL 104, leaving oxygen vacancies in the oxide layer 106. These oxygen vacancies may form one or more filaments that provide conductive pathways between the bottom electrode 102 and the top electrode 108, bringing the RRAM device 100 into its LRS. This initial formation of such a filament in the RRAM device 100 (e.g., after or during manufacture) may be referred to as "breakdown," and subsequent driving of the RRAM device 100 into the LRS may be referred to as SET (with an associated SET voltage). The SET voltage may be less than the breakdown, or formation voltage. The transistor 110 in the memory cell 160 may assist during breakdown by limiting the current flow during breakdown to avoid overdriving the RRAM device 100.

[0035] Once in the LRS, an amply positive voltage applied to the RRAM device 100 may reduce the filaments until they no longer provide an electrical bridge between the bottom electrode 102 and the top electrode 108, bringing the RRAM device 100 into its HRS. Driving the RRAM device 100 into the HRS may be referred to as RESET (with an associated RESET voltage). Adjusting the amount of breakdown current may adjust the "width" of the filaments formed in the RRAM device, with wider filaments providing more stable SET operation (potentially slowing the switching from SET to RESET) and narrower filaments providing less stable SET operation (potentially speeding up the switching from SET to RESET).

[0036] In the embodiment illustrated in FIG. 1, the bottom electrode 102 and the top electrode 108 are shown as having smaller footprints than the OEL 104 and the oxide layer 106; such an arrangement may focus the areas of filament formation in the bulk of the oxide layer 106, rather than at the edges (where non-idealities may occur). In some embodiments, only the top electrode 108 has such a smaller footprint; in other embodiments, neither the top electrode 108 nor the bottom electrode 102 has a smaller footprint.

[0037] During use of the memory cell 160 of FIG. 2, the gate node G may be coupled to a word line, the drain node D may be coupled to a bit line, and the top electrode node TE may be coupled to a load line. To cause a positive voltage drop across the RRAM device 100 (as would be needed to RESET the RRAM device 100), the top electrode node TE may be coupled to a first positive voltage (e.g., 1.5 V) and the drain node D may be coupled to ground; if a second positive voltage (e.g., 1.5 V) is applied to the gate node G, the transistor 110 may conduct and the source node S may also be at ground level. Thus, the full first positive voltage may drop across the RRAM device 100, and the gate-source voltage (between the gate node G and the source node S) may be equal to the full second positive voltage. If the first positive voltage is equal to or exceeds the RESET voltage, the RRAM device 100 may RESET.

[0038] To cause a negative voltage drop across the RRAM device 100 (as would be needed to SET the RRAM device 100), the top electrode node TE may be coupled to ground and the drain node D may be coupled to a first positive voltage (e.g., 1.5 V); if a second positive voltage (e.g., 1.5 V) is applied to the gate node G, the transistor 110 may conduct in the opposite direction and the source node S may have a voltage between the first positive voltage (applied at the drain node D) and ground (at the top electrode node TE). Thus, a voltage drop less than the full first positive voltage may be seen across the RRAM device 100, and the gate-source voltage may be less than the full second positive voltage. This phenomenon may be referred to as "source degeneration," and the decreased gate-source voltage may result in weaker operation of the transistor 110 (e.g., a reduced ability to source/sink current) relative to the larger gate-source voltage that may occur during RESET. Even in this scenario, if the voltage drop across the RRAM device 100 is equal to or exceeds the SET voltage, the RRAM device 100 may SET.

[0039] As discussed above, the operation of the memory cell 160 may thus be asymmetric; the NMOS transistor 110 may be "stronger" during RESET than SET. This asymmetry, however, may be complementary to the asymmetry in SET and RESET voltages of the RRAM device 100. In particular, the (negative) RESET voltage may have a larger magnitude than the (positive) SET voltage. Having a transistor 110 that is "well matched" in this manner to the RRAM device 100 in a memory cell 160 may reduce the energy consumed by the memory cell 160 relative to a cell in which the components

are not as well matched. For example, if the transistor 110 were a PMOS transistor, the PMOS transistor would be "stronger" during SET than RESET, and thus must be larger or more strongly driven in order to provide the greater RESET voltage required by the RRAM device 100. Additionally, PMOS transistors are typically able to drive less current than NMOS transistors, so even further compensation may be required. Thus, the use of an NMOS transistor 110 and the RRAM device 100 in a memory cell 160 may provide a particularly advantageous memory cell 160. In some embodiments of the memory cell 160, however, the transistor 110 may be a PMOS transistor.

[0040] Some conventional RRAM-based memory cells have utilized PMOS transistors and RRAM devices in which the oxide layer is disposed between the bottom electrode and the OEL (unlike the RRAM device 110, in which the OEL 104 is disposed between the oxide layer 106 and the bottom electrode 102). These RRAM devices (referred to herein as "top OEL RRAM devices") may SET in response to an amply positive voltage and RESET in response to an amply negative voltage (opposite to the RRAM device 100); a PMOS transistor may be matched to such a top OEL RRAM device in the sense that it is stronger on the RESET side than the SET side for these devices. As noted above, however, PMOS transistors are typically weaker than NMOS transistors, taking up more space for a predetermined amount of drive current than an NMOS transistor. Simply exchanging a PMOS transistor for an NMOS transistor in such a conventional RRAM-based memory cell (for example, in an effort to improve space utilization) may result in mismatch between the NMOS transistor (stronger on the "positive side" than the "negative side" due to source degeneration) and the top OEL RRAM device (needing more voltage on the "negative side" than the "positive side"). To compensate for this mismatch, the NMOS transistor may need to be made even larger, defeating any space utilization motivation.

[0041] The RRAM devices 100 disclosed herein may be structured to effectively match with an NMOS transistor 110 by including the OEL 104 between the oxide layer 106 and the bottom electrode 102. Conventional RRAM devices cannot match an NMOS transistor as effectively. These conventional RRAM devices have been constructed by forming a bottom electrode, providing an oxide on the bottom electrode by atomic layer deposition (ALD) to form an intermediate assembly, removing the intermediate assembly from the ALD chamber and moving it into a sputtering chamber (exposing the intermediate assembly to air), and then sputtering both a thin film of OEL (e.g., hafnium) and the top electrode within the sputtering chamber to avoid exposing the OEL to air outside of the sputtering chamber. In conventional approaches, exposing the thin film OEL to air would typically cause the OEL to oxidize and thereby degrade its oxygen exchange properties. Conventional approaches have thus not enabled or contemplated RRAM stacks in which the OEL is disposed "below" the oxide layer, since the OEL would undesirably oxidize in the air break between

deposition of the OEL and deposition of the oxide layer. The structures and manufacturing techniques disclosed herein thus achieve RRAM stack arrangements not previously achievable, and enable memory cells in which the transistor and RRAM device are uniquely efficient and well matched.

[0042] FIG. 3 is a detailed side cross-sectional view of an embodiment of the RRAM device 100 of FIG. 1. Embodiments of the components of the RRAM device 100 of FIG. 3 are now discussed in detail.

[0043] The bottom electrode 102 and the top electrode 108 of the RRAM device 100 may be formed of metal. For example, in some embodiments, the bottom electrode 102 and the top electrode 108 may be formed of titanium nitride, tungsten, tantalum, tantalum nitride, ruthenium, or iridium. More generally, the bottom electrode 102 and the top electrode 108 may be formed of any of the materials discussed above with reference to the gate electrode of the gate 116 of the transistor 110. The bottom electrode 102 may have a thickness 132 that may take any suitable value. For example, the thickness 132 may be between 15 and 20 nanometers. The thickness 140 of the top electrode 108 may take the form of any of the embodiments of the thickness 132 of the bottom electrode 102. In some embodiments, the bottom electrode 102 and/or the top electrode 108 may be formed by physical vapor deposition (PVD) (e.g., sputtering). In some embodiments, the bottom electrode 102 may be formed by PVD, and the top electrode 108 may be formed by ALD.

[0044] The oxide layer 106 may include any suitable oxide material. For example, the oxide layer 106 may be formed of hafnium oxide. In embodiments in which the oxide layer 106 is formed of hafnium oxide provided by ALD, the oxide layer 106 may be HfO_2 . More generally, the oxide layer 106 may be formed of any metal oxide, such as zirconium oxide, tantalum oxide, indium oxide, silicon oxide, aluminum oxide, or titanium oxide. The oxide layer 106 may have a thickness 138 that may take any suitable value. For example, the thickness 138 may be between 1 and 50 nanometers (e.g., between 3 and 10 nanometers).

[0045] In the RRAM device 100 of FIG. 3, the OEL 104 may be provided by an oxygen exchange (OE) portion 128 and a spacer 130. The spacer 130 may be disposed between the OE portion 128 and the oxide layer 106, and thus may space the OE portion 128 from the oxide layer 106. In some embodiments, the OE portion 128 may be formed of any reactive metal, such as hafnium, titanium, zirconium, aluminum, erbium, iridium, or tantalum. The OE portion 128 may have a thickness 134 that may take any suitable value. For example, the thickness 134 may be between 1 and 15 nanometers (e.g., between 2 and 6 nanometers).

[0046] In some embodiments, the spacer 130 may be formed of an oxynitride material, such as silicon oxynitride, a carbon-doped oxynitride, or hafnium oxynitride. The reactive OE portion 128

may scavenge some of the oxygen from the spacer 130, forming oxygen vacancies in the spacer 130 that can be used to form the electrically conductive filaments discussed above. As discussed below with reference to FIG. 8, the spacer 130 may be formed by depositing (e.g., by PVD) an initial spacer material, then annealing the initial spacer material to drive oxygen from the oxide layer 106 into the initial spacer material, forming the spacer 130. In some embodiments, hafnium oxynitride may be a particularly advantageous material for use as the spacer 130 because it acts as an effective oxygen barrier at low temperatures (e.g., temperatures below 500-600 degrees Celsius) and accepts oxygen at higher temperature (e.g., anneal temperatures). The spacer 130 may have a thickness 136 that may take any suitable value. For example, the thickness 136 may be between 10 angstroms and 50 nanometers (e.g., between 1 and 5 nanometers, or between 2 and 3 nanometers).

[0047] Any suitable combination of the materials discussed above may be included in an RRAM device 100. For example, in some embodiments, the bottom electrode 102 may be titanium nitride (formed by, e.g., PVD), the OE portion 128 may be hafnium (formed by, e.g., PVD), the spacer 130 may be hafnium oxynitride (formed by, e.g., PVD), the oxide layer 106 may be hafnium oxide (formed by, e.g., ALD), and the top electrode 108 may be titanium nitride (formed by, e.g., ALD).

[0048] The RRAM device 100 of FIG. 3 may be formed using any suitable technique. For example, FIGS. 4-8 illustrate various example stages in the manufacture of the RRAM device 100 of FIG. 3, in accordance with various embodiments. Any suitable patterning techniques may be used to control the shape of the components of the RRAM device 100 during manufacture (e.g., semi-additive techniques, subtractive techniques, or other techniques), and are thus not discussed further herein.

[0049] FIG. 4 is a side cross-sectional view of an assembly 200 subsequent to forming a bottom electrode 102. The bottom electrode 102 may be formed as part of an interconnect layer, as discussed above with reference to FIG. 1, and may be in conductive contact with an S/D region 118 of a transistor 110 (e.g., through one or more conductive lines and/or vias). In some embodiments, the transistor 110 may be an NMOS transistor. In some embodiments, the bottom electrode 102 may be formed by PVD (e.g., sputtering). The bottom electrode 102 of the assembly 200 may take any of the forms disclosed herein.

[0050] FIG. 5 is a side cross-sectional view of an assembly 202 subsequent to forming an OE portion 128 on the bottom electrode 102 of the assembly 200 (FIG. 4). The OE portion 128 may take any of the forms disclosed herein. In some embodiments, the OE portion 128 may be formed by PVD (e.g., sputtering); in some such embodiments, the bottom electrode 102 and the OE portion 128 may be formed in the same PVD chamber, without exposing the assembly 200 to an air break.

[0051] FIG. 6 is a side cross-sectional view of an assembly 204 subsequent to providing an initial spacer material 172 on the OE portion 128 of the assembly 202 (FIG. 5). As discussed above, the

initial spacer material 172 may be a nitride material, such as silicon nitride, a carbon-doped nitride, or hafnium nitride. In some embodiments, the OE portion 128 may be formed by PVD (e.g., sputtering); in some such embodiments, the OE portion 128 and the initial spacer material 172 may be formed in the same PVD chamber, without exposing the assembly 202 to an air break (and thus without exposing the OE portion 128 to an air break that could result in oxidation of the OE portion 128).

[0052] FIG. 7 is a side cross-sectional view of an assembly 206 subsequent to forming an oxide layer 106 and a top electrode 108 on the assembly 204 (FIG. 6). As shown, the oxide layer 106 may be formed on the initial spacer material 172, and the top electrode 108 may be subsequently formed on the oxide layer 106. The oxide layer 106 and the top electrode 108 may take any of the forms disclosed herein. In some embodiments, the oxide layer 106 and the top electrode 108 may be formed by ALD in a second chamber separate from a first chamber in which the initial spacer material 172 was formed on the assembly 202; in some such embodiments, the assembly 204 may be exposed to air as it transitions from the first chamber to the second chamber. The initial spacer material 172 may provide an oxygen diffusion barrier between the air and the OE portion 128, providing a "cap" on the OE portion 128 to prevent its oxidation during the air break.

[0053] FIG. 8 is a side cross-sectional view of an assembly 208 subsequent to annealing the assembly 206 (FIG. 7) to cause oxygen to diffuse into and across the initial spacer material 172. After anneal, the initial spacer material 172 may include oxygen that was not present before the anneal; the annealed initial spacer material 172 may provide the spacer 130 of the OEL 104. The anneal conditions may depend on the particular make-up of the assembly 206, but in some embodiments, the anneal temperature may be between 500 and 600 degrees Celsius. The assembly 208 may take the form of the RRAM device 100 of FIG. 1.

[0054] As noted above, any suitable techniques may be used to manufacture the RRAM devices 100 and memory cells 160 disclosed herein. FIG. 9 is a flow diagram of an illustrative method 1000 of manufacturing a memory cell, in accordance with various embodiments. Although the operations discussed below with reference to the method 1000 are illustrated in a particular order and depicted once each, these operations may be repeated or performed in a different order (e.g., in parallel), as suitable. Additionally, various operations may be omitted, as suitable. Various operations of the method 1000 may be illustrated with reference to one or more of the embodiments discussed above, but the method 1000 may be used to manufacture any suitable memory cell (including any suitable ones of the embodiments disclosed herein).

[0055] At 1002, a transistor may be formed in a device layer of an electronic device. For example, a transistor 110 may be formed in a device layer 154 of an electronic device 150, as discussed above with reference to FIG. 1. In some embodiments, the transistor may be an NMOS transistor.

[0056] At 1004, an interconnect structure may be formed. The interconnect structure may couple to an S/D region of the transistor (1002). For example, an interconnect structure including one or more S/D contacts 156, conductive vias 112, and/or conductive lines 114 may be formed, as discussed above with reference to FIG. 1.

[0057] At 1006, an RRAM device may be formed above the device layer. A bottom electrode of the RRAM device may be in contact with the interconnect structure, the bottom electrode may be disposed between an OEL and the device layer, and the OEL may be disposed between an oxide layer and the device layer. For example, an RRAM device 100 may be formed above the device layer 154 in the electronic device 150, in accordance with any of the embodiments discussed above with reference to FIG. 3 and FIGS. 4-8. The RRAM device 100 may include a bottom electrode 102 in contact with an interconnect structure to conductively couple the bottom electrode 102 to an S/D region 118 of the transistor 110. The bottom electrode may be disposed between an OEL 104 and the device layer 154, and the OEL 104 may be disposed between an oxide layer 106 and the device layer 154.

[0058] The RRAM devices 100 and memory cells 160 disclosed herein may be included in any suitable electronic device. FIGS. 10A-B are top views of a wafer 450 and dies 452 that may be formed from the wafer 450; the dies 452 may include any of the RRAM devices 100 or memory cells 160 disclosed herein. The wafer 450 may include semiconductor material and may include one or more dies 452 having integrated circuit elements (e.g., RRAM devices 100 and transistors 110) formed on a surface of the wafer 450. Each of the dies 452 may be a repeating unit of a semiconductor product that includes any suitable device (e.g., the electronic device 150). After the fabrication of the semiconductor product is complete, the wafer 450 may undergo a singulation process in which each of the dies 452 is separated from one another to provide discrete "chips" of the semiconductor product. A die 452 may include one or more RRAM devices 100 or memory cells 160 and/or supporting circuitry to route electrical signals to the RRAM devices 100 or memory cells 160 (e.g., interconnects including conductive vias 112 and lines 114), as well as any other integrated circuit (IC) components. In some embodiments, the wafer 450 or the die 452 may include other memory devices, logic devices (e.g., AND, OR, NAND, or NOR gates), or any other suitable circuit element. Multiple ones of these devices may be combined on a single die 452. For example, a memory array formed by multiple memory devices (e.g., multiple RRAM devices 100) may be formed on a same die 452 as a processing device (e.g., the processing device 2002 of FIG. 12) or other logic

that is configured to store information in the memory devices or execute instructions stored in the memory array.

[0059] FIG. 11 is a cross-sectional side view of a device assembly 400 that may include any of the RRAM devices 100 or memory cells 160 disclosed herein included in one or more packages. A "package" may refer to an electronic component that includes one or more IC devices that are structured for coupling to other components; for example, a package may include a die coupled to a package substrate that provides electrical routing and mechanical stability to the die. The device assembly 400 includes a number of components disposed on a circuit board 402. The device assembly 400 may include components disposed on a first face 440 of the circuit board 402 and an opposing second face 442 of the circuit board 402; generally, components may be disposed on one or both faces 440 and 442.

[0060] In some embodiments, the circuit board 402 may be a printed circuit board (PCB) including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route electrical signals (optionally in conjunction with other metal layers) between the components coupled to the circuit board 402. In other embodiments, the circuit board 402 may be a package substrate or flexible board.

[0061] The device assembly 400 illustrated in FIG. 11 includes a package-on-interposer structure 436 coupled to the first face 440 of the circuit board 402 by coupling components 416. The coupling components 416 may electrically and mechanically couple the package-on-interposer structure 436 to the circuit board 402, and may include solder balls, male and female portions of a socket, an adhesive, an underfill material, and/or any other suitable electrical and/or mechanical coupling structure.

[0062] The package-on-interposer structure 436 may include a package 420 coupled to an interposer 404 by coupling components 418. The coupling components 418 may take any suitable form for the application, such as the forms discussed above with reference to the coupling components 416. Although a single package 420 is shown in FIG. 11, multiple packages may be coupled to the interposer 404; indeed, additional interposers may be coupled to the interposer 404. The interposer 404 may provide an intervening substrate used to bridge the circuit board 402 and the package 420. The package 420 may include one or more RRAM devices 100 or memory cells 160, for example. Generally, the interposer 404 may spread a connection to a wider pitch or reroute a connection to a different connection. For example, the interposer 404 may couple the package 420 (e.g., a die) to a ball grid array (BGA) of the coupling components 416 for coupling to the circuit board 402. In the embodiment illustrated in FIG. 11, the package 420 and the circuit board 402 are

attached to opposing sides of the interposer 404; in other embodiments, the package 420 and the circuit board 402 may be attached to a same side of the interposer 404. In some embodiments, three or more components may be interconnected by way of the interposer 404.

[0063] The interposer 404 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In some embodiments, the interposer 404 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials. The interposer 404 may include metal interconnects 408 and vias 410, including but not limited to through-silicon vias (TSVs) 406. The interposer 404 may further include embedded devices 414, including both passive and active devices. Such devices may include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, electrostatic discharge (ESD) devices, and memory devices (e.g., the RRAM devices 100 or the memory cells 160). More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and microelectromechanical systems (MEMS) devices may also be formed on the interposer 404. The package-on-interposer structure 436 may take the form of any of the package-on-interposer structures known in the art.

[0064] The device assembly 400 may include a package 424 coupled to the first face 440 of the circuit board 402 by coupling components 422. The coupling components 422 may take the form of any of the embodiments discussed above with reference to the coupling components 416, and the package 424 may take the form of any of the embodiments discussed above with reference to the package 420. The package 424 may include one or more RRAM devices 100 or memory cells 160, for example.

[0065] The device assembly 400 illustrated in FIG. 11 includes a package-on-package structure 434 coupled to the second face 442 of the circuit board 402 by coupling components 428. The package-on-package structure 434 may include a package 426 and a package 432 coupled together by coupling components 430 such that the package 426 is disposed between the circuit board 402 and the package 432. The coupling components 428 and 430 may take the form of any of the embodiments of the coupling components 416 discussed above, and the packages 426 and 432 may take the form of any of the embodiments of the package 420 discussed above. Each of the packages 426 and 432 may include one or more RRAM devices 100 or memory cells 160, for example.

[0066] FIG. 12 is a block diagram of an example computing device 2000 that may include any of the RRAM devices 100 or memory cells 160 disclosed herein. A number of components are illustrated in FIG. 12 as included in the computing device 2000, but any one or more of these components may be omitted or duplicated, as suitable for the application. In some embodiments, some or all of the

components included in the computing device 2000 may be attached to one or more printed circuit boards (e.g., a motherboard). In some embodiments, various ones of these components may be fabricated onto a single system-on-a-chip (SoC) die. Additionally, in various embodiments, the computing device 2000 may not include one or more of the components illustrated in FIG. 12, but the computing device 2000 may include interface circuitry for coupling to the one or more components. For example, the computing device 2000 may not include a display device 2006, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device 2006 may be coupled. In another set of examples, the computing device 2000 may not include an audio input device 2024 or an audio output device 2008, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 2024 or audio output device 2008 may be coupled.

[0067] The computing device 2000 may include a processing device 2002 (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 2002 may interface with one or more of the other components of the computing device 2000 (e.g., the communication chip 2012 discussed below, the display device 2006 discussed below, etc.) in a conventional manner. The processing device 2002 may include one or more digital signal processors (DSPs), application-specific integrated circuits (ASICs), central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices.

[0068] The computing device 2000 may include a memory 2004, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), non-volatile memory (e.g., read-only memory (ROM)), flash memory, solid state memory, and/or a hard drive. The memory 2004 may include one or more RRAM devices 100 or memory cells 160. In some embodiments, the memory 2004 may include memory that shares a die with the processing device 2002. This memory may be used as cache memory and may include embedded dynamic random access memory (eDRAM) or spin transfer torque magnetic random-access memory (STT-MRAM).

[0069] In some embodiments, the computing device 2000 may include a communication chip 2012 (e.g., one or more communication chips). For example, the communication chip 2012 may be configured for managing wireless communications for the transfer of data to and from the computing device 2000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data

through the use of modulated electromagnetic radiation through a nonsolid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not.

[0070] The communication chip 2012 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 1402.11 family), IEEE 1402.16 standards (e.g., IEEE 1402.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultramobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 1402.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 1402.16 standards. The communication chip 2012 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 2012 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 2012 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 2012 may operate in accordance with other wireless protocols in other embodiments. The computing device 2000 may include an antenna 2022 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0071] In some embodiments, the communication chip 2012 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip 2012 may include multiple communication chips. For instance, a first communication chip 2012 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 2012 may be dedicated to longer-range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip 2012 may be dedicated to wireless communications, and a second communication chip 2012 may be dedicated to wired communications.

[0072] The computing device 2000 may include battery/power circuitry 2014. The battery/power circuitry 2014 may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of the computing device 2000 to an energy source separate from the computing device 2000 (e.g., AC line power).

[0073] The computing device 2000 may include a display device 2006 (or corresponding interface circuitry, as discussed above). The display device 2006 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display, for example.

[0074] The computing device 2000 may include an audio output device 2008 (or corresponding interface circuitry, as discussed above). The audio output device 2008 may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[0075] The computing device 2000 may include an audio input device 2024 (or corresponding interface circuitry, as discussed above). The audio input device 2024 may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0076] The computing device 2000 may include a global positioning system (GPS) device 2018 (or corresponding interface circuitry, as discussed above). The GPS device 2018 may be in communication with a satellite-based system and may receive a location of the computing device 2000, as known in the art.

[0077] The computing device 2000 may include an other output device 2010 (or corresponding interface circuitry, as discussed above). Examples of the other output device 2010 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0078] The computing device 2000 may include an other input device 2020 (or corresponding interface circuitry, as discussed above). Examples of the other input device 2020 may include an accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0079] The computing device 2000, or a subset of its components, may have any appropriate form factor, such as a hand-held or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultramobile personal computer, etc.), a desktop computing device, a server or other networked computing component, a printer, a scanner,

a monitor, a set-top box, an entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a wearable computing device.

[0080] The following paragraphs provide various examples of the embodiments disclosed herein.

[0081] Example 1 is an electronic device, including: a substrate; a resistive random access memory (RRAM) device, including a bottom electrode, an oxygen exchange layer (OEL), and an oxide layer; wherein the bottom electrode is disposed between the OEL and the substrate, and the OEL is disposed between the oxide layer and the bottom electrode.

[0082] Example 2 may include the subject matter of Example 1, and may further specify that the RRAM device further includes a spacer disposed between the OEL and the oxide layer.

[0083] Example 3 may include the subject matter of Example 2, and may further specify that the spacer is a nitride material.

[0084] Example 4 may include the subject matter of Example 3, and may further specify that the spacer includes hafnium.

[0085] Example 5 may include the subject matter of any of Examples 2-4, and may further specify that the spacer has a thickness between 10 angstroms and 5 nanometers.

[0086] Example 6 may include the subject matter of any of Examples 2-5, and may further specify that the spacer includes oxygen.

[0087] Example 7 may include the subject matter of any of Examples 1-6, and may further include a transistor having a source/drain (S/D) region coupled to the bottom electrode through an interconnect structure.

[0088] Example 8 may include the subject matter of Example 7, and may further specify that the transistor is an n-type metal oxide semiconductor (NMOS) transistor.

[0089] Example 9 may include the subject matter of any of Examples 7-8, and may further specify that the interconnect structure is entirely disposed between a device layer and an interconnect layer in which the bottom electrode is disposed.

[0090] Example 10 may include the subject matter of any of Examples 1-9, and may further specify that the bottom electrode is titanium nitride.

[0091] Example 11 may include the subject matter of any of Examples 1-10, and may further specify that the OEL is hafnium.

[0092] Example 12 may include the subject matter of any of Examples 1-11, and may further specify that the oxide layer is hafnium oxide.

[0093] Example 13 is a method of manufacturing a resistive random access memory (RRAM) device, including: forming an interconnect structure in an interlayer dielectric; after forming the interconnect structure, forming a bottom electrode in contact with the interconnect structure; and

after forming the bottom electrode, forming an oxygen exchange layer (OEL) on the bottom electrode.

[0094] Example 14 may include the subject matter of Example 13, and may further include, after forming the OEL on the bottom electrode, forming a spacer on the OEL.

[0095] Example 15 may include the subject matter of Example 14, and may further specify that forming the spacer includes: providing an initial spacer material on the OEL; providing an oxide layer on the initial spacer material; and after providing the oxide layer, annealing the initial spacer material.

[0096] Example 16 may include the subject matter of any of Examples 14-15, and may further specify that forming the spacer includes physical vapor deposition (PVD) of material of the spacer.

[0097] Example 17 may include the subject matter of Example 16, and may further specify that forming the OEL includes PVD of the OEL, and PVD of the OEL takes place in a same chamber as PVD of the material of the spacer.

[0098] Example 18 may include the subject matter of any of Examples 14-17, and may further include: after forming the OEL, forming an oxide layer above the spacer; and after forming the oxide layer, forming a top electrode above the oxide layer.

[0099] Example 19 may include the subject matter of Example 18, and may further specify that forming the oxide layer includes atomic layer deposition (ALD) of the oxide layer.

[0100] Example 20 may include the subject matter of Example 19, and may further specify that the spacer is exposed to air prior to forming of the oxide layer.

[0101] Example 21 is a method of operating a memory cell, including: using an n-type metal oxide semiconductor (NMOS) transistor to control current to a resistive random access memory (RRAM) device to cause oxygen vacancy breakdown in the RRAM device; using the NMOS transistor to control current to the RRAM device to set the RRAM device in a low resistance state; and using the NMOS transistor to control current to the RRAM device to reset the RRAM device to a high resistance state.

[0102] Example 22 may include the subject matter of Example 21, and may further specify that using the NMOS transistor to control current to the RRAM device to set the RRAM device in the low resistance state causes source degeneration of the NMOS transistor.

[0103] Example 23 may include the subject matter of any of Examples 21-22, and may further specify that the NMOS transistor is included in a device layer of a die, the RRAM device includes an oxygen exchange layer (OEL) and an oxide layer, and the OEL is disposed between the oxide layer and the device layer.

[0104] Example 24 may include the subject matter of Example 23, and may further specify that the RRAM device includes a spacer disposed between the OEL and the oxide layer.

[0105] Example 25 may include the subject matter of Example 24, and may further specify that the spacer is a nitride.

[0106] Example 26 is a computing device, including: a circuit board; a processing device coupled to the circuit board; and a memory device coupled to the processing device, and may further specify that the memory device includes a resistive random access memory (RRAM) device formed above a substrate, the RRAM device includes an oxygen exchange layer (OEL) and an oxide layer, and the OEL is disposed between the oxide layer and the substrate.

[0107] Example 27 may include the subject matter of Example 26, and may further specify that the RRAM device includes a spacer disposed between the OEL and the substrate.

[0108] Example 28 may include the subject matter of Example 27, and may further specify that the spacer includes an oxynitride.

Claims:

1. An electronic device, comprising:
a substrate;
a resistive random access memory (RRAM) device, including:
a bottom electrode,
an oxygen exchange layer (OEL), and
an oxide layer;
wherein the bottom electrode is disposed between the OEL and the substrate, and the OEL is disposed between the oxide layer and the bottom electrode.
2. The electronic device of claim 1, wherein the RRAM device further includes:
a spacer disposed between the OEL and the oxide layer.
3. The electronic device of claim 2, wherein the spacer is a nitride material.
4. The electronic device of claim 3, wherein the spacer includes hafnium.
5. The electronic device of claim 2, wherein the spacer includes oxygen.
6. The electronic device of claim 1, further comprising:
a transistor having a source/drain (S/D) region coupled to the bottom electrode through an interconnect structure.
7. The electronic device of claim 6, wherein the transistor is an n-type metal oxide semiconductor (NMOS) transistor.
8. The electronic device of claim 6, wherein the interconnect structure is entirely disposed between a device layer and an interconnect layer in which the bottom electrode is disposed.
9. The electronic device of any of claims 1-8, wherein the OEL is hafnium.
10. The electronic device of any of claims 1-8, wherein the oxide layer is hafnium oxide.
11. A method of manufacturing a resistive random access memory (RRAM) device, including:
forming an interconnect structure in an interlayer dielectric;
after forming the interconnect structure, forming a bottom electrode in contact with the interconnect structure; and
after forming the bottom electrode, forming an oxygen exchange layer (OEL) on the bottom electrode.
12. The method of claim 11, further comprising:
after forming the OEL on the bottom electrode, forming a spacer on the OEL.
13. The method of claim 12, wherein forming the spacer includes:
providing an initial spacer material on the OEL;
providing an oxide layer on the initial spacer material; and

after providing the oxide layer, annealing the initial spacer material.

14. The method of claim 12, wherein forming the spacer includes physical vapor deposition (PVD) of material of the spacer.

15. The method of claim 14, wherein forming the OEL includes PVD of the OEL, and PVD of the OEL takes place in a same chamber as PVD of the material of the spacer.

16. The method of claim 12, further comprising:

after forming the OEL, forming an oxide layer above the spacer; and

after forming the oxide layer, forming a top electrode above the oxide layer.

17. The method of claim 16, wherein forming the oxide layer includes atomic layer deposition (ALD) of the oxide layer.

18. The method of claim 17, wherein the spacer is exposed to air prior to forming the oxide layer.

19. A method of operating a memory cell, comprising:

using an n-type metal oxide semiconductor (NMOS) transistor to control current to a resistive random access memory (RRAM) device to cause oxygen vacancy breakdown in the RRAM device;

using the NMOS transistor to control current to the RRAM device to set the RRAM device in a low resistance state; and

using the NMOS transistor to control current to the RRAM device to reset the RRAM device to a high resistance state.

20. The method of claim 19, wherein the NMOS transistor is included in a device layer of a die, the RRAM device includes an oxygen exchange layer (OEL) and an oxide layer, and the OEL is disposed between the oxide layer and the device layer.

21. The method of claim 20, wherein the RRAM device includes a spacer disposed between the OEL and the oxide layer.

22. The method of claim 21, wherein the spacer is a nitride.

23. A computing device, comprising:

a circuit board;

a processing device coupled to the circuit board; and

a memory device coupled to the processing device, wherein the memory device includes a resistive random access memory (RRAM) device formed above a substrate, the RRAM device includes an oxygen exchange layer (OEL) and an oxide layer, and the OEL is disposed between the oxide layer and the substrate.

24. The computing device of claim 23, wherein the RRAM device includes a spacer disposed between the OEL and the substrate.

25. The computing device of claim 24, wherein the spacer includes an oxynitride.

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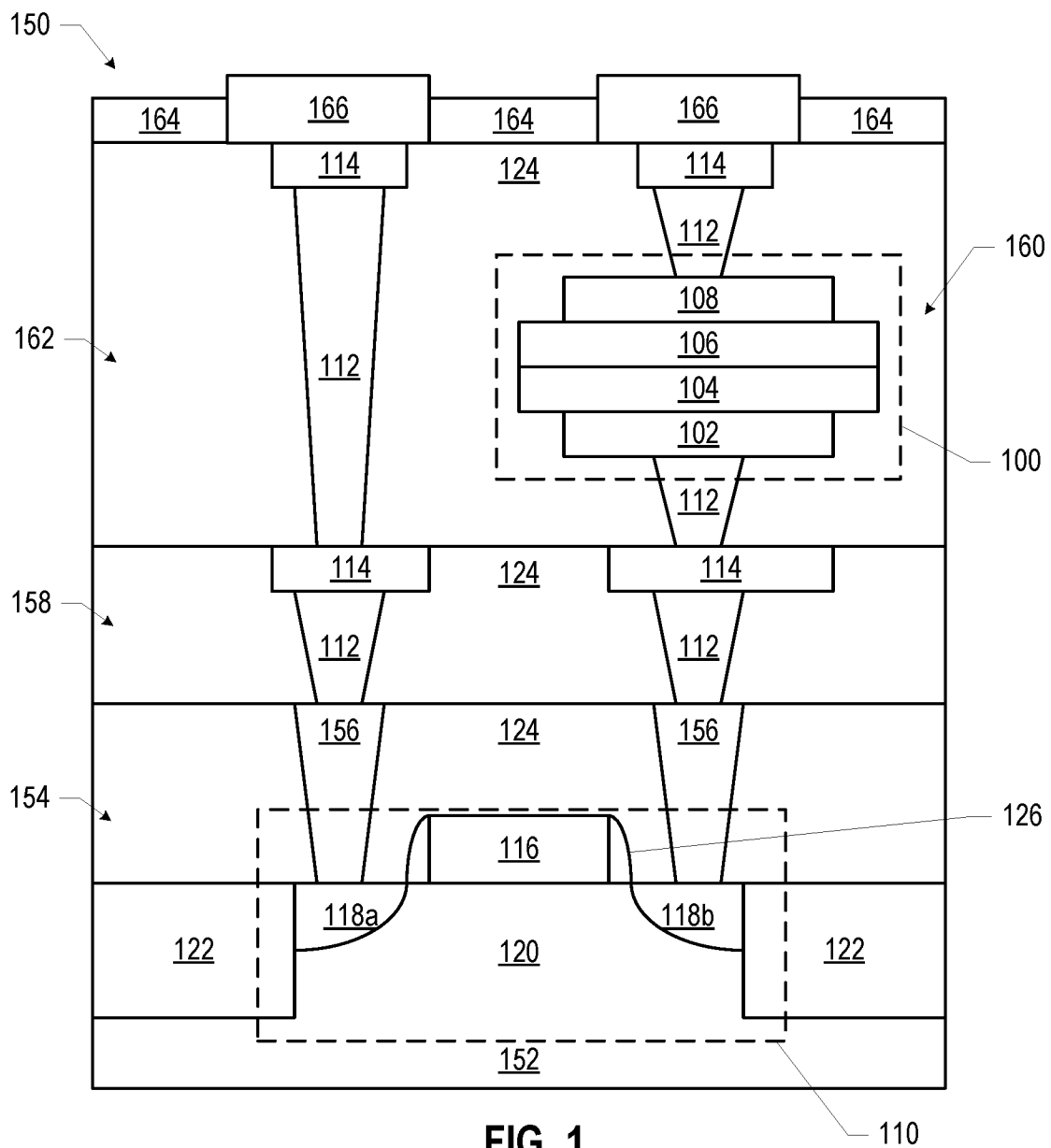


FIG. 1

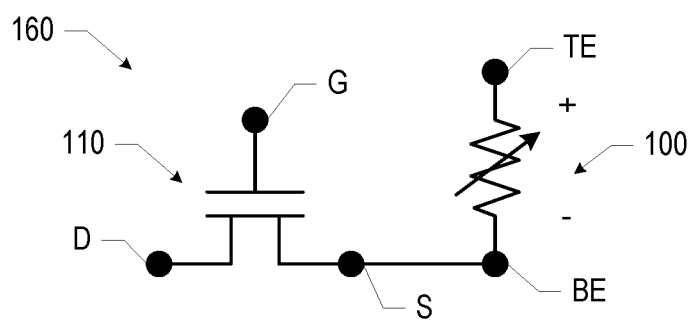


FIG. 2

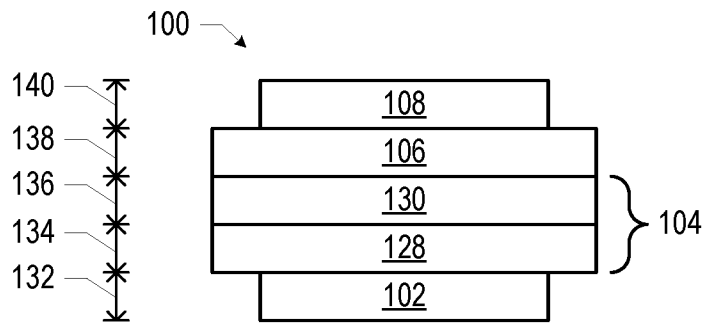


FIG. 3

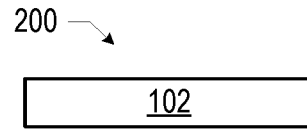


FIG. 4

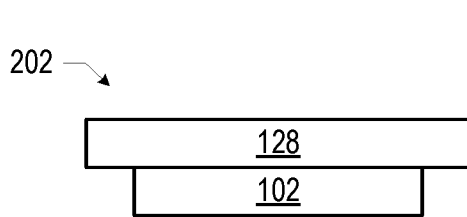


FIG. 5

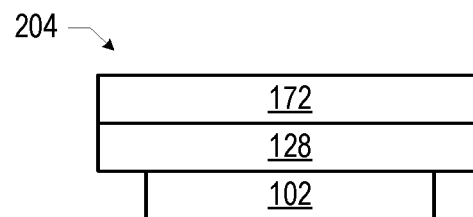


FIG. 6

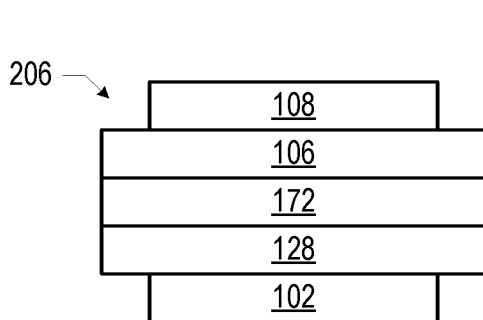


FIG. 7

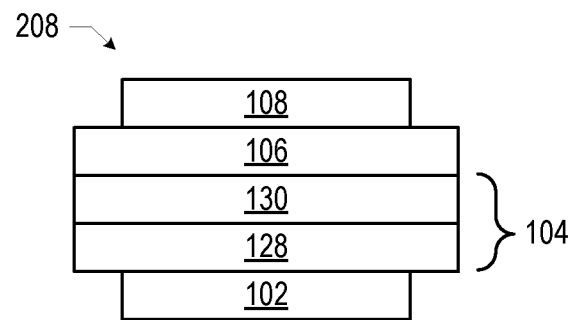
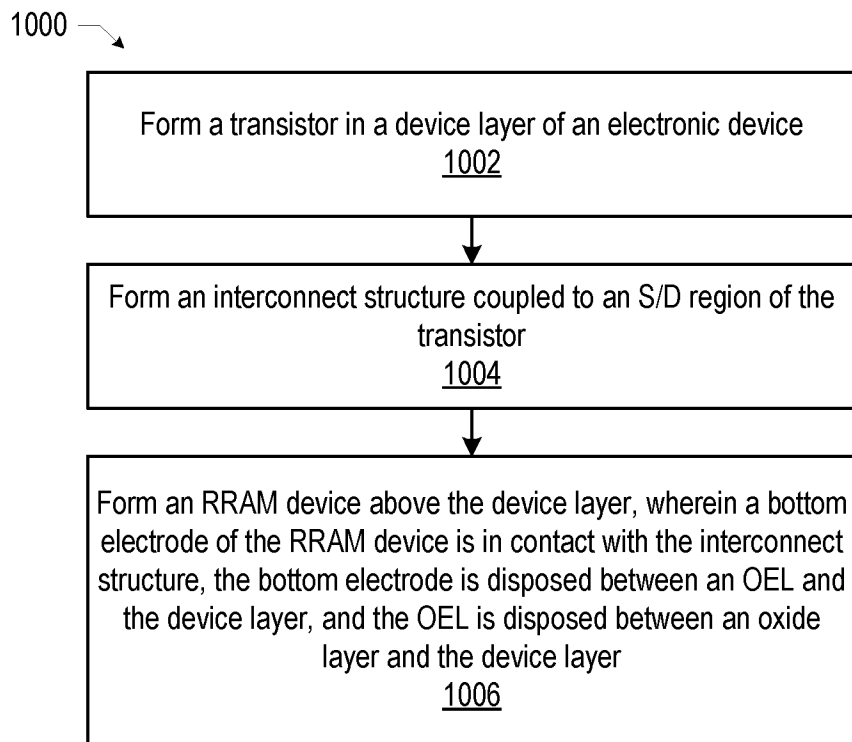
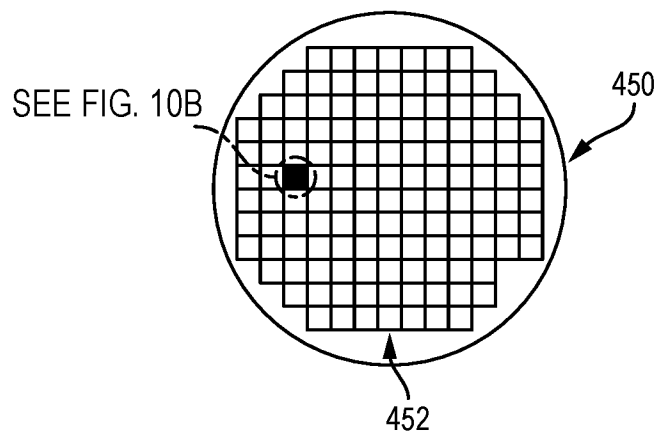
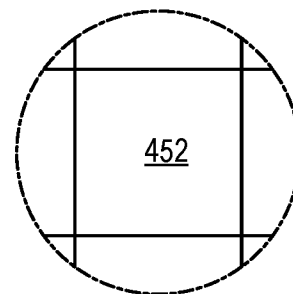


FIG. 8

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**FIG. 9****FIG. 10A****FIG. 10B**

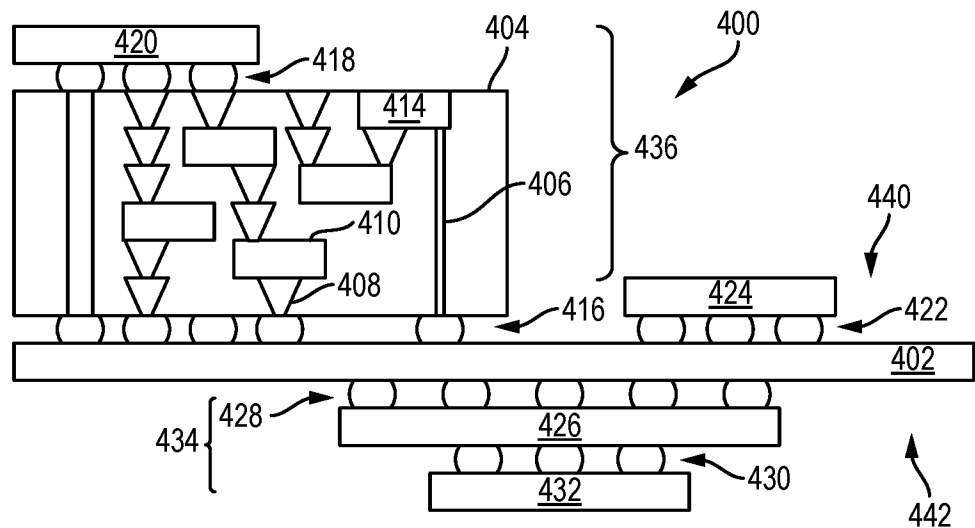


FIG. 11

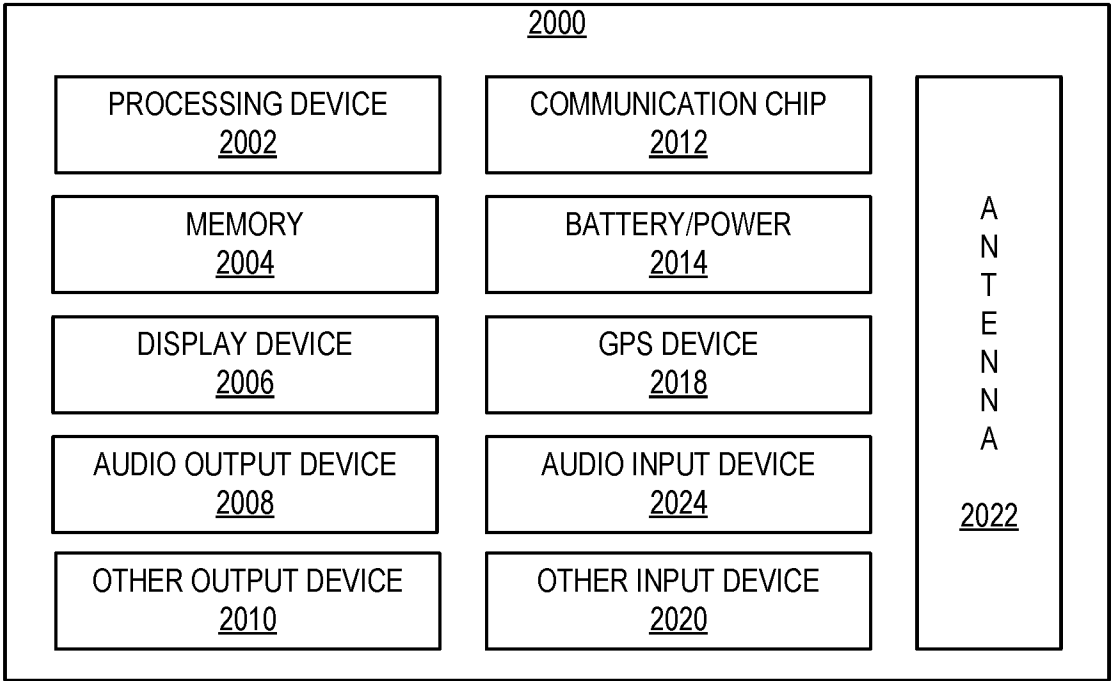


FIG. 12

A. CLASSIFICATION OF SUBJECT MATTER**H01L 45/00(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 45/00; B05D 5/12; H01L 31/032; G11C 11/21; H01L 31/173; H01L 29/66; H01L 21/285

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: resistive random access memory, oxygen exchange layer, oxide layer, spacer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2013-0170278 A1 (FREDERICK T. CHEN et al.) 04 July 2013 See paragraphs [0008]–[0011], [0030], [0034]; claim 23; and figures 6A–7B.	1–25
Y	US 2010-0021626 A1 (CHUN-I HSIEH et al.) 28 January 2010 See paragraphs [0008]–[0015]; claim 1; and figures 2a, 2b.	1–25
Y	US 2014-0175361 A1 (INTERMOLECULAR INC.) 26 June 2014 See paragraphs [0009], [0025], [0031], [0047], [0074], [0081], [0082]; claim 1; and figures 4, 5.	2–5, 8–10, 13–18, 21, 22, 25
Y	US 2015-0270134 A1 (QUALCOMM INC.) 24 September 2015 See claim 22.	6–8
Y	US 2014-0145189 A1 (EMPIRE TECHNOLOGY DEVELOPMENT, LLC.) 29 May 2014 See paragraph [0006].	23–25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

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Information on patent family members

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