

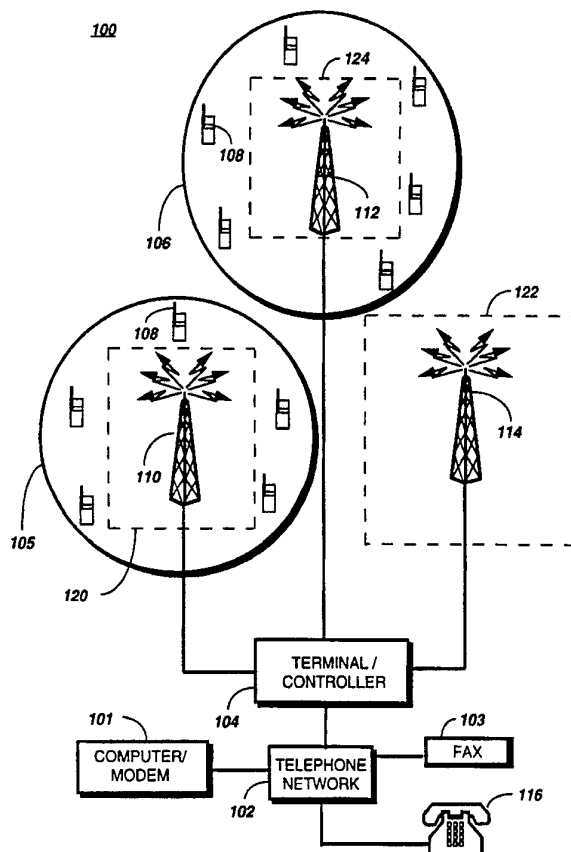


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<p>(54) Title: COMMUNICATION SYSTEM FOR COMMUNICATING WITH A PLURALITY OF SELECTIVE CALL RECEIVERS AND METHOD THEREFOR</p>		

(57) Abstract

A selective call base station (100) for receiving a signal comprising a plurality of communication signals has an Analog-to-Digital (A/D) converter (220) for digitizing the signal. A memory (204) for storing the signal as a plurality of digitized bits (502-518), and a Digital Signal Processor (DSP) (218) for converting each of the plurality of digitized bits (502-518) into a frequency domain signal (Fig. 6) that has a plurality of frequency samples. The memory (204) stores the plurality of frequency samples corresponding to each of the plurality of digitized bits (502-518). A decoder (206, 218) decodes the plurality of communication signals from the plurality of frequency samples. The decoder (206, 218) further includes a generator (718) for generating a window (902) for measuring energy of at least one frequency sample of the plurality of digitized bits (502-518) in each of the plurality of communication signals. A determinator (728) determines the at least one frequency sample of each of the plurality of communication signals having a maximum energy.



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**COMMUNICATION SYSTEM FOR COMMUNICATING WITH
A PLURALITY OF SELECTIVE CALL RECEIVERS
AND METHOD THEREFOR**

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Field of the Invention

This invention relates in general to communication systems and more particularly to a communication system and method for communicating with a plurality of selective call receivers.

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Background of the Invention

Communication on a wide band channel requires a passband filter at the input of the signal. The response of the passband filter should
15 accurately receive the wideband signal making a discriminator type demodulator suitably efficient for decoding the wideband signal. However, when the signal to be received comprises a plurality of narrowband signals within a single wideband channel, the plurality of narrow band signals are decoded by using a plurality of filters having a response tuned to each of the
20 frequencies. The plurality of filters provide a very cost intensive decoding technique.

Unfortunately, with communication on a narrow band channel, the received signal suffers from two major problems: fading and frequency offset. With fading, the envelope and the phase of the received signal vary
25 in a random manner because of multi-path effects. If a transmitted frequency modulated (FM) signal has a bandwidth less than the coherence bandwidth of the multipath channel, the random FM noise produced by the received signal phase variations will be superimposed on the desired modulation. Therefore, when a conventional discriminator is used to
30 demodulate the signal, the random FM places an upper boundary on the baseband signal-to-noise ratio achievable at the output of the frequency discriminator. Also, the upper bound of the signal-to-noise ratio (ceiling) gets lower for a narrow band signal. This ceiling results in a floor in the error rate for the demodulation.

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Additionally, the narrow band signals have a random frequency offset causing the narrow band signals to be received at different positions within their subchannels. Therefore, the plurality of narrow bandpass filters must have a frequency response at least equal to each of narrow band

subchannels. By increasing the bandwidth of the narrow bandpass filters, the signals will arrive within the bandwidth of the narrow bandpass filters. Unfortunately, to guarantee the reception of each narrow band signal, the signal to noise ratio of the filter must be severely degraded.

- 5 Thus what is needed is a method and apparatus for receiving and decoding the plurality of narrow band signals for generating a high signal to noise ratio in a cost effect manner.

Summary of the Invention

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- A method for receiving a signal comprising a plurality of communication signals comprises the steps of: a) digitizing the signal corresponding to a plurality of digitized bits; b) converting each of the plurality of digitized bits into a frequency domain signal comprising a plurality of frequency samples; c) storing the plurality of frequency samples corresponding to each of the plurality of digitized bits; and d) decoding the plurality of communication signals from the plurality of frequency samples. The step of decoding further comprises the steps of: e) generating a window for measuring energy of at least one frequency sample of the plurality of digitized bits in each of the plurality of communication signals; and f) determining the at least one frequency sample of each of the plurality of communication signals having a maximum energy.
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- A selective call base station for receiving a signal comprising a plurality of communication signals comprises an Analog-to-Digital (A/D) converter for digitizing the signal, a memory for storing the signal as a plurality of digitized bits, and a Digital Signal Processor (DSP) for converting each of the plurality of digitized bits into a frequency domain signal comprising a plurality of frequency samples. The memory stores the plurality of frequency samples corresponding to each of the plurality of digitized bits. A decoder decodes the plurality of communication signals from the plurality of frequency samples. The decoder further comprises a generator for generating a window for measuring energy of at least one frequency sample of the plurality of digitized bits in each of the plurality of communication signals. A determinator determines the at least one frequency sample of each of the plurality of communication signals having a maximum energy.
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Brief Description of the Drawings

FIG. 1 is an electrical block diagram of a selective call communication system in accordance with the preferred embodiment of the present invention.

FIG. 2 is an electrical block diagram of a selective call base station in accordance with the preferred embodiment of the present invention.

FIG. 3 is an electrical block diagram of a selective call receiver in accordance with the preferred embodiment of the present invention.

FIG. 4 is an electrical block diagram of a microcomputer based decoder/controller suitable for use in the selective call receiver of FIG. 3.

FIG. 5 is a timing diagram illustrating an example of a bit pattern of the acknowledge back signal of one of the group of the selective call receiver in accordance with the preferred embodiment of the present invention.

FIG. 6 is a frequency domain representation of a wide band channel illustrating ten subchannels representing the frequency domain representation of the acknowledge back signals in accordance with the preferred embodiment of the present invention.

FIG. 7 is a flow diagram illustrating the operation of the DSP of the selective call base station in accordance with the preferred embodiment of the present invention.

FIG. 8 illustrates a matrix representation having rows corresponding to the number of bits and columns corresponding to the number of frequency samples in accordance with the preferred embodiment of the present invention.

FIG. 9 is the frequency domain representation of the bits of a subchannel corresponding to FIG. 5 in accordance with the preferred embodiment of the present invention.

FIG. 10 is a frequency domain representation illustrating the decoding of the bits in the subchannel by generating a window in accordance with the preferred embodiment of the present invention.

FIG. 11 is a flow diagram illustrating the operation of the selective call receiver in accordance with the preferred embodiment of the present invention.

Description of a Preferred Embodiment

Referring to FIG. 1, a selective call communication system 100 in accordance with a preferred embodiment of the present invention is shown. The selective call communication system 100 comprise a terminal/controller 104 coupled to a computer (not shown) via a modem 101 and a facsimile (FAX) machine 103 and a telephone 116 via a conventional public or private telephone network 102 known to one of ordinary skill in the art. The telephone network 102 through the terminal/controller 104 is coupled to a plurality of selective call base stations (or sites) 120-124. The plurality of selective call base stations 120-124 transmit and receive signals via its respective transmitters/receivers 110-114. The details of the operation of the selective call base stations 110-114 will be discussed below. The plurality of selective call base sites 120-124 have an associated coverage area (for example, 105 and 106) into which signals from the terminal/controller 104 are broadcast and received by at least one of a plurality of selective call receivers 108.

Referring to FIG. 2, a more detailed block diagram of the selective call base stations 120-124 are shown in accordance with the preferred embodiment of the present invention. The selective call base stations 120-124 comprise a telephone interconnect 201 which allows messages to enter into the selective call communication system 100 through a public or private telephone network using, for example, a telephone 116, a computer 102, a facsimile 103 or an alphanumeric entry device (not shown). A communication terminal 202, for example the Motorola's MODEN PLUS Encoder, processes the information received through the telephone interconnect 201. A generated address and message decoded from the received information are stored in a memory 204 until the next transmission cycle.

As shown, the communication terminal 202 is coupled to a controller 206, which controls the operation of a link transmitter 208, a communicating transmitter 210, a link receiver 212, and a communicating receiver 214. An example of a controller suitable for use in the present invention is Motorola's MC6809 controller. A timing generator 216, coupled to the controller 206, provides a high accuracy clock to maintain system timing for communication and synchronization of the selective call communication system 100 including all the selective call base stations

120-124 and the plurality of selective call receiver 108 by techniques known to one skilled in the arts. Operationally, the communicating transmitter 210 transmits, to the plurality of selective call receivers 108, a signal which comprises a paging type message preferably on a first frequency at the transmission cycle. Preferably, a group of selective call receivers are intended (addressed) by the communicating transmitter 210 to receive the paging message. As is known, the paging message before transmission transmitting is encoded with the appropriate address for addressing the group of selective call receivers of the plurality of selective call receivers 108. For example, and according to the preferred embodiment of the present invention, when a group of the plurality of the selective call receivers 108 have been paged, the selective call receivers of the group that received the message will substantially simultaneously transmit a response, the acknowledge back signals. Preferably, the acknowledge back response (acknowledgment) is transmitted on a second frequency preferably substantially lower than the first frequency. The receiver 214 of the selective call base stations 120-124 receives the acknowledge back response (acknowledgment signal or ack-back signal) which is stored in a memory 204. As is well known, the receiver 214 demodulates the ack-back signal to produce preferably a baseband signal. The baseband signal is converted (digitized) from an analog signal to a digital signal by an analog-to-digital (A/D) converter 220 known to one of ordinary skill in the art. The conversion by the A/D converter 220 are received and stored by a digital Signal Processor (DSP) 218. The DSP 218, for example, can include a Motorola's DSP56100 or a Texas Instrument's TMS3000 series digital signal processors. According to the preferred embodiment of the present invention, the DSP 218 stores the digitized samples as digitized bits and continuously receives and stores the digitized samples until all bits of the ack-back signal have been received and stored. The digitized samples are retrieved and each bit is converted into its spectral domain representation. Preferably, the DSP 218 performs a Fast Fourier Transform (FFT) on each digitized bit to generate the frequency domain signal which comprises the plurality of ack-back signals received as a composite time domain signal from the responding selective call receivers of the group of selective call receiver 108. The timing generator 216 is coupled to the DSP 218 to provide synchronization and timing for processing the plurality of

digitized bits comprising the plurality of ack-back signal. The operation of the DSP 218 will be discussed in detail below.

Referring to FIG. 3, an electrical block diagram of a selective call receiver is shown in accordance with the preferred embodiment of the present invention. The selective call receiver 108 comprises an antenna 302 for intercepting transmitted radio frequency (RF) signals which are coupled to the input of a receiver 304. The RF signals are preferably selective call (paging) message signals which provide, for example, a receiver address and an associated message, such as numeric or alphanumeric message. However, it will be appreciated that other well known paging signaling formats, such as tone only signaling or tone and voice signaling, would be suitable for use as well. The receiver 304 processes the RF signal and produces at the output a data stream representative of a demodulated data information. The demodulated data information is coupled into the input of a decoder/controller 306 which processes the information in a manner well known in the art. A transmitter 334 is coupled to the antenna 302 and the decoder/controller 306. A power switch 310, coupled to the decoder/controller 306, is used to control the supply of power to the receiver 304, thereby providing a battery saving function, and to the transmitter 334 for transmitting the ack-back response subsequent to the receipt of a paging message which will be further discussed in detail below.

For purposes of this illustration, it will be assumed that the POCSAG signaling format is utilized which is well known in the art, although other signaling formats could be utilized as well. When the address is received by the decoder/controller 306, the received address is compared with one or more addresses stored in a code plug (or code memory) 322, and when a match is detected, an alert signal is generated to alert a user that a selective call message, or page, has been received. The alert signal is directed to an audible alerting device 314 for generating an audible alert or to a tactile alerting device 316 for generating a silent vibrating alert. Switches 320 allow the user of the selective call receiver to, among other things, select between the audible alert 314 and the tactile alert 316 in a manner well known in the art.

The message information which is subsequently received is stored in memory 404 (FIG. 4) and can be accessed by the user for display using one or more of the switches 320 which provide such additional functions as

reset, read, and delete, *etc.*. Specifically, by the use of appropriate functions provided by the switches 320, the stored message is recovered from memory and processed by the decoder/controller 206 for displaying by a display 308 which enables the user to view the message. The receipt of the message by the selective call receiver 108 can automatically generate the ack-back response to the selective call base station to inform it that the message was successfully received. Preferably, the user will have the opportunity to input a message by using switches 320 or some other input devices well known to one of ordinary skilled in the arts. When the message is entered, the decoder/controller 306 processes the message by encoding an addressed derived from the received message to generate the ack-back response. The encoded ack-back response is then transmitted to the selective call base station that originated the paging message by techniques well known to one of ordinary skill in the art.

The controller/decoder 306 of FIG. 3 can be implemented utilizing a microcomputer as shown in FIG. 4. FIG. 4 is an electrical block diagram of a microcomputer based decoder/controller suitable for use in the selective call receiver of FIG. 3. As shown, the microcomputer 306 is preferably of the MC68HC05 series microcomputers, such as manufactured by Motorola, Inc., which includes an on-board display driver 414. The microcomputer 306 includes an oscillator 418 which generates the timing signals utilized in the operation of the microcomputer 306. A crystal, or crystal oscillator (not shown) is coupled to the inputs of the oscillator 418 to provide a reference signal for establishing the microcomputer timing. A timer/counter 402 couples to the oscillator 418 and provides programmable timing functions which are utilized in controlling the operation of the receiver or the processor. A RAM (random access memory) 404 is utilized to store variables derived during processing, as well as to provide storage of message information which are received during operation as a selective call receiver. A ROM (read only memory) 406 stores the subroutines which control the operation of the receiver or the processor which will be discussed further. It will be appreciated that in many microcomputer implementations, the programmable-ROM (PROM) memory area can be provided either by a programmable read only memory (PROM) or an EEPROM (electrically erasable programmable read only memory). The oscillator 418, timer/counter 402, RAM 404, and ROM 406 are coupled through an address/data/control bus 408 to a central

processing unit (CPU) 410 which performs the instructions and controls the operations of the microcomputer 306.

The demodulated data generated by the receiver is coupled into the microcomputer 306 through an input/output (I/O) port 412. The
5 demodulated data is processed by the CPU 410, and when the received address is the same as stored within the code-plug memory which couples into the microcomputer through, for example an I/O port 413, the message, if any, is received and stored in RAM 404. Recovery of the stored message, and selection of the predetermined destination address, is
10 provided by the switches which are coupled to the I/O port 412. The microcomputer 306 then recovers the stored message and directs the information over the data bus 408 to the display driver 414 which processes the information and formats the information for presentation by a display 308 (FIG. 3) such as an LCD (liquid crystal display). At the time a
15 selective call receiver's address is received, the alert signal is generated which can be routed through the data bus 408 to an alert generator 416 that generates the alert enable signal which is coupled to the audible alert device that was described above. Alternatively, when the vibrator alert is selected, as described above, the microcomputer generates an alert enable
20 signal which is coupled through data bus 408 to the I/O port 413 to enable generation of a vibratory, or silent alert. Switch inputs are received by the I/O port 412 via the data bus 408. The switch inputs are processed by the CPU 410. Specifically, the CPU 410 retrieves the address of the selective call base station from RAM 404 and in conjunction with the timer counter
25 402 and the oscillator 418, the CPU 410 generates the ack-back signal which is passed via the data bus 40 to the transmitter.

The battery saver operation is controlled by the CPU 410 with battery saving signals which are directed over the data bus 408 to the I/O port 412 which couples to the power switch 310. Power is periodically supplied to
30 the receiver to enable decoding of the received selective call receiver address signals and any message information which is directed to the selective call receiver. Specifically, when the selective call receiver 108 begins decoding the paging signal, the receiver is powered by the power switch. When the paging message is received and stored, the
35 microcomputer 306 sends a signal to the power switch 310 to disable power to the receiver 304 and enable power to the transmitter for transmitting the ack-back signal.

Referring to FIG. 5, a timing diagram is shown illustrating an example of a bit pattern of an acknowledge back (ack-back) signal of one of the group of the selective call receivers in accordance with the preferred embodiment of the present invention. As discussed, the ack-back signal is at a frequency lower than the paging signal from the selective call base station. The paging signal is, for example, within a range from sixteen-to-thirty (16-30) Kbs (kilo-bits-seconds) while the ack-back signal is, for example, within a range of one hundred (100) bits-per-second. The bit pattern 500 illustrates an example of one of the ack-back signal of one of the selective call receiver, for example one subchannel, of the group of selective call receivers that were paged. The bit pattern shows bits 502, 506, 510, and 516-518 representing digital "ones" and bits 504, 508, and 512-514 representing digital "zeros". The ack-back response, preferably, comprises a bit pattern having 300 bits, the values of the bits depend on the information being conveyed. For example, an N member group of selective call receivers 108, subsequent to the members of the group responding by sending N or less ack-back responses, the selective call base station will receive composite bits comprising the N or less ack-back responses within each bit time which will be further discussed in detail below.

Referring to FIG. 6, a frequency domain representation of a thirty (30) KiloHertz (KHz) channel illustrating, for example, ten subchannels (ten ack-back responses) representing the frequency domain representation of the acknowledge back signals in accordance with the preferred embodiment of the present invention. As discussed above, since each bit received by the selective call base station comprises a composite bit, then converting the composite bit into its frequency representation generates a frequency domain signal illustrating the N, for example ten, ack-back signals in their sub channels. The preferred modulation scheme is binary frequency shift keying (FSK) with each of the ten selective call receivers 108 within the group assigned to one of the preferred ten subchannels 1-10. Each of the ten selective call receivers 108 of the group is assigned to a different subfrequency corresponding to one of the ten subchannels for example. The subchannels 1-10 have an approximate separation of 300 Hz between tones representing "ones" 602 and tones representing "zero" 612. Each subchannel 1-10 is located on a central axis 650 which marks the center of each subchannels 1-10 for decoding the "ones" or "zeros" tone of each of the ten subchannels. As is well known to those skilled in the art, the oscillator

of the selective call receiver must be sufficiently accurate to prevent a signal in its subchannel assignment to shift to either of its adjacent subchannels assigned to other selective call receivers of the group.

Referring to FIG. 7, a flow diagram illustrating the decoding operation of the DSP of the selective call base station is shown in accordance with the preferred embodiment of the present invention. Operationally, the selective call base station 120-124 (FIG. 2) receives and encodes the message intended for, e.g., a preassigned group of selective call receivers, preferably a group of ten. The encoded paging message is transmitted to the group of selective call receivers, step 702. After transmission, the selective call base station 120-124 waits for the ack-back response from the group of selective call receivers, step 704. Step 706 detects when the ack-back signal is received from the group of selective call receivers which arrive substantially simultaneously. As is well known, each selective call receiver may be located anywhere in the coverage area of the selective call base station, therefore, for example, each selective call receiver irrespective of its location will delay before transmitting its ack-back signal to ensure that all selective call receivers of the group will transmit at substantially the same time. Each selective call receiver calculates its delay depending on received paging signal, for example, the paging signal may contain information indicative of the time of transmission which is used to determine the delay time for transmitting the ack-back signal.

When the ack-back signal is received, step 708, the A/D converter includes a sample-and-hold circuit (S/H) which samples the bits, preferably, at sixty (60) KHz rate, because the highest frequency present in the ack-back signal is thirty (30) KHz. For each bit, there are six hundred (600) samples because the frequency of the ack-back signal is one hundred (100) Hz and the sampling frequency is 60 KHz. The samples are digitized, organized and stored according to the representative bit, step 710. Steps 708 and 710 are repeated until all the bits of the ack-back signal are received, for example, the three hundred bits. The digitized samples representing each bit are identified and retrieved from memory. The 600 samples are increased (padded), preferably, by four-hundred-and-twenty-four (424) "zeros" resulting in one-thousand-and-twenty-four samples (1024) which is a power of two as required by the Fast Fourier Transform (FFT), step 712. The DSP transforms the time representation of the ack-back signal into a frequency representation (frequency domain signal) by performing the FFT on each bit

of the ack-back signal, step 714. The frequency samples are stored, and then organized in a matrix format for subsequent processing, step 716.

Referring to FIG. 8, the matrix representation is illustrated with rows corresponding to the number of bits and columns corresponding to the number of frequency samples in accordance with the preferred embodiment of the present invention. The matrices 1-10 correspond to the subchannels 1-10 illustrated in FIG. 6. The rows of the matrix 1 is numbered 1-300 corresponding to the 300 bits of the ack-back signal. The column of the matrix 1 is numbered 1-51 representing the number of frequency samples of each subchannel. As previously discussed, each bit comprises 1024 frequency samples (after padding), and because the highest frequency component present is 30 KHz then 514 high-order frequency samples may be discarded without affecting the integrity of the spectral signal representation. Five hundred and ten (510) frequency samples remain for the ten subchannels 1-10. Therefore, each subchannel is represented by fifty-one (51) samples, and by processing each matrix, each subchannel can be processed independently of the others because of its unique matrix representation.

Referring again to FIG. 7, a window is generated for decoding the information of the ack-back responses on each of the plurality of frequency (subchannels), step 718. The window is positioned for locating the peak of the frequency domain signal of the subchannel 1 across the 300 bits in the subchannel 1, step 720. Preferably, the window is wide enough to measure eight lines of samples of the fifty-one (51) sample lines. Once the window is position, preferably across the lowest eight samples of the 300 bits, the eight sample lines are accumulated, step 722. The accumulated eight sample lines represents the total energy in the window. The window is then shifted to the next position, preferably shifted one sample line higher, step 724. The energy is measured again by summing (accumulating) the original seven sample lines plus the additional one sample line to obtain another energy value for the new window position, step 726.

Referring to FIG. 9, the frequency domain representation of the bits of the subchannel 1 corresponding to FIG. 5 is shown in accordance with the preferred embodiment of the present invention. The frequency domain signal of the time domain bit pattern (FIG. 5) shows how each bit appears after the spectral transformation of the subchannel 1. Bits 502, 506, 510, and 516 represent "ones" as identified by line 904 indicating the first half of the

window 902. Bits 504, 508, and 512-514 represent "zeros" as identified by line 906 indicating the second half of the window 902. As discussed, the ack-back signal is digital FSK modulated, where a binary "one" is assigned as the lower frequency tone 602 (see FIG. 6) and a binary "zero" is assigned
5 the upper frequency tone 612 (see FIG. 6). The window 902 is shown positioned over all the bits of each subchannel, where bits 502-516 correspond to the first eight bits, and the window continues over the next 292 bits to enclose the 300 bits of each ack-back signal (subchannel).

In this way, the position of the window is shifted until the maximum
10 energy is located which corresponds to the peak of the frequency domain signal across all 300 bits of the subchannel 1.

Referring to FIG. 10, the frequency domain representation illustrates the decoding of the bits in the subchannel by generating the window in accordance with the preferred embodiment of the present invention. The
15 tone 602 corresponding to the binary "one" is shown, and the tone 612 corresponding to the binary "zero" is shown by the dotted lines. The window 902 is ideally positioned to illustrate a tone occurring at its off-set from the center 650 of the subchannel 1. The dotted line representation of the "zero" tone shows the location where the zero tone would occur if the
20 bit was a "zero" instead of a "one". It is understood the a "one" and a "zero" occurs in exclusion of the other.

Referring again to FIG. 7, after energy of the second window position is measured, the energy values are compared with each other to determine the position of the window corresponding to the maximum energy, step
25 728. Step 730 checks if all window positions are measured. If not, the DSP process continues to step 724 for shifting to another window position. When all window positions are measured, step 730, the process continues to step 732 which divides the window 902 in half. The energy of the window 902 is checked to determine if the total energy exceeds a threshold
30 value, step 734. The threshold value indicates when a signal is present on the subchannel, therefore if the energy value is below the threshold, the process stops for that subchannel, step 736. Otherwise, the process continues to step 738 which compares the energy of the first half of the window 902 with the energy in the second half of the window 902. If the
35 energy in the first half of the window 902 is greater than energy of the second half of the window 902, step 740, the bit is decoded as a binary "one", step 744. Otherwise the bit is decoded as a binary "zero, step 742.

In this way, the invention decodes a plurality of subchannels representing responses from a plurality of selective call receivers. Each selective call receiver responds on a preassigned subchannels, and although there are preferably a maximum of ten selective call receivers capable of responding substantially simultaneously, the invention does not require a ten separate bandpass filters to receive each ack-back signal on each subchannel. A filter on each subchannel would not provide a cost effective solution for decoding the plurality of ack-back signals. Furthermore, since the filter's response could not be less than the total subchannel to ensure the receipt of the ack-back signal, the signal-to-noise ratio (SNR) would decrease by at least a ratio of 51-to-8 because the window is able to detect the peak of the ack-back signal within a resolution of eight samples while the filter's response would at least have to be as wide as the 51 samples to ensure that the signal is not missed.

Even if the response of the bandpass filter of each subchannel was reduced below the size of the subchannel to improve the SNR, the reduction would cause the filter to fail to detect the ack-back bits that fall outside the filter's response but are still inside the allocated subchannel. Therefore, by FFT the composite bits and decoding the plurality of ack-back signals in the frequency domain, the invention eliminates the need for a plurality of filters, thereby providing a cost effective way for detecting a plurality of ack-back signals from a plurality of selective call receivers while maximizing the SNR of the received signal.

FIG. 11 is a flow diagram illustrating the operation of the selective call receiver in accordance with the preferred embodiment of the present invention. The selective call receiver 108 receives the paging signal from the selective call base station, step 1102, and decodes its address and a message, if any, contained therein, step 1104. The paging signal preferably comprises a time of transmission which is also decoded, step 1104, to enable the selective call receiver 108 to calculate a delay time before it responds by sending an the ack-back response. The address of the selective call base station is also decoded from the received paging signal, step 1106. The selective call receiver 108 delays until a message is entered or until the time to transmit the ack-back response, step 1108. Preferably, the selective call receiver 108 provides an option to enable the user to enter, by techniques well known in the art, a message to be incorporated in the ack-back response, step 1110. If the message is not entered or the time to transmit

has not elapsed, the process continues to step 1108. Alternatively, if a message is entered, the message is encoded with the address of the base station, step 1112, or if the time has elapsed, the ack-back signal is encoded with a default message. In some instance, the selective call receiver may
5 not need to receive an address from the transmitting selective call base station, and simply transmits its message on its preassigned subchannel to the selective call base station. Upon receipt and encoding of the ack-back message, the selective call receiver delays until its time to transmit the ack-back response, step 1114. The ack-back response is transmitted to the
10 selective call base station, step 1116.

In this way, the plurality of selective call receiver in a group, by decoding the transmission time of the paging signal, knows the longest time to receive the page and transmit an ack-back message of any selective call receiver in the outer edge of the coverage area. The selective call
15 receiver is the able to delay for an appropriate time indicative of its current location ensuring that the plurality of selective call receivers respond substantially simultaneously.

In summary, a selective call base station receives a signal that comprises a plurality of communication signals. The selective call base
20 station comprises an Analog-to-Digital (A/D) converter for digitizing the signal into a plurality of digitized bits. The A/D converter further comprises a Sampling-and-Hold (S/H) circuit for sampling the signal at a predetermined sampling rate generating a plurality of digitized samples for each of the plurality of digitized bits. A memory stores the signal
25 corresponding the plurality of digitized samples, and a Digital Signal Processor (DSP) converts each of the plurality of digitized bits into a frequency domain signal that comprises a plurality of frequency samples. The DSP further comprises an identifier identifying the plurality of digitized samples corresponding to each of the plurality of digitized bits. A
30 padding circuit increases the plurality of digitized samples of the plurality of digitized bits to a power of two. The DSP performs a Fast Fourier Transform (FFT) on the plurality of digitized samples corresponding to each of the plurality of digitized bits to generate the plurality of frequency samples. A table organizer organizes the plurality of frequency samples in a
35 matrix which has a number of rows comprise the plurality of digitized bits and a number of columns comprise the plurality of frequency samples. The memory stores the plurality of frequency samples corresponding to each of

the plurality of digitized bits, and a decoder decodes the plurality of communication signals from the plurality of frequency samples. The decoder further comprises a generator for generating a window for measuring energy of at least one frequency sample of the plurality of digitized bits in each of the plurality of communication signals. The generator further comprises a controller for positioning the window on a corresponding one of the plurality of digitized bits of the frequency domain signals. An accumulator accumulates the at least one frequency sample in the window for measuring the energy of the window. The controller shifts the window for measuring another one of the plurality of frequency samples. The controller continues shifting the window until the plurality of frequency samples of the one of the plurality of communication signals have been measured. A determinator determines the at least one frequency sample of each of the plurality of communication signals that has a maximum energy. The determinator further comprises a comparator for comparing the energy of each position of the window for determining the position of the window corresponding to the maximum energy. A divider divides the window corresponding to the maximum energy into a first and second portions, and the comparator compares the first portion with the second portion for determining a binary representation of each of the digitized bits.

In this way, the invention decodes a plurality of subchannels representing responses from a plurality of selective call receivers. Each selective call receiver responds on a preassigned subchannels, and although there are preferably a maximum of ten selective call receivers capable of responding substantially simultaneously, the invention does not require a ten separate bandpass filters to receive each ack-back signal on each subchannel. A filter on each subchannel would not provide a cost effective solution for decoding the plurality of ack-back signals. Furthermore, since the filter's response could not be less than the total subchannel to ensure the receipt of the ack-back signal, the signal-to-noise ratio (SNR) would decrease by at least a ratio of 51-to-8 because the window is able to detect the peak of the ack-back signal within a resolution of eight samples while the filter's response would at least have to be as wide as the 51 samples to ensure that the signal is not missed.

Even if the response of the bandpass filter of each subchannel was reduced below the size of the subchannel to improve the SNR, the reduction would cause the filter to fail to detect the ack-back bits that fall outside the filter's response but are still inside the allocated subchannel.

- 5 Therefore, the invention provides a cost effective way for detecting a plurality of ack-back signals from a plurality of selective call receivers while maximizing the SNR of the received signal.

We claim:

CLAIMS

1. A method for receiving a signal comprising a plurality of communication signals, comprising the steps of:
 - 5 a) digitizing the signal corresponding to a plurality of digitized bits;
 - b) converting each of the plurality of digitized bits into a frequency domain signal comprising a plurality of frequency samples;
 - c) storing the plurality of frequency samples corresponding to each of the plurality of digitized bits; and
 - 10 d) decoding the plurality of communication signals from the plurality of frequency samples, the step of decoding further comprising the steps of:
 - e) generating a window for measuring energy of at least one frequency sample of the plurality of digitized bits in each of the plurality of communication signals; and
 - 15 f) determining the at least one frequency sample of each of the plurality of communication signals having a maximum energy.
2. The method according to claim 1 wherein the step of digitizing further comprising a step of sampling the signal at a predetermined sampling rate
20 for generating a plurality of digitized samples for each of the plurality of digitized bits.
3. The method according to claim 2 wherein the step of converting further comprising steps of:
 - 25 identifying the plurality of digitized samples corresponding to each of the plurality of digitized bits;
 - increasing the plurality of digitized samples of the plurality of digitized bits to a power of two; and
 - performing a Fast Fourier Transform (FFT) on the plurality of digitized
30 samples corresponding to each of the plurality of digitized bits for generating the plurality of frequency samples.

4. The method according to claim 1 wherein the step of storing further comprising a step of organizing the plurality of frequency samples in a matrix representation having a number of rows comprising the plurality of digitized bits and a number of columns comprising the plurality of
- 5 frequency samples corresponding to one of the plurality of communication signals.
5. The method according to claim 1 wherein the step of generating further comprising steps of:
- 10 positioning the window on the at least one frequency sample across the plurality of digitized bits of one of the plurality of communication signals;
- accumulating the at least one frequency sample in the window for measuring the energy of the window; and
- 15 shifting the window for measuring another one of the plurality of frequency samples, the step of shifting continues until the plurality of frequency samples of the one of the plurality of communication signals have been measured.
- 20 6. The method according to claim 1 wherein the step of determining further comprising steps of:
- comparing the energy of each position of the window for determining the position of the window corresponding to the maximum energy;
- dividing the window corresponding to the maximum energy into a
- 25 first and second portions ; and
- comparing the first portion with the second portion for determining a binary representation of each of the plurality of digitized bits.

7. In a selective call communication system, a method for communicating with a plurality of selective call receivers, comprising the steps of:
- a) transmitting a selective call signal to the plurality of selective call receivers;
 - 5 b) receiving a signal comprising acknowledgment signals from at least one of the plurality of selective call receivers receiving the selective call signal;
 - c) digitizing the signal;
 - d) storing the signal corresponding to a plurality of digitized bits;
 - 10 e) converting each of the plurality of digitized bits into a frequency domain signal comprising a plurality of frequency samples; and
 - f) storing the plurality of frequency samples corresponding to each of the plurality of digitized bits; and
 - g) decoding the acknowledgment signals from the plurality of
 - 15 frequency samples, the step of decoding further comprising the steps of:
 - h) generating a window for measuring energy of at least one frequency sample of the plurality of digitized bits of the acknowledgment signals; and
 - i) determining the at least one frequency sample of the
 - 20 acknowledgment signals having a maximum energy.
8. The method according to claim 7 wherein the step of digitizing further comprising a step of sampling the signal at a predetermined sampling rate for generating a plurality of digitized samples for each of the plurality of
- 25 digitized bits.
9. The method according to claim 8 wherein the step of converting further comprising steps of:
- identifying the plurality of digitized samples corresponding to each of
 - 30 the plurality of digitized bits;
 - increasing the plurality of digitized samples of the plurality of digitized bits to a power of two; and
 - performing a Fast Fourier Transform (FFT) on the plurality of digitized samples for spectral transforming each of the plurality of digitized bits into
 - 35 a frequency representation thereof.

10. The method according to claim 7 wherein the step of storing further comprising a step of organizing the plurality of frequency samples in a matrix representation having a number of rows comprising the plurality of digitized bits and a number of columns comprising the plurality of
5 frequency samples.

11. The method according to claim 7 wherein the step of generating further comprising steps of:
 positioning the window on the at least one frequency sample across
10 the plurality of digitized bits of one of the acknowledgment signals;
 accumulating the at least one frequency sample for measuring the energy of the window; and
 shifting the window for measuring another of the plurality of
15 frequency samples, the step of shifting continuing until the plurality of frequency samples of the one of the acknowledgment signals have been measured.

12. The method according to claim 7 wherein the step of determining further comprising steps of:
20 comparing the energy of each position of the window for determining the position of the window corresponding to the maximum energy;
 dividing the window corresponding to the maximum energy into a first and second portions; and
25 comparing the first portion with the second portion for determining a binary representation of the plurality of digitized bits.

13. A selective call base station for receiving a signal comprising a plurality of communication signals, comprising:
- an Analog-to-Digital (A/D) converter for digitizing the signal;
 - a memory for storing the signal as a plurality of digitized bits;
 - 5 a Digital Signal Processor (DSP) for converting each of the plurality of digitized bits into a frequency domain signal comprising a plurality of frequency samples;
 - said memory for storing the plurality of frequency samples corresponding to each of the plurality of digitized bits; and
 - 10 a decoder for decoding the plurality of communication signals from the plurality of frequency samples, the decoder further comprising:
 - a generator for generating a window for measuring energy of at least one frequency sample of the plurality of digitized bits in each of the plurality of communication signals; and
 - 15 a determinator for determining the at least one frequency sample of each of the plurality of communication signals having a maximum energy.
14. The selective call base station according to claim 13 wherein the A/D
- 20 converter further comprising a Sampling-and-Hold (S/H) circuit for sampling the signal at a predetermined sampling rate generating a plurality of digitized samples for each of the plurality of digitized bits.
15. The selective call base station according to claim 14 wherein the DSP
- 25 further comprising:
- an identifier for identifying the plurality of digitized samples corresponding to each of the plurality of digitized bits;
 - a padding circuit for increasing the plurality of digitized samples of the plurality of digitized bits to a power of two; and
 - 30 wherein the DSP performs a Fast Fourier Transform (FFT) on the plurality of digitized samples corresponding to each of the plurality of digitized bits for generating the plurality of frequency samples.

16. The selective call base station according to claim 13 wherein the DSP further comprises a table organizer for organizing the plurality of frequency samples in a matrix representation having a number of rows comprising the plurality of digitized bits and a number of columns comprising the plurality of frequency samples corresponding to one of the plurality of communication signals.

17. The selective call base station according to claim 13 wherein the generator further comprises:

10 a controller for positioning the window on the at least one frequency sample across the plurality of digitized bits of one of the plurality of communication signals;

 an accumulator for accumulating the at least one frequency sample in the window for measuring the energy of the window; and

15 the controller shifting the window for measuring another one of the plurality of frequency samples, the controller continues shifting the window until the plurality of frequency samples of the one of the plurality of communication signals have been measured.

20 18. The selective call base station according to claim 13 wherein the determinator further comprising:

 a comparator for comparing the energy of each position of the window for determining the position of the window corresponding to the maximum energy;

25 a divider for dividing the window corresponding to the maximum energy into a first and second portions; and

 the comparator compares the first portion with the second portion for determining a binary representation of each of the digitized bits.

19. A selective call communication system comprising a selective call base station for communicating with a plurality of selective call receivers, the selective call base station comprising:
- 5 a transmitter for transmitting a selective call signal to the plurality of selective call receivers;
 - a receiver for receiving a signal comprising acknowledgment signals from at least one of the plurality of selective call receivers receiving the selective call signal;
 - an Analog-to-Digital (A/D) converter for digitizing the signal;
 - 10 a memory for storing the signal corresponding a plurality of digitized bits;
 - a Digital Signal Processor (DSP) for converting each of the plurality of digitized bits into a frequency domain signal comprising a plurality of frequency samples; and
 - 15 said memory for storing the plurality of frequency samples corresponding to each of the plurality of digitized bits; and
 - a decoder for decoding the acknowledgment signals from the plurality of frequency samples, the decoder further comprising:
 - 20 a generator for generating a window for measuring energy of at least one frequency sample of the plurality of digitized bits of the acknowledgment signals; and
 - a determinator for determining the at least one frequency sample of the acknowledgment signals having a maximum energy.
- 25 20. The selective call base station according to claim 19 wherein the A/D converter further comprising a Sampling-and-Hold (S/H) circuit for sampling the signal at a predetermined sampling rate generating a plurality of digitized samples for each of the plurality of digitized bits.

21. The selective call base station according to claim 20 wherein the DSP further comprising steps of:
- an identifier for identifying the plurality of digitized samples corresponding to each of the plurality of digitized bits;
 - 5 a padding circuit for increasing the plurality of digitized samples of the plurality of digitized bits to a power of two; and
 - wherein the DSP performs a Fast Fourier Transform (FFT) on the plurality of digitized samples for spectral transforming each of the plurality of digitized bits into a frequency representation thereof.
- 10
22. The selective call base station according to claim 19 wherein the DSP further comprises a table organizer for organizing the plurality of frequency samples in a matrix representation having a number of rows comprising the plurality of digitized bits and a number of columns comprising the
- 15 plurality of frequency samples.
23. The selective call base station according to claim 19 wherein the generator further comprising steps of:
- a controller for positioning the window on the at least one frequency
 - 20 sample across the plurality of digitized bits of one of the acknowledgment signals;
 - an accumulator for accumulating the at least one frequency sample for measuring the energy of the window; and
 - the controller shifting the window for measuring another of the
 - 25 plurality of frequency samples, the controller continues shifting the window until the plurality of frequency samples of the one of the acknowledgment signals have been measured.
24. The selective call base station according to claim 19 wherein the
- 30 determinator further comprising:
- a comparator for comparing the energy of each position of the window for determining the position of the window corresponding to the maximum energy;
 - a divider for dividing the window corresponding to the maximum
 - 35 energy into a first and second portions; and
 - the comparator comparing the first portion with the second portion for determining a binary representation of the plurality of digitized bits.

25. A selective call base station for receiving a signal comprising a plurality of communication signals, comprising:

- an Analog-to-Digital (A/D) converter for digitizing the signal into a plurality of digitized bits, the A/D converter further comprises a Sampling-and-Hold (S/H) circuit for sampling the signal at a predetermined sampling rate generating a plurality of digitized samples for each of the plurality of digitized bits;
- a memory for storing the signal corresponding the plurality of digitized samples;
- a Digital Signal Processor (DSP) for converting each of the plurality of digitized bits into a frequency domain signal comprising a plurality of frequency samples, the DSP further comprising:
 - an identifier for identifying the plurality of digitized samples corresponding to each of the plurality of digitized bits;
 - a padding circuit for increasing the plurality of digitized samples of the plurality of digitized bits to a power of two;
 - wherein the DSP performs a Fast Fourier Transform (FFT) on the plurality of digitized samples corresponding to each of the plurality of digitized bits for generating the plurality of frequency samples; and
 - a table organizer for organizing the plurality of frequency samples in a matrix representation having a number of rows comprising the plurality of digitized bits and a number of columns comprising the plurality of frequency samples;
- said memory for storing the plurality of frequency samples corresponding to each of the plurality of digitized bits; and
- a decoder for decoding the plurality of communication signals from the plurality of frequency samples, the decoder further comprising:
 - a generator for generating a window for measuring energy of at least one frequency sample of the plurality of digitized bits in each of the plurality of communication signals, the generator further comprises:

- a controller for positioning the window on a corresponding one of the plurality of digitized bits of the frequency domain signals;
an accumulator for accumulating the at least one frequency sample in the window for measuring the energy of the window; and
5 the controller shifting the window for measuring another one of the plurality of frequency samples, the controller continues shifting the window until the plurality of frequency samples of the one of the plurality of communication signals have been measured;
a determinator for determining the at least one frequency sample of
10 each of the plurality of communication signals having a maximum energy, the determinator further comprising:
a comparator for comparing the energy of each position of the window for determining the position of the window corresponding to the maximum energy;
15 a divider for dividing the window corresponding to the maximum energy into a first and second portions; and
the comparator comparing the first portion with the second portion for determining a binary representation of each of the digitized bits.

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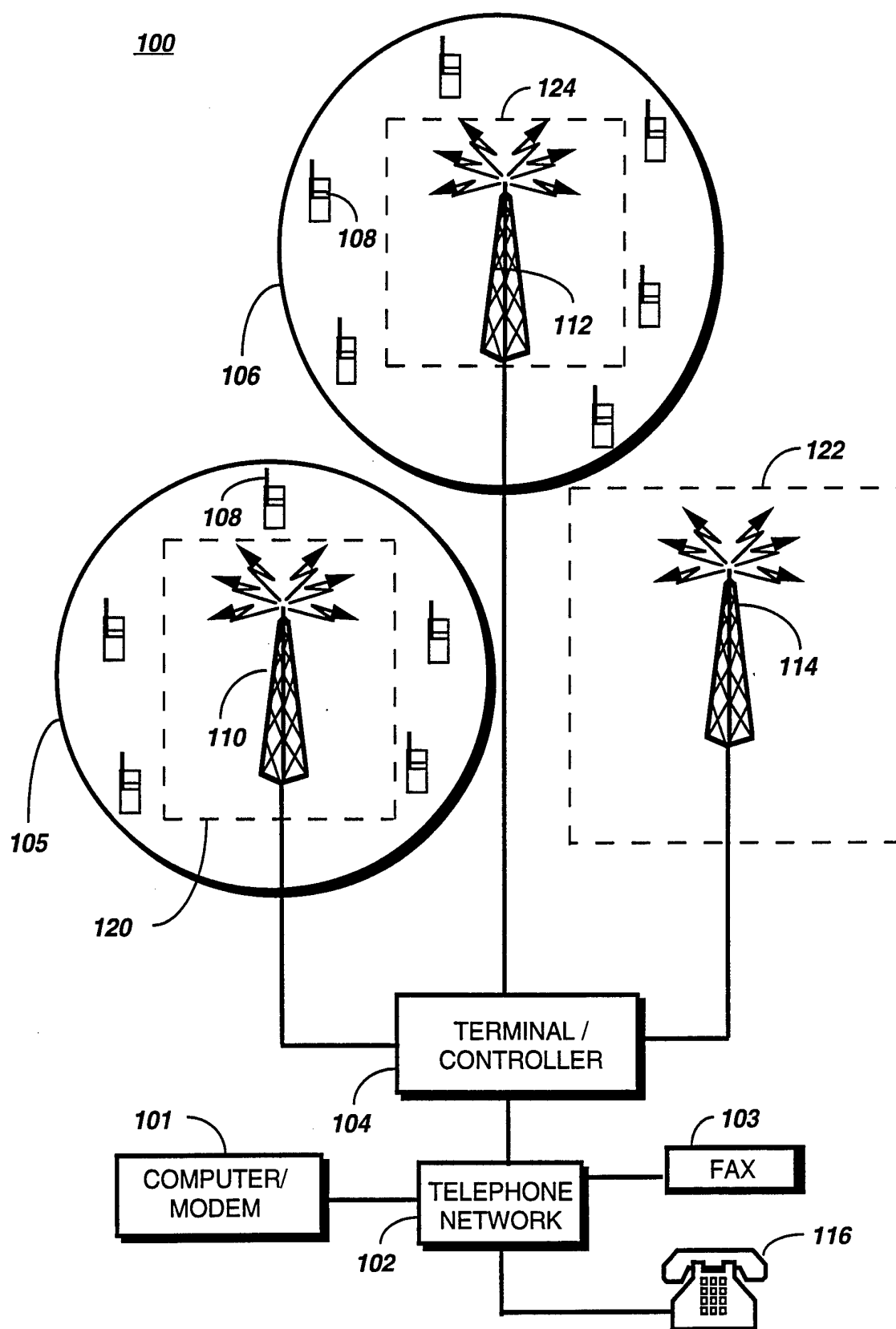
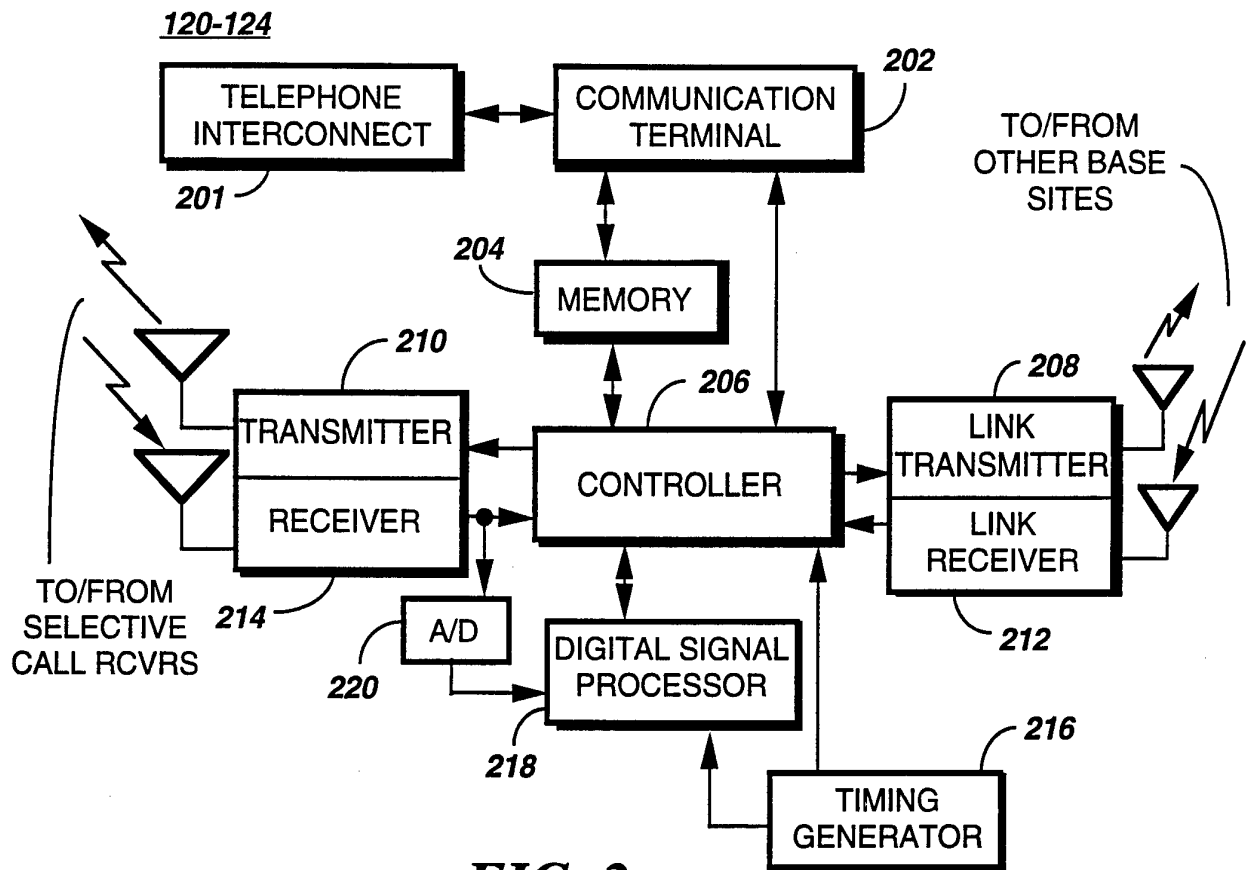
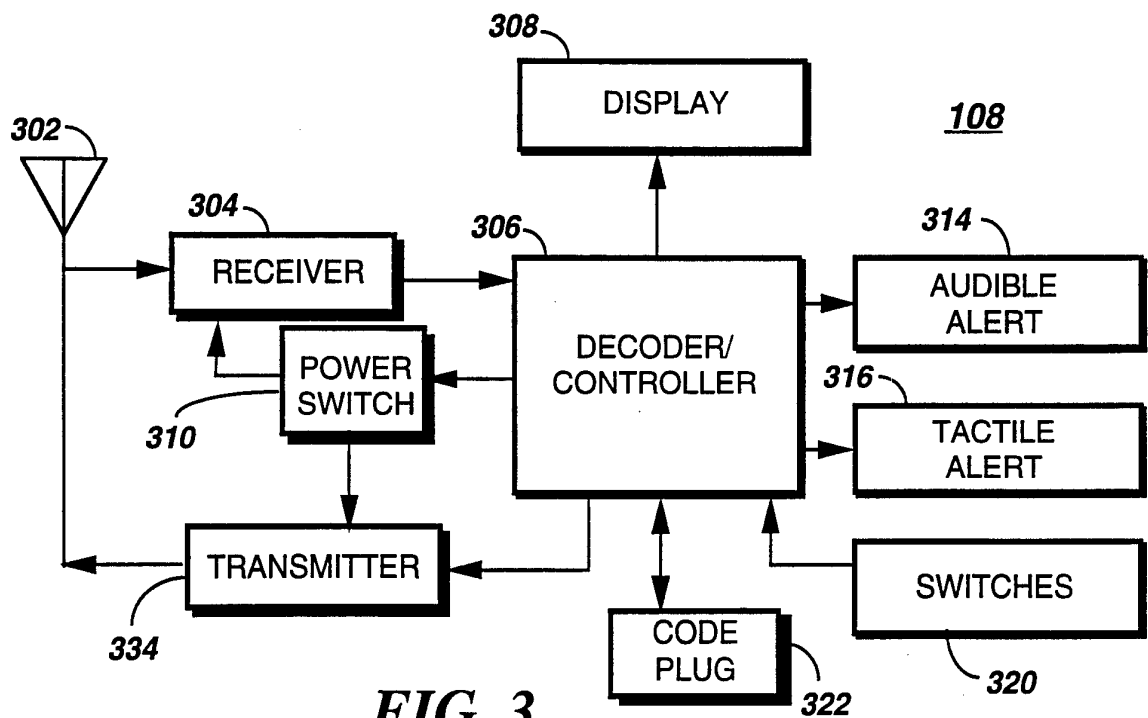
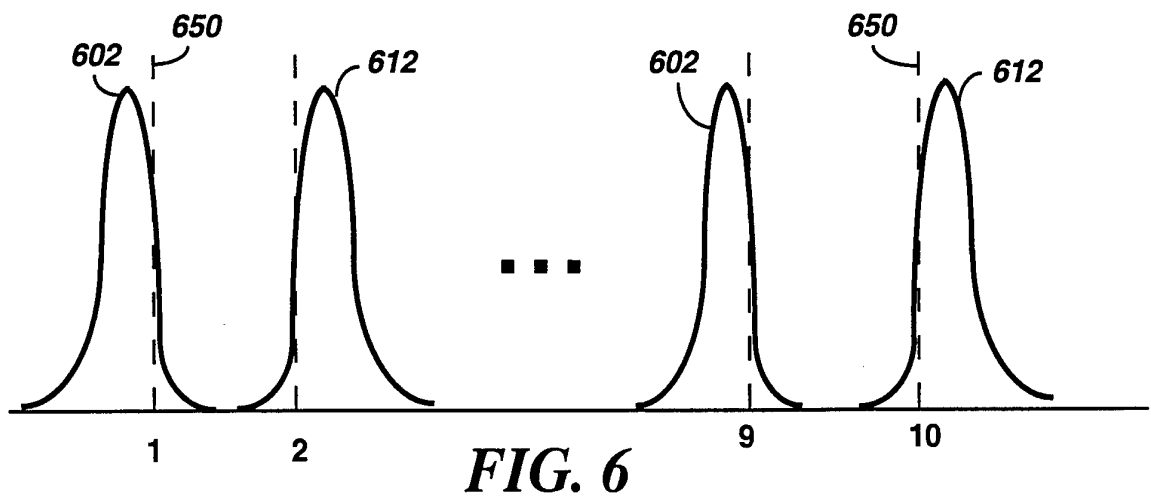
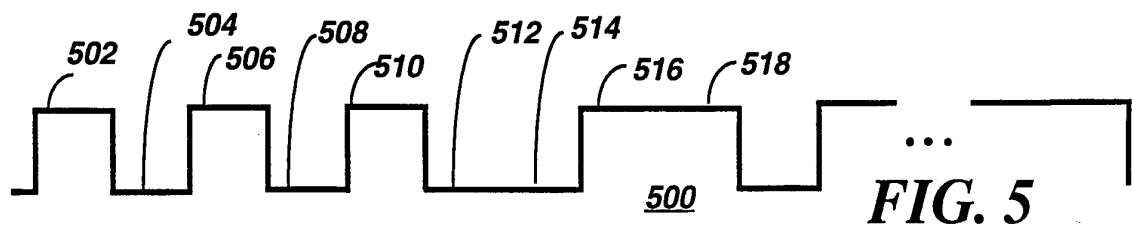
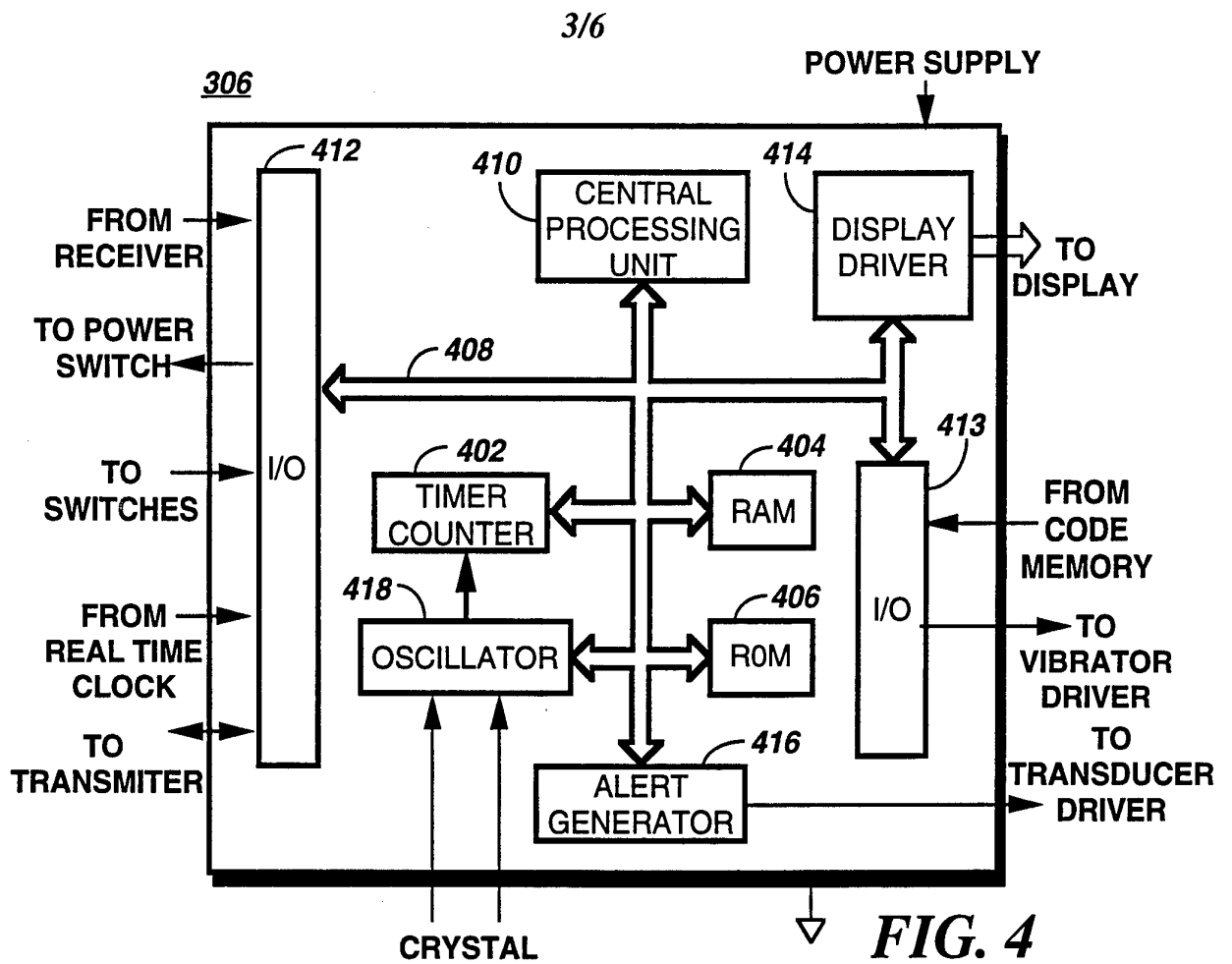


FIG. 1

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**FIG. 2****FIG. 3**



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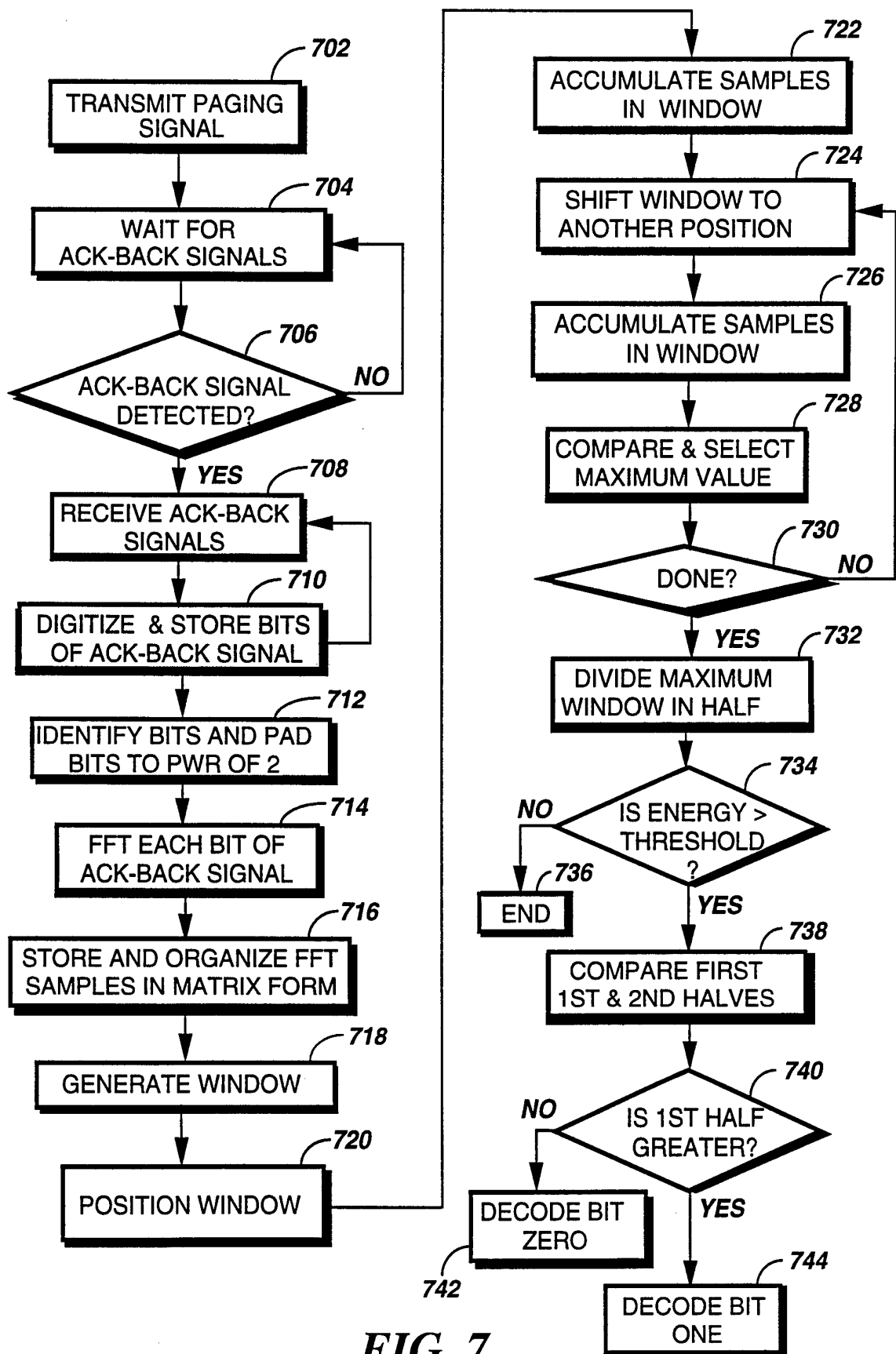
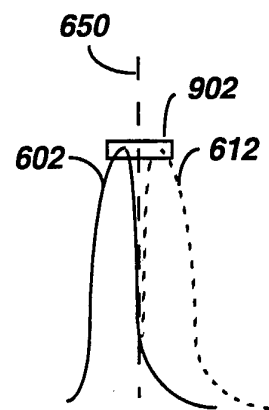
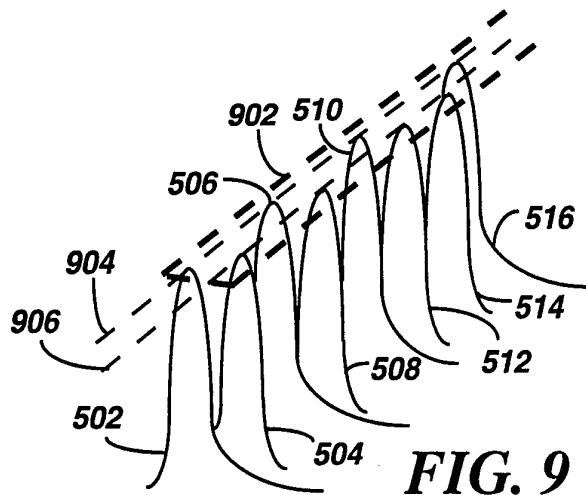
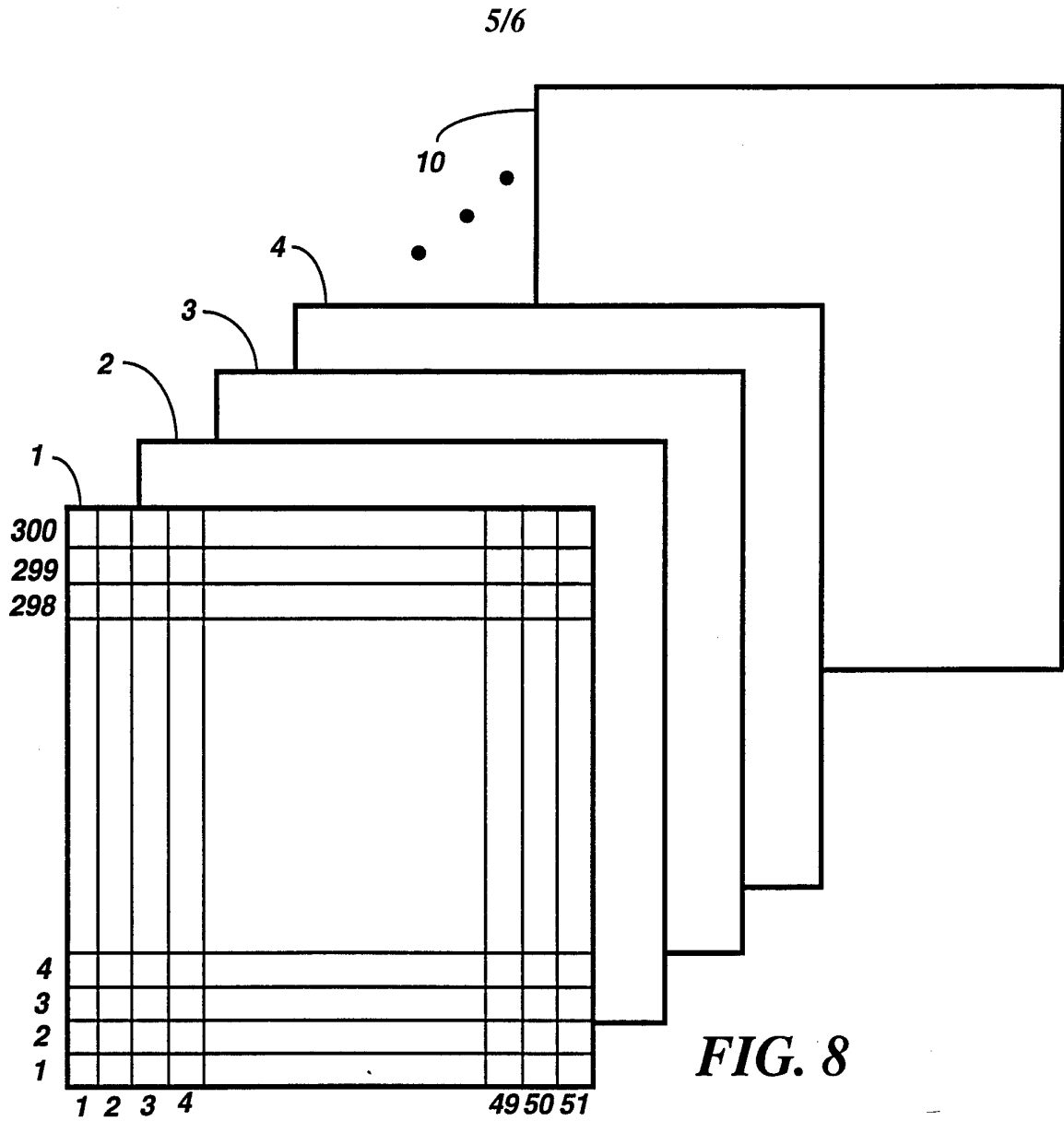
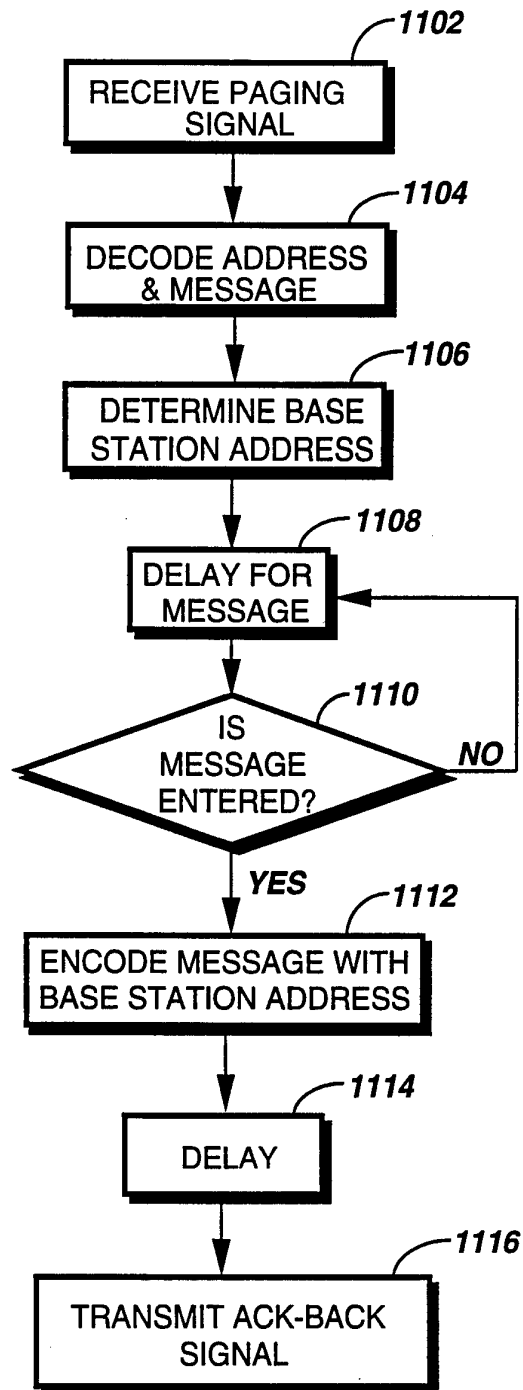


FIG. 7



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**FIG. 11**

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/09312

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) : H04B 7/00

US CL : 455/38.1

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 455/38.1, 38.2, 33.3, 54.1, 56.1; 340/825.44; 370/23, 110.3; 364/724.08, 724.09, 726, 567

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
None

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
None

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 5,260,700 (MERCHANT et al) 9 November 1993, col.1, lines 62-67.	1-25
Y	US, A, 4,245,325 (KIKUCHI et al) 13 Jananuary 1981, abstract and figures 1-18.	1-25

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:	*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	*Z* document member of the same patent family
O document referring to an oral disclosure, use, exhibition or other means	
P document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

28 SEPTEMBER 1994

Date of mailing of the international search report

DEC 06 1994

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