

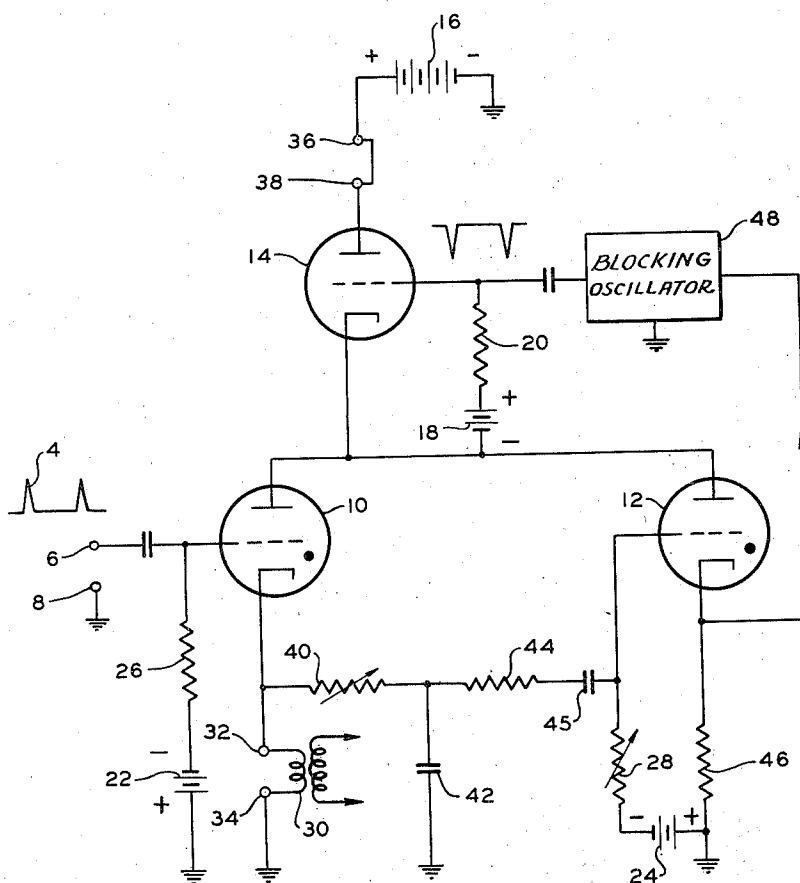
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ELECTRONIC PULSE SHAPING CIRCUIT

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ELECTRONIC PULSE SHAPING CIRCUIT

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The invention described herein may be manufactured and used by or for the Government for governmental purposes, without the payment to me of any royalty thereon.

This invention relates to electronic circuits particularly adaptable for use as pulse or sweep generators, keyers, modulators and the like.

It is a principal object of the invention to provide a circuit for the aforementioned purposes which is relatively simple and flexible and which is largely independent of the impedance of the load fed by the circuit.

For a detailed description of the invention, together with other and further objects thereof, reference is had to the following description taken in connection with the single figure of the drawing, which is a circuit diagram of one form of my invention.

In the drawing, tubes 10 and 12, which are preferably arc-discharge tubes of the Thyatron type, have their space-current paths from anode to cathode in parallel.

In series with both tubes is the space-current path of a vacuum tube 14, preferably one having high perveance and high emission. The anode of tube 14 is connected to the positive terminal of a space-current source 16, the negative terminal of which is grounded.

The grid of the tube 14 can be biased at zero potential or biased positive with respect to its cathode by means of a voltage source 18 connected between the grid and cathode through a relatively high resistance 20, so that the impedance of said tube is normally low.

Tubes 10 and 12 are normally maintained non-conducting by means of negative biases applied to their grids from voltage sources 22 and 24 through relatively high resistances 26 and 28. The load circuit 30 is connected to terminals 32 and 34 in the cathode circuit of tube 10, or it may be connected to terminals 36 and 38 in the plate circuit of tube 14 by removing the short circuit across said terminals, or load circuits can be connected at both points. Because the tube 10 is non-conducting, no current can flow through the load circuit.

The grid of tube 10 is adapted to be intermittently rendered positive by means of sharp positive pulses, such as shown at 4, from a keying source adapted to be connected to terminals 6 and 8. Each pulse is sufficient to overcome the negative grid bias on tube 10 and render said tube conducting so that plate current will flow through tubes 10 and 14 and the load circuit 30.

The potential drop across load circuit is now

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applied to the grid of tube 12 through an adjustable R-C circuit comprising resistor 40 and condenser 42. The output of this circuit is applied to the grid of tube 12 through a decoupling resistor 44 and blocking condenser 45. After a time interval, depending upon the time constant of R-C circuit 40-42, said grid will be rendered sufficiently positive to overcome the negative bias from source 24 and render tube 12 conducting, whereby a pulse of voltage will be developed across resistor 43 in the cathode circuit of tube 12.

The voltage pulse across resistor 46 is now applied to a negative pulse generator 48 which will deliver a sharp pulse of negative voltage to the grid of tube 14, thereby biasing it to cutoff and rendering it non-conducting, whereby the plate current through tubes 10 and 12 and their load circuits will be interrupted and the voltage at their anodes reduced sufficiently to render them non-conducting. This cycle of operation is repeated at every positive pulse applied to the grid of tube 10.

Negative pulse generator 48 may take the form of a conventional blocking oscillator which is started by a positive pulse and which blocks itself after the first voltage cycle generated thereby. One example of such blocking oscillator is described in Bedford Patent 2,358,297, issued September 19, 1944. In general, circuit 48 acts to amplify and invert the pulse applied thereto from resistor 46, and any circuit which will perform this function can be used.

It will be seen that the character and duration of the pulses through load circuit 30 will depend upon several factors. One factor is the time constant of the R-C circuit which can be adjusted to any desired interval by adjusting the value of resistor 40. Other factors are the ionizing time of tube 12 and the starting time in pulse generator 48 and the pulse duration of the output thereof. If the total time delay due to all the above factors is greater than the duration of input pulses 4 and less than the intervals therebetween, then there will occur a single pulse through the load circuit for each input pulse 4. If the total time delay is greater than the interval between input pulses, then there will be one pulse in output circuit 30 for every two or more input pulses, in which case the network will act as a frequency divider. On the other hand, if said time delay is less than the duration of each pulse 4, then there will be two or more pulses in output circuit 30 for each pulse in the input. The latter feature makes it possible to generate groups of output pulses for each pulse at the input, the num-

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ber in each group depending upon the duration of the input pulses and the time delay factors above mentioned.

A particular feature of the circuit is the fact that the operation is largely independent of the impedance of the load 30, since the impedance of tubes 10 and 14 when they are conducting is relatively small compared to the load impedance. Hence the voltage drop across said load and the time operation of the succeeding circuits is substantially independent of the load impedance.

The pulse shape across load 30 will be substantially rectangular if said load is resistive. Other pulse shapes can be derived by making said load circuit reactive or a combination of reactance and resistance. By making load circuit 30 a constant charging circuit, the output wave will be a sawtooth wave, the duration of which can be controlled by adjusting the time constant of R-C circuit 40-42.

Other uses and features will be obvious to those skilled in the art, and it is aimed in the appended claims to cover all changes and modifications as fall within the true spirit and scope of the invention.

I claim:

1. An electronic circuit comprising at least first, second and third grid-controlled electron tubes, said first and second tubes having their space-current paths connected in parallel and connected to a source of space-current in series with the space-current path of said third tube, an impedance in the cathode circuit of said second tube, said first and second tubes being normally non-conducting arc-discharge tubes, means to render said first tube conducting, whereby space-current will flow through said first and third tubes, an adjustable time delay circuit for transmitting the output of said first tube to the grid of said second tube and render it conducting whereby space-current will flow through said impedance, and means responsive to current flow in said impedance to render said third tube non-conducting thereby interrupting the space-current flow through all of said tubes.

2. An electronic circuit comprising at least first, second and third grid-controlled electron tubes, said first and second tubes having their space-current paths connected in parallel and connected to a source of space-current in series with the space-current path of said third tube, a load circuit connected in the cathode circuit of said first tube, a resistor in the cathode circuit of said second tube, said first and said second tubes being arc-discharge tubes having their grids negatively biased to cutoff, said third tube being a high perveance vacuum tube having its grid positively biased so that it is normally of low impedance, means to apply a sharp positive pulse to the grid of said first tube to render it conducting whereby space-current will flow through said load circuit, an adjustable resistance-capacity time-constant circuit for transmitting the voltage drop across said load circuit to the grid of said second tube and render it conducting whereby space-current will flow through said resistor, a blocking oscillator circuit coupled to the output of said resistor for generating a sharp negative pulse for each pulse of voltage across said resistor, and means for applying said negative pulse to the grid of said third tube to render it non-conducting thereby interrupting the space-current flow through all of said tubes.

3. An electronic circuit comprising at least first, second and third electron tubes, said first

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and second tubes having their space-current paths connected in parallel and connected to a source of space-current in series with the space-current path of said third tube, an impedance in the cathode circuit of said second tube, said first and second tubes being normally biased to render them non-conducting, means to render said first tube conducting, whereby space-current will flow through said first and third tubes, means including a time delay circuit responsive to the output of said first tube to render said second tube conducting whereby space-current will flow through said impedance, and means responsive to current flow in said impedance to render said third tube non-conducting thereby interrupting the space-current flow through all of said tubes.

4. An electronic circuit comprising at least first, second and third electron tubes, said first and second tubes having their space-current paths connected in parallel and connected to a source of space-current in series with the space-current path of said third tube, an impedance in series with the space-current path of said second tube, said first and second tubes being normally non-conducting arc-discharge tubes, means to render said first tube conducting, whereby space-current will flow through said first and third tubes, means including a time delay circuit responsive to the output of said first tube to render said second tube conducting whereby space-current will flow through said impedance, and means responsive to current flow in said impedance to render said third tube non-conducting thereby interrupting the space-current flow through all of said tubes.

5. An electronic circuit comprising at least first, second and third electron tubes, said first and second tubes having their space-current paths connected in parallel and connected to a source of space-current in series with the space-current path of said third tube, an impedance in the cathode circuit of said second tube, said first and second tubes being normally non-conducting arc-discharge tubes, means to render said first tube conducting, whereby space-current will flow through said first and third tubes, means including a time delay circuit responsive to the output of said first tube to render said second tube conducting whereby space-current will flow through said impedance, and means responsive to current flow in said impedance to render said third tube non-conducting thereby interrupting the space-current flow through all of said tubes.

6. An electronic circuit comprising at least first, second and third electron tubes, said first and second tubes having their space-current paths connected in parallel and connected to a source of space-current in series with the space-current path of said third tube, a load circuit connected in series with the space-current paths of said first and third tubes, an impedance in the output circuit of said second tube, said first and said second tubes being arc-discharge tubes normally at cutoff, said third tube being biased to render it normally of low impedance, means to render said first tube conducting whereby space-current will flow through said first and third tubes and said load circuit, a time delay circuit responsive to said space-current flow to render said second tube conducting whereby space-current will flow through said impedance, means coupled to the output of said impedance for generating a sharp pulse for each change of voltage across said impedance, and means for applying said sharp pulse to said third tube to render it

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non-conducting thereby interrupting the space-current flow through all of said tubes.

7. An electronic circuit comprising at least first, second and third electron tubes, said first and second tubes having their space-current paths connected in parallel and connected to a source of space-current in series with the space-current path of said third tube, a load circuit connected to said first tube, a resistor in the cathode circuit of said second tube, said first and said second tubes being arc-discharge tubes normally at cutoff, said third tube being a vacuum tube biased so that it is normally of low impedance, means to apply a pulse to said first tube to render it conducting whereby space-current will flow through said load circuit, a time delay circuit for transmitting the voltage drop across said load circuit to said second tube to render it conducting whereby space-current will flow through said resistor, a pulse generator keyed by the output of said resistor for generating a sharp pulse for each change of voltage across said resistor, and means for applying said sharp pulse to said third tube to render it non-conducting thereby interrupting the space-current flow through all of said tubes.

8. An electronic network comprising at least first, second and third grid-controlled electron tubes, said first and second tubes having their space-current paths connected in parallel and connected to a source of space-current in series with the space-current path of said third tube, a load circuit connected in the cathode circuit of said first tube, a resistor in the cathode circuit of said second tube, said first and said second tubes having their grids negatively biased to cut-

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off, said third tube having its grid positively biased so that it is normally of low impedance, means to apply spaced pulses to the grid of said first tube to render it conducting whereby space-current will flow through said load circuit, a time delay circuit for transmitting the voltage drop across said load circuit to the grid of said second tube to render it conducting whereby space-current will flow through said resistor, a pulse-forming circuit coupled across said resistor for generating a sharp pulse for each pulse of voltage across said resistor, and means for applying said sharp pulse to the grid of said third tube to render it non-conducting thereby interrupting the space-current flow through all of said tubes.

9. The invention set forth in claim 8, wherein the total time delay of said electronic network is greater than the interval between said spaced pulses.

10. The invention set forth in claim 8, wherein the total time delay of said electronic network is greater than the duration of said spaced pulses but less than the intervals therebetween.

11. The invention set forth in claim 8, wherein the total time delay of said electronic network is less than the duration of said spaced pulses.

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