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(71) 가 가 가 1006
가 가 가

(72) 가 가 가 4-17-15

7-1-548

15-5

(74)

:

(54)

1 () RAM ,

(7) (8)가 (MC
...) (7) (8) ((BL0, NBL0)
~(BLn, NBLn) , (8) ((BL
0~BLn), (NBL0~NBLn)) , 1 (SLD)

1

(trapping line), (trapping region)

1	(a)	1	RAM	, (b)
2		1	RAM	
3	2	-		
4	2	-		
5	2	-		
6	2	-		
7		1	RAM	
8		1	RAM	
9		RAM		
10		2	RAM	
11		2	RAM	
12		RAM		
13		3	RAM	
14		1	RAM	
15		RAM		
16		RAM		

* * *

MATA : 1 MATB : 2

MC : BL0~BLn, NBL0~NBLn :

ex : WLOA~WLnA, WLOB~WLnB :

SA0~SAn : SLD, SLDM1 : 1

SLDM2 : 2 P :

PLT : N :

Q1 : (MOS) Q2 : MOS

PLTMT2 : WLMT :

MBL0~MBL3 : SLDM3 : 3

VSSL : Nwell :

BP :

PLTMT, VCP2 : (4)

PLTMT2 : 5 ()

JT : OD :

in : NSA0, NSA1 : N

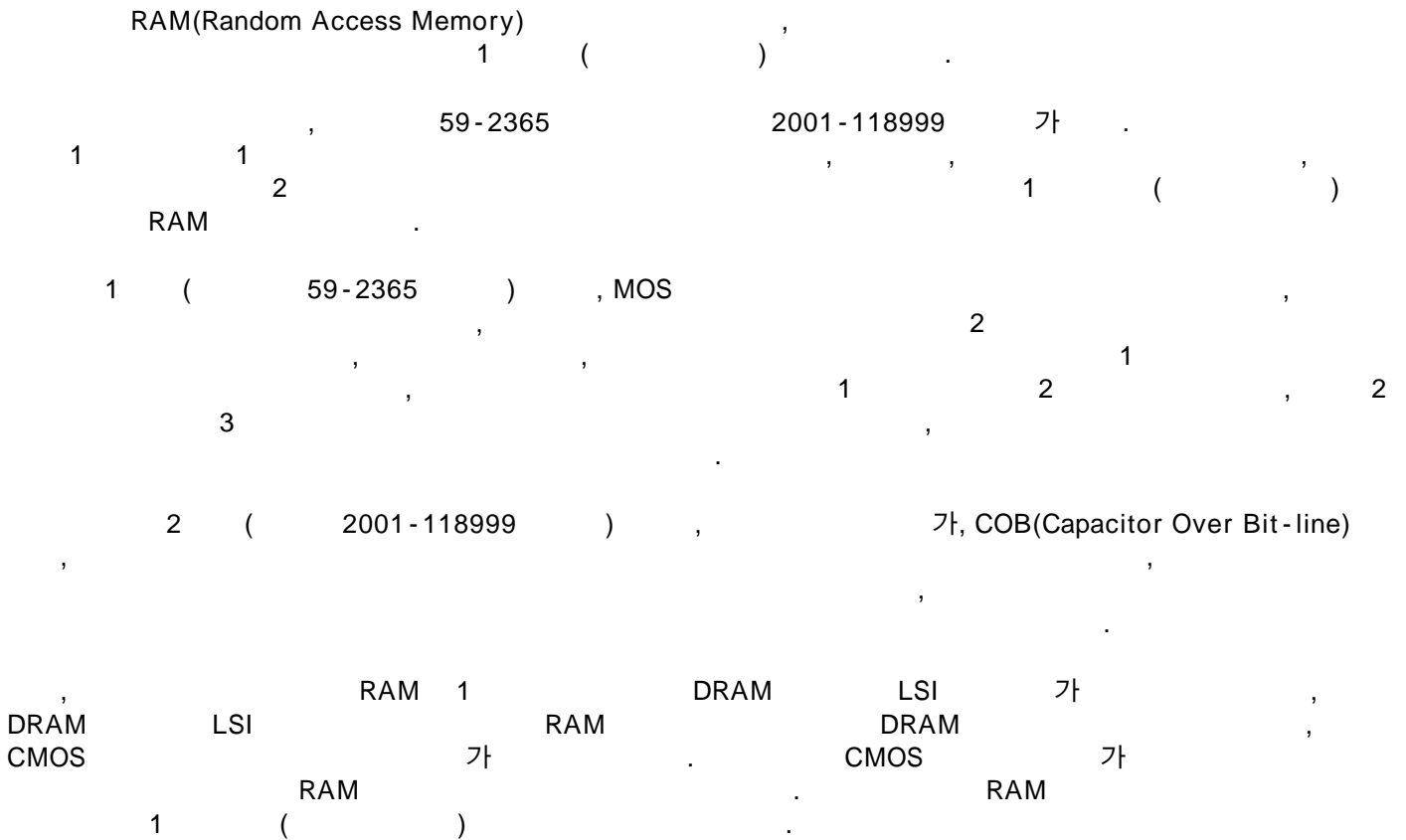
PSA0, PSA1 : P

SG0, SG1 : G1, G2 :

4 : 5 :

6 : 7 :

8 : 10 :



1 1 2 1 2 1 MOS 1 2
 , 1 2
 , 2 가 가
 , 2 가 가
 1 MOS 1 2
 1 2 1 2
 2 가 2
 N , 2 , 2 , P
 N , 2 (P) 가 2 가 , 2 , N
 P
 , P N 2
 2
 가

()

(1)

14 1
 14 , 10 RAM (10) , 1
 , 3 , 2 (10) (1)
 2 , 5 (3) , 4
 (5) , (10) 16 (6)
 (6) (8) , 2 (10) 2 (7) , (8) (8)
 (9) (7) , CMOS

RAM , (7) 1 () .

(5) , (6) () (6)

(6) (2) , (4)

가 . 가 .

1 (8) , 32 , 1 , 1

32 . 1 (8) 32 , 1 32 , 1

32 x 32 = 1024 (6) , 64 (8)가 , (5) 2

(6)가 16 1024 x 64 x 16 = 1M가 . (5) 2

1M x 2 = 2M .

1 (a) , 14 2 (8) (7)

1 (a) MATA (7) , MATB , WL
 0A~WLnA WLOB~WLnB , BL0~BLn NBL0~NBLn , 1 (BL0
 , NBL0)~(BLn, NBLn) . MC 1 1
 , SA0~SAn CMOS PLT (MC) (MC)

(MC) 가 , 1 (WLOA) (MC) , (MC)
 (MC)) (MC) (a) (WL1A)
 (7) (SA0~SAn) . WLDA WLDB

1 (a) , SLD (MATA, MATB) , (BL0~BLn) ,
 (NBL0~NBLn) 1 (SLD) , 1 (SL
 (VDD)가 (BL0~BLn, NBL0~NBLn) 1 . Cbs (BL0~BLn, NBL0~NBL

D) n) 1 (SLD) .

1 (SLD) (MATA) (BL0~BLn) , (MATB)
 (NBL0~NBLn) , (VDD) . (SLD) ,
 (MC) (SA0~SAn) , 1

(MC) , Q2 가 P 1 (b) , Q1 P MOS
 , Q1, Q2) N MOS MOS (Q1) (Q2)
 (Q1) MOS (BL) (Q1) , (Q1) (WL)
 MOS (Q2) (N) , MOS (Q2) (P)

(PLT) .

2 (MATA) , (trapping re
 gion)(JT) 2 (MATA) , BL0~BL7 1
 , SAsect0 SAsect1 , WL , WLMT 2
 , PLT (MC) (MC) , 1 (WL)
 (MC) (MC)

PLTMT 2 , SLDM1 1 , 1

(BL0~BL7) . SLDM2 2 2
 1 (SLDM1) (WL) 1 (SLDM1) (SLDM2) (WLMT)
 (VIA1)(VDD)가 2 (SLDM2) (VDD) (WL) (WLMT)
 1 (SLDM1) . JT (PLT) (PLTMT)
 VIA1 1 2 x
 CW 1
 1 (SLDM1) (BL0~BL7) (MATA) (MATA)
 2 (SLDM2) (WLMT) (CW) (WLMT)
 3 2 (MATA) - 4 (JT) -
 WL 3 (MC) (PLT) 2 (WL) 1 (SLDM1) 2 (n+)
 1 (SLDM1) 2 (SLDM2) 1 (SLDM1) (n+)
 (VIA1) (VDD) 1 (SLDM1)
 (CW) (NWELL) (8) (PLT)
 2 (4) (PLTMT) (WLMT) (PLTMT) (P)
 LTMT) (WLMT) (PLTMT) (S)
 LDM2) 3 (WLMT) (4) (PLTMT)
 2 (WLMT)
 2 (WLMT, WLMT) 4 (WLMT) 2 (WLMT, WLMT) (PLTMT) (W)
 2 (WLMT, WLMT) (SLDM2) 가 2 (PLTMT) (W)
 (WLMT) 2 (SLDM2) 2 (PLTMT) (WLMT) 2 (WLMT) 1
 4 (JT) (PLT) (PLTMT) (VIA1) (CW)
 (WLMT) (WLMT) (VIA1)
 1 (CW) (WL) (PLT)
 5 2 (PLT) V-V 6 2 (SLDM2) -
 5 1 (PLMT) (BL) 1 (SLDM1)
 (JT) 2 (VIA1) (CW) (PLMT) (PLTMT)
 (PLT)
 6 1 (BL) 1 (SLDM1) (SLDM1)
 2 2 (SLDM2) 1 (SLDM1) (VIA1)
 1 (SLDM1) 3~ 6
 2, 3 6 (VDD) 1 (SLDM1) 2 (SLDM1) (SLDM2)
 1 (VDD) 1 (SLDM1) 1 (SLDM1) (BL)
 2 3 1 (SLDM1) (VDD) (NWELL)
 1 (SLDM1)

(WL) (PLT) (PLT) (WL) (MATA)
 (PLT) (PLT) (PLT) 2 (SLDM2) (PLTMT)) ,
 (JT) (PLT) (VIA1, CW) (PLTMT) (PLT) (PLT)
 가가 . (PLT) (PLT)
 4 (SLDM2) , 2 (WLMT) (WL) (PLTMT) 2
 1 (b) () MOS
 가 . 가 , CMOS
 가가 . 가 가 .
 (WL) (PLT)
 (BL) 1 (SLDM1) 1 (SLDM1)
 (BL) 1 (SLDM1)
 7 RAM
 7 , BL0~BL5 NBL0~NBL5 1 (BL0~BL5, NBL0~
 (BL0, NBL0)~(BL5, NBL5) . MBL0~MBL3 (BL0~BL5, NBL0~
 NBL5) (6) () , 3
 (6)
 SLDM1 , (BL0~BL5) (NBL0~NBL5) 1
 , 1 (8) . SLDM2 1 (SLDM1) 2 , 2
 VIA1)() 1 (SLDM1) 1 (SLDM1) (SLDM2) ()
 , (VDD)가 (JT) 2 (VIA1)
 (6)
 SLDM3 3 , 3 (MBL0~MBL3) ()
) 2 (SLDM2) 2 (SLDM2) (VIA2)(
 × (7 MBL2 MBL3) 1 , 3 (SLDM3) , 2
 , (6) 7 가 (8) (7) , 14
 (4) (VBP, VCP, VDD, VSS)
 (VDD) (7) , 3 (SLDM3) (VIA3)()
 (4) (VDD)
 1 (7) (SA0~SA_n) , 2 (SLDM2)
 (VSS) (SLDM1) (SA0~SA_n) , 3 (SLDM3) () 1 (SLD
 M1)
 1 (SLDM1) ((VDD)) 2 3 (SLDM2, SLDM3)
 3 , 1 2 1 2 가 (SLDM1, SLDM2)
 , (VDD) , (7) (6) (VDD) 1

(SLDM1) , (6) 가 , 가

7 (P) , PLTMT (VCP) (4) , 1 (b)
 (MBL0~MBL3) (8) 2

7 PLTMT2 (VCP) (5) (PLTMT)
 (3) (PLTMT2) (JT) (7)
 (5) (8) (PLTMT) (VIA2)
 (x)

5 (PLTMT2) , 2 (7 MBL3 , 1) (JT)
) 1 (8) 1 (PLTMT) 5 1 (PLTMT2)
 (4) (MATA, MATB) (PLT) (VCP) (4)
 , 5 (PLTMT2) , (8) (VCP) (PLTMT) (2)
 VCP) (PLTMT) (4) (PLT) (VCP) (PLTMT) (2)
 , (JT) (PLT) (VCP)

5 (PLTMT2) , (7) (8) (PLT) (8)
 (4) (PLTMT) (PLT) , (8)
 (8) (8) (PLT) (PLT) (8)
 (PLT) (8) (PLT) (PLT) (8)

7 , BP , VSSL , (BP, VSSL)
 (MBL0~MBL3) , (3) (8)
 (BP, VSSL) , 2 (JT, JT) 1 (8) (7)
 , 2 (BP) (VSSL) , (4) (VCP)
 (4) (VSS)

RAM 가 RAM , , RAM
 (8) () (8) (JT) RAM
 RAM (WLMT) , RAM

()

8 RAM (MC)

8 , WL , BL , PLT , SLDM1 (BL, BL)
 1 (BL) 1 , 1 MOS . SLDM2 2 (Q1) , 1
 . MC 1 (b) , 1 MOS (MC) (Q1) , 1
 MOS (Q2) 4 , 2 8 1

8 , OD (MC) (OD) (WL) (Q1) . VIA1 1 (SLDM1) (PLT) MOS (Q2) (MC) (MC) 2 (SLDM2) (WL) (MC) 1 (MC) 8 (MC) MOS (Q2) 가 (MC) (MC) (in) (PLT) (PLT) MOS (Q2) (PLT) (WL) (Q1) (Q1) (BL) 가 (BL) (Q1) (ex) (ex) (ex) (CW) (ex) (Q1) (SLDM1) (BL) (BL) (ex) (Q1) (CW) (ex) (Q1) (SLDM1) (BL) (ex) (Q1) (MC)(R0) (MC)(M0) (MC)(R0) (MC)(M180) (MC)(R0) (MC)(R180) (MC)(R0) (MC)(R0), MC(M0), MC(M180), MC(R180) (MC) 가 (WL) 4 4 (MC) MOS (Q2) RAM 가 가 (2) 2 RAM (BL0) (NBL0) , 9 , 9 , BL0, BL1, NBL0, NBL1 (BL1) (NBL1) (1) (8) NSA0, NSA1, PSA0, PSA1 (CMOS) (BL0, BL1) (NBL0, NBL1) , 1 () (PSA0) (BL0, NBL0) N (NSA0) P (NSA1) P (PSA1) (BL1, NBL1) N ((BL0, NBL0) , (BL1, NBL1)) 가 . 9 , 2 가 2 , 2 1 , 2 가 가 2 2 가 가 10 (BL0, BL1, NBL0, NBL1) , () 1 , 10 1 2 (10 1

) (NBL0) 10 (10 0) (BL0)
 , 10 (10 0) (NBL1)
 10 (10 1) (BL1)
 . , 2 ((BL0, NBL0), (BL1, NBL1))
 .

) P , 1 (BL0, NBL0) N (NSA0)
 (NSA1) P (PSA0) , 1 (BL1, NBL1) N
 . P 2 (PSA1)가, 2 (NSA0, NSA1) 가 1
 , P (PSA0, PSA1) 1 . 10 x
 1 2 .

2 CMOS 4 (NSA0, PSA0, NSA1, PSA1)
 , , 가가 . 2 4

1) , 2 CMOS N (NSA0, NSA1) P (PSA0, PSA
 , 1 , N P

11 , 10 가 .

11 , MBL0, MBL1 (8) 3 (BL0,
 NBL0, BL1, NBL1) , 2 1
 11 (11 1) (NBL0) 11 (11 0)
 (11 1) (BL1) 11 (11 0)
 (NBL1)

11 , SG0 (BL0, NBL0) (MBL0, MBL1) , SG1
 (BL1, NBL1) (MBL0, MBL1) (SG0) ,
 (BL0, BL1) , (SG1) , (SG0, SG1)
 (NBL0, NBL1) . 2
 , 2 (MBL0, MBL1)

G0, SG1) (SG0, SG1) , (MBL0, MBL1) , (S
 (BL0, BL1, NBL0, NBL1) 2 , 2 (SG0, SG1)

1) (BL0, BL1) (SG1)가 1 (NBL0, NBL
 (BL1, NBL1)) (SG0, SG1) , ((BL0, NBL0),
 , , 가가

(3)

3 13 .

12 , OD 12 , Q1 Q2 , BL NBL

, S (Q1) (Q2) (Q1, Q2) (NBL) (BL) (Q1) (Q2) (OD) (OD)

(Q1, Q2) (S) (G1, G2) (L1) (L1)

가 (Q1, Q2) 가 (Q1, Q2) (Q1, Q2) mV (Q1, Q2)

13 (G2) 12 (Q1, Q2) (OD) 13 (G1) (L2) (L1) (L2 > L1) (OD) (OD) (L2 > 2 · L1)

(Q1, Q2) (S) (OD) (OD)

(L2)가 (Q1, Q2) 가 (OD) (OD)

1 가

가

2

MOS 가

2

(²) (²) (²)

N P P N

(57)

1.

1 MOS

1

1

2.

1

1 2

1 2

1 2

1

2

1

2

1

3.

1

가 MOS

1

4.

3

1 1

5.

1

1

6.

5 ,
1 ,

7.
5 ,
1 ,

8.
1 ,
1 2 가 ,
1 2 ,
1 2

9.
8 ,
1 가 ,
2 ,

10.
8 ,
2 , 2 1 , 2

11.
8 ,
1 ,
2 , 3 ,
2 , 3 3

12.
1 MOS ,
가 ,

가

13.

,
,
.
,
1
1, 1 MOS
1 가

14.

13 ,
.

15.

13 ,
1 가 ,

16.

13 ,
.

17.

13 ,
1 가 ,

18.

13 ,

가 ,

19.

13

1 2

1 2

1

2

1

1

2

1

가

2

2

20.

1

MOS

1 2

가

1

1 2

가

1

2

1 2

2

1 2

21.

20

1

가

2

1

1

1

22.

, 1 MOS 1

가 MOS

가

23.

22

2 , 4 8

4

4

4

4

24.

1 2 1 MOS 1

1 2

1

2

1 2

25.

24

2

26.

1 2 1 MOS 1

1 2

1

2

2

2

2

가

27.

26

1

2

1

2

28.

26

2

2

N

, P

29.

27

2

2

가 1

30.

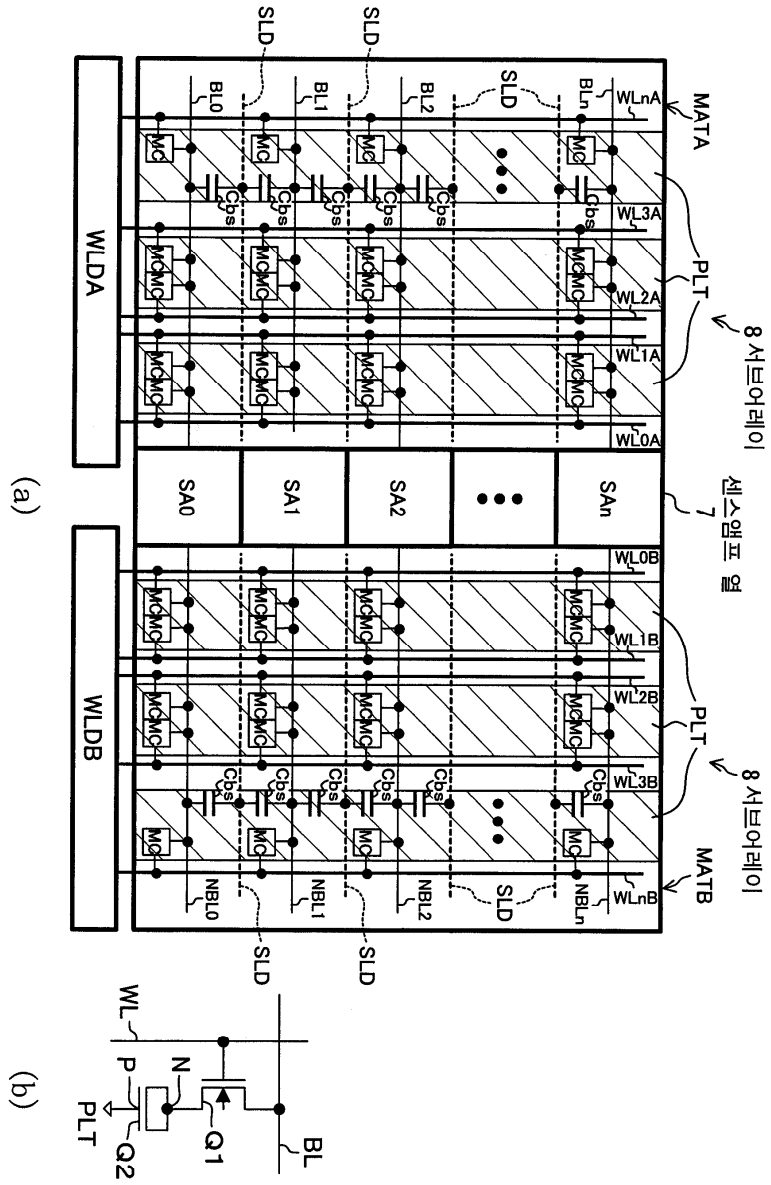
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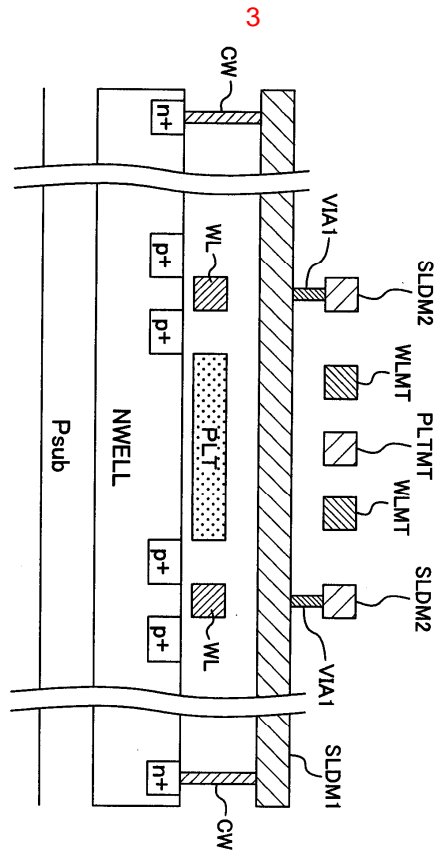
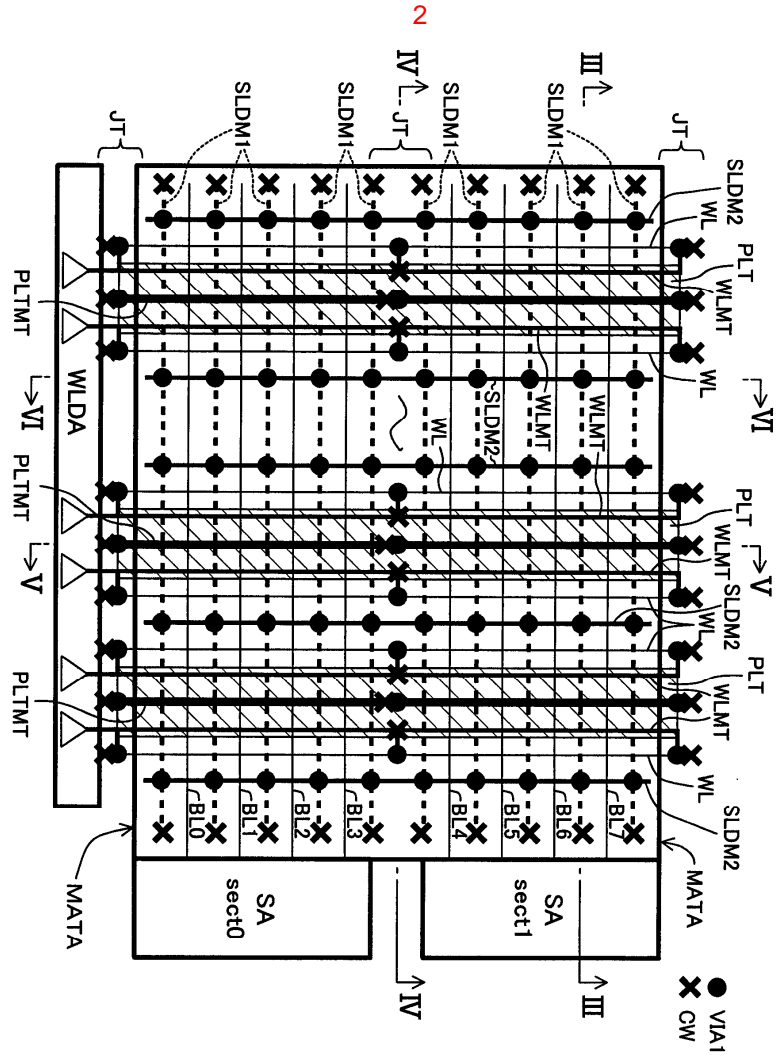
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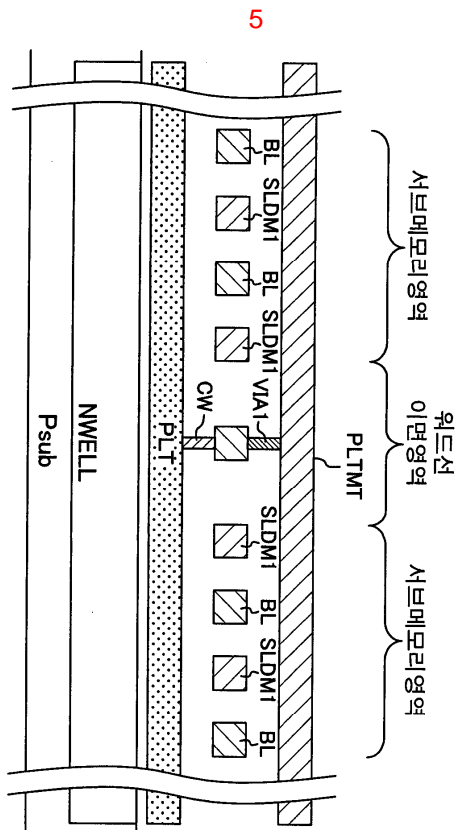
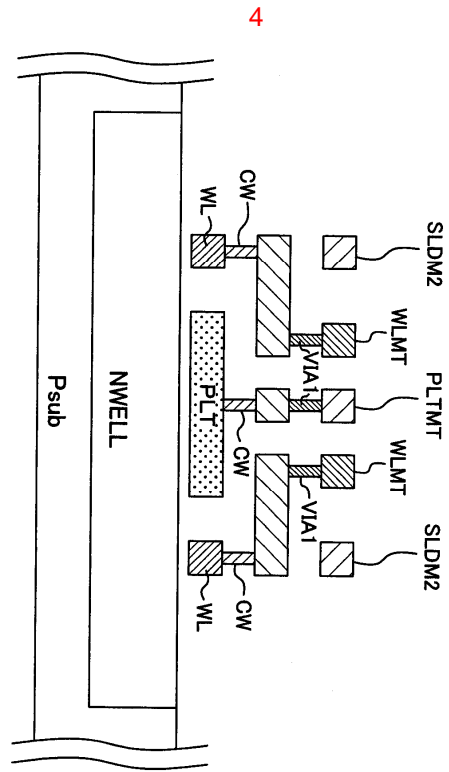
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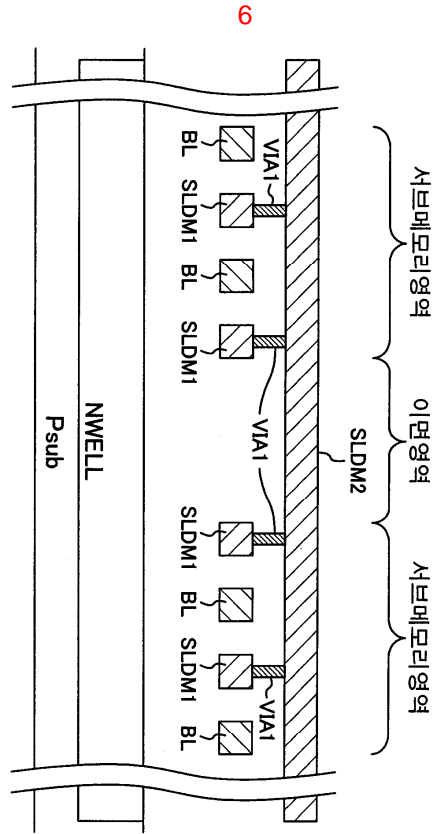
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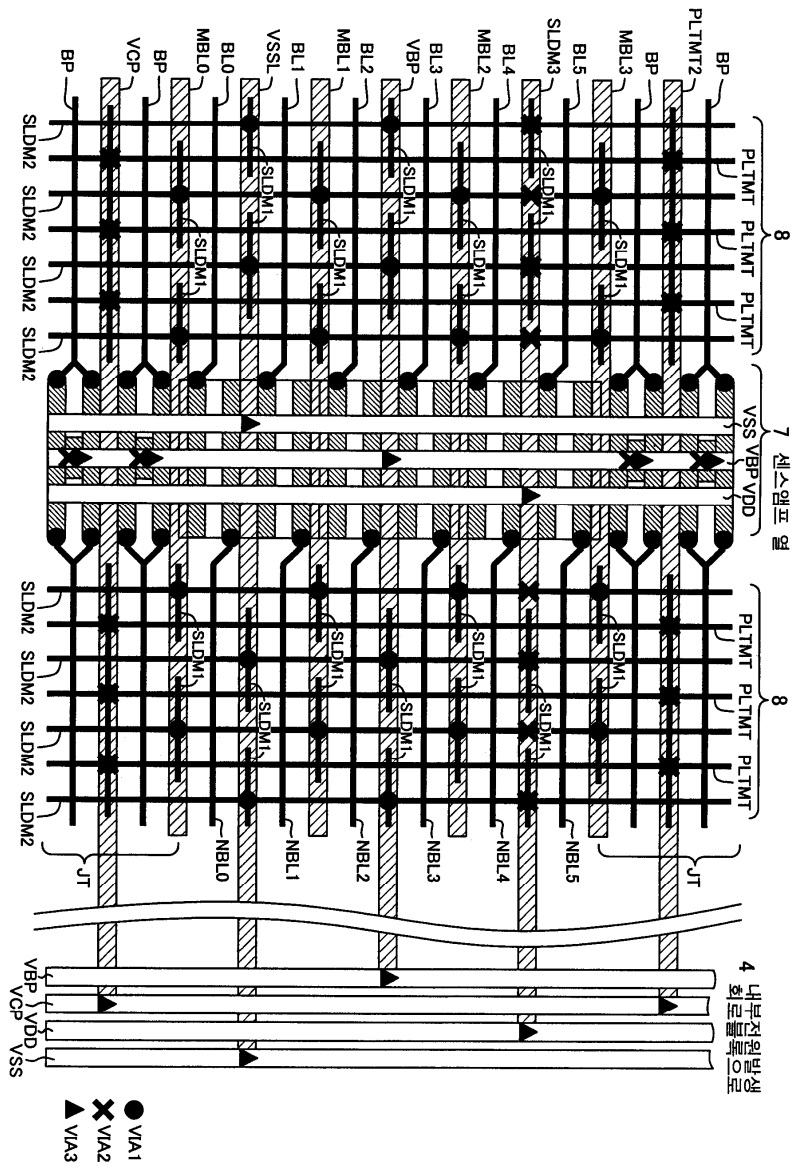


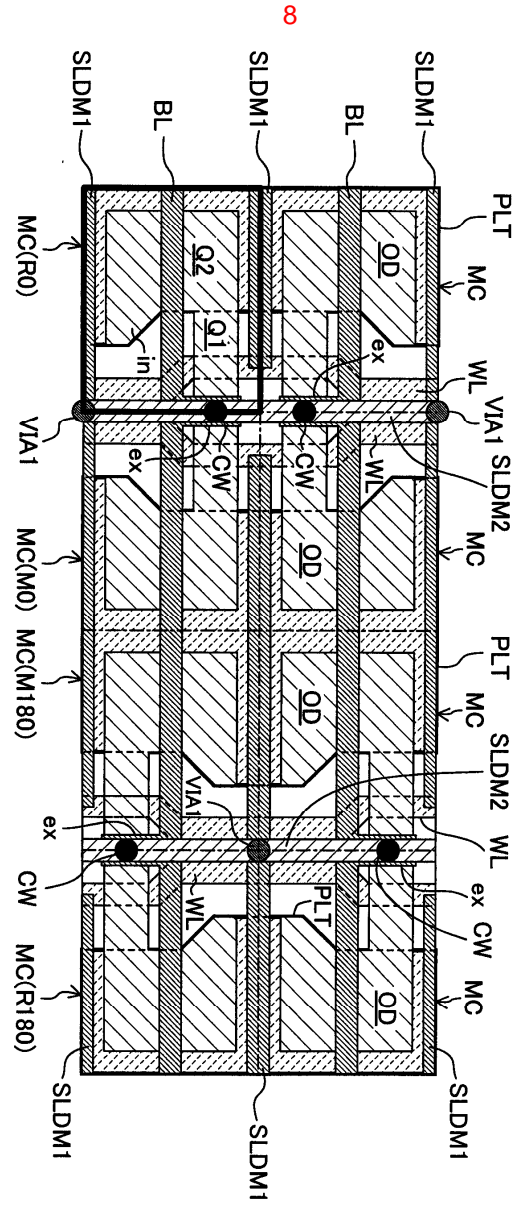


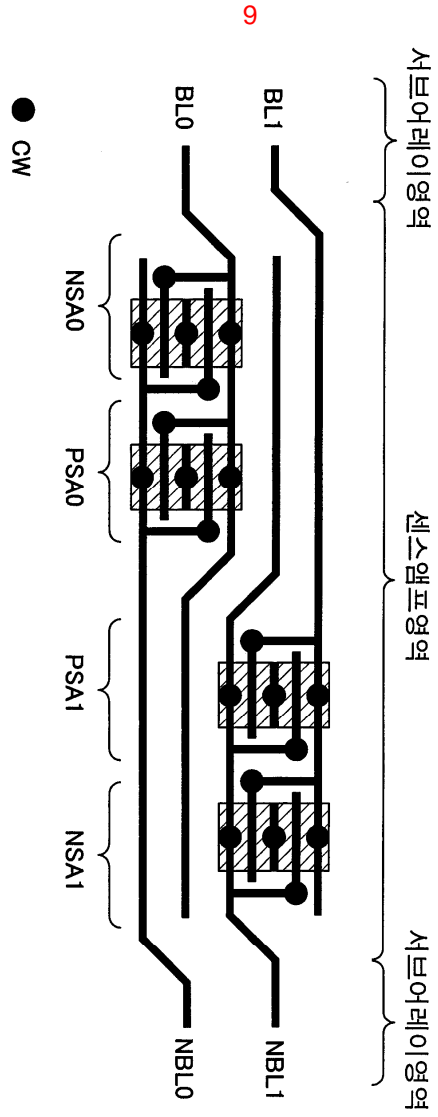


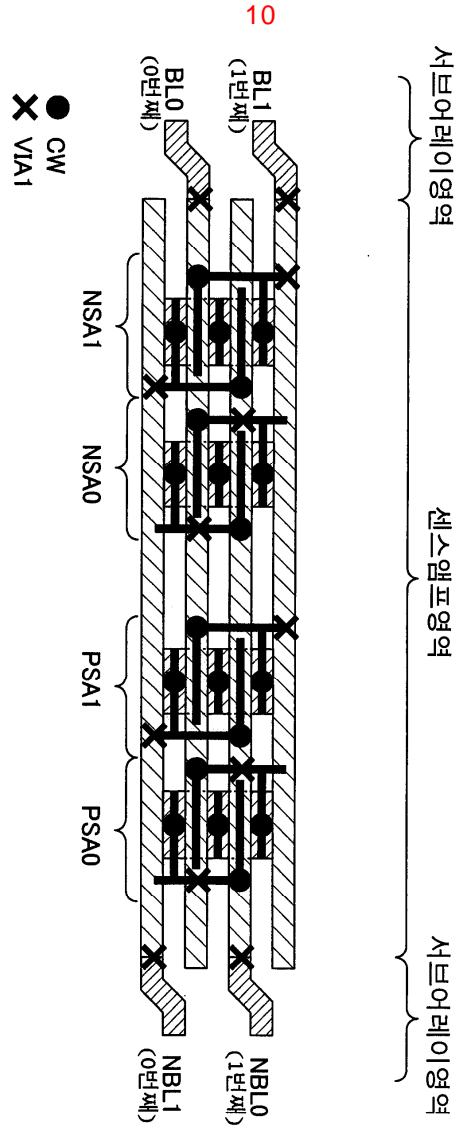


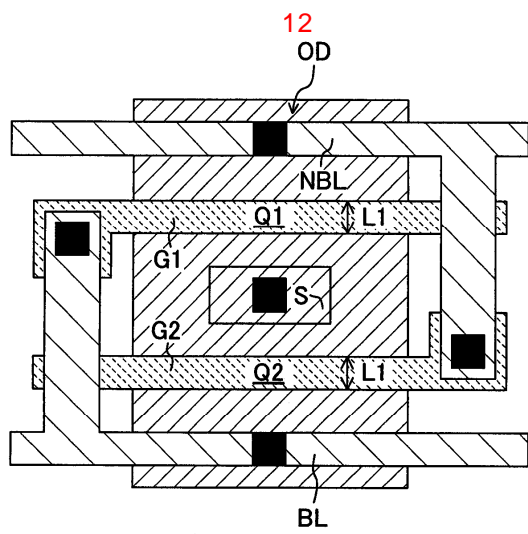
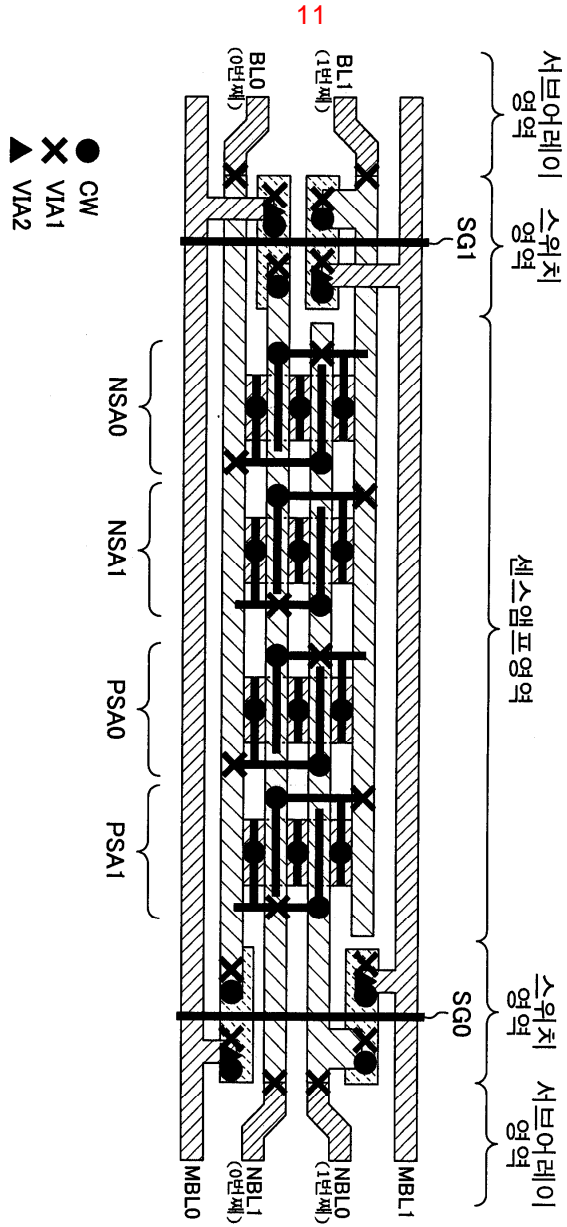
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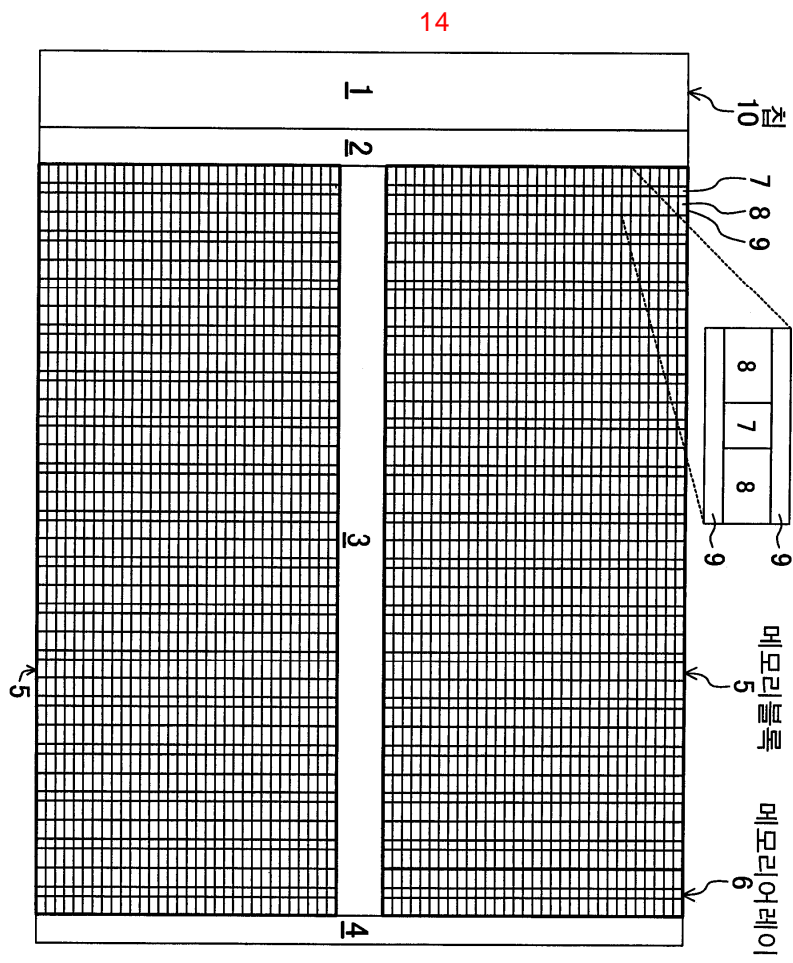
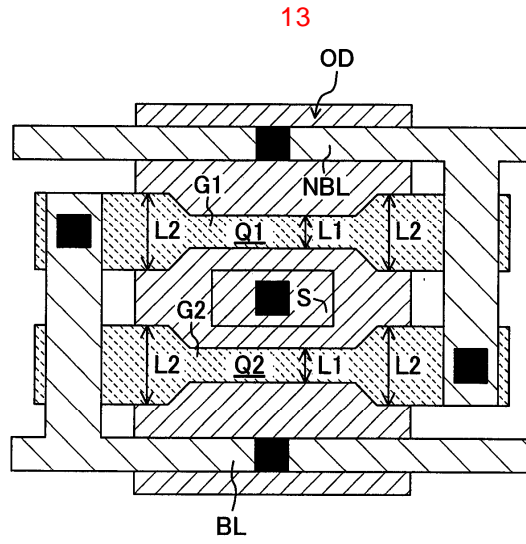




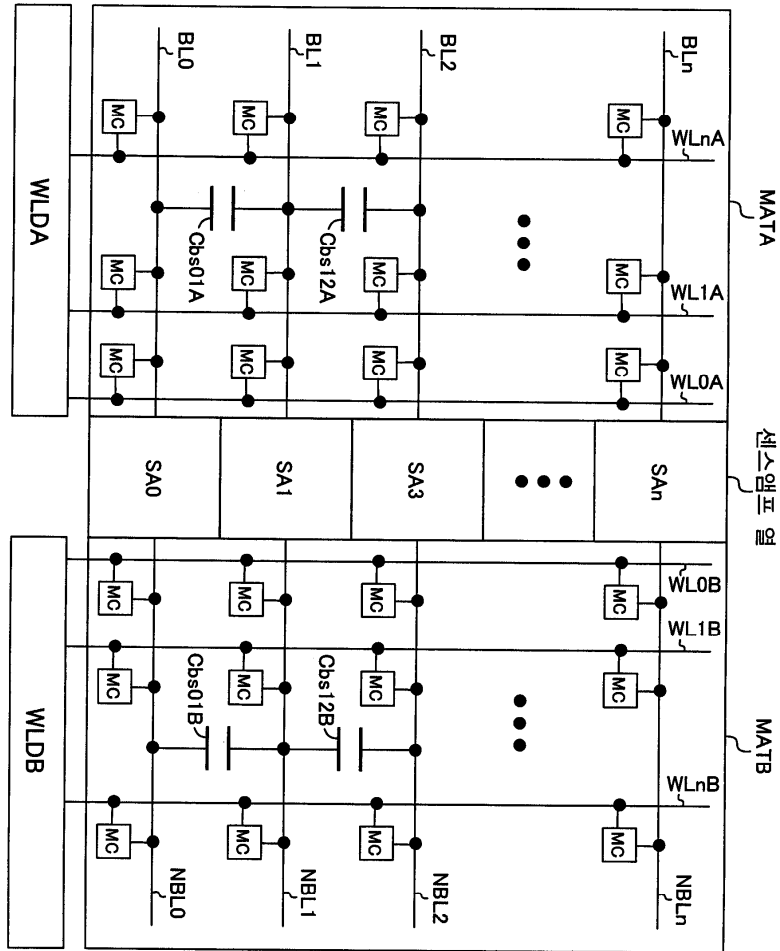








15



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