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FAIL-SAFE TIME DELAY RELAY

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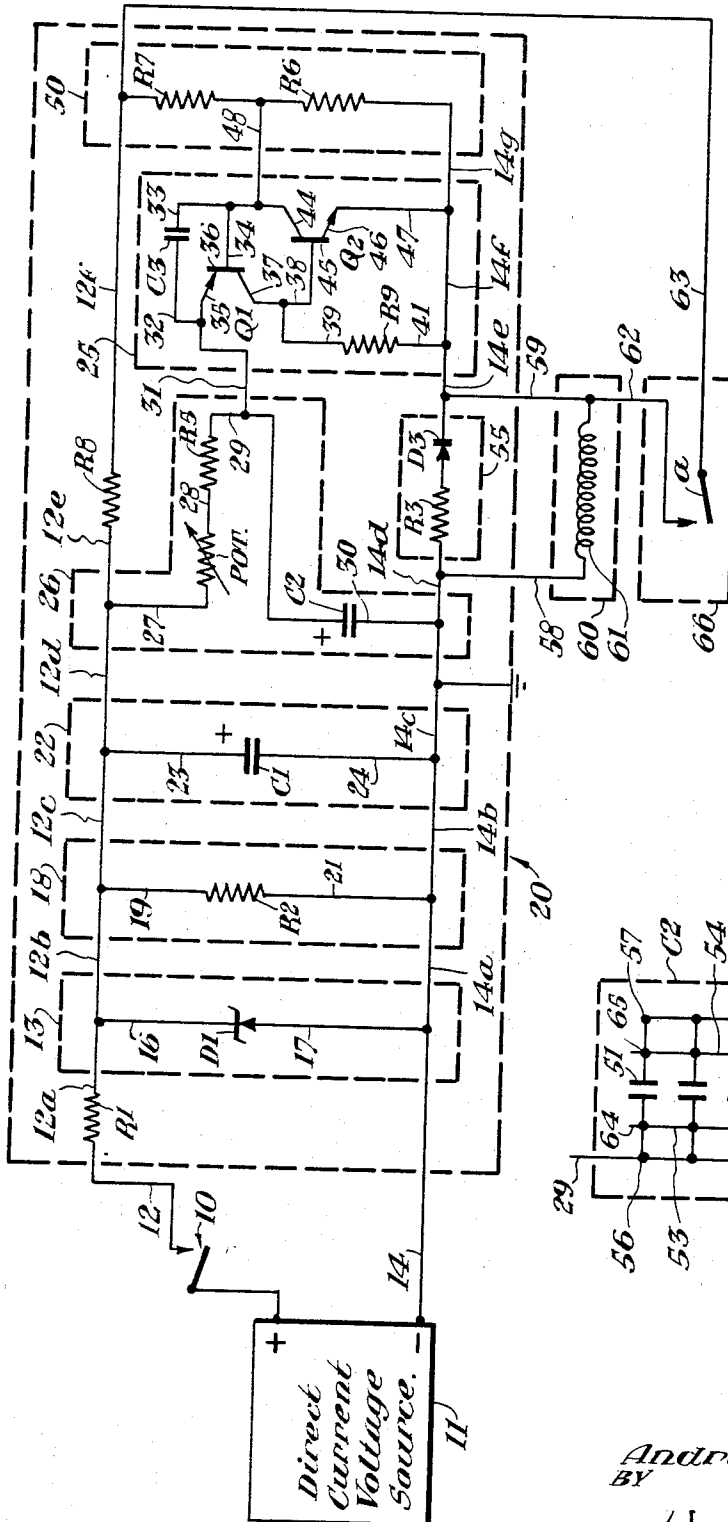


Fig. 1.

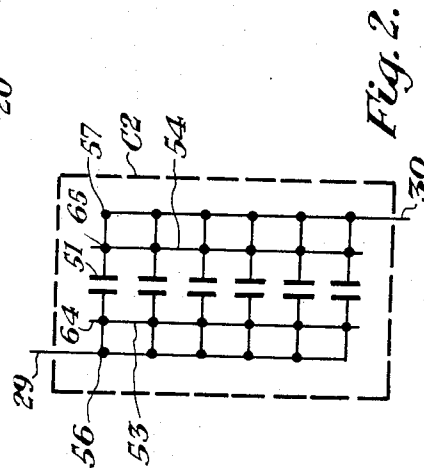


Fig. 2.

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1

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FAIL-SAFE TIME DELAY RELAY

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This invention relates to a solid state time element relay.

More specifically, this invention relates to a fail-safe solid state time element relay which is immune to relay pickup due to early triggering induced by circuit component failure or induced voltage transients. The time delay relay of the invention is capable of a broad range of adjustable time intervals followed by a quick relay pickup at the end of the time intervals. In addition there is absolute certainty that release of the relay will occur in a vitally safe manner.

The time element relay of this invention finds particular application in the railway signaling field and it should be recognized at the outset that, while the invention may have application in other fields, the invention to be described advances the time delay relay art in the railway signaling area of technology. Throughout the description of the invention it should be kept in mind that fail-safe operation of a time delay relay in any rapid mass transit field is not just a goal to be sought but a goal that must be attained in the unequivocal sense. No longer are vehicles of mass transit pursuing headway and speeds measured in units of minutes and units of velocity between zero and 60 miles per hour, but the mass transit systems of today and years to come will measure headway between vehicles in seconds and speed of the vehicles in hundreds of miles per hour. It is against this background of rapidly changing and advancing technology that the invention to be described gains true perspective and the need for "vital," "fail-safe" operation.

Prior art time element relays for railway signaling have incorporated a gear train, driven by a stepping mechanism or a governor controlled direct current motor, which gradually closed the contacts. In this type of system to ensure vital, fail-safe full pickup time it was necessary to provide "check" contacts, which would close only with the relay mechanism fully released and this would occur in connection with related external circuitry. These relays have always required periodic oiling and adjustment and, of course, are subject to wear.

More recently, time delay relays employing solid state techniques have entered the art for use in other applications where vital, fail-safe operation is not critical. Typical of these solid state time element relays is the relay and related circuitry depicted in the General Electric Transistor Manual, 6th Edition, page 198, which has a unijunction transistor as its active element. This unijunction transistor per the Manual noted above may have substituted therefor a silicon controlled switch and in place of the silicon controlled switch there may be substituted a pair of transistors. These substitutions are of course those which may be deemed to be obvious expedients. It should be recognized that these obvious substitutions do not provide a vital, fail-safe relay. In the general version of the time delay relay noted above a capacitor is charged through a high value of resistance to some specific proportion of full charge, at which time a semiconductor "trigger" device discharges the capacitor through a small relay, which picks up and is thereafter held up over a front contact. In this typical solid state time delay relay as well as the recent prior art it will be observed that in case of reverse leakage at the transistor or transistors, as the case may be, the pickup time of the time delay relay

2

could be greatly shortened due to the capacitor receiving additional charging current through the transistor. Furthermore, if a high supply voltage were to suddenly appear and the transistor became shorted, the relay would pick up with no time delay at all. This would result in tragic consequence in a mass transit system of the type previously outlined. In addition, at the higher supply voltage, a momentary interruption in the supply will cause a loss of reference voltage at the transistor, causing it to trigger early, with enough stored energy from the capacitor to pick up the relay. All of these just noted problems are completely obviated by the invention to be described hereafter.

It is therefore an object of this invention to provide a solid state fail-safe relay circuit that is immune to early triggering and relay pickup.

Another object of this invention is to provide a solid state time delay relay circuit in which there is provided a standby reference voltage source to thereby instantly prevent early triggering and relay pickup in the event that there is a momentary interruption of the supply voltage.

Yet another object of this invention is to provide a relay time delay circuit with the highly desirable capability of withstanding wide ranges in power input, induced voltage transients and shorted active elements while maintaining a reasonable control over the time delay period involved.

Another object of this invention is to provide a relay time delay circuit which has its fail-safe qualities enhanced by a novel multiple capacitor timing element.

In the attainment of the foregoing objects this invention embraces the need for a solid state time delay relay which will not pick up due to early triggering brought about by externally and internally induced transient voltage signals while simultaneously affording the capacity to provide adjustable time intervals followed by quick relay pickup at the end of the intervals.

The time delay relay includes in combination an externally controlled direct current voltage source which supplies power to a solid state relay energization control circuit, which circuit includes a first and second transistor each having an emitter, a base and a collector. Interposed between the direct current power source and the solid state relay energization control means is an adjustable time delay voltage storage circuit which is mutually electrically connected to both the direct current power source and the solid state relay energization control circuit.

A safety voltage storage circuit is electrically connected to both the direct current voltage source and the adjustable time delay voltage storage circuit. This safety voltage storage circuit provides a standby reference voltage for the first and second transistors of the solid state relay energization control circuit. The relay to be actuated and a reference voltage control circuit are both electrically connected to the solid state relay energization control circuit. The emitter of the first transistor is electrically connected to the time delay voltage storage circuit and the base of the first transistor is mutually electrically connected to the collector of the second transistor and the reference voltage control circuit. The collector of the first transistor is electrically connected to the base of the second transistor while the emitter of the second transistor is electrically connected to the coil of the relay.

The first transistor will become conducting when the voltage level in the adjustable time delay voltage storage circuit exceeds the reference voltage level in the reference voltage control circuit. The second transistor is rendered conducting upon the commencement of conduction of the first transistor. The final basic component of the system is a bypass circuit for the solid state relay energization control circuit and the reference voltage control circuit.

This bypass circuit is electrically connected to the direct current voltage source and controlled by the relay to provide a bypass circuit to maintain the relay energized.

Simultaneously with the conduction of the first and second transistors the adjustable time delay voltage storage circuit delivers its stored energy through the transistors to energize the relay and the reference voltage is brought to zero by the completion of the bypass circuit to the relay. This results in the relay being quickly picked up and maintained picked up by the combined action of the stored voltage energy in the adjustable time delay storage circuit and the bypass circuit.

Other objectives and advantages of the present system will become apparent from the ensuing description of illustrative embodiments thereof, in the course of which reference is had to the accompanying drawings.

FIG. 1 is a circuit embodying the invention.

FIG. 2 is a novel capacitor arrangement.

A description of the above embodiment will follow and then the novel features of the invention will be presented in the appended claims.

Reference is now made to FIG. 1. In FIG. 1 there is depicted a circuit which provides the variable time delay sought by this invention. It will be noted that there appear not only the basic components of the circuitry set forth here but there are a number of blocks or boxes shown in dotted outline. Each of these blocks or boxes shown in dotted outline is intended to include one or more of the various means to be referred to hereafter. It is hoped that this approach will aid in the understanding of what is intended to be included in the various means recited hereafter, and what is intended to be included within each of the various means as the description ensues. Furthermore, it is believed that this approach will facilitate an understanding of the claims which appear appended hereafter, and set forth the precise invention as claimed.

Accordingly, there is present here a direct current voltage source 11. In this instance the direct current voltage source may be a 10, 12 or 16-volt source and the delay for this system, as shown in this preferred embodiment, may range from 3 to 30 seconds and from ½ to 5 minutes in duration. It will be appreciated that while these are suggested ranges of time delay, they may be varied to be longer or shorter dependent upon the circuit parameters selected by those wishing to employ the invention.

Accordingly, it is seen that there is a direct current voltage source 11 which supplies the power to operate a relay 60, shown here in dotted outline in the right-hand portion of FIG. 1. This relay 60 and its coil 61 is the principal component to be operated at the end of a predetermined time delay which has been designed into the system. And as has been pointed out earlier, this relay 60 must receive its energy with a distinctive and sudden input in order that the relay 60 and its coil 61 react quickly to the application of energy at the end of the predetermined time delay involved. It will be seen that two electrical leads 12 and 14 emanate from the direct current voltage source 11. The electrical lead 12 has a portion thereof interrupted by the presence of a switch 10 which will control the application of the direct current energy to the various components in the circuit to be described. The electrical leads 12 and 14, to the extent that they are the same electrical leads, have portions thereof designated 12a through 12f and 14a through 14g, respectively. This has been done to further enhance the understanding of the theory of the circuit operation which will now ensue.

Serially connected to the input lead 12 is a resistor R1, which resistor R1 limits the power input to the circuitry and has a value selected to match the nominal supply voltage. Connected across the electrical leads 12a and 14 is a Zener diode D1 which limits the voltage which will appear across the electrical leads 12a and 14 to a pre-

determined maximum level. This Zener diode D1, which is incorporated in the dotted outline portion of this figure, has been designated a voltage limiting means 13 and this voltage limiting means 13, which includes the Zener diode D1, provides the capacity to prevent the delivery of momentary increases in power to the remaining portions of the circuitry depicted to the right of the Zener diode D1. In other words, momentary increases in power supply voltage from the direct current voltage source 11 will be clipped off by the Zener diode D1. This increase which may arise may trace its source to a sudden voltage pulse in the line wires when the direct current voltage source and its related system is involved in railway signaling. It goes without saying that any sudden voltage increase will have its effectiveness controlled by the Zener diode D1 of the voltage limiting means 13.

Connected across the electrical leads 12b and 14a is a resistor R2 which is enclosed in a dotted outline block which will be designated as the excess voltage drainoff means, the precise function of which will be made clear hereafter. The electrical leads 12b and 14a and their extensions 12c and 14b convey the supply voltage to the capacitor C1 connected by electrical leads 23 and 24 to the leads 12c and 14b. The capacitor C1 is shown enclosed in the dotted outline box 22 and will be referred to hereafter as a safety voltage storage means 22. Adjacent to the safety voltage storage means 22 there is a box shown in dotted outline and designated by the reference numeral 26. This will be hereafter referred to as an adjustable time delay storage means. This adjustable time delay storage means includes a variable resistance potentiometer connected electrically by lead 27 to the lead 12d. There is also a resistor R5 in series with the variable potentiometer connected thereby by electrical lead 28. The resistor R5 and its function in the system will be explained hereafter. The resistor R5 is connected electrically via the electrical lead 29 to a capacitor C2, as well as by an electrical lead 31 to the emitter 35 of a transistor Q1. This transistor Q1 will be referred to hereafter as the first transistor. The capacitor C2 is in turn connected to the electrical lead 14c by lead 30. It will be appreciated that the electrical lead 14, as well as 14a, b, c and d, is respectively electrically connected to a ground depicted here at the bottom of the figure. This ground is a connection to a magnetic shielding 20 shown in dotted outline. This magnetic shielding 20 and its function will be explained more fully hereafter.

The adjustable time delay storage means 26 is connected via electrical lead 12e, a resistor R8, and lead 12f, to the reference voltage control means 50, which reference voltage control means 50 is shown in dotted outline. The reference voltage control means 50 includes a pair of resistors R6 and R7. Interposed between the reference voltage control means 50 and the adjustable time delay storage means 26 is a solid state relay energization control means 25, which solid state relay energization control means 25 has a pair of transistors Q1 and Q2. The emitter 35 of first transistor Q1, as has been noted, is electrically connected via the lead 31 to the adjustable time delay voltage storage means 26. The base 36 of the transistor Q1 is connected by lead 34 to a lead 33 which in turn is connected by lead 48 to the reference voltage control means 50. The collector 37 of the transistor Q1 is electrically connected via the lead 38 to the base 45 of the second transistor Q2, while the collector 44 of the second transistor Q2 is electrically connected to the lead 33 which in turn is electrically connected to the lead 34 and the base 36 of the transistor Q1. The collector 37 of the first transistor Q1, as well as the base 45 of the second transistor Q2, is mutually electrically connected via the lead 38 and the lead 39 to a resistor R9, and lead 41 to electrical lead 14e which is an extension, as has been noted, of the electrical lead 14.

Interposed in the circuitry between the adjustable time

5

delay storage means 26 and the solid state relay energization control means 25 is a signal transient suppression means 55. This signal transient suppression means 55, shown in dotted outline, includes a resistor R3 and a diode D3 in series between the electrical leads 58 and 59 which emanate from the leads 14d and 14e, respectively. Leads 58 and 59 are connected to the opposite ends of the relay coil 61 of the relay 60 shown in dotted outline. Directly beneath the relay 60 is a box shown in dotted outline which will be referred to hereafter as a bypass means 66. This bypass means 66 includes a contact *a* which completes a circuit between the right-hand end of the relay coil 61 and the reference voltage control means 50 over the electrical lead 63 which enters at the top right-hand corner of the reference voltage control means 50. It will be appreciated that when the relay 60 is energized it is intended that the contact *a* be picked up and complete a circuit over the front contact *a* of this relay 60, and at this point the bypass means 66 will complete a circuit, as noted earlier, and there will be a circuit completed from the reference voltage control means 50 through the lead 63, front contact *a* of the relay 60, lead 62, coil 61, lead 58, leads 14d, 14c, 14b, 14a and 14 to the direct current voltage source to thereby provide a circuit which will maintain the relay 60 energized.

FIG. 2 depicts a multiple capacitor arrangement that may be utilized in place of the capacitor C2 shown in FIG. 1. This multiple capacitor arrangement plays a significant role in the fail-safe qualities of this time delay circuit. The capacitor C2 in FIG. 2 is shown in dotted outline and includes a plurality of capacitors, in this instance, six capacitors, electrically coupled in the manner shown. It will be appreciated that, for example, capacitor 51, which is typical of the remaining capacitors depicted, has four electrical connections present. The first electrical connection is that at the point 56 where the one half of the capacitor 51 is secured to the electrical lead 29. The other half of the capacitor 51 is connected to electrical lead 30 at the point 57. And in order to provide a fail-safe environment there have been soldered across all the leads depicted here two wires 53 and 54 which are soldered, for example, at points 64 and 65 to either side of the capacitor 51. It can therefore be appreciated that in the event a solder joint fails at any one of these capacitors, there would remain an additional solder joint on that side of the capacitor to the end that while the entire group of capacitors might become open-circuited at lead 29 or 30, there is little likelihood of losing one or two of the six capacitors.

Turning now to the operation of the circuit just described, when the switch 10 is closed the direct current voltage source 11 will be connected to the adjustable time delay circuitry and the following will occur. Upon the closing of the switch 10 the voltage level, which is controlled as has been noted by the voltage limiting means 13, will therefore appear across some of the remaining components depicted to the right of the voltage limiting means 13. The direct current voltage selected for this particular design would be approximately 7.5 volts. The resistors R6 and R7, which form the reference voltage control means 50, act as a voltage divider for the transistors Q1 and Q2. These resistors R6 and R7, which are much higher in resistance than the resistor R8 and the resistance of the coil 61, provide a trigger reference voltage for the transistors Q1 and Q2 of the solid state relay energization control means 25. The resistors R6 and R7 function as a conventional voltage divider which provides the reference voltage to be applied to the base 36 of the first transistor Q1 via the leads 34, 33 and 48.

The adjustable time delay storage means 26, as has been noted, includes a capacitor C2. In this particular embodiment, while this capacitor C2 is shown as one capacitor it is to be understood that this capacitor C2 is a multiple capacitor arrangement which is set forth in FIG. 2.

6

This capacitor C2 charges gradually through the time adjustment variable resistance potentiometer over the electrical leads 27, 28, resistor R5, lead 29, to the capacitor C2 which is connected via the lead 30 to ground. Resistor R5 limits the minimum time adjustment for the time delay function of the circuit while the variable resistance potentiometer may be varied to control the time required to charge the capacitor C2 and therefore provide the adjustable time delay for the time relay circuitry being described.

The transistor Q1 of the solid state relay energization control means 25 will conduct when the emitter 35 becomes more positive than the base 36. This will occur after the capacitor C2 in the adjustable time delay storage means 26 has been charged to a point where the voltage present in the capacitor C2 exceeds the reference voltage provided by the reference voltage control means 50 and its related resistors R6 and R7. In other words, when the emitter 35 of the transistor Q1 becomes more positive than the base 36 of the transistor Q1, transistor Q1 will conduct and the capacitor C2, in a manner to be described hereafter, will discharge through the lead 29, lead 31, to the transistor Q1. The transistor Q1, in this embodiment of the invention, is normally nonconducting until capacitor C2 has charged to a level which exceeds the voltage reference level provided by the resistors R6 and R7 of the reference voltage control means 50. When transistor Q1 conducts it will bias transistor Q2 into conduction. In other words, the base 45 of the transistor Q2 will become more positive than its emitter 46.

With transistor Q2 conducting, transistor Q1 will be further biased into conduction. This further biasing of transistor Q1 into conduction is a regenerative action and therefore drives both transistors Q1 and Q2 into saturation, and they will remain triggered until the current through them is reduced to some small value inherent in the transistors selected. As has been noted, once the capacitor C2 of the adjustable time delay storage means 26 has been charged to a level which exceeds the reference voltage supplied by the reference voltage control means 50, the capacitor C2 will discharge through electrical leads 29, 31, transistor Q1, and transistor Q2 to leads 14f, 14e, 59, through relay coil 61 of relay 60, lead 58, leads 14d, 30, to the capacitor C2, thereby causing the relay 60 to pick up due to energy from capacitor C2, and close the contact *a* of the bypass means 66 which therefore completes a circuit from the right-hand end of coil 61 over the lead 62, the front contact *a* of the relay 60, lead 63, to the lead 12f, where the lead 12f enters the reference voltage control means 50. This completed circuit just noted will hold the relay 60 picked up by the circuit just described, due to energy from the direct current voltage source. This completed circuit causes the reference voltage at the junction of the resistors R6 and R7 to go to zero, and the transistors Q1 and Q2 remain conductive due to a very small current which is above the cutoff current of the transistors Q1 and Q2, which current passes through the variable resistance potentiometer and the resistance R5 of the adjustable time delay storage means 26, and the transistors Q1, Q2 and the leads 14f, 14e, 59, coil 61, lead 58, lead 14d, lead 14c to ground. It is therefore to be appreciated that the relay 60 is maintained energized by the bypass circuit which includes the bypass means 66 but there is an additional path in which a low level of current is constantly flowing. That path includes the transistors Q1 and Q2 just noted.

In the preferred embodiment the voltage drop in the transistors Q1 and Q2 at this point in the operation is about .4 of a volt, and the voltage drop in the coil 61, due to the holding current, is about 2.7 volts. Accordingly, the capacitor C2 stabilizes at a charge of 2.7 volts plus .4 of a volt or 3.1 volts.

The resistor R2, which forms the heart of the excess voltage drainoff means 18, performs the important func-

tion of providing a rapid drainoff of residual charges that appear on the capacitor C2 of the adjustable time delay storage means 26. Since whether or not a circuit triggers the transistors Q1 and Q2 it will be observed that any residual charges at the capacitor C2 will drain off more rapidly through the resistor R2 which, by design, is about 5K, to ground than through resistors R6 and R7 of the reference voltage control means which combined resistance is about 2700K, to ground. In other words, there is a preferential path through the resistor R2 which provides the important function of draining off excess voltage which will appear on the capacitor C2 which when fully charged discharges through the transistors Q1 and Q2 to energize the relay 60 in a manner described earlier.

The capacitor C1 which is connected across the leads 12c and 14b via the leads 23 and 24 provides what is termed a safety voltage storage function and therefore the designation of this capacitor as a safety voltage storage means 22. The capacitor C1 of the safety voltage storage means 22 stores enough energy to prevent early triggering of the transistors Q1 and Q2 due to loss of the reference voltage during any momentary interruption of input power. In other words, the capacitor C1 stores sufficient energy to maintain the reference voltage at a level that will not permit the transistors Q1 and Q2 to fire when there appears a momentary interruption in power from the direct current voltage source 11. The capacitor C1 of the safety voltage storage means 22 is also important from the standpoint that should there be an induced pulse impressed in the line wires that supply the direct current voltage source from the power supply and should this pulse be of a negative nature, this would cause a reduction in the reference voltage which could cause early triggering of the transistors Q1 and Q2 if the safety voltage storage means capacitor C1 were not present within the circuitry and did not have available the stored energy needed to maintain this reference voltage. Again, it should be appreciated that this provides a feature of fail-safe operation which is of great importance to the safety and the integrity of the time delay circuitry involved here.

When the direct current voltage source 11 and the circuits that supply the power to the relay are opened, as when the switch 10 is opened, the reference voltage which, as has been noted, is zero due to the bypass circuitry around the reference voltage control means 50, the capacitor C2 discharges completely through transistors Q1 and Q2, the relay coil 61 causing the relay 60 to release. The resistor R3 of the signal transient suppression means 55 is important for the following reasons. If the resistor R3 were shunted so that it were out of the circuit, the transistors Q1 and Q2 would cease to conduct at some low value of current. This would leave a small positive charge on the capacitor C2. Accordingly, if resistor R3 were removed, i.e. R3 were opened, collapse of the electromagnetic field of the relay coil 61 would prolong the discharge of capacitor C2 of the time delay storage means 26 until it assumed a small negative charge. This, of course, would affect the time period of the next delay which would be bad. Accordingly, it can be seen that by adjusting the value of the resistor R3 in the signal transient suppression means 55, the capacitor C2 can be left with exactly a zero charge. The signal transient suppression means 55 includes a diode D3. This diode D3 is important for it prevents current from being shunted around the relay coil 61, which would tend to prevent the relay from picking up, and also prevent the early triggering of the transistors Q1 and Q2 due to an induced signal which may appear within the system upon the release of an adjacent relay. While, for purposes of example, this sudden transient voltage just noted might be induced by the release of an adjacent relay, it should be recognized that this suddenly induced voltage spike might come from any source externally of the relay here being described.

If the resistance R3 and the diode D3 were not present,

a voltage spike induced in the coil 61 of the relay 60 could add to the voltage present on the capacitor C2 to produce a total voltage exceeding the reference voltage which of course would cause the transistors Q1 and Q2 to be triggered which would result in the premature pickup of the relay which of course must never occur in this type of fail-safe environment.

The capacitor C3, which is connected across the emitter 35 and the base 36 of the transistor Q1 by the leads 32 and 33, functions as a buffer to the transistor Q1 should there be an induced voltage spike which somehow reaches this first transistor Q1. The capacitance of the capacitor C3 cooperates with a magnetic shield 20, referred to earlier, to protect the transistor Q1 from such a voltage spike. Accordingly, the capacitor C3 prevents the early triggering of the transistor Q1 due to instantaneous voltages at the transistor Q1, magnetically or electrostatically induced which could cause a sudden variation in the reference voltage which would, of course, possibly cause transistor Q1 to be triggered into conduction presenting the premature pickup of the relay which at all cost must be avoided.

The resistor R8, which is in the circuit between the electrical leads 12e and 12f, limits the holding current which will appear in the bypass circuit which includes the contact a of the relay 60, and this resistor R8 is selected merely to provide some nominal level of holding current in the coil 61 of the relay 60.

The resistor R9 electrically connected via the leads 39 and 41 to the leads 38 and 14e, respectively, is needed to stabilize the bias on the transistor Q2 to prevent leakage from the transistor Q1 from triggering transistors Q1 and Q2 early due to some high ambient temperatures. The inclusion of this resistor R9 is a standard technique involved to obviate this possible early triggering due to elevated ambient temperatures experienced by the system.

It will therefore be appreciated that the circuitry just described sets forth an embodiment of a time delay relay that is inherently safe on release and which can operate contacts quickly at the end of the time delay involved rather than gradually. The basic safety feature is that in the event of early triggering the relay will not pick up because there is not enough stored energy in the timing capacitors of the adjustable time delay storage means 26.

Obviously, certain modifications and variations of the invention as hereinbefore set forth may be made without departing from the spirit and scope thereof, and therefore only such limitations should be imposed as are indicated in the appended claims.

Having thus described my invention, what I claim is:

1. A fail-safe solid state time element relay which is immune to relay pickup due to early triggering, said time delay relay capable of adjustable time intervals followed by quick relay pickup at the end of said time intervals, said time element relay having in combination:
 - (1) an externally controlled direct current voltage source,
 - (2) solid state relay energization control means,
 - (3) a predetermined time delay voltage storage means electrically connected to said solid state relay energization control means,
 - (4) a safety voltage storage means electrically connected between said direct current voltage source and said predetermined time delay voltage storage means,
 - said voltage storage means storing energy from said direct current voltage source to thereby provide a standby reference voltage to said solid state relay energization control means.
 - (5) an excess voltage drainoff means for said predetermined time delay voltage storage means electrically connected to said predetermined time delay voltage storage means,
 - (6) reference voltage control means electrically connected to said solid state relay energization control means,

- (7) a relay electrically connected to said solid state relay energization control means,
- (8) a bypass means for said solid state relay energization control means and said reference voltage control means,
- said bypass means electrically connected to said direct current voltage source and controlled by said relay to provide a bypass circuit to maintain said relay energized.
2. The fail-safe solid state time element relay of claim 1 wherein said solid state relay energization control means includes a first and second transistor each having an emitter, a base and a collector,
- said emitter of said first transistor electrically connected to said time delay voltage storage means,
- said base of said first transistor mutually electrically connected to said collector of said second transistor and said reference voltage control means,
- said collector of said first transistor electrically connected to said base of said second transistor while said emitter of said second transistor is electrically connected to said relay,
- said first transistor becomes conducting when the voltage level in said predetermined time delay voltage storage means exceeds the reference voltage level in said reference voltage control means,
- said second transistor is rendered conducting upon the commencement of said first transistor conduction, simultaneously with the conduction of said first and second transistors said time delay voltage storage means delivers its stored voltage energy through said transistors to energize said relay and said reference voltage is brought to zero by the completion of said bypass circuit through said bypass means to said relay, whereby said relay is quickly picked up and maintained picked up by the combined action of said stored voltage in said predetermined time delay voltage storage means and said circuit through said bypass means.
3. The fail-safe solid state time element relay of claim 2 wherein said predetermined time delay storage means includes a series circuit which includes a variable resistance, a fixed resistance and a multiple capacitor means;
- said multiple capacitor means charges gradually through said variable resistance and said fixed resistance which respectively provide a time adjustment function and a minimum time adjustment for said time element relay.
4. The fail-safe solid state time element relay of claim 3 wherein said multiple capacitor means includes a plurality of capacitors electrically connected in parallel, each capacitor having a pair of leads,
- said plurality of electrically connected parallel capacitors having an additional parallel pair of electrical connections across all of said capacitor leads, one said pair of additional electrical connections positioned on either side of said plurality of capacitors and in electrical contact with said pairs of electrical leads to thereby provide a fail-safe capacitor arrangement immune from the effects of possible failure of said parallel electrical connection.
5. The fail-safe solid state time element relay of claim 4 wherein said safety voltage storage means includes a capacitor which stores enough energy to prevent early triggering due to loss of said reference voltage during any momentary interruption of input power from said direct current voltage source or the appearance in the direct current voltage source of an externally induced signal of negative nature.
6. The fail-safe solid state time element relay of claim 5 wherein said excess voltage drainoff means includes a resistive element having a resistive value which is less than the total resistive value of said reference voltage control means, said excess voltage drainoff means there-

by providing a rapid drainoff of residual charges on said multiple capacitor means whether or not said solid state relay energization means is triggered into conduction.

7. The fail-safe solid state time element relay of claim 6 wherein said relay includes transient signal suppression means to prevent relay energizing current from bypassing the coil of said relay and simultaneously preventing early energization of said relay due to externally induced transient voltage signals which would momentarily increase the voltage at said multiple capacitor means which would produce an early triggering of said solid state relay energization means.

8. The fail-safe solid state time element relay of claim 7 wherein said transient signal suppression means also prevents early energization of said relay due to externally induced transient voltage signals which would momentarily reduce said reference voltage in said reference voltage means which would produce an early triggering of said solid state relay energization means.

9. The fail-safe solid state time element relay of claim 8 which includes a voltage limiting means electrically connected to said direct current voltage source and said predetermined time delay storage means,

said voltage limiting means clipping off excess voltage transients which may be impressed upon the direct current voltage source.

10. A fail-safe solid state time element relay which is immune to relay pickup due to early triggering brought about by externally and internally induced transient voltage signals, said time delay relay capable of adjustable time intervals followed by quick relay pickup at the end of said time intervals, said time element relay having in combination,

- (1) an externally controlled direct current voltage source,
 - (2) solid state relay energization control means which includes a first and a second transistor each having an emitter, a base and a collector,
 - (3) a predetermined time delay voltage storage means electrically connected to said solid state relay energization control means,
 - (4) a safety voltage storage means electrically connected between said direct current voltage source and said predetermined time delay voltage storage means, said voltage storage means storing energy from said direct current voltage source to thereby provide a standby reference voltage to said first and second transistors of said solid state relay energization control means,
 - (5) reference voltage control means electrically connected to said solid state relay energization control means,
 - (6) a relay electrically connected to said solid state relay energization control means,
- said emitter of said first transistor electrically connected to said time delay voltage storage means, said base of said first transistor mutually electrically connected to said collector of said second transistor and said reference voltage control means,
- said collector of said first transistor electrically connected to said base of said second transistor while said emitter of said second transistor is electrically connected to said relay,
- said first transistor becomes conducting when the voltage level in said predetermined time delay voltage storage means exceeds the reference voltage level in said reference voltage control means,
- said second transistor is rendered conducting upon the commencement of conduction of said first transistor,
- (7) a bypass means for said solid state relay energization control means and said reference voltage control means,

said bypass means electrically connected to said direct current voltage source and controlled by said relay to provide a bypass circuit to maintain said relay energized,

simultaneously with the conduction of said first and second transistors said time delay voltage storage means delivers its stored voltage energy through said transistors to energize said relay and said reference voltage is brought to zero by the completion of said bypass circuit through said bypass means to said relay, whereby said relay is quickly picked up and maintained picked up by the combined action of said storage voltage in said predetermined time delay voltage storage means and said circuit through said bypass means.

11. The fail-safe solid state time element relay of claim 10 wherein said solid state relay energization control means includes an excess voltage drainoff means electrically connected to said predetermined time delay storage means.

12. The fail-safe solid state time element relay of claim 11 wherein said predetermined time delay storage means includes a series circuit which includes a variable resistance, a fixed resistance and a multiple capacitor means; said multiple capacitor means charges gradually through said variable resistance and said fixed resistance which respectively provide a time adjustment function and a minimum time adjustment for said time element relay.

13. The fail-safe solid state time element relay of claim 12 wherein said multiple capacitor means includes a plurality of capacitors electrically connected in parallel, each capacitor having a pair of leads, said plurality of electrically connected parallel capacitors having an additional parallel pair of electrical connections across all of said capacitor leads, one of said pair of additional electrical connections positioned on either side of said plurality of capacitors and in electrical contact with said pairs of electrical leads to thereby provide a fail-safe capacitor arrangement immune from the effects of possible failure of said parallel electrical connection.

14. The fail-safe solid state time element relay of claim 13 wherein said safety voltage storage means includes a capacitor which stores enough energy to prevent early triggering due to loss of said reference voltage during

any momentary interruption of input power from said direct current voltage source or the appearance in the direct current voltage source of an externally induced signal of negative nature.

15. The fail-safe solid state time element relay of claim 14 wherein said excess voltage drainoff means includes a resistive element having a resistive value which is less than the total resistive value of said reference voltage control means, said excess voltage drainoff means thereby providing a rapid drainoff of residual charges on said multiple capacitor means whether or not said solid state relay energization means is triggered into conduction.

16. The fail-safe solid state time element relay of claim 12 wherein said relay includes transient signal suppression means to prevent relay energizing current from bypassing the coil of said relay and simultaneously preventing early energization of said relay due to externally induced transient voltage signals which would momentarily increase the voltage at said multiple capacitor means which would produce an early triggering of said solid state relay energization means.

17. The fail-safe solid state time element relay of claim 16 wherein said transient signal suppression means also prevents early energization of said relay due to externally induced transient voltage signals which would momentarily reduce said reference voltage in said reference voltage means which would produce an early triggering of said solid state relay energization means.

18. The fail-safe solid state time element relay of claim 17 which includes a voltage limiting means electrically connected to said direct current voltage source and said predetermined time delay storage means,

said voltage limiting means clipping off excess voltage transients which may be impressed upon the direct current voltage source.

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