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(54) Title of the Invention: **Generation of a control stream for a tile**
Abstract Title: **Tiling based on sample positions in pixels in the tile**

(57) A method and system for processing primitives within a tiling unit of a graphics processing system comprises determining whether a polygon 510 falls within a tile 508 based on positions of samples 502 within each pixel. If it is determined that the primitive does overlap a tile based on the positions of samples within pixels in a tile, an association between the tile and the primitive is stored to indicate that the primitive is present in the tile. For example, an identifier for the primitive may be added to a control stream for the tile to indicate that the primitive is present in the tile. A smaller bounding box 506 for the tile may be generated based on the positions of samples in the tile. It may be determined if the intersection of a triangle with a tile or the bounding box of the intersection contain any samples from the tile.

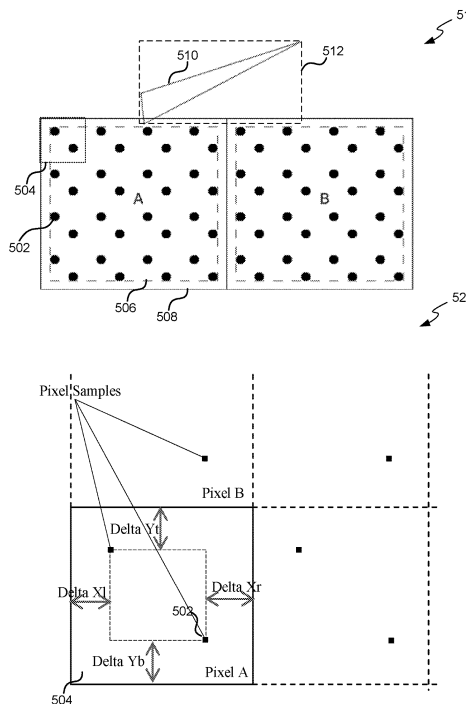


FIG. 5

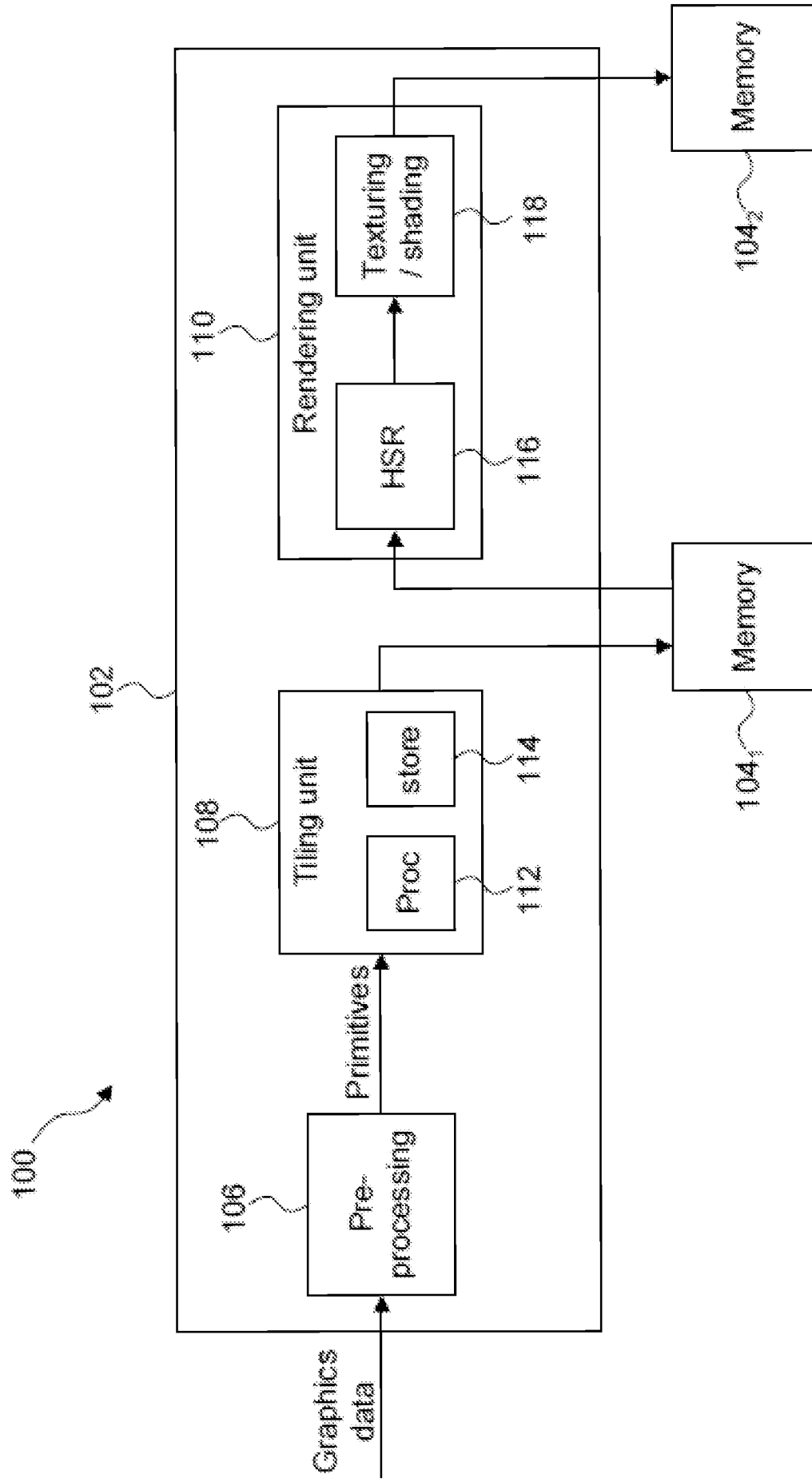


FIG. 1

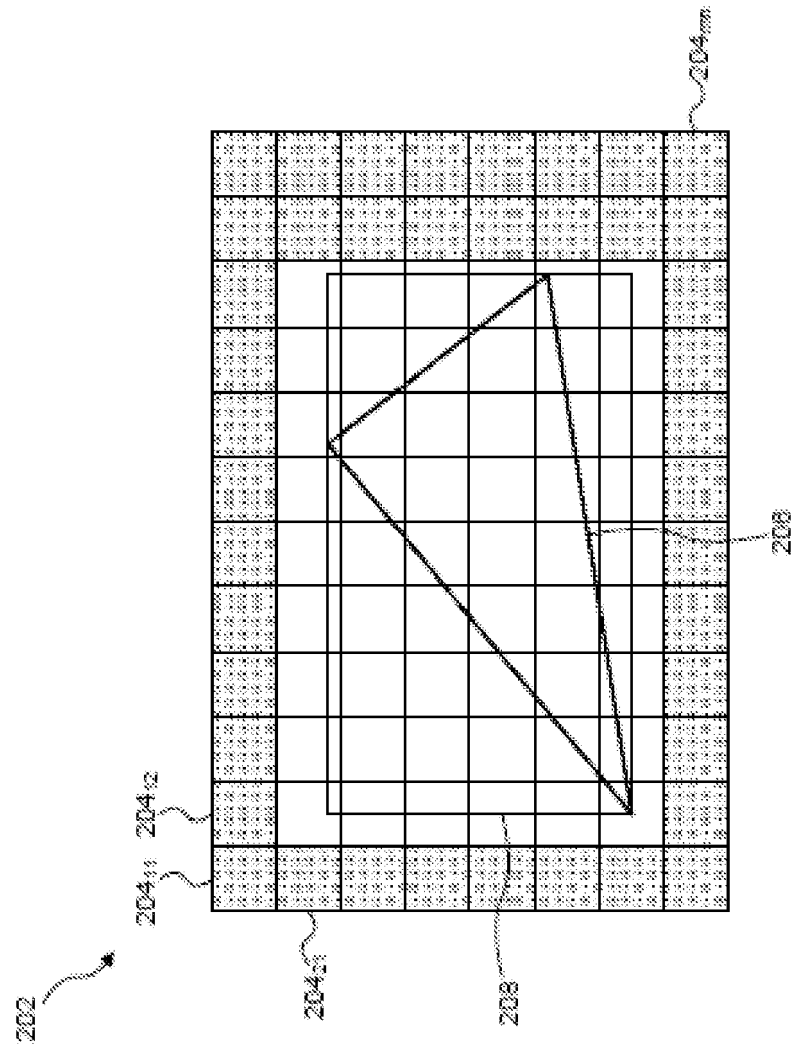


FIG. 2

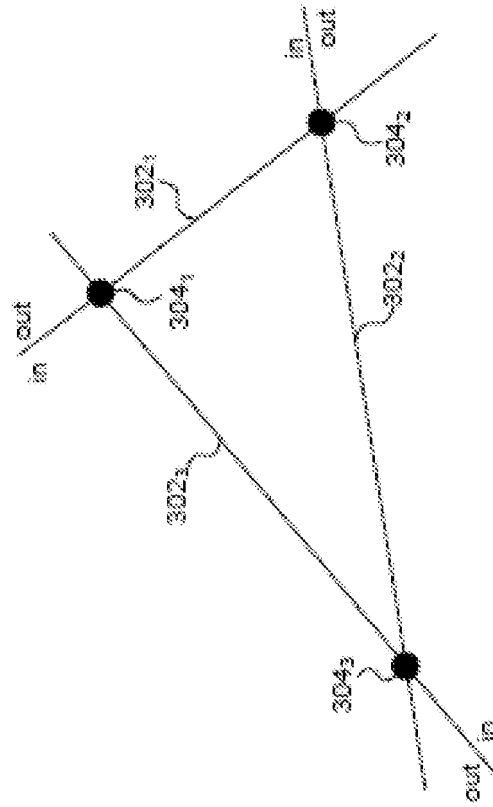


FIGURE 3

FIG. 3

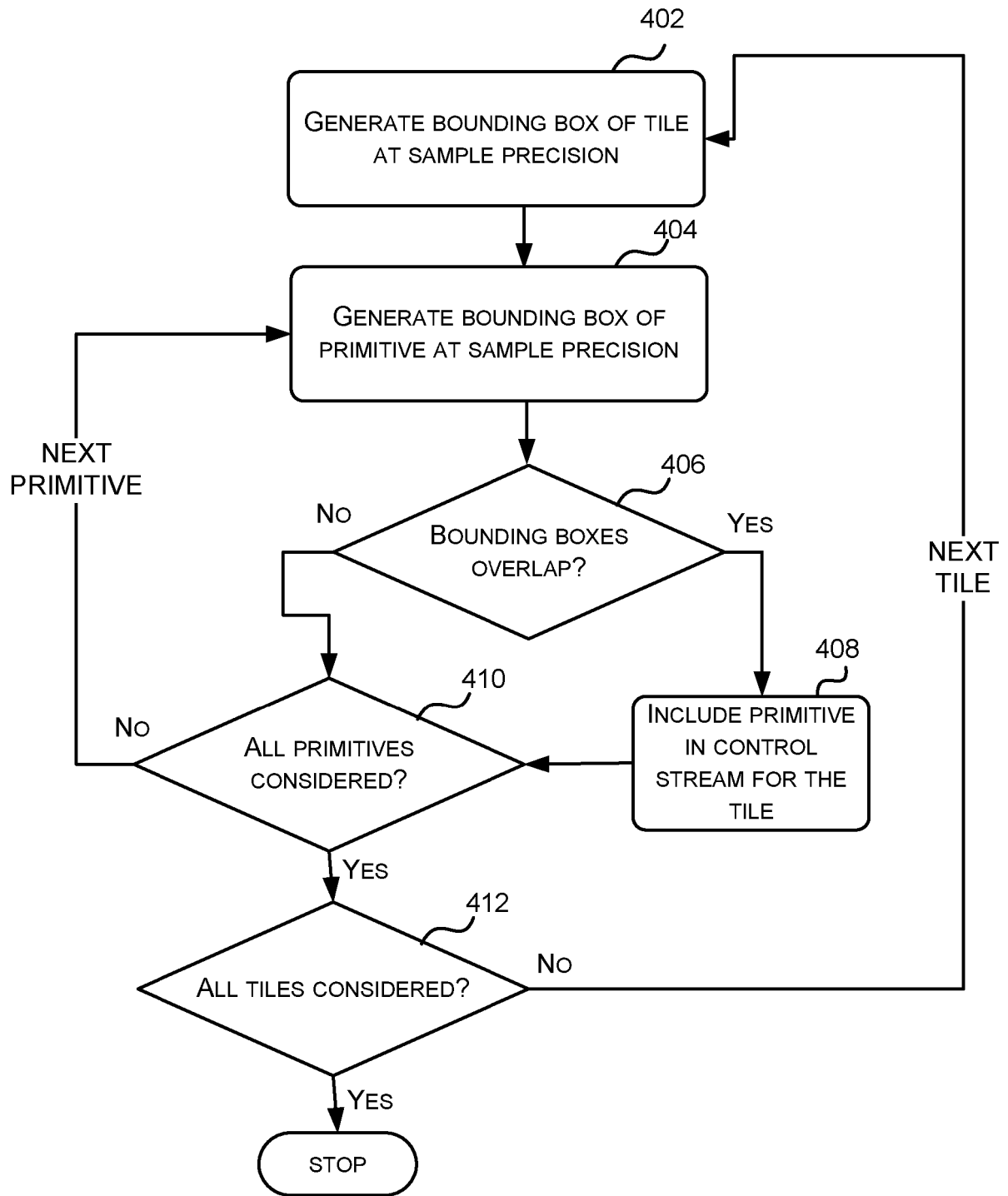


FIG. 4

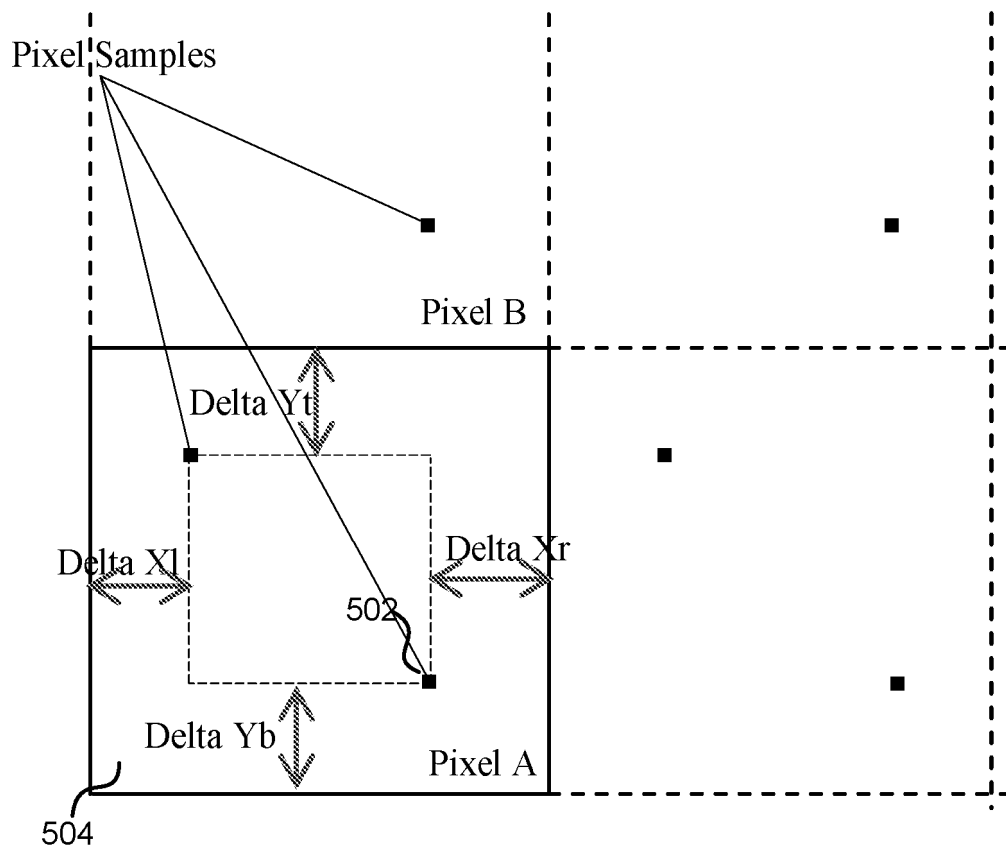
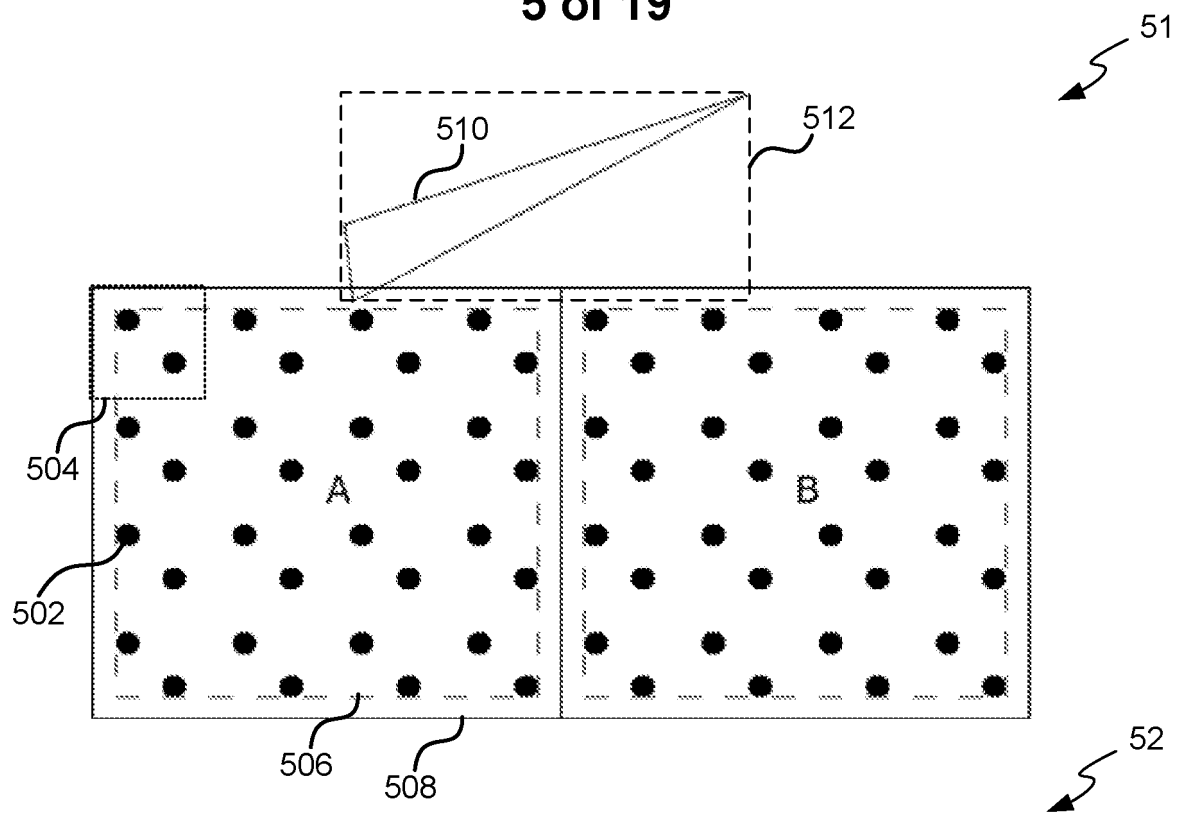


FIG. 5

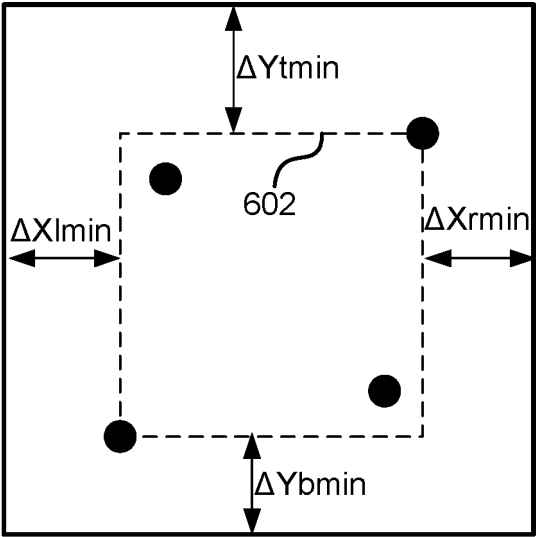
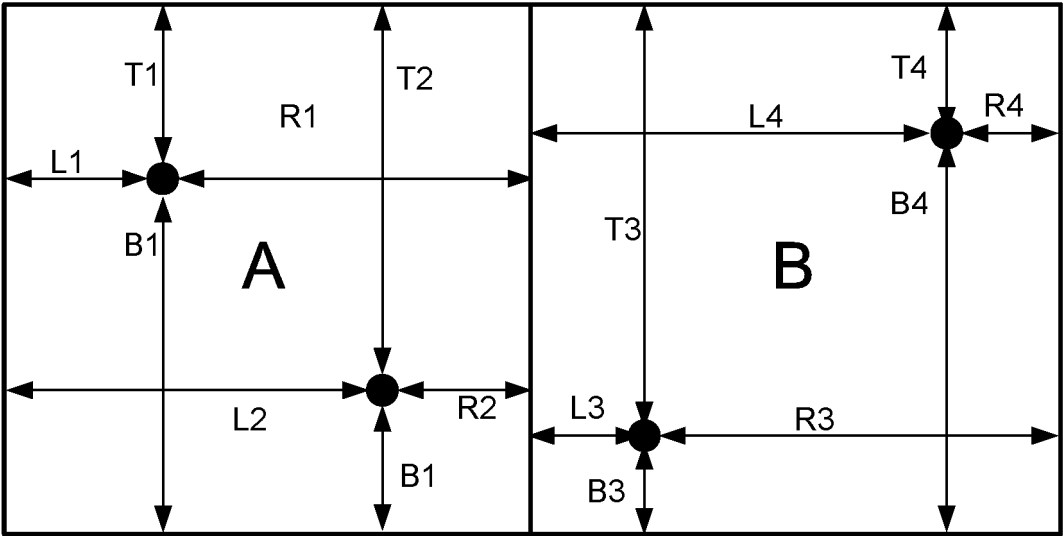


FIG. 6

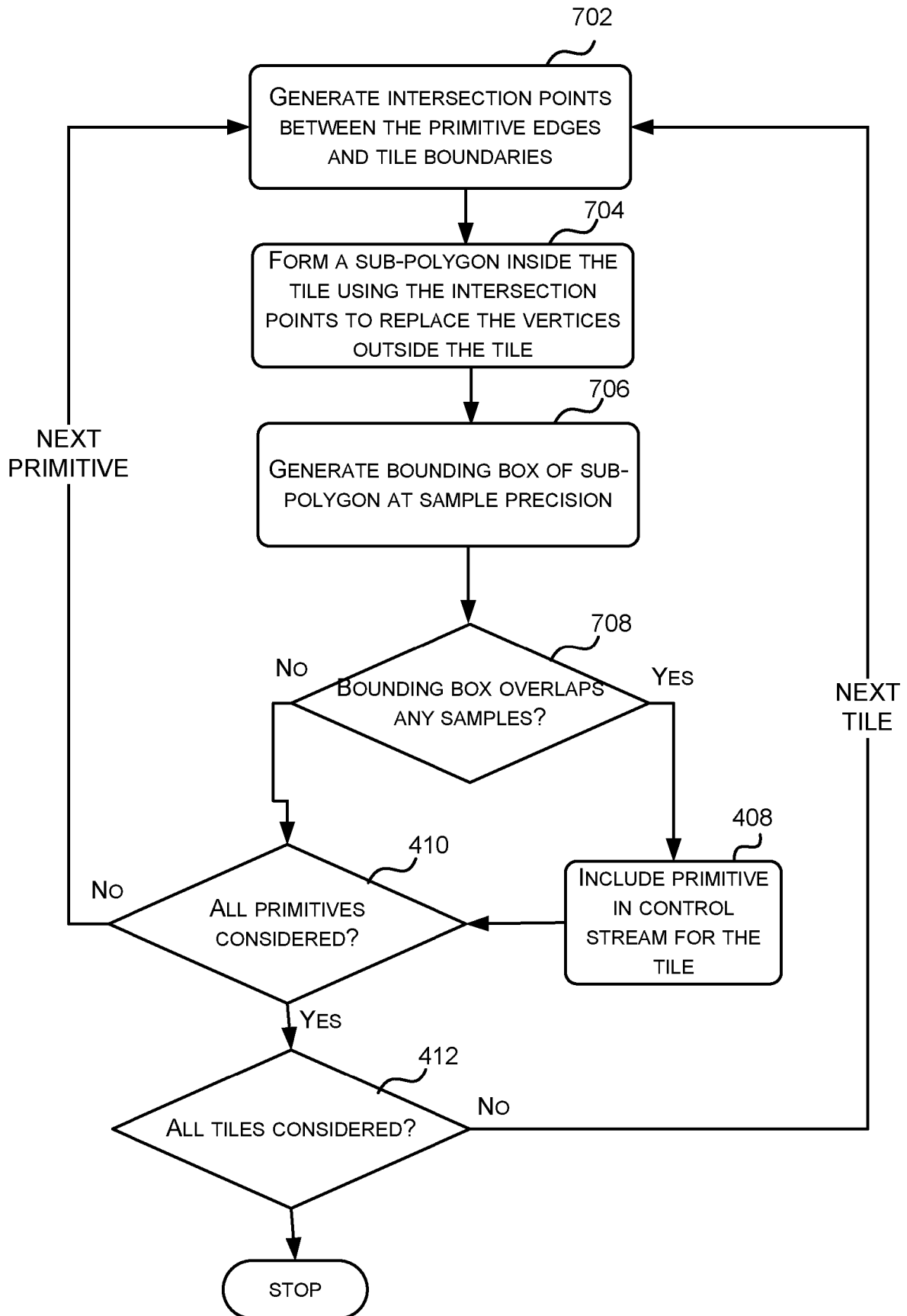


FIG. 7

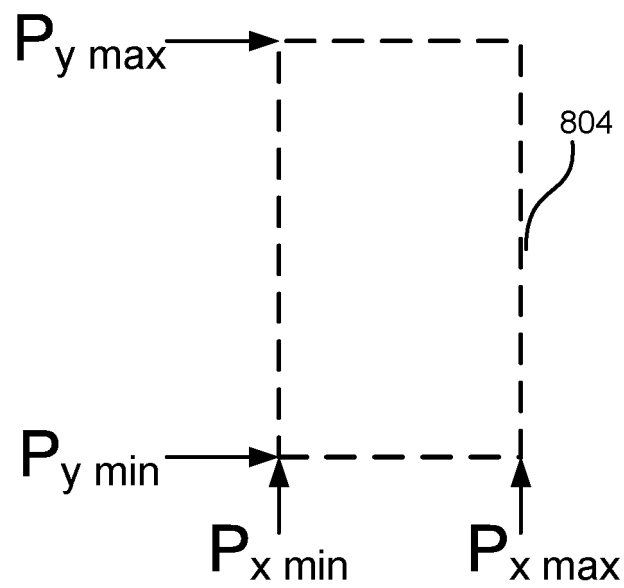
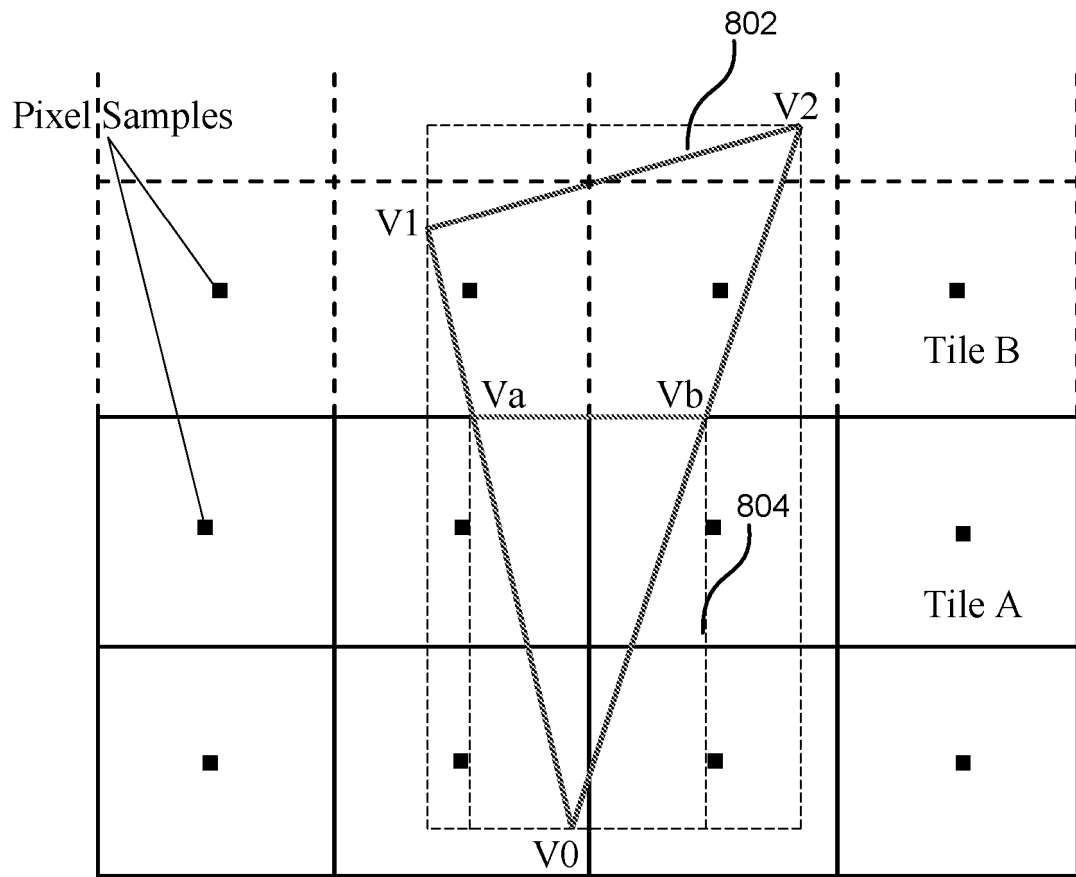


FIG. 8

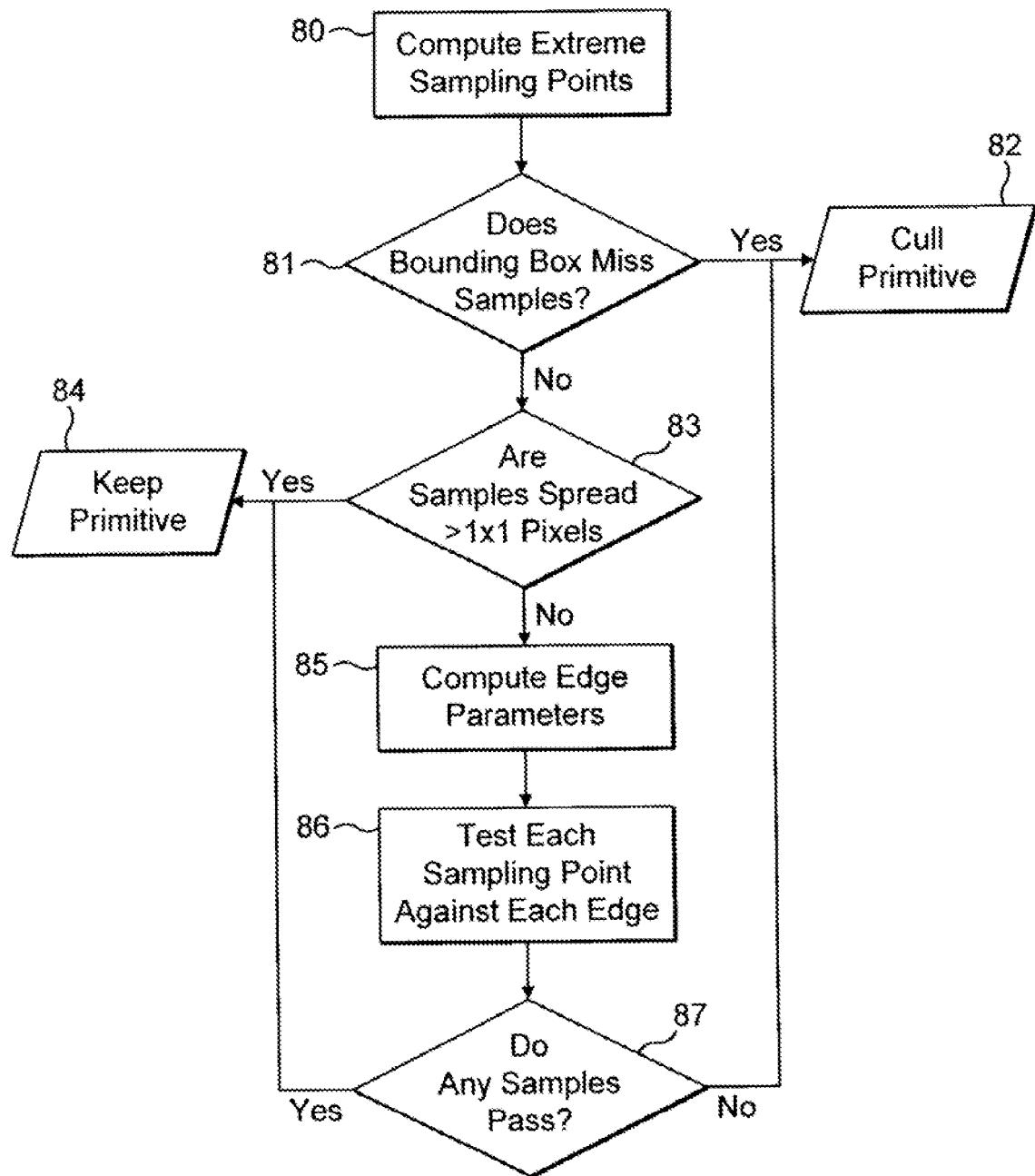


FIG. 9

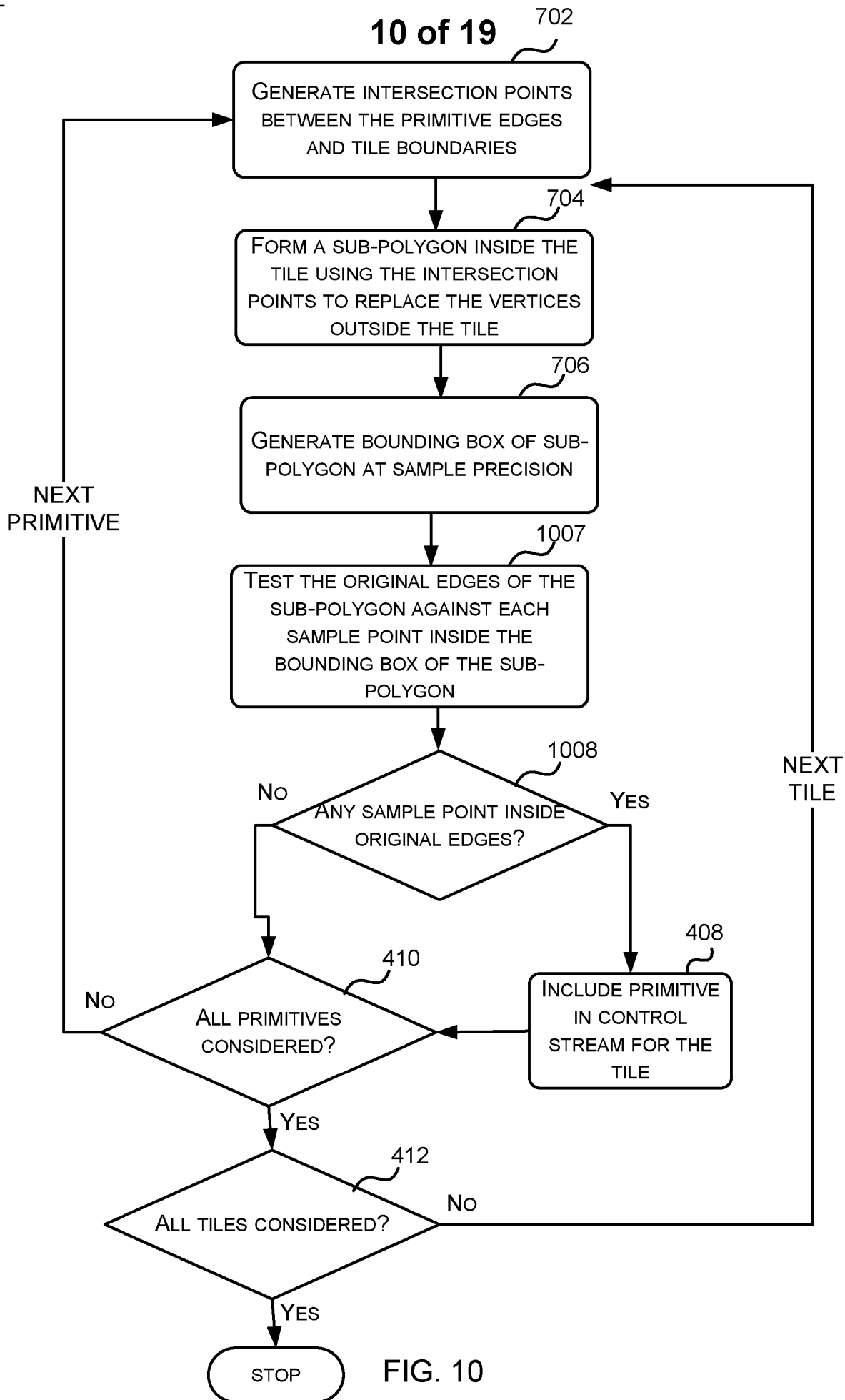


FIG. 10

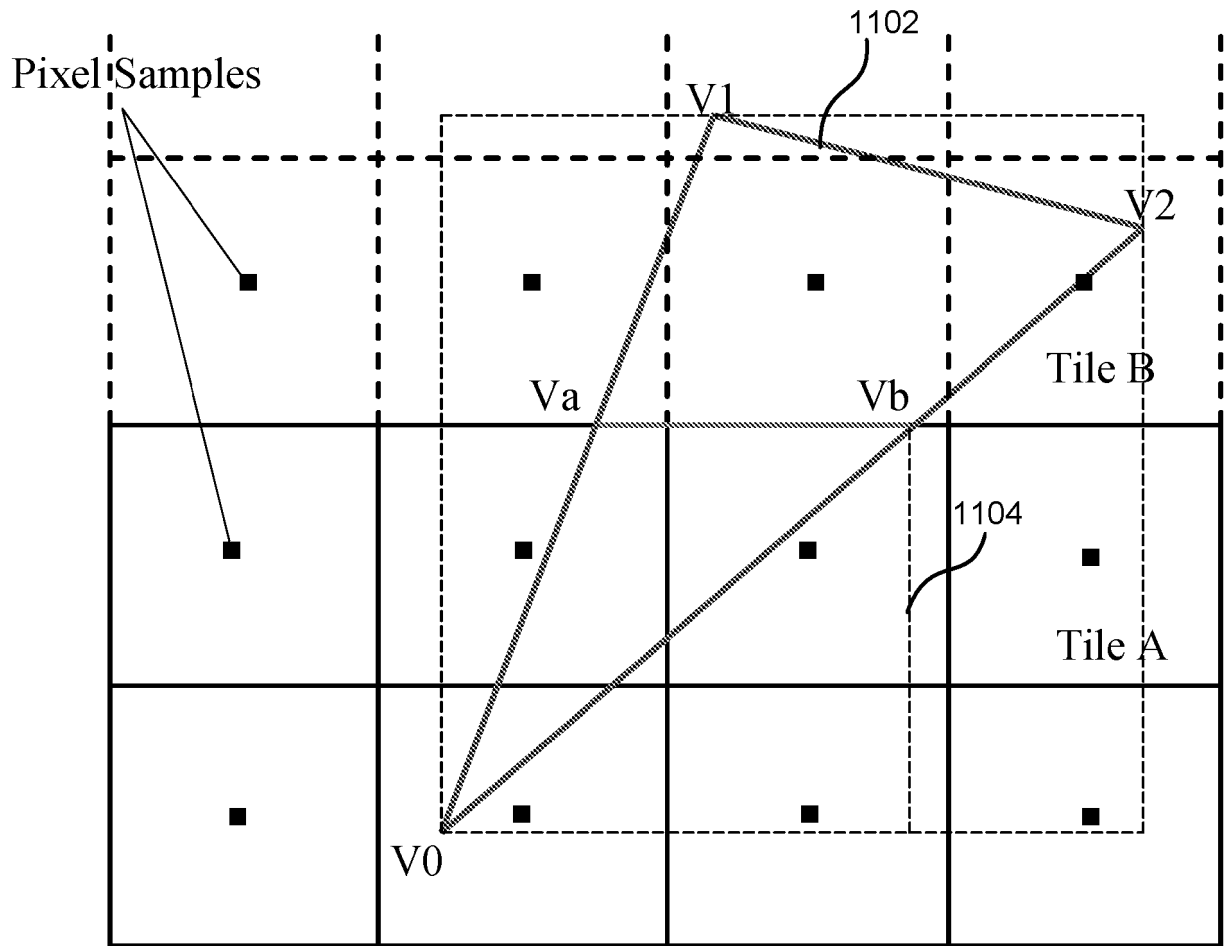


FIG. 11

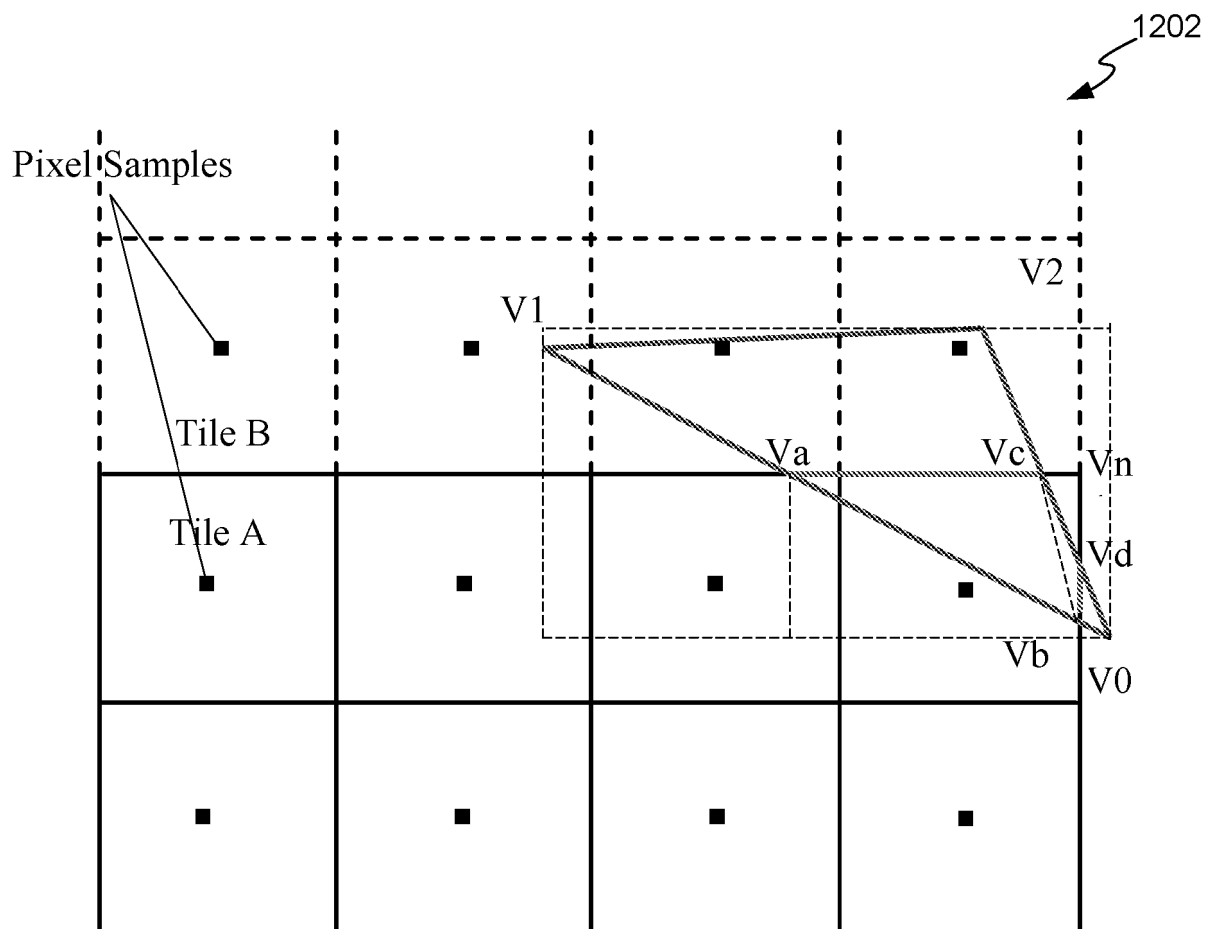
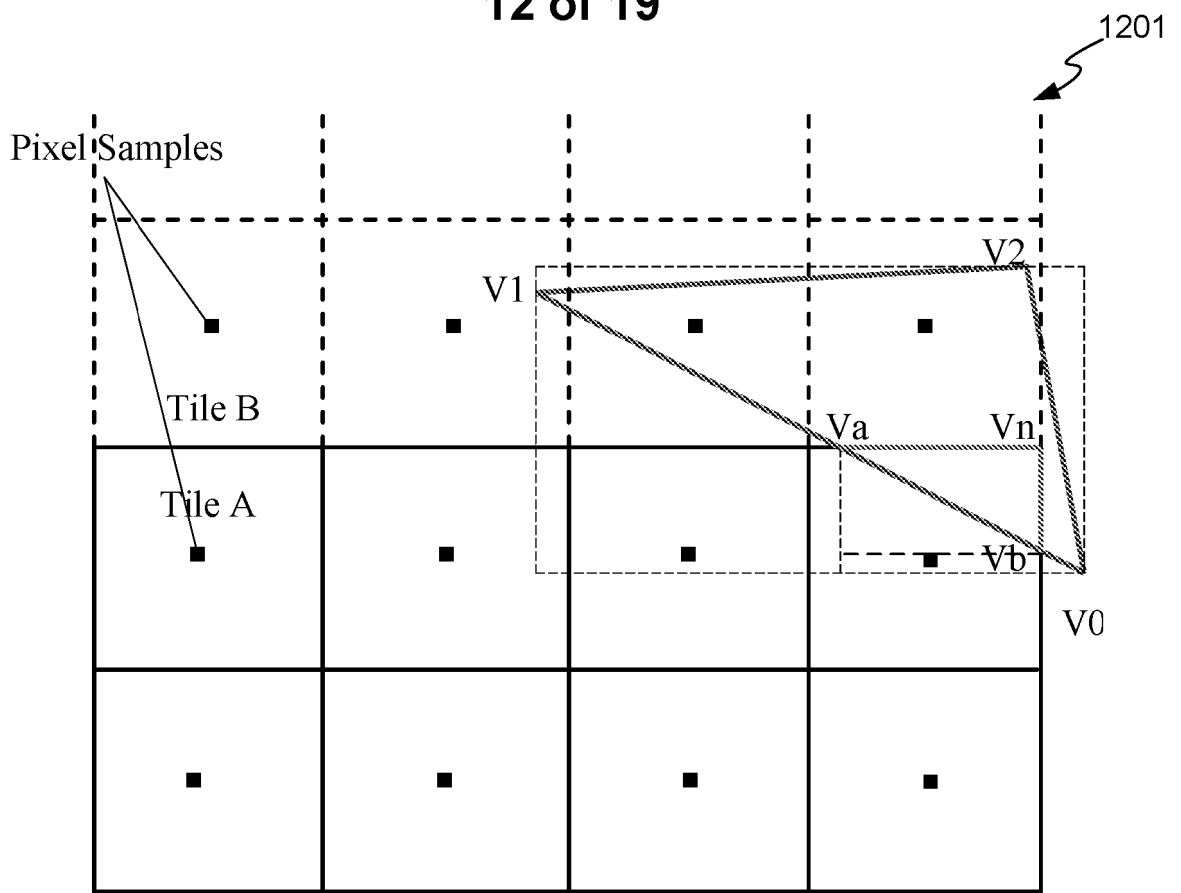


FIG. 12

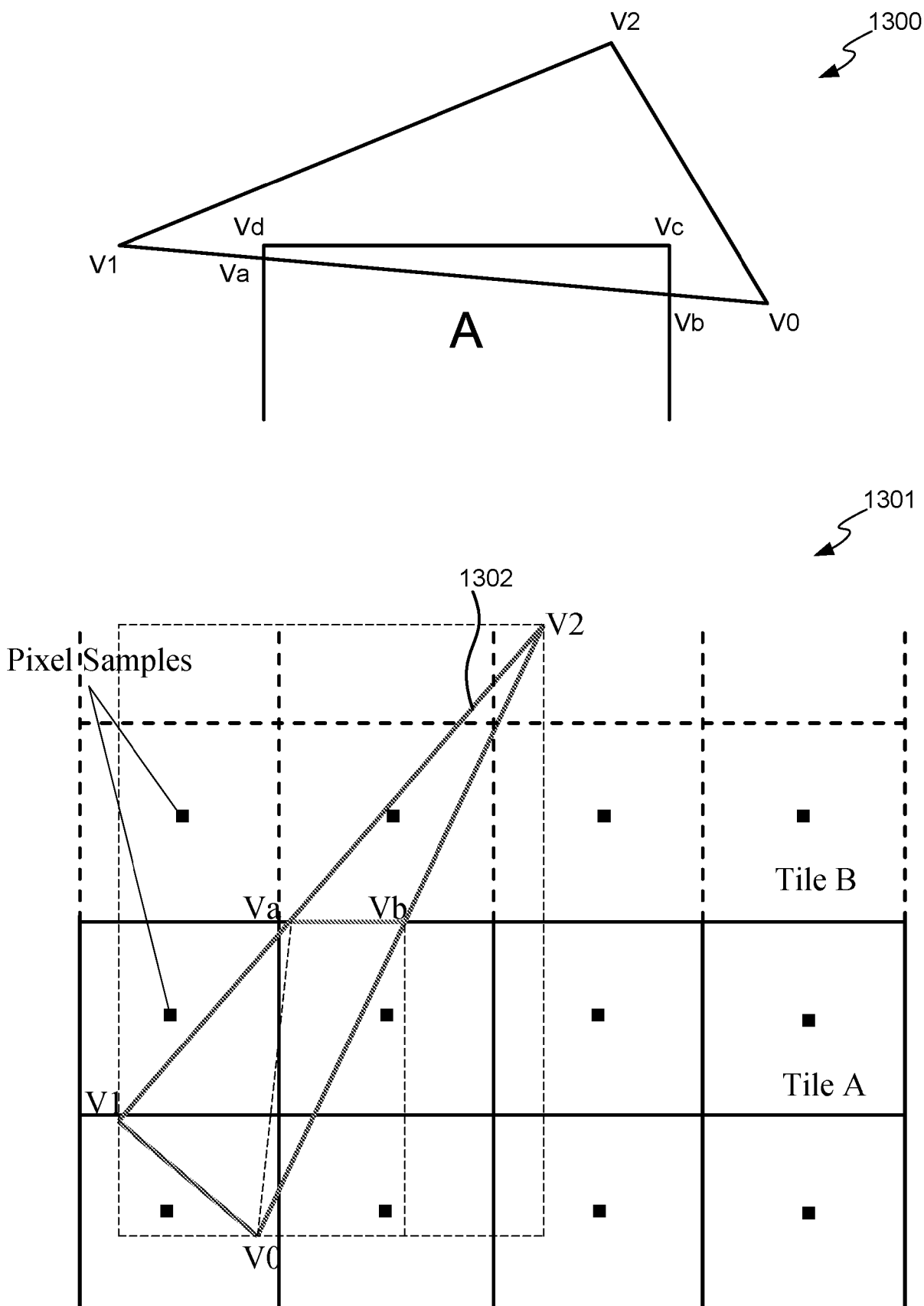


FIG. 13

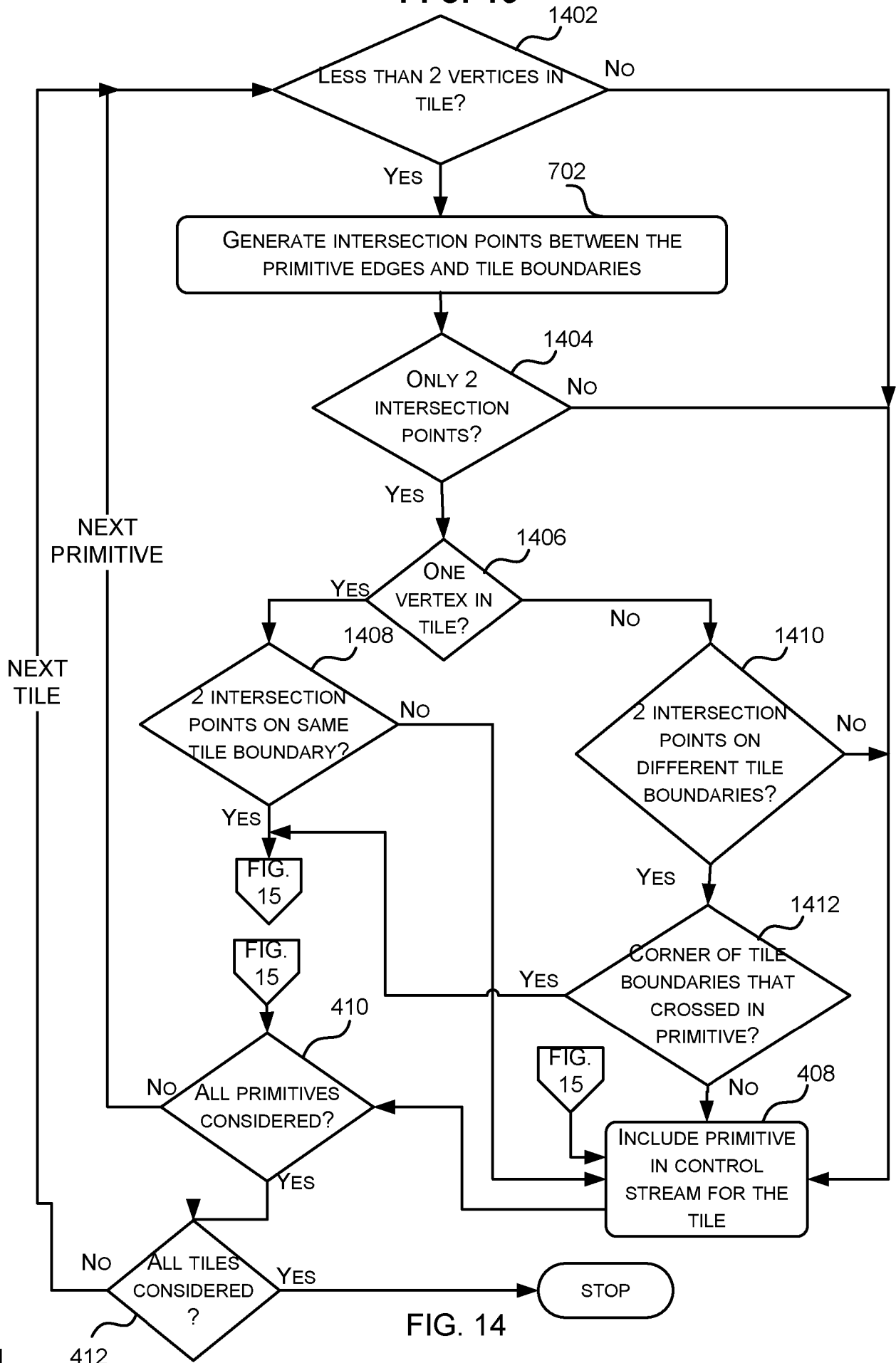


FIG. 14

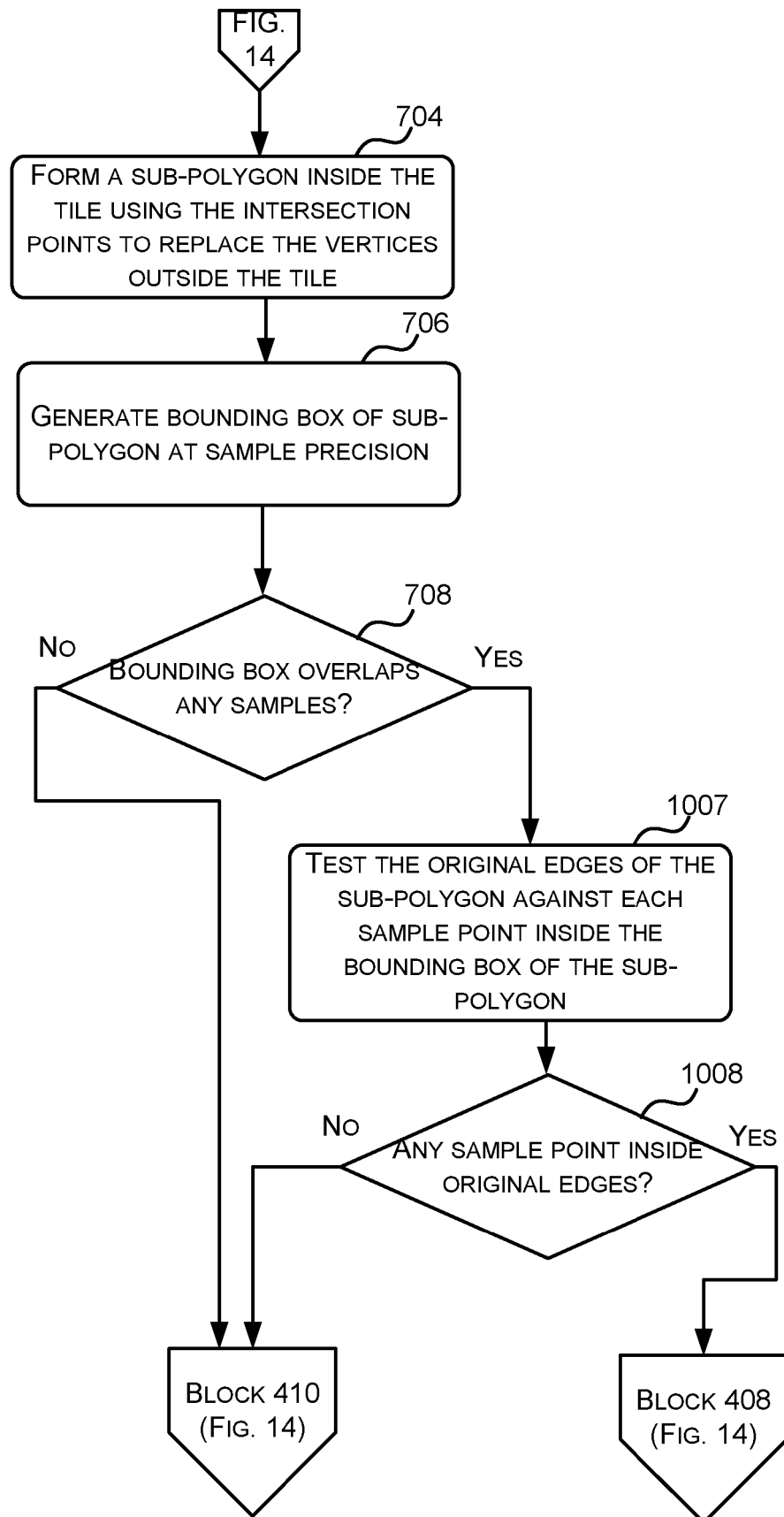


FIG. 15

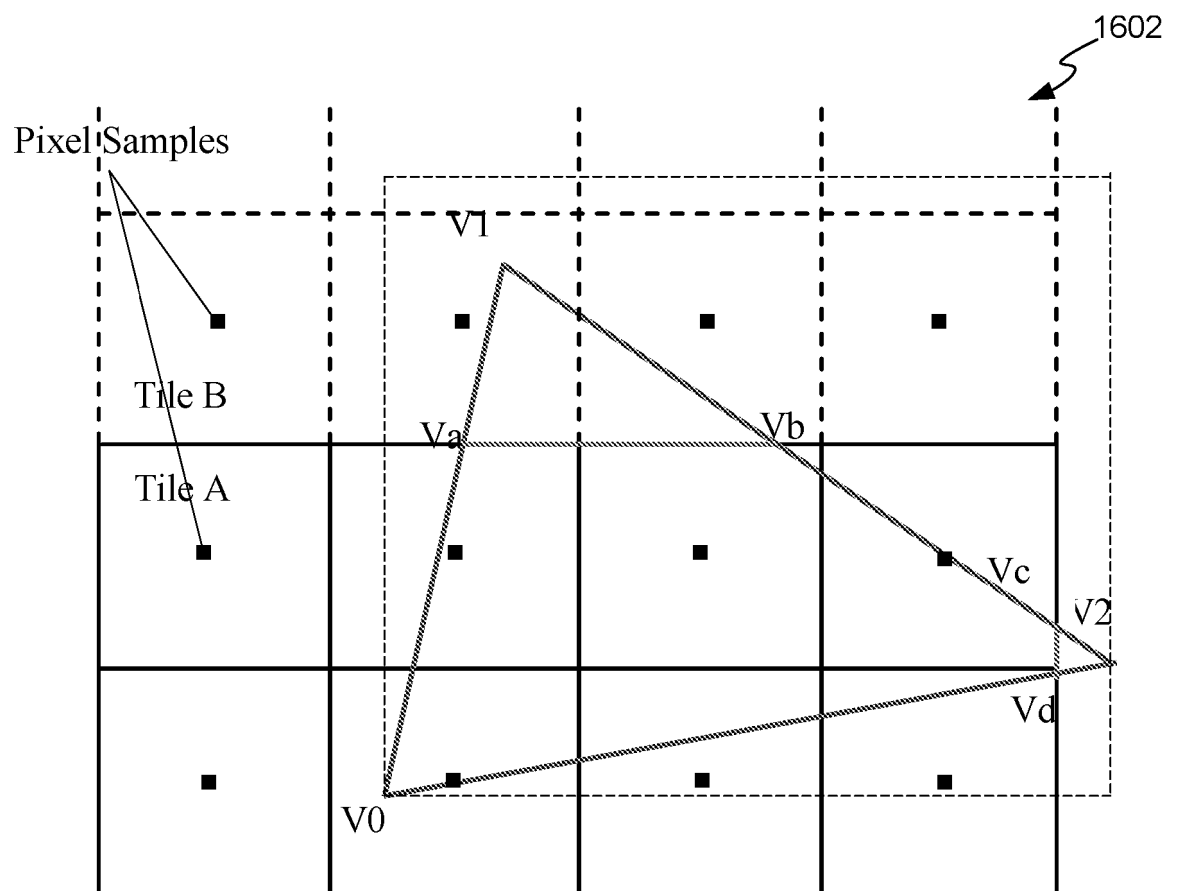
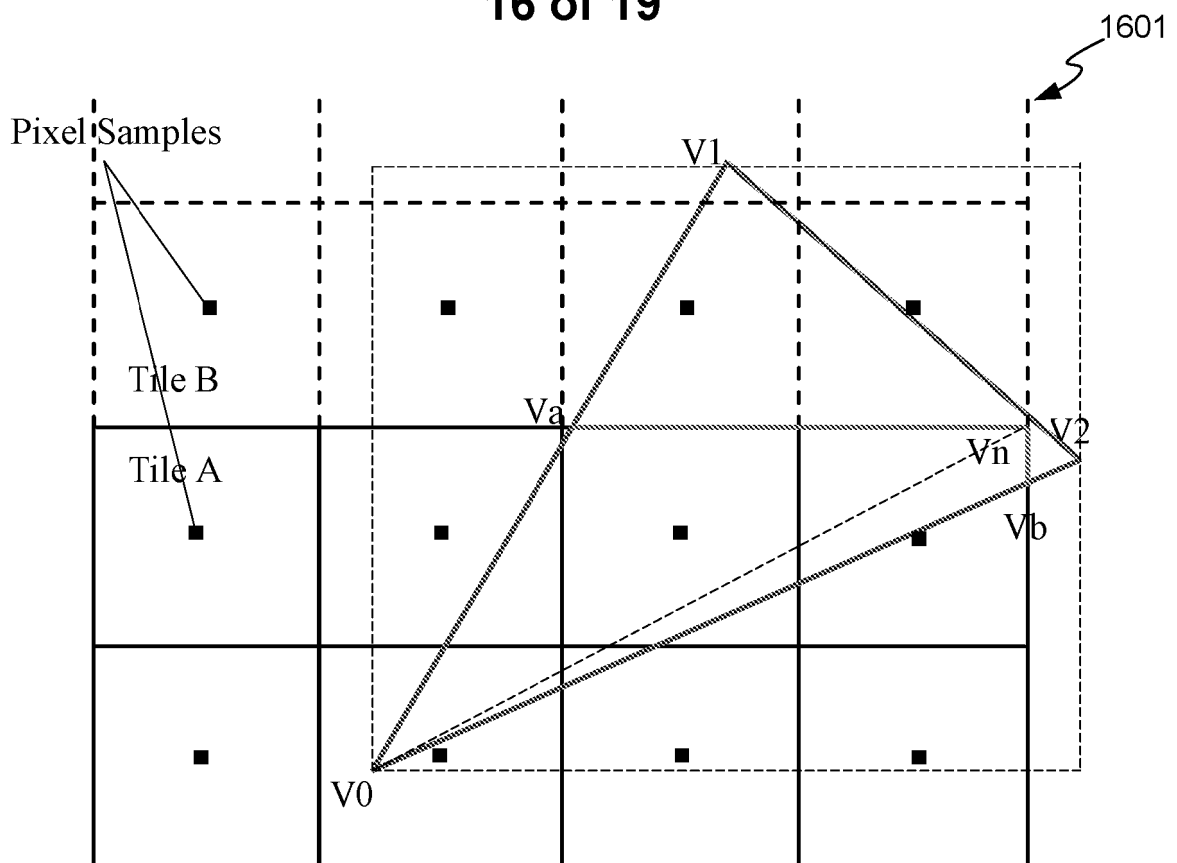


FIG. 16

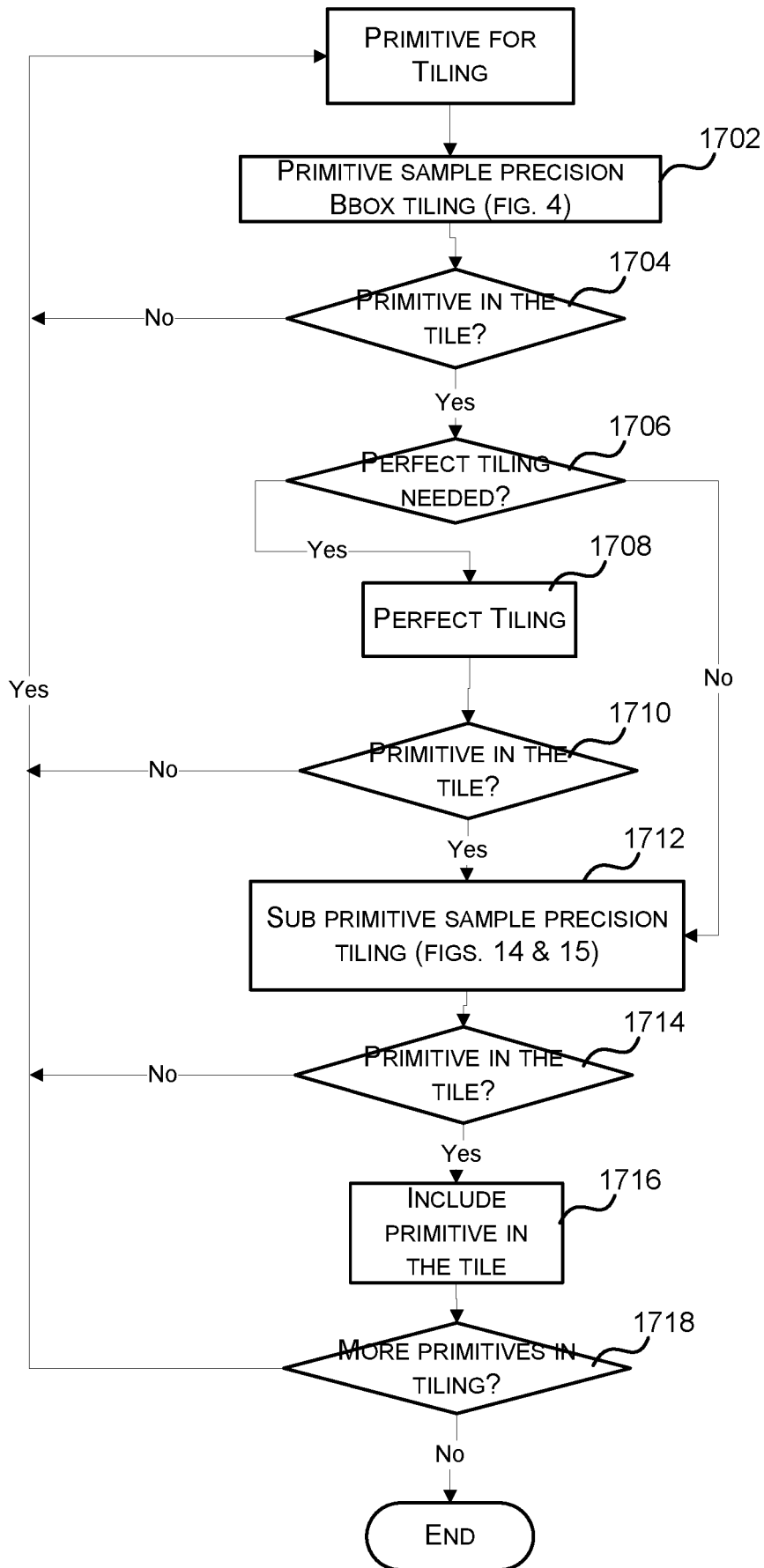


FIG. 17

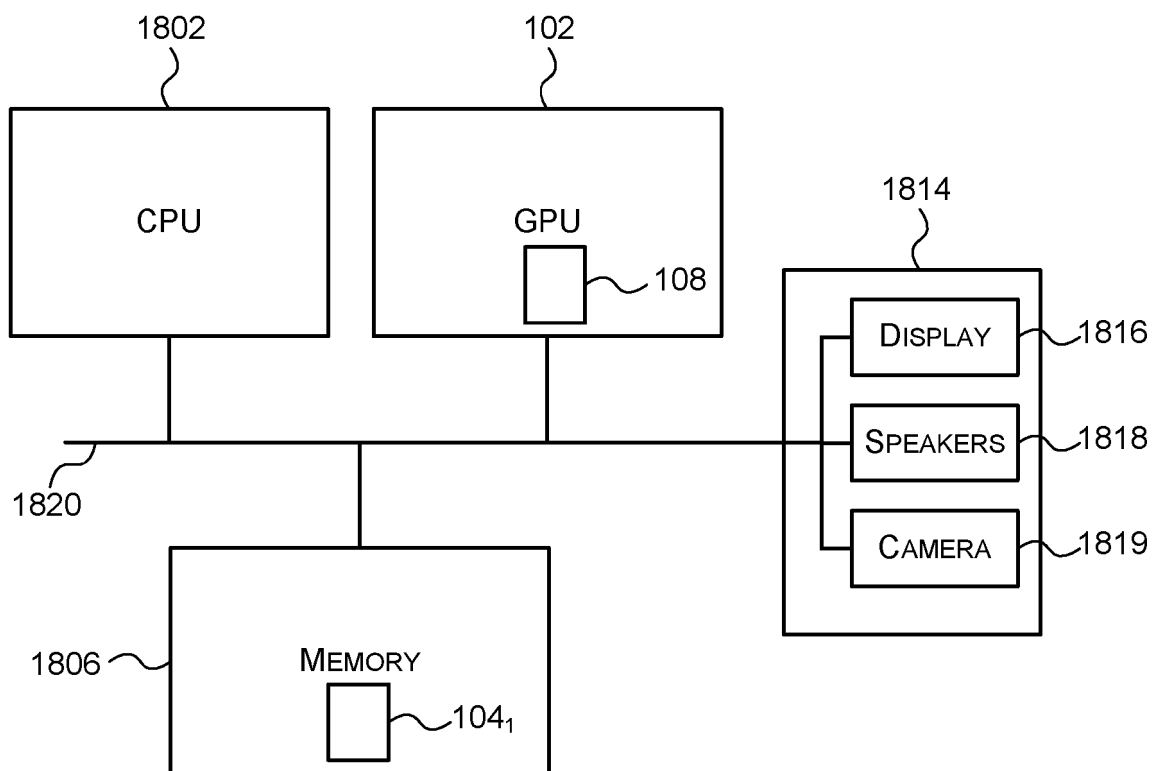


FIG. 18

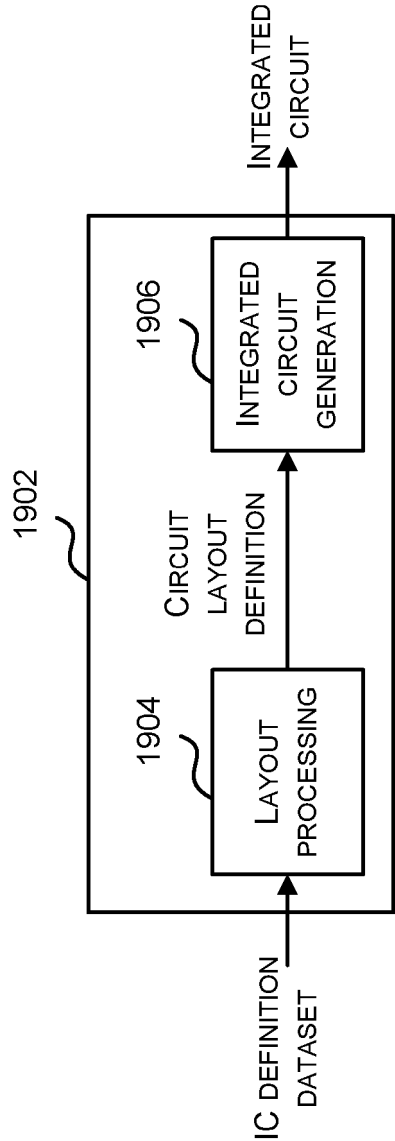


FIG. 19



The following terms are registered trade marks and should be read as such wherever they occur in this document:

Java (Page 37)

OpenCL (Page 37)

GENERATION OF A CONTROL STREAM FOR A TILE

Background

[0001] Graphics processing systems are used to process graphics data. For example, an application running on a computing system may need to render an image of a three dimensional (3D) scene for display to a user. The application can send graphics data to a graphics processing system to be rendered, wherein the graphics data describes primitives to be rendered. As is known in the art, primitives are usually convex polygons, such as triangles or convex quadrilaterals, wherein a primitive typically has its position in the rendering space of the graphics processing system defined by the position of its vertices, and may have its appearance defined by other attributes such as colour or texture attributes. An object in a scene may be represented by one or more primitives. As graphics processing systems progress, their capability to render complex images improves, and as such applications make use of this and provide more complex images for graphics processing systems to render. This means that the number of primitives in images tends to increase, so the ability of a graphics processing system to process the primitives efficiently becomes more important.

[0002] One known way of improving the efficiency of a graphics processing system is to render an image in a tile-based manner. In this way, the rendering space into which primitives are to be rendered is divided into a plurality of tiles, which can then be rendered independently from each other. In order to render primitives, a rendering unit uses memory to store intermediate results (e.g. depth values and primitive identifiers, etc.) for different sample positions. If the rendering unit operates on a tile at a time then most (or all) of this memory can be situated “on-chip”, i.e. on the Graphics Processing Unit (GPU), which might not be possible if the whole rendering space is rendered at once. Therefore, in a tile-based graphics system, the number of read and write operations between the GPU and an off-chip memory (i.e. which may be referred to as “system memory”) is

typically reduced compared to a non-tile-based graphics system. Since read and write operations between the GPU and the system memory are typically very slow and use lots of power (compared to operations performed within the GPU), tile-based graphics systems are often more efficient (in terms of power and speed) than non-tile-based graphics systems. A tile-based graphics system includes a tiling unit to tile the primitives. That is, the tiling unit determines, for a primitive, which of the tiles of a rendering space the primitive is in. Then, when a rendering unit renders the tile, it can be given information indicating which primitives should be used to render the tile.

[0003] For example, FIG. 1 shows some elements of a tile-based graphics processing system 100 which may be used to render an image of a 3D scene. The graphics processing system 100 comprises a graphics processing unit (GPU) 102 and two portions of memory 104₁ and 104₂. It is noted that the two portions of memory 104₁ and 104₂ may, or may not, be parts of the same physical memory, and both memories 104₁ and 104₂ may be situated “off-chip”, i.e. not on the same chip as the GPU 102. Communication between the memories (104₁ and 104₂) and the GPU 102 may take place over a communications bus in the system 100.

[0004] The GPU 102 comprises a pre-processing module 106, a tiling unit 108 and a rendering unit 110. The tiling unit 108 comprises processing logic 112 and a data store 114, and the rendering unit 110 comprises a hidden surface removal (HSR) module 116 and a texturing/shading module 118. The graphics processing system 100 is arranged such that graphics data describing a sequence of primitives provided by an application is received at the pre-processing module 106. The pre-processing module 106 performs functions such as geometry processing including clipping and culling to remove primitives which do not fall into a visible view. The pre-processing module 106 may also project the primitives into screen-space. The pre-processing module 106 outputs primitives to the tiling unit 108.

[0005] The tiling unit 108 receives the primitives from the pre-processing module 106 and determines which of the primitives are present within each of the tiles of the rendering space of the graphics processing system 100. A primitive may be in one or more of the tiles of the rendering space. The tiling unit 108 assigns primitives to tiles of the rendering space by creating display lists for the tiles, wherein the display list for a tile includes indications of primitives (i.e. primitive IDs) which are present in the tile. The display lists and the primitives are outputted from the tiling unit 108 and stored in the memory 104₁. The rendering unit fetches the display list for a tile and the primitives relevant to that tile from the memory 104₁, and the HSR module 116 performs hidden surface removal to thereby remove fragments of primitives which are hidden in the scene. The remaining fragments are passed to the texturing/shading module 118 which performs texturing and/or shading on the fragments to determine pixel colour values of a rendered image which can be passed to the memory 104₂ for storage in a frame buffer. The rendering unit 110 processes primitives in each of the tiles and when the whole image has been rendered and stored in the memory 104₂, the image can be outputted from the graphics processing system 100 and, for example, displayed on a display. In the example shown in FIG. 1, the tile-based graphics processing system 100 is a deferred rendering system, meaning that the rendering unit 110 performs hidden surface removal on a primitive fragment prior to performing texturing and/or shading on the primitive fragment in order to render the scene. However, in other examples, graphics processing systems might not be deferred rendering systems, such that texturing and/or shading is performed on a primitive fragment before hidden surface removal is performed on the primitive fragment.

[0006] FIG. 2 shows an example of a rendering space 202 which has been divided into an 8x12 array of tiles 204, wherein the tile in the mth row and the nth column is referred to as 204_{mn}. A primitive 206 is illustrated. The tiling unit 108 operates to determine which of the tiles 204 the primitive 206 is in. The primitive 206 is “in” a tile 204 if the primitive 206 at least partially overlaps with

the tile 204. The tiling unit 108 determines a bounding box 208 by finding the minimum and maximum x and y coordinates of the three vertices of the primitive 206 and forming the bounding box 208 from those coordinates. The tiling unit 108 can thereby determine that the primitive 206 is not in any of the tiles 204 which are not in the bounding box 208. A tile 204 is “in” the bounding box 208 if the tile 204 at least partially overlaps with the bounding box 208. In some examples, the bounding box may be determined at tile-resolution, whereby the bounding box may be increased in size such that the edges of the bounding box fall on tile boundaries. In FIG. 2, the tiles which are dotted (i.e. the top and bottom rows of tiles, the first column and the last two columns of tiles of the rendering space 202) are outside of the bounding box 208 and therefore, on that basis, the tiling unit 108 can determine that the primitive 206 is not in those tiles. In a very simple implementation, the tiling unit 108 might simply indicate that the primitive is in all of the tiles in the bounding box 208. However, this means that the primitive is indicated as being in some tiles which it is not actually in. This can lead to additional memory consumption due to the storage of unnecessary primitives and/or primitive IDs in memory 104₁, and inefficiencies in the rendering unit 110 as primitives are read from memory 104₁ and are processed for tiles in which they are not visible. Therefore, it is generally preferable for the tiling unit 108 to determine which of the tiles in the bounding box 208 the primitive is in.

[0007] For each tile in the bounding box 208 (e.g. each of the white tiles in FIG. 2) tiling calculations can be performed to determine whether the primitive 206 is in the tile. For example, the tiling calculations to determine whether the primitive 206 is in a tile 204 might include calculations for each edge of the primitive. For example, as illustrated in FIG. 3, equations representing edge lines (302₁, 302₂ and 302₃) defining the edges of the primitive 206 are determined using the locations of the vertices (304₁, 304₂ and 304₃) of the primitive 206. Then for each edge line 302, a test can be performed to determine whether a tile 204 is inside or outside the respective edge line 302 by comparing a position of a test point in the tile with the equation of the edge

line 302. The test point in the tile may be different for testing with respect to different edges, i.e. the test point may be edge-specific. For example, for testing whether a tile is inside edge line 302₁ the test point is in the bottom left of the tile; for testing whether a tile is inside edge line 302₂ the test point is in the top left of the tile; and for testing whether a tile is inside edge line 302₃ the test point is in the bottom right of the tile. If it is determined that the tile is inside all of the edge lines 302 then it is determined that the primitive is in the tile. However, if it is determined that the tile is outside any of the edge lines 302 then it is determined that the primitive is not in the tile.

[0008] The tiling calculations may be performed for each of the tiles in the bounding box 208 in order to determine whether the primitive is in the respective tiles. For each edge of the primitive, and for each tile in the bounding box, the comparison of the position of the edge-specific test point in the tile with the equation of the appropriate edge line typically involves performing one or more floating point operations. Floating point operations are costly to perform (in terms of time and power consumption). This may cause a problem, particularly due to the tendency for the number of primitives in an image to increase, because the number of floating point operations involved in the tiling process may become large enough to significantly detrimentally affect the performance of the graphics processing system 100. Therefore, it would generally be beneficial to reduce the time and power that is consumed in the tiling process.

[0009] The embodiments described below are provided by way of example only and are not limiting of implementations which solve any or all of the disadvantages of known method for tile-based rendering.

Summary

[0010] This Summary is provided to introduce a selection of concepts in a simplified form that are further described below in the Detailed Description. This Summary is not intended to identify key features or essential features of

the claimed subject matter, nor is it intended to be used to limit the scope of the claimed subject matter.

[0011] A method of determining associations between tiles and primitives within a tiling unit of a graphics processing system is described. The method comprises determining whether a primitive falls within a tile based on positions of samples within pixels in the tile. If it is determined that the primitive does fall within a tile based on the positions of samples within pixels in the tile, data can be stored to indicate which of the tiles the primitives is determined to be in. For example, if it is determined that the primitive does fall within a tile, an identifier for the primitive may be added to a control stream for the tile and if it is determined that the primitive does not fall within the tile, the identifier for the primitive is not added to the control stream for the tile. In alternative examples, the associations between primitives and tiles may be stored in different ways. For example, in some alternative examples, a list of tiles could be stored for each primitive, wherein the list of tiles for a primitive includes tile IDs of the tiles in which the primitive is present. Various different methods are described to make the determination and these may be used separately or in any combination.

[0012] A first aspect provides a method of processing primitives within a tiling unit of a graphics processing system, the method comprising: determining whether a primitive that covers at least one sample position in a rendering space falls within a tile based on positions of samples within pixels in the tile; and in response to determining that a primitive that covers at least one sample position in a rendering space does fall within a tile based on the positions of samples within pixels in the tile, storing an association between the tile and the primitive to indicate that the primitive is present in the tile.

[0013] A second aspect provides a graphics processing system comprising a tiling unit for processing primitives for each of a plurality of tiles, the tiling unit being configured to: determine whether a primitive that covers at least one sample position in a rendering space falls within a tile based on positions of

samples within pixels in the tile; and cause an association between the tile and the primitive to be stored to indicate that the primitive is present in the tile in response to determining that the primitive that covers at least one sample position in a rendering space does fall within the tile based on the positions of samples within pixels in the tile.

[0014] A third aspect provides an integrated circuit manufacturing system comprising: a non-transitory computer readable storage medium having stored thereon a computer readable description of an integrated circuit that describes a graphics processing system; a layout processing system configured to process the integrated circuit description so as to generate a circuit layout description of an integrated circuit embodying the graphics processing system; and an integrated circuit generation system configured to manufacture the graphics processing system according to the circuit layout description, wherein the graphics processing system comprises a tiling unit for processing primitives for each of a plurality of tiles, the tiling unit being configured to: determine whether a primitive that covers at least one sample position in a rendering space falls within a tile based on positions of samples within pixels in the tile; and cause an association between the tile and the primitive to be stored to indicate that the primitive is present in the tile in response to determining that a primitive that covers at least one sample position in a rendering space does fall within a tile based on the positions of samples within pixels in the tile.

[0015] The graphics processing system which implements one or more of the methods described herein may be embodied in hardware on an integrated circuit. There may be provided a method of manufacturing, at an integrated circuit manufacturing system, a graphics processing system which implements one or more of the methods described herein. There may be provided an integrated circuit definition dataset that, when processed in an integrated circuit manufacturing system, configures the system to manufacture a graphics processing system which implements one or more of the methods described herein. There may be provided a non-transitory

computer readable storage medium having stored thereon a computer readable description of an integrated circuit that, when processed, causes a layout processing system to generate a circuit layout description used in an integrated circuit manufacturing system to manufacture a graphics processing system which implements one or more of the methods described herein.

[0016] There may be provided an integrated circuit manufacturing system comprising: a non-transitory computer readable storage medium having stored thereon a computer readable integrated circuit description that describes the graphics processing system which implements one or more of the methods described herein; a layout processing system configured to process the integrated circuit description so as to generate a circuit layout description of an integrated circuit embodying the graphics processing system which implements one or more of the methods described herein; and an integrated circuit generation system configured to manufacture the graphics processing system which implements one or more of the methods described herein according to the circuit layout description.

[0017] There may be provided computer program code for performing a method as described herein. There may be provided non-transitory computer readable storage medium having stored thereon computer readable instructions that, when executed at a computer system, cause the computer system to perform the method as described herein.

[0018] The above features may be combined as appropriate, as would be apparent to a skilled person, and may be combined with any of the aspects of the examples described herein.

Brief Description of the Drawings

[0019] Examples will now be described, in detail, with reference to the accompanying drawings, in which:

[0020] FIG. 1 is a schematic diagram of a graphics processing system;

[0021] FIG. 2 shows a primitive in tiles of a rendering space;

[0022] FIG. 3 illustrates edge lines which define the edges of a primitive;

[0023] FIG. 4 is a flow diagram of a first example method of generating control streams for tiles in a tiling unit of a GPU;

[0024] FIG. 5 is a schematic diagram showing an example primitive and its position with reference to one or more tiles;

[0025] FIG. 6 is a schematic diagram showing sample positions within a pixel;

[0026] FIG. 7 is a flow diagram of a second example method of generating control streams for tiles in a tiling unit of a GPU;

[0027] FIG. 8 is a schematic diagram showing an example primitive and its position with reference to one or more tiles;

[0028] FIG. 9 is a flow diagram of a method of assessing a primitive and parts of the method may be used in the methods of FIGs. 7 and 10;

[0029] FIG. 10 is a flow diagram of a third example method of generating control streams for tiles in a tiling unit of a GPU;

[0030] FIG. 11 is a schematic diagram showing an example primitive and its position with reference to one or more tiles;

[0031] FIG. 12 is a schematic diagram showing example primitives and their position with reference to one or more tiles;

[0032] FIG. 13 is a schematic diagram showing example primitives and their position with reference to one or more tiles;

[0033] FIG. 14 is a flow diagram of part of a fourth example method of generating control streams for tiles in a tiling unit of a GPU;

[0034] FIG. 15 is a flow diagram of part of a fourth example method of generating control streams for tiles in a tiling unit of a GPU;

[0035] FIG. 16 is a schematic diagram showing example primitives and their position with reference to one or more tiles;

[0036] FIG. 17 is a flow diagram of a fifth example method of generating control streams for tiles in a tiling unit of a GPU;

[0037] FIG. 18 shows a computer system in which a graphics processing system is implemented; and

[0038] FIG. 19 shows an integrated circuit manufacturing system for generating an integrated circuit embodying a graphics processing system.

[0039] The accompanying drawings illustrate various examples. The skilled person will appreciate that the illustrated element boundaries (e.g., boxes, groups of boxes, or other shapes) in the drawings represent one example of the boundaries. It may be that in some examples, one element may be designed as multiple elements or that multiple elements may be designed as one element. Common reference numerals are used throughout the figures, where appropriate, to indicate similar features.

Detailed Description

[0040] The following description is presented by way of example to enable a person skilled in the art to make and use the invention. The present invention is not limited to the embodiments described herein and various modifications to the disclosed embodiments will be apparent to those skilled in the art. Embodiments will now be described by way of example only.

[0041] As described above, a tiling unit within a GPU receives the primitives and determines which of the primitives are present within each of the tiles of the rendering space of the graphics processing system. The tiling unit outputs data which can be used to indicate which of the tiles a primitive is in. If a

primitive is determined to be present in a tile then an association between the primitive and the tile is stored, thereby indicating that the primitive is present in the tile. In most of the examples described herein the tiling unit outputs a control stream (which may also be referred to as a control list or display list) for each tile, where a control stream comprises one or more primitive identifiers (IDs) for primitives which are present in the tile. However, it is to be understood that in some other examples, the data indicating the associations between primitives and tiles (i.e. which primitives are present in which tiles) could take a different form, e.g. for each primitive a list of tile IDs indicating the tiles in which the primitive is present could be stored. This alternative way of storing the associations between primitives and tiles could be particularly useful in an immediate mode renderer.

[0042] Described herein are a number of methods for determining whether to include a primitive ID in the control stream for a tile and these methods may be implemented independently of each other, or any two or more of these methods may be implemented together. The methods (which may also be referred to as methods for forming the control streams) may be implemented within a tiling unit and an improved tiling unit (which implements any one or more of the methods) is also described herein.

[0043] The methods described herein determine whether a primitive falls within a tile based on the positions of a plurality of sample points within pixels in the tile. The analysis based on the positions of sample points per tile (where there may be one or more sample points per pixel) as described herein reduces the number of primitive IDs that are included in a control stream for a tile but are subsequently discarded in the rendering unit (e.g. during rasterization) after they have been fetched from memory. The rendering unit is configured to determine rendered values at the sample positions within a tile, and a primitive may be relevant to the rendering at a sample position if the primitive overlaps the sample position.

[0044] Where two or more of the methods described herein are combined, only those primitives that are identified as needing to be added to the control stream for a tile in a first method (i.e. those primitives which are not excluded from the control stream using the first method) are fed into the next method (e.g. as members of a set of candidate primitives). Once a method has identified that a primitive does not need to be added to a control stream for a tile, no further analysis of the primitive is performed. An exception to this is where a primitive is divided into a plurality of sub-polygons and in such examples, each sub-polygon is tested individually. Once a method has identified based on one of the plurality of sub-polygons that the sub-polygon does not need to be added to a control stream for a tile, no further analysis of that sub-polygon is performed; however, the ID for the primitive may still be added to the control stream for the tile as a consequence of analysis of another of the sub-polygons formed from the primitive. A primitive divided into a plurality of sub-polygons is added to the control stream for a tile if any one or more of the sub-polygons is needed in the tile.

[0045] Those primitives which are initially included in a control stream of a tile but are then fetched and discarded in the rendering unit (e.g. during rasterization) may be referred to as 'non-contributing primitives' or 'invisible primitives' as they have no effect on the rendered output of the tile. The methods and apparatus described herein reduce the number of non-contributing primitives which are included in a control stream for a tile.

[0046] By reducing the number of non-contributing primitives included in a control stream for a tile using the methods described herein, unnecessary workload in the rendering unit is reduced (i.e. the rendering unit fetches fewer non-contributing primitives so the amount of data transferred between the GPU and the system memory is reduced) and as triangle-size reduces, the proportional saving in processing load increases. Experimental results have shown that by using the three methods described herein together (e.g. as shown in FIG. 17), the number of primitives included in control streams can be reduced and the percentage of non-contributing primitives fetched and then

discarded by the rendering unit can be reduced by a factor of the order of 10 in some examples (with the most significant improvements being seen in examples where there were many small primitives).

[0047] The graphics processing system 100 shown in FIG. 1 may be used to implement methods of the examples described herein. As described above, the graphics processing system 100 is a tile-based deferred rendering graphics processing system which includes a GPU 102 and two portions of memory 104₁ and 104₂. As mentioned above, the two portions of memory 104₁ and 104₂ may, or may not, be parts of the same physical memory, and both memories 104₁ and 104₂ may be situated “off-chip”, i.e. not on the same chip as the GPU 102. Communication between the memories (104₁ and 104₂) and the GPU 102 may take place over a communications bus in the system 100. The GPU 102 comprises a pre-processing module 106, a tiling unit 108 and a rendering unit 110. The tiling unit 108 comprises processing logic 112 and a data store 114, and the rendering unit 110 comprises a hidden surface removal (HSR) module 116 and a texturing/shading module 118.

[0048] In operation, the graphics processing system 100 receives graphics data (e.g. from an application) describing a sequence of primitives. The pre-processing module 106 performs functions such as geometry processing including clipping and culling to remove primitives which do not fall into a visible view. The pre-processing module 106 may also project the primitives into screen-space. The pre-processing module 106 outputs primitives to the tiling unit 108.

[0049] The tiling unit 108 determines which of the primitives are present within each of the tiles of the rendering space of the graphics processing system 100. The processing logic 112 of the tiling unit 108 performs the operations of the tiling unit 108 (including determining whether to include a primitive ID in the control stream for a tile using one or more of the methods described herein), and the data store 114 stores data of intermediate results of the tiling

process, such as results of tiling calculations and partially filled control streams. The processing logic 112 may be implemented in dedicated hardware designed specifically for performing the operations of the tiling unit 108. Alternatively, the processing logic 112 may be implemented by executing software on a processor wherein the software is written such that when it is executed it causes the processor to perform the operations of the tiling unit 108.

[0050] In various examples, once all of the primitives for a render have been tiled then the control streams are complete and they are passed to the off-chip memory 104₁ for storage therein. In other examples, the tiling unit 108 might not use an internal store (such as store 114) to store control streams, and instead primitive identifiers may be written directly to control streams in memory 104₁ as tiling is performed. Furthermore, in some further examples, the internal store 114 may be implemented in the tiling unit 108, but the internal store 114 might not be big enough to store all of the control streams for all of the tiles at once. Therefore, the internal store 114 may be used to gather tiling results that can then be written out to memory 104₁ in chunks (or “batches”) as the tiling is performed. This can avoid inefficient memory access patterns when primitives are written to different control streams in memory 104₁.

[0051] The rendering unit 110 can then render the primitives in each of the tiles in accordance with the control streams. In order to render the primitives for a tile, the rendering unit 110 retrieves the control stream from the memory 104₁ for the tile. The rendering unit 110 can then retrieve the primitives indicated by the control stream as being in the tile currently being rendered. These primitives may be retrieved from the memory 104₁. The rendering unit 110 then renders the primitives in the tile. In the example shown in FIG. 1, the rendering unit 110 implements deferred rendering whereby hidden surface removal is performed before texturing and/or shading, but in other examples non-deferred rendering may be implemented. The rendered result is then output and can be passed to the memory 104₂ for storage, e.g. in a frame

buffer. The rendering unit 110 processes primitives in each of the tiles and when the whole image has been rendered and stored in the memory 104₂, the image can be outputted from the graphics processing system 100 and, for example, displayed on a display.

[0052] A first method of determining whether a primitive should be associated with a tile (e.g. whether a primitive ID should be added to a control stream for a tile) can be described with reference to FIGs. 4-6. As described above, this method may be implemented in a tiling unit 108.

[0053] As shown in the flow diagram of FIG. 4, a bounding box 506 of a tile 508 is generated at sample precision (block 402) and this is shown graphically in the first diagram 51 in FIG. 5. As shown in FIG. 5, all the samples 502 in a tile 508 form a bounding box 506 that is smaller than the tile borders and this bounding box 506 may be referred to as the 'restricted sample bounding box' in a tile. The sample points may, for example, be at 1/16 pixel precision in 16.4 fixed point format (i.e. with 16 integer bits followed by 4 fractional bits), while the representation of X and Y coordinates on screen may be in 16.8 fixed point format (i.e. with 16 integer bits followed by 8 fractional bits).

[0054] The method then considers each primitive in a set of candidate primitives (which comprise all primitives or alternatively, the set may be a proper subset of a set comprising all primitives) and for each primitive 510 in the set, generates a bounding box 512 of the primitive at the sample precision being used (block 404), e.g. in 16.8 fixed point format. It is then determined if the two bounding blocks 506, 512 overlap (block 406) and if they overlap ('Yes' in block 406), the ID for the primitive 510 is added to the control stream for the tile (block 408).

[0055] As shown in FIG. 4, the method may iterate through each primitive in the set of candidate primitives to generate a control stream for a tile and then once all primitives in the set have been considered for a particular tile ('Yes' in block 410), the method may be repeated until a control stream has been

generated for every tile ('Yes' in block 412). It will be appreciated, however, that aspects of the method may be performed in parallel (e.g. some or all of the tiles may be considered in parallel) and the set of candidate primitives may be the same for all tiles (e.g. where the candidate set comprises all primitives) or may be different for different tiles or groups of tiles. The method could alternatively iterate through each tile to add a primitive to each tile control stream where needed and then once all the tiles have been considered for a particular primitive the method may be repeated until all the primitives have been considered.

[0056] Using the method shown in FIG. 4, the primitive 510 is not added to the control stream for either of tiles A and B. This is in contrast to known methods which would add the ID of the primitive to the control stream for both tile A and tile B (because the bounding box 512 overlaps with the tile areas for tile A (denoted 508) and tile B) even though the bounding box of the primitive does not cover any sample point in the tile.

[0057] The generation of the bounding box of a tile at sample precision (in block 402) may be determined based on the distances between the samples inside a pixel and the boundary of the pixel and this is shown in more detail in the second diagram 52 in FIG. 5. As shown in FIG. 5, Delta Xl (which may also be written ΔX_l) is the distance between the left boundary of a pixel and the minimum X value of all the samples inside the pixel, Delta Xr (which may also be written ΔX_r) is the distance between the right boundary of a pixel and the maximum X value of all the samples inside the pixel. Similarly Delta Yt (which may also be written ΔY_t) is the distance on the top pixel boundary and Delta Yb (which may also be written ΔY_b) is the distance on the bottom pixel boundary. Although FIG. 5 shows multiple sample positions per pixel, in other examples there may only be a single sample position per pixel.

[0058] Given tile boundaries defined by four parameters which define the maximum and minimum extent of the tile along two perpendicular axes (X and Y) that are TileXmin, TileXmax, TileYmin, TileYmax, (i.e. such that the four

corners of the tile have coordinates (TileXmin, TileYmax), (TileXmax, TileYmax), (TileXmax, TileYmin) and (TileXmin, TileYmin)) all in pixel precision (integer format), the bounding box of a tile at sample precision (e.g. 16.8 format) is defined by four parameters: TileXmin+Delta Xl, TileXmax-Delta Xr, TileYmin + Delta Yt, TileYmax – Delta Yb, which define the maximum and minimum extent of the bounding box of the tile at sample precision along the two perpendicular axes.

[0059] If the bounding box of a primitive at sample precision (as determined in block 404) is defined by four parameters PrimXmin, PrimXmax, PrimYmin, PrimYmax (which again define the maximum and minimum extent of the bounding box along the two perpendicular axes), then the bounding boxes do not overlap ('No' in block 406), i.e. the primitive is not considered to be in the tile, if:

PrimXmax < (TileXmin + Delta Xl) or
PrimXmin > (TileXmax - Delta Xr) or
PrimYmax < (TileYmin + Delta Yt) or
PrimYmin > (TileYmax - Delta Yb)

[0060] The elimination of primitives from a control stream using the method shown in FIG. 4 is performed without having to calculate the edge equations of any of the primitives. Where this method is used in combination with other methods (e.g. known methods and/or other methods described herein), it may be used first to eliminate one or more primitives and so avoid the computational effort that would otherwise be performed to calculate the edge equations of a primitive which is ultimately discarded because it has no effect on the rendered output (e.g. as shown in FIG. 17).

[0061] In the examples shown in FIG. 5, the number of samples 502 and the sample positions within each pixel 504 are the same. The method of FIG. 4 may still be used if the number of samples and/or sample positions differs between pixels, as can be described with reference to FIG. 6. In the example

shown in FIG. 6, the "worst case" sample positions are used, i.e. a bounding box at sample precision 602 is defined which is guaranteed to encompass all of the sample positions in all of the pixels in the tile and then the bounding boxes do not overlap ('No' in block 406), i.e. the primitive is not considered to be in the tile, if:

$$\begin{aligned} \text{PrimXmax} &< (\text{TileXmin} + \Delta X_{l_{\min}}) \text{ or} \\ \text{PrimXmin} &> (\text{TileXmax} - \Delta X_{r_{\min}}) \text{ or} \\ \text{PrimYmax} &< (\text{TileYmin} + \Delta Y_{t_{\min}}) \text{ or} \\ \text{PrimYmin} &> (\text{TileYmax} - \Delta Y_{b_{\min}}) \end{aligned}$$

Where:

$$\begin{aligned} \Delta X_{l_{\min}} &= \min (L_1, L_2, \dots) \\ \Delta X_{r_{\min}} &= \min (R_1, R_2, \dots) \\ \Delta Y_{t_{\min}} &= \min (T_1, T_2, \dots) \\ \Delta Y_{b_{\min}} &= \min (B_1, B_2, \dots) \end{aligned}$$

Where L_x , R_x , T_x , B_x are the distances from a sample position x to each of the edges of the pixel (as shown in FIG. 6).

[0062] In an alternative to the method shown in FIG. 6, if there are different proper subsets of pixels with different numbers of samples and/or different sample positions, multiple bounding boxes for a tile at sample precision may be generated (in block 402), i.e. one for each proper subset, and then the bounding boxes do not overlap ('No' in block 406), i.e. the primitive is not considered to be in the tile, if:

$$\begin{aligned} \text{PrimXmax} &< (\text{TileXmin} + \Delta X_{l_x}) \text{ or} \\ \text{PrimXmin} &> (\text{TileXmax} - \Delta X_{r_x}) \text{ or} \\ \text{PrimYmax} &< (\text{TileYmin} + \Delta Y_{t_x}) \text{ or} \\ \text{PrimYmin} &> (\text{TileYmax} - \Delta Y_{b_x}) \end{aligned}$$

where ΔX_{l_x} , ΔX_{r_x} , ΔY_{t_x} , ΔY_{b_x} are the values for subset X .

[0063] A second method of determining whether a primitive should be associated with a tile (e.g. whether a primitive ID should be added to a control stream for a tile) can be described with reference to FIGs. 7-9. This method requires additional processing compared to the method described above with reference to FIGs. 4-6, but results in additional non-contributing primitives not being added to the control stream. As described below, the two methods may be used together (e.g. the candidate set of primitives considered by the second method may comprise only those primitives that are identified as needing to be added to the control stream for a tile in the first method). The method may be implemented in a tiling unit 108.

[0064] As shown in the flow diagram of FIG. 7, the intersection points between the edges of a primitive (e.g. a triangle) are generated (block 702). Referring to the primitive 802 (with vertices V0, V1, V2) shown in FIG. 8, these intersection points are Va and Vb. Line equations of the edges of the primitive (e.g. the triangle) may be used to generate the intersection points between triangle edges and tile boundaries (in block 702). Although the method is described with reference to primitives which are triangles, the method may also be used for other primitive types (e.g. quads and lines).

[0065] Referring to the example shown in FIG. 8, the equation of the edge between V0 and V1 may have the form $Ax + By + C = 0$. When the edge crosses the left tile boundary $X_{tileleft}$, then the coordinates of the intersection point are:

$$X_{intersec} = X_{tileleft}$$

$$Y_{intersec} = -(C + A * X_{tileleft}) / B$$

When the edge crosses the right tile boundary $X_{tileright}$, then the coordinates of the intersection point are:

$$X_{intersec} = X_{tileright}$$

$$Y_{intersec} = -(C + A * X_{tileright}) / B$$

When the edge crosses the top tile boundary $Y_{tiletop}$, then the coordinates of the intersection point are:

$$X_{intersec} = - (C + B * Y_{tiletop}) / A$$

$$Y_{intersec} = Y_{tiletop}$$

When the edge crosses the bottom tile boundary $Y_{tilebottom}$, then the coordinates of the intersection point are:

$$X_{intersec} = - (C + B * Y_{tilebottom}) / A$$

$$Y_{intersec} = Y_{tilebottom}$$

[0066] Once the intersection points have been generated (in block 702), a sub-polygon is then formed inside the tile using the intersection points to replace the vertices outside the tile (block 704). Referring again to the example shown in FIG. 8, intersection point V_a replaces vertex V_1 and intersection point V_b replaces vertex V_2 as both V_1 and V_2 are outside Tile A.

[0067] A bounding box 804 for the sub-polygon (with vertices V_0 , V_a , V_b) is generated at sample precision (block 706) and this sample precision bounding box of the sub-polygon is tested against the sample positions in the tile (block 708). Only if the bounding box of the sub-polygon 804 overlaps at least one sample position ('Yes' in block 708), is the ID for the primitive 802 added to the control stream for the tile (block 408), thereby associating the primitive 802 with the tile.

[0068] The determination (in block 708) of whether the bounding box of the sub-polygon overlaps any of the samples may be performed using part of a method described in GB Patent No. 2401522 and shown in FIG. 9 (which corresponds to FIG. 10 in GB2401522). Four pixel sampling locations in the tile $\{S_{00}, S_{01}, S_{10}, S_{11}\}$ are first identified (block 80) using the bounding box of the sub-polygon 804 as follows:

$$S_{x\ min} = \lceil p_{x\ min} \rceil$$

$$s_{x\ max} = \lfloor p_{x\ max} \rfloor$$

$$s_{y\ min} = \lceil p_{y\ min} \rceil$$

$$s_{y\ max} = \lceil p_{y\ max} \rceil$$

$$S_{00} = (s_{x\ min}, s_{y\ min})$$

$$S_{01} = (s_{x\ max}, s_{y\ min})$$

$$S_{10} = (s_{x\ min}, s_{y\ max})$$

$$S_{11} = (s_{x\ max}, s_{y\ max})$$

where $\lfloor x \rfloor$ and $\lceil x \rceil$ are the standard 'floor' and 'ceiling' operators.

[0069] It can then be determined if the bounding box of the sub-polygon 804 misses all sample locations in the tile, e.g. all sample locations in tile A (block 81) and if it does ('Yes' in block 81, which corresponds to a 'No' in block 708 of FIG. 7) then the ID for the primitive 802 is not included in the control stream for the tile (i.e. the primitive is culled, using the terminology shown in FIG. 9) and the method of FIG. 9 does not proceed further in relation to the particular primitive and the particular tile (although the method may be repeated in a subsequent iteration of the method of FIG. 7 for the same primitive but a different tile, e.g. tile B). It can be determined if the bounding box of the sub-polygon misses all four sampling locations in the tile (in block 81) using the test:

IF $(s_{x\ min} > s_{x\ max} \text{ OR } s_{y\ min} > s_{y\ max})$ THEN MISSES

[0070] If the bounding box of the sub-polygon 804 does not miss all sample locations in the tile, e.g. in tile A ('No' in block 81 which corresponds to a 'Yes' in block 708 of FIG. 7) then the ID for the primitive 802 is included in the control stream for the tile (block 408, with the rest of the method blocks in

FIG. 9 not being used), or is further tested with the third method as described below with reference to FIGs. 9-11.

[0071]As shown in FIG. 7, the method may iterate through each primitive in a set of candidate primitives (which may comprise all primitives or alternatively, the set may be a proper subset of a set comprising all primitives and may, for example, be generated using the first method as described above with reference to FIGs. 4-6) to generate a control stream for a tile and then once all primitives in the set have been considered for a particular tile ('Yes' in block 410), the method may be repeated until a control stream has been generated for every tile ('Yes' in block 412). It will be appreciated, however, that aspects of the method may be performed in parallel (e.g. some or all of the tiles may be considered in parallel) and the set of candidate primitives may be the same for all tiles (e.g. where the candidate set comprises all primitives) or may be different for different tiles (e.g. where the candidate set is generated using the first method described above with reference to FIGs. 4-6) or groups of tiles. The method could alternatively iterate through each tile to add a primitive to each tile control stream where needed and then once all the tiles have been considered for a particular primitive the method may be repeated until all the primitives have been considered.

[0072]Using the method shown in FIG. 7, the primitive 802 is not added to the control stream for tile A. This is in contrast to known methods which would add the ID of the primitive to the control stream for tile A even though the bounding box of the primitive does not cover any sample point in the tile (e.g. because the bounding box for the whole primitive 802 covers four of the sample positions in tile A).

[0073]In the method shown in FIG. 7 and described above, the intersection points are generated between the primitive edges and the tile boundaries (in block 702). In a variation of this method, the intersection points may instead be generated between the primitive edges and the bounding box of the tile at sample precision (e.g. as generated in block 402 of FIG. 4). This results in a

smaller sub-polygon (as generated in block 704) and a smaller bounding box of the sub-polygon (as generated in block 706); however, otherwise the method proceeds as described above. The method may be implemented in a tiling unit of a GPU.

[0074] A third method of determining whether a primitive should be associated with a tile (e.g. whether a primitive ID should be added to a control stream for a tile) can be described with reference to FIGs. 9-11. This method requires additional processing compared to the methods described above with reference to FIGs. 4-6 and FIGs. 7-9, but results in additional non-contributing primitives not being added to the control stream. As described below, this method may be implemented in combination with either or both of the methods described above.

[0075] As shown in the flow diagram of FIG. 10, the intersection points between the edges of a primitive (e.g. a triangle) and tile boundaries are generated (block 702). Referring to the primitive 1102 (with vertices V0, V1, V2) shown in FIG. 11, these intersection points are Va and Vb. Line equations of the edges of the primitive (e.g. the triangle) may be used to generate the intersection points between triangle edges and tile boundaries (in block 702). These intersection points may be generated (in block 702) using the method described above with reference to FIG. 8. As noted above, although the method is described with reference to primitives which are triangles, the method may also be used for other primitive types (e.g. quads and lines).

[0076] Once the intersection points have been generated (in block 702), a sub-polygon is then formed inside the tile using the intersection points to replace the vertices outside the tile (block 704). Referring again to the example shown in FIG. 11, intersection point Va replaces vertex V1 and intersection point Vb replaces vertex V2 as both V1 and V2 are outside Tile A. A bounding box 1104 for the sub-polygon (with vertices V0, Va, Vb) is generated at sample precision (block 706).

[0077] Each of the sample points inside the bounding box of the sub-polygon 1104 is then tested against the original edges of the sub-polygon (where an original edge is an edge of the sub-polygon which is also at least part of an edge of the primitive from which the sub-polygon was formed) to see if there are any sample points inside the sub-polygon (block 1007). The new edge (between vertices Va and Vb in the example shown in FIG. 11) does not need to be tested because this edge lies on the boundary of tile A so all sample positions within tile A will be within this new edge of the sub-primitive. Only if there is a sample point inside the sub-polygon ('Yes' in block 1008), is the ID for the primitive 1102 included in the control stream for the tile (block 408). If there are no sample points inside the sub-polygon ('No' in block 1008), then the ID is not included in the control stream for the tile.

[0078] The testing of original edges against the sample positions in the bounding block 1104 (in block 1007) may be performed using another part of the method described in GB Patent No. 2401522 and shown in FIG. 9; however, unlike in the description of GB 2401522, in the method of FIG. 10, the edges checked are the original edges of sub-polygon instead of all the edges from the triangle as in GB Patent No. 2401522.

[0079] The edge parameters for each of the original edges of the sub-polygon are computed (block 85) and then each sampling point within the bounding box of the sub-polygon 1104 is tested against each edge (block 86) and if any of the samples pass ('Yes' in block 87, which corresponds to 'Yes' in block 1008) i.e. such that any of the samples are inside the sub-polygon, then the ID of the primitive 1102 is added to the control stream for the tile (in block 408).

[0080] The edge parameters for an edge i are denoted A_i, B_i, C_i , and depend upon the end points of the edge (i.e. the edge equation is $A_i x + B_i y + C_i = 0$). If these end points are denoted (x_i, y_i) and (x_{i+1}, y_{i+1}) then:

$$A_i = y_i - y_{i+1}$$

$$B_i = x_{i+1} - x_i$$

$$C_i = x_i y_{i+1} - x_{i+1} y_i$$

and the four test inequalities for an edge and for the four distinct sampling locations $S_{x\ min}, S_{x\ max}, S_{y\ min}, S_{y\ max}$ (as defined above) are:

$$A_i S_{x\ min} + B_i S_{y\ min} + C_i \geq 0$$

$$A_i S_{x\ max} + B_i S_{y\ min} + C_i \geq 0$$

$$\Leftrightarrow A_i (S_{x\ min} + 1) + B_i S_{y\ min} + C_i \geq 0$$

$$\Leftrightarrow A_i S_{x\ min} + B_i S_{y\ min} + C_i \geq -A_i$$

$$A_i S_{x\ min} + B_i S_{y\ max} + C_i \geq 0$$

$$\Leftrightarrow A_i S_{x\ min} + B_i S_{y\ min} + C_i \geq -B_i$$

$$A_i S_{x\ max} + B_i S_{y\ max} + C_i \geq 0$$

$$\Leftrightarrow A_i S_{x\ min} + B_i S_{y\ min} + C_i \geq -B_i - A_i$$

[0081] The edge parameters which are computed (in block 85) relate only to the original edges of the sub-polygon and not to the newly added edge (e.g. between Va and Vb) which corresponds to the edge of the tile. When calculating the edge parameters (in block 85), the entire edges of the primitive may be used (i.e. between the original vertices of the primitive, e.g. for one edge between V0 and V1 and a second edge between V2 and V0 in the example shown in FIG. 11) or the edges of the sub-polygon may be used (e.g.

for one edge between V_0 and V_a and a second edge between V_b and V_0 in the example shown in FIG. 11).

[0082] By re-using parts of the method described in GB2401522 as described above, existing hardware within a tiling unit can be re-used. This reduces the amount of additional hardware that is required to implement the methods described herein and thereby reduces the size and power consumption of the hardware that implements the methods described herein.

[0083] The testing sample positions against edge equations (in block 86 of FIG. 9 which along with block 85 corresponds to block 1007 of FIG. 10) is done in reduced precision corresponding to 16.8 fixed point format of X and Y coordinates, rather than at full precision floating point as in rasterization process, to simplify and speed up the calculations in hardware. As the reduced precision is used in the method, errors may be introduced in the calculation. The reduced precision is safe when the triangle is relatively small therefore the accumulated errors in the iteration from the triangle vertices are limited, as the method in GB2401522 is designed for testing small triangles within a few pixels across. The error that is introduced is proportionally larger for larger primitives than for smaller primitives due to the accumulated effect in the calculation of interpolation between vertices of the triangle.

Consequently for smaller primitives, the original vertices may be used to compute the edge parameters (in block 85) and for larger primitives, the intersection points (as generated in block 702) may be used instead. The decision as to which vertices to use (i.e. the original ones or the intersection points) may be made for the whole primitive (e.g. based on whether the primitive covers less than a predefined number of tiles, such as less than 4×4 tiles) or may be made on an edge by edge basis (e.g. based on whether the length of the edge exceeds a predefined threshold value or not).

[0084] As shown in FIG. 10, the method may iterate through each primitive in a set of candidate primitives to generate a control stream for a tile and then once all primitives in the set have been considered for a particular tile ('Yes' in

block 410), the method may be repeated until a control stream has been generated for every tile ('Yes' in block 412). It will be appreciated, however, that aspects of the method may be performed in parallel (e.g. some or all of the tiles may be considered in parallel). The method could alternatively iterate through each tile to add a primitive to each tile control streams where needed and then once all the tiles have been considered for a particular primitive the method may be repeated until all the primitives have been considered.

[0085] The candidate set of primitives may comprise all primitives or alternatively, the set may be a proper subset of a set comprising all primitives and may, for example, be generated using the first method as described above with reference to FIGs. 4-6 and/or the second method as described above with reference to FIGs. 7-9. The set of candidate primitives may be the same for all tiles (e.g. where the candidate set comprises all primitives) or may be different for different tiles (e.g. where the candidate set is generated using the first method described above with reference to FIGs. 4-6 and/or the second method as described above with reference to FIGs. 7-9) or groups of tiles.

[0086] Using the method shown in FIG. 10, the primitive 1102 is not added to the control stream for tile A. This is in contrast to known methods which would add the ID of the primitive to the control stream for tile A.

[0087] In the method shown in FIG. 10 and described above, the intersection points are generated between the primitive edges and the tile boundaries (in block 702). In a variation of this method, the intersection points may instead be generated between the primitive edges and the bounding box of the tile at sample precision (e.g. as generated in block 402 of FIG. 4). This results in a smaller sub-polygon (as generated in block 704) and a smaller bounding box of the sub-polygon (as generated in block 706) which may result in fewer sample points to test against the original edges (in block 1007); however, otherwise the method proceeds as described above.

[0088] In the description of the methods of FIGs. 7 and 10 above, it is assumed that the arrangement of sample points in each pixel is the same (as noted above, there may be one or more sample points in each pixel). If the arrangement of sample points is not the same in each pixel, the methods of FIGs. 7 and 10 are not affected and can be implemented as described above unless a sample precision bounding box for the tile is used to generate the intersection points instead of the actual tile boundaries (in block 702). In this case the worst case sample positions may be used to generate the sample precision bounding box (e.g. as described above with reference to FIG. 6).

[0089] In the examples shown in FIGs. 8 and 11, there is a single vertex, V_0 , in tile A and two intersection points (V_a and V_b) on the same tile boundary. Examples where there is a single vertex in tile A and either two intersection points on different tile boundaries or more than two intersection points are described below with reference to FIG. 16.

[0090] In other examples, however, there may be no vertices within the tile, as shown in the two examples 1201, 1202 in FIG. 12 and the first example 1300 in FIG. 13. In the first example 1201, there are two points of intersection, V_a and V_b and these are on tile boundaries that intersect at a corner of the tile V_n . This results in a triangular sub-polygon with vertices V_a , V_n and V_b being created (in block 704) and the method can then proceed as shown in either or both of FIGs. 7 and 10 and described above.

[0091] In the second example 1202 in FIG. 12, there are four points of intersection, V_a , V_b , V_c and V_d and these are on tile boundaries that intersect at a corner of the tile V_n and the sub-polygon is a quadrilateral instead of a triangle. In various examples, where the sub-polygon is a quadrilateral (or in general has more than 3 edges), the ID of the primitive may be added to the control stream for the tile without further consideration (e.g. as shown in FIGs. 14 and 15 and described below). Alternatively, the sub-polygon having more than three edges may be divided into two or more triangles (e.g. V_a , V_c , V_b and V_c , V_d , V_b) and each of these triangles may be fed as sub-polygons into

the methods of either or both of FIGs. 7 and 10. The sub-polygons which are part of the same primitive may be flagged such that it is clear that they are part of the same primitive and the primitive ID is included in the control stream (or the primitive is otherwise associated with the tile) if any samples are inside any of the two or more sub-polygons formed from the primitive.

[0092] As shown in the first example 1300 in FIG. 13, it is possible for there to be no vertices within the tile and two points of intersection, V_a and V_b , which lie on opposite boundaries of the tile. In such examples, the ID of the primitive may be added to the control stream for the tile or alternatively, the sub-polygon within the tile (e.g. V_a , V_b , V_c , V_d) may be divided into two or more triangles (e.g. V_a , V_c , V_b and V_a , V_d , V_b) and each of these triangles may be fed as sub-polygons into the methods of either or both of FIGs. 7 and 10. The sub-polygons which are part of the same primitive may be flagged such that it is clear that they are part of the same primitive, the primitive ID is included in the control stream if any samples are inside any of the two or more sub-polygons formed from the primitive.

[0093] In the second example 1301 shown in FIG. 13, there are two vertices, V_0 and V_1 , in tile A. When the primitive is truncated (in blocks 702 and 704) this also results in a sub-polygon which is a quadrilateral with vertices V_0 , V_1 , V_a and V_b . In various examples, where the sub-polygon is a quadrilateral, the ID of the primitive may be added to the control stream for the tile without further consideration. Alternatively, the quadrilateral sub-polygon may then be divided into two triangles (e.g. V_0 , V_1 , V_a and V_0 , V_a , V_b) and both of these triangles may be fed as sub-polygons into the methods of either or both of FIGs. 7 and 10. As described above, the two sub-polygons which are part of the same primitive may be flagged such that it is clear that they are part of the same primitive, the primitive ID is included in the control stream if any samples are inside any of the two sub-polygons. Using the method shown in FIG. 10 for each of the two triangles (V_a, V_b, V_0) and (V_a, V_0, V_1) formed from the sub-polygon (V_a, V_b, V_0, V_1), the primitive 1302 is not added to the control stream for tile A, even though the bounding box of each of the sub-polygon

triangles covers two sample points in tile A. Instead, it can be decided using the method shown in FIG. 10 that the two sample points in the bounding box of the sub-polygon triangles are all located outside the sub-polygon (i.e. outside both of the triangles formed from the quadrilateral sub-polygon). This is in contrast to known methods which would add the ID of the primitive 1302 to the control stream for tile A.

[0094] FIGs. 14 and 15 show a flow diagram of an example method which combines the methods of FIGs. 7 and 10 along with a test relating to the number of vertices in a tile, as described above with reference to FIGs. 12 and 13. In this method, if any primitive has two or more vertices in the tile (No in block 1402) e.g. as shown in example 1301 in FIG. 13, then the ID of the primitive is added to the control stream for the tile (block 408) without further consideration. As described above, however, such primitives may alternatively be handled by dividing the sub-polygon (which may be a quadrilateral) into multiple triangles and then feeding the multiple triangles (as separate, but related sub-polygons) into the method of FIG. 15 (e.g. by starting at block 706 for each of the triangles).

[0095] If the primitive has less than two vertices in the tile ('Yes' in block 1402, i.e. one vertex in the tile or no vertices in the tile), the intersection points between the primitive edges and the tile boundaries are generated (block 702), as described above. In this method, if there are more than two intersection points ('No' in block 1404), then the ID of the primitive is added to the control stream for the tile (block 408) without further consideration, e.g. for example 1202 in FIG. 12, which has no vertices in the tile and more than two intersection points, the ID of the primitive is added to the control stream for the tile (block 408) without further consideration. As described above, however, such primitives may alternatively be handled by dividing the sub-polygon (which may be a quadrilateral) into multiple triangles and then feeding the multiple triangles (as separate, but related sub-polygons) into the method of FIG. 15 (e.g. by starting at block 706 for each of the triangles).

[0096] If the primitive has only two intersection points ('Yes' in block 1404), the method then divides depending upon whether there is only one vertex in the tile ('Yes' in block 1406 then 1408) or no vertex in the tile ('No' in block 1406 then 1410).

[0097] As shown in FIG. 14, the ID of the primitive is added to the control stream (in block 408) if there is only one vertex in the tile ('Yes' in block 1406) but the two intersection points are not on the same boundary ('No' in block 1408) or if there is no vertex in the tile ('No' in block 1406) but the two intersection points are not on different tile boundaries ('No' in block 1410). Additionally, the ID of the primitive is then added to the control stream (in block 408) if there is no vertex in the tile ('No' in block 1406), the two intersection points are on different tile boundaries ('Yes' in block 1410) but those two different boundaries do not meet at a corner within the primitive ('No' in block 1412). As described above, however, such primitives may alternatively be handled by dividing the sub-polygon (which may be a quadrilateral) into multiple triangles and then feeding the multiple triangles (as separate, but related sub-polygons) into the method of FIG. 15 (e.g. by starting at block 706 for each of the triangles).

[0098] If the ID of the primitive has not yet been added to the control stream, the method proceeds onto FIG. 15 which shows a concatenation of the tests from FIGs. 7 and 10. As described above with reference to FIG. 7, a sub-polygon is formed inside the tile using the intersection points to replace the vertices outside the tile (block 704) and then a bounding box of the sub-polygon is generated at sample precision (block 706). If the bounding box overlaps any samples ('Yes' in block 708), the method proceeds to the tests described above with reference to FIG. 10 and the original edges of the sub-polygon are tested against each sample point inside the bounding box of the sub-polygon (block 1007). If there is any sample point inside the original edges ('Yes' in block 1008), the ID of the primitive is added to the control stream for the tile (block 408). If, however, the bounding box does not overlap any samples ('No' in block 708) or there are no sample points inside the

original edges ('No' in block 1008), then the primitive ID is not added to the control stream.

[0099] As shown in FIG. 14, the method may iterate through each primitive to generate a control stream for a tile and then once all primitives have been considered for a particular tile ('Yes' in block 410), the method may be repeated until a control stream has been generated for every tile ('Yes' in block 412). It will be appreciated, however, that aspects of the method may be performed in parallel (e.g. some or all of the tiles may be considered in parallel). The method may alternatively iterate through each tile to add a primitive to each covered tile's tile control stream, and once all the tiles have been considered for a particular primitive, the method may be repeated until all the primitives have been considered.

[00100] FIG. 16 shows two further examples 1601, 1602 of primitives which cannot be eliminated from the control stream of tile A using the method of FIGs. 14 and 15. In the first example 1601, the primitive has a single vertex in tile A, V0 ('Yes' in block 1402) and only two intersection points, Va and Vb ('Yes' in block 1404). However, the intersection points are not on the same tile boundary ('Yes' in block 1406 followed by 'No' in block 1408) and so the primitive is included in the control stream (in block 408). In the second example 1602, the primitive has a single vertex in tile A, V0 ('Yes' in block 1402) and four intersection points, Va, Vb, Vc and Vd ('No' in block 1404) and so the primitive is included in the control stream (in block 408).

[00101] As described above, the sub-polygons in examples 1601, 1602 may alternatively each be divided into multiple triangles and these may all be fed into the methods described herein as separate (but linked) primitives.

[00102] FIG. 17 shows a flow diagram of an example method which combines all the methods described above. The method described above with reference to FIG. 4 is applied first (block 1702 with block 1704 corresponding to the test in block 406 of FIG. 4). If the primitive is not

eliminated by this assessment (in block 1702), i.e. if it cannot be determined that the bounding boxes do not overlap ('No' in block 406 which corresponds to 'No' in block 1704), then the method proceeds with a further assessment of the primitive. In the method shown in FIG. 17, a technique referred to as 'perfect tiling' may optionally be used to eliminate some further primitives in the tile (block 1708). This technique is also described in GB2401522 (e.g. in FIG. 4 of that patent). Perfect tiling involves comparing the edge equations of a primitive with the integer tile boundaries to check if the corner of the tile is inside the primitive. In perfect tiling, there is no comparison of sample points and the assessment is performed at the corner of the tile boundaries. In the example shown in FIG. 17, perfect tiling is not performed ('No' in block 1706) if the bounding box of the primitive overlaps only one tile in the X and/or Y direction.

[00103] As part of the perfect tiling method (in block 1708) the edge equations of the primitive are calculated and these are then re-used in the subsequent assessment of the primitive (in block 1712). The primitive sample precision bounding box technique (block 1702 and FIG. 4) does not require calculation of the edge equations and so it is efficient to eliminate some primitives (in block 1704) prior performing perfect tiling (in block 1708) and/or the other methods described herein which do require calculation of the edge equations.

[00104] If the primitive is not eliminated by the perfect tiling assessment (in block 1708), where implemented, then the method proceeds with a further assessment of the primitive using the method shown in FIGs. 14 and 15 (block 1712 with block 1714 corresponding to the decision points in blocks 1402, 1404, 1408, 1410, 1412, 708 and 1008). As described above, this assessment involves the use of edge equations (in block 1007) and these edge equations may have already been calculated (in block 1708).

[00105] As shown in FIG. 17, the method may iterate through each primitive to generate a control stream for a tile (block 1718) and then once all

primitives have been considered for a particular tile ('No' in block 1718), the method may be repeated until a control stream has been generated for every tile (not shown in FIG. 17). It will be appreciated, however, that aspects of the method may be performed in parallel (e.g. some or all of the tiles may be considered in parallel).

[00106] In the methods described above, any testing that is performed in relation to sampling points within a pixel only identifies whether any sample position is within the primitive / sub-primitive / bounding box. In many implementations, there is no determination of which sampling point falls within the primitive / sub-primitive / bounding box. As also described above, each pixel may comprise a single sampling point or may comprise a plurality of sampling points and the analysis is performed at the reduced sample precision (e.g. 16.8 format).

[00107] In the examples shown in the accompanying drawings, each primitive covers at least one sample position within the rendering space, although in the case of non-contributing primitives for a tile, the primitive may not cover a sample position within the particular tile being considered (e.g. in FIG. 8, the primitive 802 does not cover any sample positions in tile A but does cover two sample positions in tile B). However, the methods described herein may, in various examples, be used for primitives that do not necessarily cover any sample positions in any tile within the rendering space.

[00108] As described above, the methods described herein may be implemented in an improved tiling unit in a GPU (e.g. as shown in FIG. 1). The methods may be implemented in software and/or hardware and as described above, in various examples, existing hardware may be re-used to perform elements of the methods described herein.

[00109] By using the methods described herein, the number of primitives (and in particular the number of non-contributing primitives) that are added to the control stream for a tile is reduced. This reduces the effect used in

subsequent operations within the rendering unit and so improves the efficiency of the overall graphics processing system. As primitive sizes become smaller, the efficiency savings that can be achieved using the methods described herein is expected to become larger.

[00110] The methods described herein are performed before rasterization (which is performed within the rendering unit 110 in FIG. 1). By reducing the number of primitives in a control stream for a tile, rasterization is simplified. Unlike rasterization, the methods described herein only determine if any sample point is within a primitive and the methods are agnostic to which sample point is within the primitive (i.e. the methods described herein eliminate primitives before the per-sample analysis is performed). Rasterisation renders image values at the sample positions. In a tile-based graphics system, a rendering unit can perform rendering in a tile-by-tile manner using the control stream for a tile to identify primitives which are relevant to the rendering of the tile.

[00111] In most of the examples described above the primitives are associated with tiles by storing primitive IDs in control streams for the tiles. In other examples, associations between primitives and tiles may be stored differently, e.g. for each primitive a tile list could be stored which includes tile IDs of tiles in which the primitive is present.

[00112] FIG. 18 shows a computer system in which the graphics processing systems and methods described herein may be implemented. The computer system comprises a CPU 1802, a GPU 102, a memory 1806 and other devices 1814, such as a display 1816, speakers 1818 and a camera 1819. A tiling unit 108 which implements one or more of the methods described herein is implemented on the GPU 102. In other examples, the tiling unit 108 may be implemented on the CPU 1802. The components of the computer system can communicate with each other via a communications bus 1820. A store 104₁ is implemented as part of the memory 1806.

[00113] The graphics processing system 100 of FIG. 1 is shown as comprising a number of functional blocks. This is schematic only and is not intended to define a strict division between different logic elements of such entities. Each functional block may be provided in any suitable manner. It is to be understood that intermediate values described herein as being formed by a functional block need not be physically generated by the functional block at any point and may merely represent logical values which conveniently describe the processing performed by the graphics processing system between its input and output.

[00114] The methods described herein may be embodied in hardware on an integrated circuit. The graphics processing systems described herein may be configured to perform any of the methods described herein. Generally, any of the functions, methods, techniques or components described above can be implemented in software, firmware, hardware (e.g., fixed logic circuitry), or any combination thereof. The terms “module,” “functionality,” “component”, “element”, “unit”, “block” and “logic” may be used herein to generally represent software, firmware, hardware, or any combination thereof. In the case of a software implementation, the module, functionality, component, element, unit, block or logic represents program code that performs the specified tasks when executed on a processor. The algorithms and methods described herein could be performed by one or more processors executing code that causes the processor(s) to perform the algorithms/methods. Examples of a computer-readable storage medium include a random-access memory (RAM), read-only memory (ROM), an optical disc, flash memory, hard disk memory, and other memory devices that may use magnetic, optical, and other techniques to store instructions or other data and that can be accessed by a machine.

[00115] The terms computer program code and computer readable instructions as used herein refer to any kind of executable code for processors, including code expressed in a machine language, an interpreted language or a scripting language. Executable code includes binary code,

machine code, bytecode, code defining an integrated circuit (such as a hardware description language or netlist), and code expressed in a programming language code such as C, Java or OpenCL. Executable code may be, for example, any kind of software, firmware, script, module or library which, when suitably executed, processed, interpreted, compiled, executed at a virtual machine or other software environment, cause a processor of the computer system at which the executable code is supported to perform the tasks specified by the code.

[00116] A processor, computer, or computer system may be any kind of device, machine or dedicated circuit, or collection or portion thereof, with processing capability such that it can execute instructions. A processor may be any kind of general purpose or dedicated processor, such as a CPU, GPU, System-on-chip, state machine, media processor, an application-specific integrated circuit (ASIC), a programmable logic array, a field-programmable gate array (FPGA), physics processing units (PPUs), radio processing units (RPU), digital signal processors (DSPs), general purpose processors (e.g. a general purpose GPU), microprocessors, any processing unit which is designed to accelerate tasks outside of a CPU, etc. A computer or computer system may comprise one or more processors. Those skilled in the art will realize that such processing capabilities are incorporated into many different devices and therefore the term 'computer' includes set top boxes, media players, digital radios, PCs, servers, mobile telephones, personal digital assistants and many other devices.

[00117] It is also intended to encompass software which defines a configuration of hardware as described herein, such as HDL (hardware description language) software, as is used for designing integrated circuits, or for configuring programmable chips, to carry out desired functions. That is, there may be provided a computer readable storage medium having encoded thereon computer readable program code in the form of an integrated circuit definition dataset that when processed in an integrated circuit manufacturing system configures the system to manufacture a GPU configured to perform

any of the methods described herein, or to manufacture a GPU comprising any apparatus described herein. An integrated circuit definition dataset may be, for example, an integrated circuit description.

[00118] Therefore, there may be provided a method of manufacturing, at an integrated circuit manufacturing system, a graphics processing system as described herein. Furthermore, there may be provided an integrated circuit definition dataset that, when processed in an integrated circuit manufacturing system, causes the method of manufacturing a graphics processing system to be performed.

[00119] An integrated circuit definition dataset may be in the form of computer code, for example as a netlist, code for configuring a programmable chip, as a hardware description language defining an integrated circuit at any level, including as register transfer level (RTL) code, as high-level circuit representations such as Verilog or VHDL, and as low-level circuit representations such as OASIS (RTM) and GDSII. Higher level representations which logically define an integrated circuit (such as RTL) may be processed at a computer system configured for generating a manufacturing definition of an integrated circuit in the context of a software environment comprising definitions of circuit elements and rules for combining those elements in order to generate the manufacturing definition of an integrated circuit so defined by the representation. As is typically the case with software executing at a computer system so as to define a machine, one or more intermediate user steps (e.g. providing commands, variables etc.) may be required in order for a computer system configured for generating a manufacturing definition of an integrated circuit to execute code defining an integrated circuit so as to generate the manufacturing definition of that integrated circuit.

[00120] An example of processing an integrated circuit definition dataset at an integrated circuit manufacturing system so as to configure the system to manufacture a GPU will now be described with respect to FIG. 19.

[00121] FIG. 19 shows an example of an integrated circuit (IC) manufacturing system 1902 which comprises a layout processing system 1904 and an integrated circuit generation system 1906. The IC manufacturing system 1902 is configured to receive an IC definition dataset (e.g. defining a GPU as described in any of the examples herein), process the IC definition dataset, and generate an IC according to the IC definition dataset (e.g. which embodies a GPU as described in any of the examples herein). The processing of the IC definition dataset configures the IC manufacturing system 1902 to manufacture an integrated circuit embodying a GPU as described in any of the examples herein.

[00122] The layout processing system 1904 is configured to receive and process the IC definition dataset to determine a circuit layout. Methods of determining a circuit layout from an IC definition dataset are known in the art, and for example may involve synthesising RTL code to determine a gate level representation of a circuit to be generated, e.g. in terms of logical components (e.g. NAND, NOR, AND, OR, MUX and FLIP-FLOP components). A circuit layout can be determined from the gate level representation of the circuit by determining positional information for the logical components. This may be done automatically or with user involvement in order to optimise the circuit layout. When the layout processing system 1904 has determined the circuit layout it may output a circuit layout definition to the IC generation system 1906. A circuit layout definition may be, for example, a circuit layout description.

[00123] The IC generation system 1906 generates an IC according to the circuit layout definition, as is known in the art. For example, the IC generation system 1906 may implement a semiconductor device fabrication process to generate the IC, which may involve a multiple-step sequence of photo lithographic and chemical processing steps during which electronic circuits are gradually created on a wafer made of semiconducting material. The circuit layout definition may be in the form of a mask which can be used in a lithographic process for generating an IC according to the circuit

definition. Alternatively, the circuit layout definition provided to the IC generation system 1906 may be in the form of computer-readable code which the IC generation system 1906 can use to form a suitable mask for use in generating an IC.

[00124] The different processes performed by the IC manufacturing system 1902 may be implemented all in one location, e.g. by one party. Alternatively, the IC manufacturing system 1902 may be a distributed system such that some of the processes may be performed at different locations, and may be performed by different parties. For example, some of the stages of: (i) synthesising RTL code representing the IC definition dataset to form a gate level representation of a circuit to be generated, (ii) generating a circuit layout based on the gate level representation, (iii) forming a mask in accordance with the circuit layout, and (iv) fabricating an integrated circuit using the mask, may be performed in different locations and/or by different parties.

[00125] In other examples, processing of the integrated circuit definition dataset at an integrated circuit manufacturing system may configure the system to manufacture a graphics processing system without the IC definition dataset being processed so as to determine a circuit layout. For instance, an integrated circuit definition dataset may define the configuration of a reconfigurable processor, such as an FPGA, and the processing of that dataset may configure an IC manufacturing system to generate a reconfigurable processor having that defined configuration (e.g. by loading configuration data to the FPGA).

[00126] In some embodiments, an integrated circuit manufacturing definition dataset, when processed in an integrated circuit manufacturing system, may cause an integrated circuit manufacturing system to generate a device as described herein. For example, the configuration of an integrated circuit manufacturing system in the manner described above with respect to FIG. 19 by an integrated circuit manufacturing definition dataset may cause a device as described herein to be manufactured.

[00127] In some examples, an integrated circuit definition dataset could include software which runs on hardware defined at the dataset or in combination with hardware defined at the dataset. In the example shown in FIG. 19, the IC generation system may further be configured by an integrated circuit definition dataset to, on manufacturing an integrated circuit, load firmware onto that integrated circuit in accordance with program code defined at the integrated circuit definition dataset or otherwise provide program code with the integrated circuit for use with the integrated circuit.

[00128] The methods described herein may be performed by a computer configured with software in machine readable form stored on a tangible storage medium e.g. in the form of a computer program comprising computer readable program code for configuring a computer to perform the constituent portions of described methods or in the form of a computer program comprising computer program code means adapted to perform all the steps of any of the methods described herein when the program is run on a computer and where the computer program may be embodied on a computer readable storage medium. Examples of tangible (or non-transitory) storage media (which may be volatile or non-volatile) include disks, thumb drives, memory cards, semiconductor-based memory, optical / magnetic / phase change memory etc. and do not include propagated signals. The software can be suitable for execution on a parallel processor or a serial processor such that the method steps may be carried out in any suitable order, or simultaneously.

[00129] A particular reference to “logic” refers to structure that performs a function or functions. An example of logic includes circuitry that is arranged to perform those function(s). For example, such circuitry may include transistors and/or other hardware elements available in a manufacturing process. Such transistors and/or other elements may be used to form circuitry or structures that implement and/or contain memory, such as registers, flip flops, or latches, logical operators, such as Boolean operations, mathematical operators, such as adders, multipliers, or shifters, and interconnect, by way of example. Such elements may be provided as custom

circuits or standard cell libraries, macros, or at other levels of abstraction. Such elements may be interconnected in a specific arrangement. Logic may include circuitry that is fixed function and circuitry can be programmed to perform a function or functions; such programming may be provided from a firmware or software update or control mechanism. Logic identified to perform one function may also include logic that implements a constituent function or sub-process. In an example, hardware logic has circuitry that implements a fixed function operation, or operations, state machine or process.

[00130] Any range or device value given herein may be extended or altered without losing the effect sought, as will be apparent to the skilled person.

[00131] It will be understood that the benefits and advantages described above may relate to one embodiment or may relate to several embodiments. The embodiments are not limited to those that solve any or all of the stated problems or those that have any or all of the stated benefits and advantages.

[00132] Any reference to 'an' item refers to one or more of those items. The term 'comprising' is used herein to mean including the method blocks or elements identified, but that such blocks or elements do not comprise an exclusive list and an apparatus may contain additional blocks or elements and a method may contain additional operations or elements. Furthermore, the blocks, elements and operations are themselves not impliedly closed.

[00133] The steps of the methods described herein may be carried out in any suitable order, or simultaneously where appropriate. The arrows between boxes in the figures show one example sequence of method steps but are not intended to exclude other sequences or the performance of multiple steps in parallel. Additionally, individual blocks may be deleted from any of the methods without departing from the spirit and scope of the subject matter described herein. Aspects of any of the examples described above may be combined with aspects of any of the other examples described to form further

examples without losing the effect sought. Where elements of the figures are shown connected by arrows, it will be appreciated that these arrows show just one example flow of communications (including data and control messages) between elements. The flow between elements may be in either direction or in both directions.

[00134] The applicant hereby discloses in isolation each individual feature described herein and any combination of two or more such features, to the extent that such features or combinations are capable of being carried out based on the present specification as a whole in the light of the common general knowledge of a person skilled in the art, irrespective of whether such features or combinations of features solve any problems disclosed herein. In view of the foregoing description it will be evident to a person skilled in the art that various modifications may be made within the scope of the invention.

Claims

1. A method of processing primitives within a tiling unit of a graphics processing system, the method comprising:

determining whether a primitive that covers at least one sample position in a rendering space falls within a tile based on positions of samples within pixels in the tile; and

in response to determining that a primitive that covers at least one sample position in a rendering space does fall within a tile based on the positions of samples within pixels in the tile, storing an association between the tile and the primitive to indicate that the primitive is present in the tile.

2. A method according to claim 1, wherein said storing an association between the tile and the primitive comprises adding an identifier for the primitive to a control stream for the tile (408).

3. A method according to claim 1, wherein said storing an association between the tile and the primitive comprises adding an identifier for the tile to a tile list for the primitive.

4. A method according to any of the preceding claims, further comprising rendering primitives in a tile using the stored associations, wherein the rendering is performed at each sample position within the tile.

5. A method according to any of the preceding claims, wherein the determination is performed at a reduced sample precision.

6. A method according to any of the preceding claims, wherein determining whether a primitive falls within a tile based on positions of samples within pixels in a tile comprises:

generating a bounding box of the tile at sample precision (402);

generating a bounding box of the primitive at sample precision (404);

determining if the bounding boxes overlap (406); and

in response to determining that the bounding boxes do not overlap, determining that the primitive does not fall within the tile.

7. A method according to any of the preceding claims, wherein determining whether a primitive falls within a tile based on positions of samples within pixels in a tile comprises:

generating any intersection points between edges of the primitive and boundaries of the tile (702);

forming a sub-polygon inside the tile by replacing vertices of the primitive outside the tile with the intersection points (704);

generating a bounding box of the sub-polygon at sample precision (706);

determining if the bounding box of the sub-polygon overlaps any samples in the tile (708); and

in response to determining that the bounding box of the sub-polygon overlaps any samples in the tile, determining that the primitive falls within the tile.

8. A method according to claim 7, wherein generating any intersection points between edges of the primitive and boundaries of the tile comprises:

generating a bounding box of the tile at sample precision (402); and

generating any intersection points between edges of the primitive and edges of the bounding box of the tile at sample precision.

9. A method according to claim 7 or 8, wherein forming a sub-polygon inside the tile by replacing vertices of the primitive outside the tile with the intersection points comprises:

forming an initial sub-polygon inside the tile by replacing vertices of the primitive outside the tile with the intersection points; and

if the initial sub-polygon has more than three vertices, dividing the initial sub-polygon into a plurality of smaller sub-polygons, each having only three vertices,

and wherein a bounding box is generated at sample precision for each smaller sub-polygon and it is determined, for each generated bounding box, if it overlaps any samples in the tile.

10. A method according to any of claims 7-9, wherein determining if the bounding box of the sub-polygon overlaps any samples in the tile comprises:

identifying four sampling locations in the tile using the bounding box of the sub-polygon (80); and

determining if the bounding box of the sub-polygon misses all four sampling locations in the tile (81).

11. A method according to any of the preceding claims, wherein determining whether a primitive falls within a tile based on positions of samples within pixels in a tile comprises:

generating any intersection points between edges of the primitive and boundaries of the tile (702);

forming a sub-polygon inside the tile by replacing vertices of the primitive outside the tile with the intersection points (704);

generating a bounding box of the sub-polygon at sample precision (706);

testing each edge of the sub-polygon which is also part of an edge of the primitive against each sample point in the bounding box of the sub-

polygon to determine if any sample point is inside the sub-polygon (1007, 1008); and

in response to determining that any sample point is inside the sub-polygon, determining that the primitive falls within the tile.

12. A method according to claim 11, wherein generating any intersection points between edges of the primitive and boundaries of the tile comprises:

generating a bounding box of the tile at sample precision (402); and

generating any intersection points between edges of the primitive and edges of the bounding box of the tile at sample precision.

13. A method according to claim 11 or 12, wherein forming a sub-polygon inside the tile by replacing vertices of the primitive outside the tile with the intersection points comprises:

forming an initial sub-polygon inside the tile by replacing vertices of the primitive outside the tile with the intersection points; and

if the initial sub-polygon has more than three vertices, dividing the initial sub-polygon into a plurality of smaller sub-polygons, each having only three vertices,

and wherein a bounding box is generated at sample precision for each smaller sub-polygon and wherein testing each edge of the sub-polygon which is also part of an edge of the primitive against each sample point in the bounding box of the sub-polygon to determine if any sample point is inside the sub-polygon comprises:

for each smaller sub-polygon, testing each edge of the smaller sub-polygon which is also part of an edge of the primitive against each sample point in the bounding box of the smaller sub-polygon to determine if any sample point is inside the smaller sub-polygon.

14. A method according to any of claims 11-13, wherein testing each edge of the sub-polygon which is also part of an edge of the primitive against each sample point in the bounding box of the sub-polygon to determine if any sample point is inside the sub-polygon comprises:

computing edge parameters for each edge of the sub-polygon which is also part of an edge of the primitive (85); and

testing each sample point in the bounding box of the sub-polygon against each edge (86).

15. A method according to any of claims 1-5, wherein determining whether a primitive falls within a tile based on positions of samples within a pixel comprises:

determining how many vertices of the primitive fall within the tile (1402);

in response to determining that two or more vertices fall outside the tile, determining that the primitive falls within the tile;

in response to determining that less than two vertices fall within the tile, generating any intersection points between edges of the primitive and boundaries of the tile (702);

in response to generating more than two intersection points, determining that the primitive falls within the tile;

in response to generating exactly two intersection points for a primitive with only one vertex in the tile and where the intersection points are on different boundaries of the tile, determining that the primitive falls within the tile;

in response to generating exactly two intersection points for a primitive with no vertices in the tile and where the intersection points are on the same

boundary of the tile or on different boundaries of the tile that do not cross within the primitive, determining that the primitive falls within the tile; and

in response to generating exactly two intersection points for a primitive with only one vertex in the tile and where the intersection points are on same boundary of the tile and in response to generating exactly two intersection points for a primitive with no vertices in the tile and where the intersection points are on different boundaries of the tile which cross within the primitive:

forming a sub-polygon inside the tile by replacing vertices of the primitive outside the tile with the intersection points (704);

generating a bounding box of the sub-polygon at sample precision (706);

determining if the bounding box of the sub-polygon overlaps any samples in the tile (708);

in response to determining that the bounding box of the sub-polygon overlaps any samples in the tile, determining that the primitive falls within the tile;

in response to determining that the bounding box of the sub-polygon does not overlap any samples in the tile, testing each edge of the sub-polygon which is also part of an edge of the primitive against each sample point in the bounding box of the sub-polygon to determine if any sample point is inside the sub-polygon (1007, 1008); and

in response to determining that any sample point is inside the sub-polygon, determining that the primitive falls within the tile.

16. The method according to claim 15, further comprising, prior to determining how many vertices of the primitive fall within the tile:

generating a bounding box of the tile at sample precision (402);

generating a bounding box of the primitive at sample precision (404);
and

determining if the bounding boxes overlap (406); and

only in response to determining that the bounding boxes overlap,
determining how many vertices of the primitive fall within the tile.

17. A graphics processing system comprising a tiling unit for processing primitives for each of a plurality of tiles, the tiling unit being configured to:

determine whether a primitive that covers at least one sample position in a rendering space falls within a tile based on positions of samples within pixels in the tile; and

cause an association between the tile and the primitive to be stored to indicate that the primitive is present in the tile in response to determining that the primitive that covers at least one sample position in a rendering space does fall within the tile based on the positions of samples within pixels in the tile.

18. A graphics processing system according to claim 17, wherein the tiling unit is configured to cause an association between the tile and the primitive to be stored by causing an identifier for the primitive to be added to a control stream for the tile (408).

19. A graphics processing system according to claim 17, wherein the tiling unit is configured to cause an association between the tile and the primitive to be stored by causing an identifier for the tile to be added to a tile list for the primitive.

20. A graphics processing system according to any of claims 17-19, further comprising a rendering unit configured to: render primitives in a tile using the stored associations, wherein the rendering is performed at each sample position within the tile.

21. A graphics processing system according to any of claims 17-20, wherein the tiling unit is configured to perform the determination at a reduced sample precision.

22. A graphics processing system according to any of claims 17-21, wherein the tiling unit is configured to determine whether a primitive falls within a tile based on positions of samples within pixels in a tile by:

generating a bounding box of the tile at sample precision;

generating a bounding box of the primitive at sample precision;

determining if the bounding boxes overlap; and

in response to determining that the bounding boxes do not overlap, determining that the primitive does not fall within the tile.

23. A graphics processing system according to any of claims 17-22, wherein the tiling unit is configured to determine whether a primitive falls within a tile based on positions of samples within pixels in a tile by:

generating any intersection points between edges of the primitive and boundaries of the tile;

forming a sub-polygon inside the tile by replacing vertices of the primitive outside the tile with the intersection points;

generating a bounding box of the sub-polygon at sample precision;

determining if the bounding box of the sub-polygon overlaps any samples in the tile; and

in response to determining that the bounding box of the sub-polygon overlaps any samples in the tile, determining that the primitive falls within the tile.

24. A graphics processing system according to claim 23, wherein the tiling unit is configured to generate any intersection points between edges of the primitive and boundaries of the tile by:

generating a bounding box of the tile at sample precision; and

generating any intersection points between edges of the primitive and edges of the bounding box of the tile at sample precision.

25. A graphics processing system according to claim 23 or 24, wherein the tiling unit is configured to form a sub-polygon inside the tile by replacing vertices of the primitive outside the tile with the intersection points by:

forming an initial sub-polygon inside the tile by replacing vertices of the primitive outside the tile with the intersection points; and

if the initial sub-polygon has more than three vertices, dividing the initial sub-polygon into a plurality of smaller sub-polygons, each having only three vertices,

and wherein a bounding box is generated at sample precision for each smaller sub-polygon and it is determined, for each generated bounding box, if it overlaps any samples in the tile.

26. A graphics processing system according to any of claims 23-25, wherein the tiling unit is configured to determine if the bounding box of the sub-polygon overlaps any samples in the tile by:

identifying four sampling locations in the tile using the bounding box of the sub-polygon; and

determining if the bounding box of the sub-polygon misses all four sampling locations in the tile.

27. A graphics processing system according to any of claims 17-26, wherein the tiling unit is configured to determine whether a primitive falls within a tile based on positions of samples within pixels in a tile by:

generating any intersection points between edges of the primitive and boundaries of the tile;

forming a sub-polygon inside the tile by replacing vertices of the primitive outside the tile with the intersection points;

generating a bounding box of the sub-polygon at sample precision;

testing each edge of the sub-polygon which is also part of an edge of the primitive against each sample point in the bounding box of the sub-polygon to determine if any sample point is inside the sub-polygon; and

in response to determining that any sample point is inside the sub-polygon, determining that the primitive falls within the tile.

28. A graphics processing system according to claim 27, wherein the tiling unit is configured to generate any intersection points between edges of the primitive and boundaries of the tile by:

generating a bounding box of the tile at sample precision; and

generating any intersection points between edges of the primitive and edges of the bounding box of the tile at sample precision.

29. A graphics processing system according to claim 27 or 28, wherein the tiling unit is configured to form a sub-polygon inside the tile by replacing vertices of the primitive outside the tile with the intersection points by:

forming an initial sub-polygon inside the tile by replacing vertices of the primitive outside the tile with the intersection points; and

if the initial sub-polygon has more than three vertices, dividing the initial sub-polygon into a plurality of smaller sub-polygons, each having only three vertices,

and wherein a bounding box is generated at sample precision for each smaller sub-polygon and wherein testing each edge of the sub-polygon which is also part of an edge of the primitive against each sample point in the bounding box of the sub-polygon to determine if any sample point is inside the sub-polygon comprises:

for each smaller sub-polygon, testing each edge of the smaller sub-polygon which is also part of an edge of the primitive against each sample point in the bounding box of the smaller sub-polygon to determine if any sample point is inside the smaller sub-polygon.

30. A graphics processing system according to any of claims 27-29, wherein the tiling unit is configured to test each edge of the sub-polygon which is also part of an edge of the primitive against each sample point in the bounding box of the sub-polygon to determine if any sample point is inside the sub-polygon by:

computing edge parameters for each edge of the sub-polygon which is also part of an edge of the primitive; and

testing each sample point in the bounding box of the sub-polygon against each edge.

31. A graphics processing system according to any of claims 17-31, wherein the tiling unit is configured to determine whether a primitive falls within a tile based on positions of samples within a pixel by:

determining how many vertices of the primitive fall within the tile;

in response to determining that two or more vertices fall outside the tile, determining that the primitive falls within the tile;

in response to determining that less than two vertices fall within the tile, generating any intersection points between edges of the primitive and boundaries of the tile;

in response to generating more than two intersection points, determining that the primitive falls within the tile;

in response to generating exactly two intersection points for a primitive with only one vertex in the tile and where the intersection points are on different boundaries of the tile, determining that the primitive falls within the tile;

in response to generating exactly two intersection points for a primitive with no vertices in the tile and where the intersection points are on the same boundary of the tile or on different boundaries of the tile that do not cross within the primitive, determining that the primitive falls within the tile; and

in response to generating exactly two intersection points for a primitive with only one vertex in the tile and where the intersection points are on same boundary of the tile and in response to generating exactly two intersection points for a primitive with no vertices in the tile and where the intersection points are on different boundaries of the tile which cross within the primitive:

forming a sub-polygon inside the tile by replacing vertices of the primitive outside the tile with the intersection points;

generating a bounding box of the sub-polygon at sample precision;

determining if the bounding box of the sub-polygon overlaps any samples in the tile;

in response to determining that the bounding box of the sub-polygon overlaps any samples in the tile, determining that the primitive falls within the tile;

in response to determining that the bounding box of the sub-polygon does not overlap any samples in the tile, testing each edge of the sub-polygon which is also part of an edge of the primitive against each sample point in the bounding box of the sub-polygon to determine if any sample point is inside the sub-polygon; and

in response to determining that any sample point is inside the sub-polygon, determining that the primitive falls within the tile.

32. The graphics processing system according to claim 31, the tiling unit is further configured, prior to determining how many vertices of the primitive fall within the tile, to:

generate a bounding box of the tile at sample precision;

generate a bounding box of the primitive at sample precision; and

determine if the bounding boxes overlap; and

only in response to determining that the bounding boxes overlap, determine how many vertices of the primitive fall within the tile.

33. A graphics processing system configured to perform the method of any of claims 1 to 16.

34. The graphics processing system of any of claims 17-32 wherein the graphics processing system is embodied in hardware on an integrated circuit.

35. Computer readable code configured to perform the steps of the method of any of claims 1 to 16 when the code is run on a computer.

36. A computer readable storage medium having encoded thereon the computer readable code of claim 35.

37. A method of manufacturing, at an integrated circuit manufacturing system, a graphics processing system as claimed in any of claims 17 to 32.

38. An integrated circuit definition dataset that, when processed in an integrated circuit manufacturing system, configures the integrated circuit manufacturing system to manufacture a graphics processing system as claimed in any of claims 17 to 32.

39. A computer readable storage medium having stored thereon a computer readable description of an integrated circuit that, when processed in an integrated circuit manufacturing system, causes the integrated circuit manufacturing system to manufacture a graphics processing system as claimed in any of claims 17 to 32.

40. An integrated circuit manufacturing system comprising:

a non-transitory computer readable storage medium having stored thereon a computer readable description of an integrated circuit that describes a graphics processing system;

a layout processing system configured to process the integrated circuit description so as to generate a circuit layout description of an integrated circuit embodying the graphics processing system; and

an integrated circuit generation system configured to manufacture the graphics processing system according to the circuit layout description,

wherein the graphics processing system comprises a tiling unit for processing primitives for each of a plurality of tiles, the tiling unit being configured to:

determine whether a primitive that covers at least one sample position in a rendering space falls within a tile based on positions of samples within pixels in the tile; and

cause an association between the tile and the primitive to be stored to indicate that the primitive is present in the tile in response to determining that a primitive that covers at least one sample position in a rendering space does fall within a tile based on the positions of samples within pixels in the tile.



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Patents Act 1977: Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
X,Y	X:1-5, 7, 9-11, 13-15, 17-21, 23, 25-27, 29-31 and 33-40 Y: 8, 12, 16, 24, 28 and 32	US 2013/0342547 A1 (LUM et al) see whole document particularly paragraphs [0074] to [0086] and figures 5A-C and 6A and 6B
X,Y	X: 1-6, 17-22 and 33-40 Y: 8, 12, 16, 24, 28 and 32	US 8704836 B1 (NVIDIA CORP) See whole document particularly column 19 line 32 to column 20 line 25 and figure 6A
X	1-5, 17-21 and 33-40	GB 2511817 A (IMAGINATION TECH LTD) See whole document particularly page 3 lines 12-29
X	1-5, 17-21 and 33-40	US 2011/0080406 A1 (HAKURA et al) See whole document particularly paragraphs [0083]-[0084]
X	1-5, 17-21 and 33-40	GB 2401522 A (IMAGINATION TECH LTD) See whole document particularly from the last paragraph starting on page 15 onwards
X	1-5, 17-21 and 33-40	US 7400325 B1 (NVIDIA CORP) See whole document particularly column 8 lines 4-17

Categories:

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.



Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC^X :

Worldwide search of patent documents classified in the following areas of the IPC

G06T

The following online and other databases have been used in the preparation of this search report

EPODOC, WPI and TXTE

International Classification:

Subclass	Subgroup	Valid From
G06T	0011/40	01/01/2006
G06T	0015/00	01/01/2011