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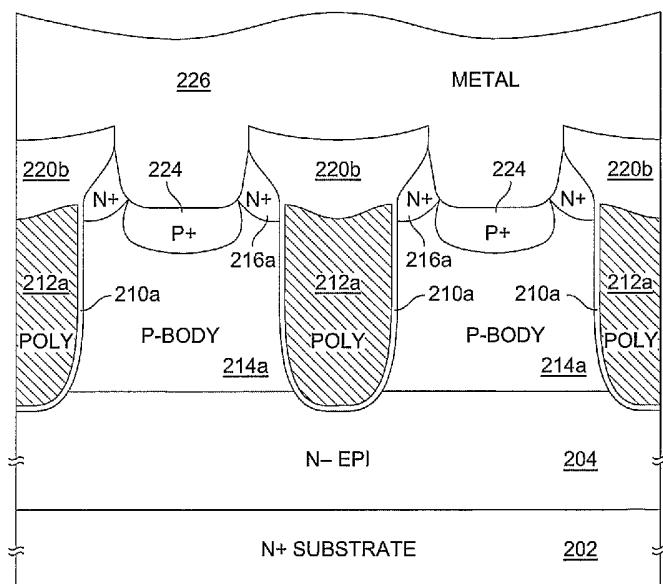
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(54) Title: STRUCTURE AND METHOD FOR FORMING A TRENCH MOSFET HAVING SELF-ALIGNED FEATURES



(57) Abstract: In accordance with an embodiment of the present invention, a semiconductor device is formed as follows. An exposed surface area of a silicon layer where silicon can be removed is defined. A portion of the silicon layer is removed to form a middle section of a trench extending into the silicon layer from the exposed surface area of the silicon layer. Additional exposed surface areas of the silicon layer where silicon can be removed are defined. Additional portions of the silicon layer are removed to form outer sections of the trench such that the outer sections of the trench extend into the silicon layer from the additional exposed surface areas of the silicon layer. The middle section of the trench extends deeper into the silicon layer than the outer sections of the trench.

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STRUCTURE AND METHOD FOR FORMING A TRENCH MOSFET HAVING SELF-ALIGNED FEATURES

BACKGROUND OF THE INVENTION

5 [0001] The present invention relates to semiconductor MOSFET technology and more particularly to a trench MOSFET having self-aligned features.

[0002] Power MOSFETs (metal oxide semiconductor field effect transistors) are well known in the semiconductor industry. One variety of power MOSFETs is the vertically-conducting trench MOSFET. A cross-section view of such a MOSFET is shown in Fig. 1.

10 MOSFET 100 has trenches 111 each including a polysilicon gate 112 insulated from body regions 114 by a gate dielectric 110. Source regions 116 flank each side of trenches 111. Dielectric layer 120 insulates gates 112 from overlying metal layer 126. Substrate region 102 forms the drain of MOSFET 100.

15 [0003] When MOSFET 100 is biased in the on state, current flows vertically between source regions 116 and substrate 102. The current capability of MOSFET 100 in the on state is a function of the drain to source resistance ($R_{ds_{on}}$). To improve the current capability of the MOSFET, it is necessary to reduce the $R_{ds_{on}}$. One way to reduce the $R_{ds_{on}}$ of the trench MOSFET is to increase the trench density (i.e., to increase the number of trenches per unit area). This may be achieved by reducing the cell pitch. However, reducing the cell pitch of 20 MOSFETs is limited by the particulars of the MOSFET cell structure and the specific process recipe used to manufacture the MOSFET. Reducing the cell pitch is made further difficult by such limitations of the manufacturing process technology as the minimum critical dimensions the photolithography tools are configured to resolve, the minimum required spacing between different cell regions as dictated by the design rules, and the misalignment tolerances.

25 [0004] The different dimensions that determine the minimum cell pitch for trench MOSFET 100 are shown in Fig. 1. Dimension A is the minimum trench width the photolithography tools are configured to resolve, dimension B is the minimum contact opening the photolithography tools are configured to resolve, dimension C is the minimum trench-to-contact spacing dictated by the design rules, and dimension D is the contact 30 registration error tolerance or contact misalignment tolerance. The minimum cell pitch for

MOSFET 100 thus equals A + B + 2C + 2D. Reduction of any of these dimensions without complicating the process technology is difficult to achieve.

[0005] Thus, a new approach wherein the cell pitch of the trench MOSFET can be reduced without increasing the process complexity is desirable.

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BRIEF SUMMARY OF THE INVENTION

[0006] In accordance with an embodiment of the present invention, a semiconductor device is formed as follows. An exposed surface area of a silicon layer where silicon can be removed is defined. A portion of the silicon layer is removed to form a middle section of a trench extending into the silicon layer from the exposed surface area of the silicon layer. Additional exposed surface areas of the silicon layer where silicon can be removed are defined. Additional portions of the silicon layer are removed to form outer sections of the trench such that the outer sections of the trench extend into the silicon layer from the additional exposed surface areas of the silicon layer. The middle section of the trench extends deeper into the silicon layer than the outer sections of the trench.

[0007] In another embodiment, a gate electrode partially filling the trench to below the outer sections of the trench is formed.

[0008] In another embodiment, the silicon layer comprises a body region. Impurities are implanted to form a first region in the body region. The first region extends along a surface 20 of the body region and directly below the outer sections of the trench.

[0009] In another embodiment, a dielectric layer extending only across a top surface of the trench is formed. Exposed silicon is removed until: (i) of the first region, only portions located substantially directly below the outer sections of the trench remain, the remaining portions of the first region forming source regions of the semiconductor device, and (ii) a 25 surface area of the body region becomes exposed.

[0010] In another embodiment, a sidewall of the dielectric layer is exposed. The exposed sidewall of the dielectric layer together with an exposed sidewall of each source region forms a sidewall of a contact opening for contacting the body region and source region.

[0011] In accordance with another embodiment of the present invention, a semiconductor 30 device is formed as follows. A masking layer is formed over a silicon layer. The masking layer has an opening through which a surface area of the silicon layer is exposed. The silicon

layer is isotropically etched through the masking layer opening so as to remove a bowl-shaped portion of the silicon layer. The bowl-shaped portion has a middle portion along the exposed surface area of the silicon layer and outer portions extending directly underneath the masking layer. The outer portions of the removed silicon layer which extend directly underneath the masking layer form outer sections of a trench. Additional portions of the silicon layer are removed through the masking layer opening so as to form a middle section of the trench which extends deeper into the silicon layer than the outer sections of the trench.

5 [0012] In accordance with yet another embodiment of the present invention, a semiconductor device is formed as follows. A plurality of trenches is formed in a silicon layer. A first region of a first conductivity type is formed in the silicon layer. An insulating layer filling an upper portion of each trench is formed. Exposed silicon is removed until at least: (i) an edge of the insulating layer in each trench is exposed, and (ii) of the first region, only a portion adjacent each trench sidewall remains. The remaining portion of the first region adjacent each trench sidewall forms a source region of the semiconductor device.

10 15 [0013] In accordance with another embodiment of the present invention, a semiconductor device comprises a trench in a silicon layer. A source region is in the silicon layer adjacent each sidewall of the trench. The trench sidewalls are shaped along the silicon layer such that the trench sidewalls fan out near the top of the trench to extend directly over at least a portion of each source region.

20 [0014] In another embodiment, a gate electrode partially fills the trench but overlaps each source region along the trench sidewalls. An insulating layer substantially fills a remaining portion of the trench over the gate electrode. A sidewall of the insulating layer in the trench together with a sidewall of a corresponding source region form a sidewall of a contact opening through which contact is made at least with the source region.

25 [0015] In another embodiment, a body region is adjacent each trench sidewall, and the body regions are of opposite conductivity type to that of the source regions. A metal layer contacts the body regions and the source regions through the contact opening.

30 [0016] In accordance with another embodiment of the present invention, a semiconductor device comprises a plurality of trenches in a silicon layer. An insulating layer fills an upper portion of each trench. A source region is in the silicon layer adjacent each trench sidewall such that a sidewall of each insulating layer together with a sidewall of a corresponding source region forms a contact opening between every two adjacent trenches.

[0017] The following detailed description and the accompanying drawings provide a better understanding of the nature and advantages of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

5 [0018] Fig. 1 shows a cross-section view of a conventional trench MOSFET;

[0019] Figs. 2A-2K show cross-section views at different stages of manufacturing a trench MOSFET in accordance with an embodiment of the present invention;

[0020] Fig. 3 is a graph showing the effect of cell pitch reduction on $R_{ds(on)}$;

[0021] Figs. 4A and 4B show an alternate method for forming trenches in accordance with 10 another embodiment of the invention; and

[0022] Fig. 5 is an exemplary cross-section view corresponding to that in Fig. 2K, and is provided to show a more accurate representation of the contours of the trenches in accordance with one embodiment of the invention.

15

DETAILED DESCRIPTION OF THE INVENTION

[0023] In accordance with the present invention, a structure and method for forming a trench MOSFET having self-aligned features which result in cell pitch reduction without increasing the process complexity are disclosed. In one embodiment, trenches are formed in an epitaxial layer in such manner that the trench sidewalls fan out near the top of the trench 20 over source regions. An insulating layer formed along a top portion of each trench together with the source regions define the contact openings between adjacent trenches for contacting the source and body regions. This structure and method of forming the trenches leads to a MOSFET which has source regions and contact openings self-aligned to the trenches. This in turn enables the 2D portion of the cell pitch of prior art MOSFET 100 (Fig. 1) to be 25 eliminated and the dimension B to be reduced to thus obtain a reduced cell pitch without introducing any process complexities

[0024] Figs. 2A-2K are cross-section views at different stages of manufacturing a trench MOSFET in accordance with an embodiment of the present invention. In Fig. 2A, a lightly doped N-type epitaxial layer 204 extends over a highly-doped N-type substrate 202. A layer 30 of a material which is resistant to silicon etch having a thickness in the range of 2,000-

10,000Å is formed over epitaxial layer 204. In one embodiment, an oxide layer having a thickness of about 5,000Å is used. Using a masking step, predefined portions of the layer of material resistant to silicon etch are removed so that only regions 206 remain. In the embodiment wherein an oxide layer is used, conventional dry or wet etch may be used to 5 remove the predefined portions of the oxide layer.

[0025] In Fig. 2B, a first silicon etch is carried out to form a mid-section 208 of a plurality of trenches. The spacing between regions 206 defines the width of mid-section 208 which is in the range of 0.2-2.0µm. Mid-section 208 extends from the exposed surface areas of epitaxial layer 204 to a depth in the range of 0.5-3.0µm. In one embodiment, the width and 10 depth of mid-section 208 are about 0.35µm and 1.0µm, respectively. Conventional methods for etching silicon, for example, reactive ion etching (REI), may be used to form mid-section 208 of the trenches.

[0026] In Fig. 2C, portions of regions 206 are removed to expose additional surface areas 207 of epitaxial layer 204. Smaller regions 206a having a thickness in the range of 1,000- 15 9,000Å thus remain. In the embodiment where regions 206 are from oxide, regions 206 are isotropically etched so that smaller oxide regions 206a having a thickness of about 2,500Å remain.

[0027] In Fig. 2D, a second silicon etch is carried out to remove portions of epitaxial layer 204 along its exposed surfaces to thereby form outer sections 208b of the trenches. As 20 shown, mid-section 208a extends deeper than outer sections 208b. Outer sections 208b extend from surface areas 208b of epitaxial layer 204 to a depth in the range of 0.1-1.0µm. In one embodiment, the depth of outer sections 208b is about 0.4µm. Note that the second silicon etch also removes silicon from along the bottom of the mid-section 208 though it is not necessary to do so. As with the first silicon etch, conventional methods for etching 25 silicon, for example, reactive ion etching (REI), may be used for the second silicon etch.

[0028] While Figs. 2A-2D show one method for forming trenches having a deep mid-section and shallow outer sections, the invention is not limited to this particular method. For example, an alternate method for forming trenches having similar physical characteristics is shown in Figs. 4A and 4B. After forming isolated regions 206 of for example oxide or 30 photoresist, as in Fig. 2A, an isotropic silicon etch is carried out so that openings 203 are created in epitaxial layer 204 between adjacent regions 206 as shown in Fig. 4A. The isotropic etch removes silicon from under regions 206 as shown. Next, keeping regions 206

intact, a conventional silicon etch is carried out to form deeper mid-sections 203a of the trenches as shown in Fig. 4B. As can be seen, each trench has a deep mid-section 203a and shallow outer sections 203b extending under regions 206.

[0029] Referring back to Figs. 2A-2K, in Fig. 2E, remaining regions 206a may optionally

5 be removed at this stage of the process. An insulating layer 210 is then formed along the surface of epitaxial layer 204 using conventional methods. Sidewalls of the trenches are thus coated with insulating layer 210. Insulating layer 210 has a thickness in the range of 50-1,000Å. In one embodiment, insulating layer 210 is a gate oxide having a thickness of about 400Å.

10 [0030] Next, using conventional polysilicon deposition techniques, a polysilicon layer 212 having a thickness in the range of 1,000-15,000Å is deposited over insulating layer 210 to fill the trenches. In one embodiment, polysilicon layer 212 has a thickness of about 5,500Å and is doped with impurities. In yet another embodiment, prior to forming polysilicon layer 212, a thick insulating layer is formed along the bottom of the mid-section 208a of the trenches.

15 This advantageously reduces the gate capacitance of the MOSFET.

[0031] In Fig. 2F, polysilicon layer 212 is etched back to form gates 212a in mid-section 208a of the trenches. Polysilicon layer 212 is etched back such that its upper surface is recessed below the outer sections 208b of the trenches. This insures that no polysilicon is left in the outer sections 208b of the trenches which may otherwise short the gate to the source 20 and also block the source and body implants carried out later in the process. However, the extent to which the polysilicon layer 212 is etched back must be carefully controlled to insure that at least a portion of the gate overlaps with the source regions formed in later steps. Conventional polysilicon etching techniques may be used to etch back polysilicon layer 212.

[0032] P-type body regions 214 are then formed in epitaxial layer 204 between adjacent

25 trenches by implanting P-type impurities such as boron. The P-type implant is symbolically shown by arrows 218 which indicate that no mask is needed. Body regions 214 extend into epitaxial layer 204 to a depth primarily dictated by the target channel length. Next, highly-doped N-type regions 216 are formed in body regions 214 by implanting N-type impurities such as arsenic or phosphorous. N-type regions 216 extend along the top surface of body 30 regions 214 and directly below outer sections 208b of the trenches. The N-type implant is symbolically shown by arrows 219 which indicate that no masking is needed for this implant either. Conventional ion implantation techniques may be used for both implant steps.

[0033] In Fig. 2G, a dielectric layer 220, such as BPSG, is formed over the entire structure using conventional techniques. Dielectric layer 220 has a thickness in the range of 2,000-15,000 Å. In one embodiment, the thickness of dielectric layer 220 is about 8,000 Å. Next, a conventional dielectric flow step is carried out to obtain a planar surface as shown in Fig. 2H. 5 Dielectric layer 220a is then etched until silicon is reached as shown in Fig. 2I. After the dielectric etch, dielectric regions 220b which are fully contained in the trenches remain while surface areas of N-type regions 216 are exposed.

[0034] In Fig. 2J, a conventional silicon etch is carried out to form contact openings 222. Sufficient amount of silicon is removed so that along with the upper portion of N-type 10 regions 216 a top layer of body regions 214 is also removed. This insures that: (i) a top surface of body regions 214a becomes exposed so that contact can be made to body regions 214a, (ii) of N-type region 216, source regions 216a separated by body regions 214a remain, and (iii) sidewall areas of source regions 216a become exposed so that contact can be made to source regions 216a. In Fig. 2K, metal layer 226 is deposited to contact body regions 214a 15 and source regions 216a. Before metal 226 is deposited, a layer of heavily doped P-type region 224 may optionally be formed along the top surface of body regions 214a using conventional ion implantation techniques. The heavily doped region 224 helps achieve an ohmic contact between metal 226 and body region 214a. As shown, metal layer 224 is insulated from gates 212a by the dielectric layer 220b extending along the top surface of each 20 trench.

[0035] Referring back to Fig. 2J, the silicon etch carried out to form contact openings 222 exposes portions of insulating layer 210 extending along the sidewalls of outer sections 208b of the trenches. As can be seen, the exposed portions of insulating layer 210 together with the exposed sidewall area of source regions 216a advantageously define contact openings 222 25 between adjacent trenches. Thus, with no masking steps used in forming either source regions 216a or contact openings 222, source regions 216a and contact openings 222 which are self-aligned to the trenches are formed.

[0036] Because source regions 216a and contact openings 222 are self-aligned to the 30 trenches, the need to account for contact misalignment as in conventional techniques (dimension D in Fig. 1) is eliminated. Furthermore, the contact openings (dimension B in Fig. 1) can be made smaller than the photolithography tools are typically configured to resolve. Thus, not only the 2D term is eliminated from the minimum cell pitch A + B + 2C +

2D of the conventional trench MOSFET in Fig. 1, but the term B can be made much smaller. For the same process technology, a much smaller cell pitch is therefore obtained without increasing the process complexity.

[0037] The small cell pitch results in an increase in the number of trenches per unit area which in turn has the desirable effect of lowering the $R_{ds_{on}}$. This is more clearly shown in Fig. 3. Fig. 3 is a graph showing the effect of cell pitch reduction on $R_{ds_{on}}$. The vertical axis represents $R_{ds_{on}}$ and the horizontal axis represents the cell pitch. The numbers along the vertical axis are merely illustrative and do not reflect actual values of $R_{ds_{on}}$. Two curves are shown with the upper curve corresponding to a gate-source bias of 4.5V and the lower curve corresponding to a gate-source bias of 10V. For the same process technology, the self-aligned features of the present invention result in a reduction of the cell pitch from 1.8 μ m to 1.0 μ m. This cell pitch reduction results in about a 30% reduction in $R_{ds_{on}}$ in the case of 10V biasing and about a 25% reduction in the case of 4.5V biasing.

[0038] The cross-section views in Figs. 2A-2K are merely illustrative and are not intended to limit the layout or other structural aspects of the cell array. Furthermore, these figures may not accurately reflect the actual shape of all the various regions as they would appear in an actual device. Fig. 5 is an exemplary cross-section view corresponding to that in Fig. 2K, and is provided to show a more accurate representation of the contours of the trenches in accordance with one embodiment of the invention. Because of the small dimensions of some of the regions and the effects of such processing steps as temperature cycles, a rounding of many of the corners occurs during processing. As a result, the trenches appear Y-shaped as shown in Fig. 5 rather than T-shaped as shown in Fig. 2K. However, it is to be understood that the invention is not limited to a particular shape of the trenches.

[0039] While the above is a complete description of the embodiments of the present invention, it is possible to use various alternatives, modifications and equivalents. For example, the process steps depicted in Figs. 2A-2K are for manufacturing an N-channel MOSFET. Modifying these process steps to obtain an equivalent P-channel MOSFET would be obvious to one skilled in the art in light of the above teachings. Similarly, modifying the process steps to obtain other types of semiconductor devices such as insulated gate bipolar transistor (IGBT) would be obvious to one skilled in the art in light of the above teachings.

[0040] Also, body region 214 (Fig. 2F) may be formed earlier in the processing sequence. For example, in Fig. 2A, prior to forming regions 206, P-type impurities may be implanted

into epitaxial layer 204 or a P-type epitaxial layer may be grown over epitaxial layer 204. Similarly, N-type regions 216 (Fig. 2F) may be formed earlier in the processing sequence. For example, a blanket implant of N-type impurities may be carried out to form a highly-doped N-type region in the body region before forming the trenches. The highly-doped N-type region however needs to extend deeper into the body region than that depicted in Fig. 2F so that after the trenches are formed, at least a portion of the N-type region extends below the outer sections of the trenches. Also, a deeper silicon etch would be required in Fig. 2J in order to reach a surface of the body region.

5 [0041] In a further variation, epitaxial layer 204 may have a graded doping concentration rather than a fixed doping concentration, or may be made of a number of epitaxial layers each having a different doping concentration, or may be eliminated all together depending on the design goals. Moreover, the trenches may extend clear through epitaxial layer 204 and terminate within substrate 202.

10 [0042] Therefore, the scope of the present invention should be determined not with reference to the above description but should, instead, be determined with reference to the appended claim, along with their full scope of equivalents.

WHAT IS CLAIMED IS:

- 1 1. A method of forming a semiconductor device, comprising:
2 defining an exposed surface area of a silicon layer where silicon can be
3 removed;
4 removing a portion of the silicon layer to form a middle section of a trench
5 extending into the silicon layer from the exposed surface area of the silicon layer;
6 defining additional exposed surface areas of the silicon layer where silicon can
7 be removed; and
8 removing additional portions of the silicon layer to form outer sections of the
9 trench, the outer sections of the trench extending into the silicon layer from the additional
10 exposed surface areas of the silicon layer, the middle section of the trench extending deeper
11 into the silicon layer than the outer sections of the trench.
- 1 2. The method of claim 1 wherein the step of removing additional
2 portions of the silicon layer shapes the sidewalls of the trench such that an upper portion of
3 trench sidewalls fan out near the top of the trench to extend directly over a portion of the
4 silicon layer adjacent each trench sidewall.
- 1 3. The method of claim 1 wherein:
2 the step of defining an exposed surface area of a silicon layer comprises
3 forming and removing a portion of an insulating layer to define the exposed surface area of
4 the silicon layer; and
5 the step of defining additional exposed surface areas of the silicon layer
6 comprises isotropically etching remaining regions of the insulating layer to expose the
7 additional surface areas of the silicon layer.
- 1 4. The method of claim 1 wherein the silicon layer comprises a body
2 region, the method further comprising:
3 prior to forming the trench, implanting impurities to form a first region of a
4 conductivity type opposite that of the body region along a surface of the body region such
5 that after the trench is formed: (i) the trench extends through the first region and the body
6 region so as to divide each of the first region and the body region into two portions, and (ii)
7 the two portions of the first region extend along surface areas of corresponding two portions
8 of the body region and directly below the outer sections of the trench.

1 5. The method of claim 4 wherein the body region is an epitaxial layer.

1 6. The method of claim 4 wherein the silicon layer comprises an epitaxial
2 layer, the method further comprising:

3 implanting impurities to form the body region in the epitaxial layer, the body
4 region having a conductivity type opposite that of the epitaxial layer.

1 7. The method of claim 1 further comprising:
2 forming a gate electrode partially filling the trench to below the outer sections
3 of the trench.

1 8. The method of claim 7 wherein the step of forming a gate electrode
2 comprises:

3 forming a gate insulator extending at least along the trench sidewalls;
4 depositing polysilicon; and
5 etching back the polysilicon so that the polysilicon partially fills the trench to
6 below the outer sections of the trench.

1 9. The method of claim 7 wherein the silicon layer comprises a body
2 region, the method further comprising:
3 implanting impurities to form a first region in the body region, the first region
4 extending along a surface of the body region and directly below the outer sections of the
5 trench.

1 10. The method of claim 9 further comprising:
2 forming the body region prior to forming the trenches.

1 11. The method of claim 9 wherein the body region is an epitaxial layer,
2 and the trench extends through the body region.

1 12. The method of claim 9 wherein:
2 the silicon layer comprises an epitaxial layer extending over a substrate, the
3 body region being in the epitaxial layer, and
4 the epitaxial layer, the substrate, and the first region have a conductivity type
5 opposite that of the body region.

1 13. The method of claim 9 further comprising:
2 forming a dielectric layer extending only across a top surface of the trench;
3 and

4 removing exposed silicon until: (i) of the first region, only portions located
5 substantially directly below the outer sections of the trench remain, the remaining portions of
6 the first region forming source regions of the semiconductor device, and (ii) a surface area of
7 the body region becomes exposed.

1 14. The method of claim 13 wherein the exposed silicon removing step
2 exposes a sidewall of the dielectric layer, the sidewall of the dielectric layer together with an
3 exposed sidewall of each source region forming a sidewall of a contact opening for
4 contacting the body region and source region.

1 15. The method of claim 13 wherein the step of forming a dielectric layer
2 comprises:

3 forming a dielectric layer extending over the trench and the body region, the
4 dielectric layer substantially filling a remaining portion of the trench over the gate electrode;
5 performing a dielectric flow to planarize the top surface of the dielectric layer;
6 and

7 uniformly etching the dielectric layer until silicon is reached, wherein upon
8 reaching silicon: (i) only a portion of the dielectric layer extending across the top surface of
9 the trench remains, and (ii) a surface area of the first region is exposed.

1 16. The method of claim 13 further comprising:
2 forming a highly doped region of the same conductivity type as the body
3 region along the exposed surface area of the body region; and
4 forming a metal layer to contact the highly doped region and the source
5 regions.

1 17. A method of forming a trench MOSFET, comprising:
2 forming a first insulating layer over a silicon layer;
3 removing predefined portions of the first insulating layer to define isolated
4 exposed surface areas of the silicon layer;

5 performing a first silicon etch to form a middle section of each of a plurality of
6 trenches extending into the silicon layer from the isolated exposed surface areas of the silicon
7 layer;

8 isotropically etching remaining regions of the first insulating layer to expose
9 additional surface areas of the silicon layer; and

10 performing a second silicon etch to form outer sections of each trench, the
11 outer sections of the trenches extending into the silicon layer from the additional exposed
12 surface areas of the silicon layer, the middle section of each trench extending deeper into the
13 silicon layer than its outer sections.

1 18. The method of claim 17 wherein the isotropically etching step shapes
2 the sidewalls of each trench such that an upper portion of the trench sidewalls fan out near the
3 top of the trench to extend directly over a portion of the silicon layer adjacent each trench
4 sidewall.

1 19. The method of claim 17 further comprising:
2 forming a gate insulator extending at least along the sidewalls of each trench;
3 and
4 forming a polysilicon layer partially filling each trench to below the outer
5 sections of each trench.

1 20. The method of claim 19 wherein the silicon layer comprises an
2 epitaxial layer in which the trench is formed, the method further comprising:
3 implanting impurities to form body regions of opposite conductivity type to
4 that of the epitaxial layer in the epitaxial layer between adjacent trenches; and
5 implanting impurities to form a first region of opposite conductivity type to
6 that of the body regions in each body region, each first region extending along a surface of a
7 corresponding body region and directly below the outer sections of adjacent trenches.

1 21. The method of claim 20 further comprising:
2 forming a substantially planar surface using a second insulating layer such that
3 a surface area of each first region is exposed while the second insulating layer substantially
4 fills a remaining portion of each trench over the corresponding gate electrode; and
5 removing exposed silicon until: (i) of each first region, only portions located
6 substantially directly below the outer sections of adjacent trenches remain, the remaining

7 portions of the first region forming source regions of the MOSFET, and (ii) a surface area of
8 each body region becomes exposed.

1 22. The method of claim 21 wherein the exposed silicon removing step
2 exposes a sidewall of the second insulating layer in each trench such the sidewall of the
3 second insulating layer in each trench together with exposed sidewalls of source regions form
4 contact openings between every two adjacent trenches, the method further comprising:

5 forming a metal layer to contact the exposed surface area of each body region
6 and the exposed sidewalls of the source regions through the contact openings.

1 23. The method of claim 21 wherein the step of forming a substantially
2 planar surface comprises:

3 forming a second insulating layer extending over the trenches and the body
4 regions, the second insulating layer substantially filling a remaining portion of each trench
5 over the corresponding gate electrode;

6 performing a dielectric flow to planarize the top surface of the second
7 insulating layer; and

8 uniformly etching the dielectric layer until silicon is reached, wherein upon
9 reaching silicon: (i) only portions of the second insulating layer extending across the top
10 surface of each trench remain, and (ii) a surface area of each first region is exposed.

1 24. A method of forming a semiconductor device, comprising:

2 forming a masking layer over a silicon layer, the masking layer having an
3 opening through which a surface area of the silicon layer is exposed;

4 isotropically etching the silicon layer through the masking layer opening so as
5 to remove a bowl-shaped portion of the silicon layer, the bowl-shaped portion having a
6 middle portion along the exposed surface area of the silicon layer and outer portions
7 extending directly underneath the masking layer, wherein the outer portions of the removed
8 silicon layer extending directly underneath the masking layer form outer sections of a trench;
9 and

10 removing additional portions of the silicon layer through the masking layer
11 opening so as to form a middle section of the trench which extends deeper into the silicon
12 layer than the outer sections of the trench.

1 25. The method of claim 24 wherein the silicon layer comprises a body
2 region, the method further comprising:

3 forming a gate electrode partially filling the trench;

4 forming an insulating layer substantially filling a remaining portion of the
5 trench over the gate electrode;

6 removing exposed silicon adjacent the trench such that: (i) an edge of the
7 insulating layer in the trench becomes exposed, the edge of the insulating layer forming a
8 sidewall of a contact opening; and (ii) a surface area of the body region becomes exposed;
9 and

10 forming a metal layer contacting the exposed surface areas of the body region
11 through the contact opening.

1 26. A method of forming a semiconductor device, comprising:

2 forming a plurality of trenches in a silicon layer;

3 forming an insulating layer filling an upper portion of each trench; and

4 removing exposed silicon from adjacent the trenches to expose an edge of the
5 insulating layer in each trench, the exposed edge of the insulating layer in each trench
6 defining a portion of each contact opening formed between every two adjacent trenches.

1 27. The method of claim 26 further comprising:

2 prior to removing exposed silicon, forming a first region of a first conductivity
3 type in the silicon layer so that after said exposed silicon removing step, of the first region,
4 only a portion adjacent each trench sidewall remains, the remaining portion of the first region
5 adjacent each trench sidewall forming a source region of the semiconductor device,

6 wherein the step of removing exposed silicon further exposes a sidewall of
7 each source region such that the exposed edge of the insulating layer in each trench together
8 with the exposed sidewall of a corresponding source region form one sidewall of a contact
9 opening between every two adjacent trenches.

1 28. The method of claim 26 further comprising:

2 forming a gate electrode filling a lower portion of each trench, the insulating
3 layer substantially filling a remaining portion of each trench.

1 29. A method of forming a semiconductor device, comprising:
2 forming a plurality of trenches in a silicon layer;
3 forming a first region along a surface of the silicon layer;
4 forming an insulating layer fully contained within each trench, the insulating
5 layer in each trench extending directly over a portion of the first region adjacent each trench
6 sidewall; and

7 removing exposed silicon from adjacent each trench until, of the first region,
8 only the portions adjacent the trench sidewalls remain, the remaining portions of the first
9 region adjacent the trench sidewalls forming source regions which are self-aligned to the
10 trenches.

1 30. A method of forming a semiconductor device, comprising:
2 removing portions of a silicon layer such that a trench having sidewalls which
3 fan out near the top of the trench to extend directly over a portion of the silicon layer is
4 formed in the silicon layer; and
5 forming source regions in the silicon layer adjacent the trench sidewall such
6 that the source regions extend into the portions of the silicon layer directly over which the
7 trench sidewalls extend.

1 31. A method of forming a semiconductor device, comprising:
2 removing portions of a silicon layer such that a plurality of trenches are
3 formed each having sidewalls which fan out near the top of the trench to extend directly over
4 a portion of the silicon layer adjacent each trench sidewall;
5 forming a gate electrode partially filling each trench;
6 forming an insulating layer in each trench, the insulating layer extending over
7 each gate electrode and over the portions of the silicon layer which extend directly under the
8 trench sidewalls; and
9 removing exposed silicon to expose an edge of the insulating layer in each
10 trench, the exposed edge of the insulating layer in each trench defining a portion of each
11 contact opening formed between every two adjacent trenches.

1 32. The method of claim 31 further comprising:
2 forming a first region of a first conductivity type in the silicon layer, wherein
3 the step of removing exposed silicon removes portions of the first region such that of the first

4 region only portions adjacent each trench sidewall remain, the remaining portions of the first
5 region adjacent each trench sidewall forming a source region of the semiconductor device.

1 33. A semiconductor device comprising:
2 a trench in a silicon layer; and
3 a source region formed in the silicon layer adjacent each sidewall of the
4 trench, wherein the trench sidewalls are shaped along the silicon layer such that the trench
5 sidewalls fan out near the top of the trench to extend directly over a substantial portion of
6 each source region.

1 34. The semiconductor device of claim 33 further comprising:
2 a gate electrode partially filling the trench but overlapping each source region
3 along the trench sidewalls; and
4 an insulating layer substantially filling a remaining portion of the trench over
5 the gate electrode, wherein a sidewall of the insulating layer in the trench together with a
6 sidewall of a corresponding source region form a sidewall of a contact opening through
7 which contact is made at least with the source region.

1 35. The semiconductor device of claim 34 further comprising:
2 a body region adjacent each trench sidewall, the body regions being of
3 opposite conductivity type to that of the source regions; and
4 a metal layer contacting the body regions and the source regions through the
5 contact opening.

1 36. The semiconductor device of claim 33 wherein the insulating layer is
2 fully contained within the trench.

1 37. A trench MOSFET comprising:
2 a plurality of trenches formed in silicon layer such that sidewalls of each
3 trench along the silicon layer fan out near the top of the trench to extend directly over a
4 portion of the silicon layer;
5 a gate electrode partially filling each trench;
6 an insulating layer substantially filling a remaining portion of each trench, the
7 insulating layer in each trench being fully contained within the trench;
8 a plurality of body regions in the silicon layer, each body region extending
9 between two adjacent trenches; and

10 a source region formed adjacent each trench sidewall in the body regions such
11 that the insulating layer extends directly over at least a portion of each source region, the
12 source regions being of opposite conductivity type to the body regions.

1 38. The trench MOSFET of claim 37 wherein sidewalls of the insulating
2 layer in each trench together with corresponding sidewalls of the source regions form a
3 contact opening between every two adjacent trenches.

1 39. The trench MOSFET of claim 38 further comprising:
2 a metal layer contacting the body region and the source regions through the
3 contact openings.

1 40. The trench MOSFET of claim 37 wherein the gate electrode in each
2 trench overlaps corresponding source regions but is recessed below the portion of the trench
3 sidewalls where the trench sidewalls start to fan out.

1 41. The trench MOSFET of claim 37 wherein:
2 the silicon layer further comprises an epitaxial layer extending over a
3 substrate, the body regions being formed in the epitaxial layer, and
4 the substrate, the epitaxial layer, and the source regions have a conductivity
5 type opposite that of the body regions.

1 42. A semiconductor device comprising:
2 a plurality of trenches in a silicon layer;
3 an insulating layer filling an upper portion of each trench, the insulating layer
4 being contained within each trench; and
5 a source region formed in the silicon layer adjacent each trench sidewall such
6 that a sidewall of the insulating layer in each trench together with a sidewall of a
7 corresponding source region form a contact opening between every two adjacent trenches.

1 43. The semiconductor device of claim 42 wherein the insulating layer in
2 each trench extends over a substantial portion of corresponding source regions, the
3 semiconductor device further comprising:
4 a metal layer contacting at least the source regions through the contact
5 openings.

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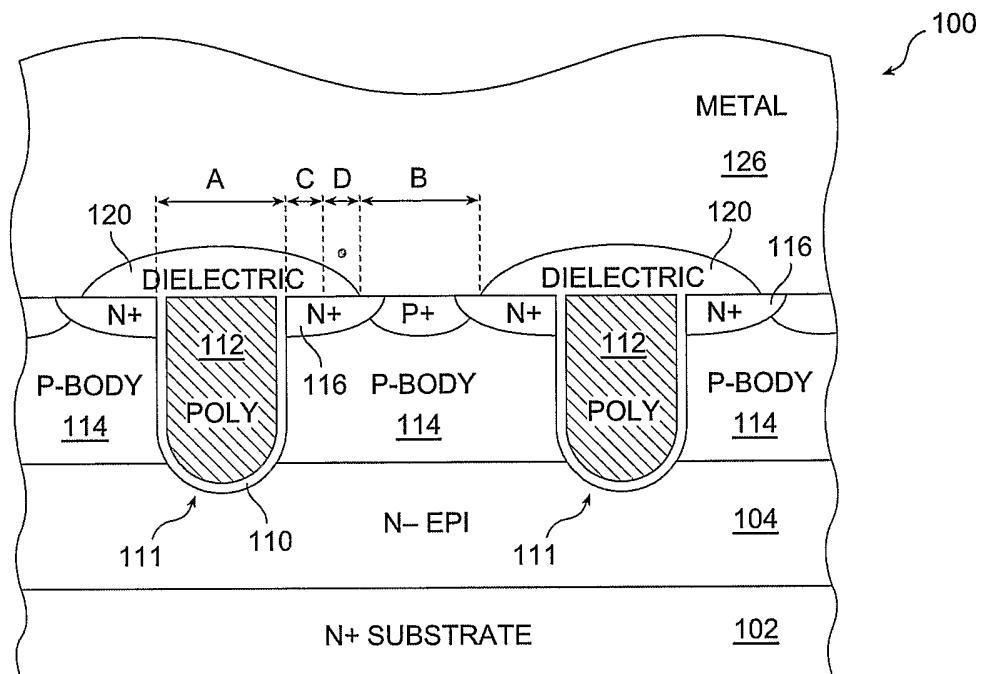


FIG. 1
(PRIOR ART)

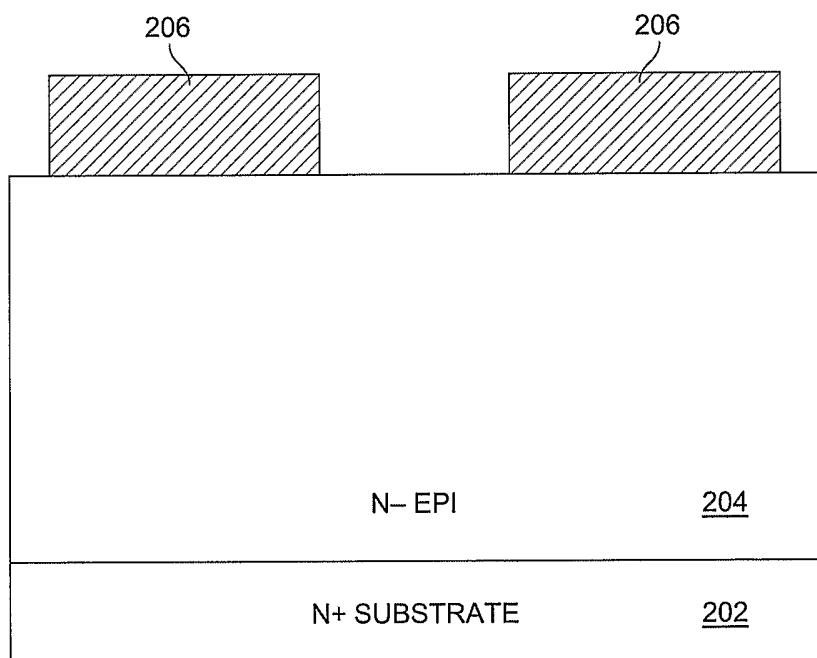


FIG. 2A

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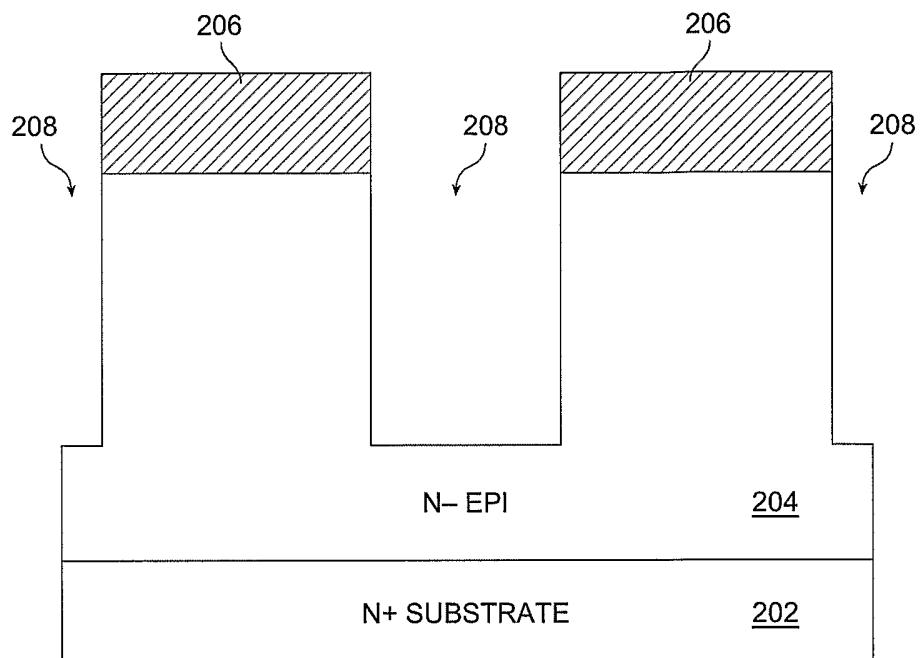


FIG. 2B

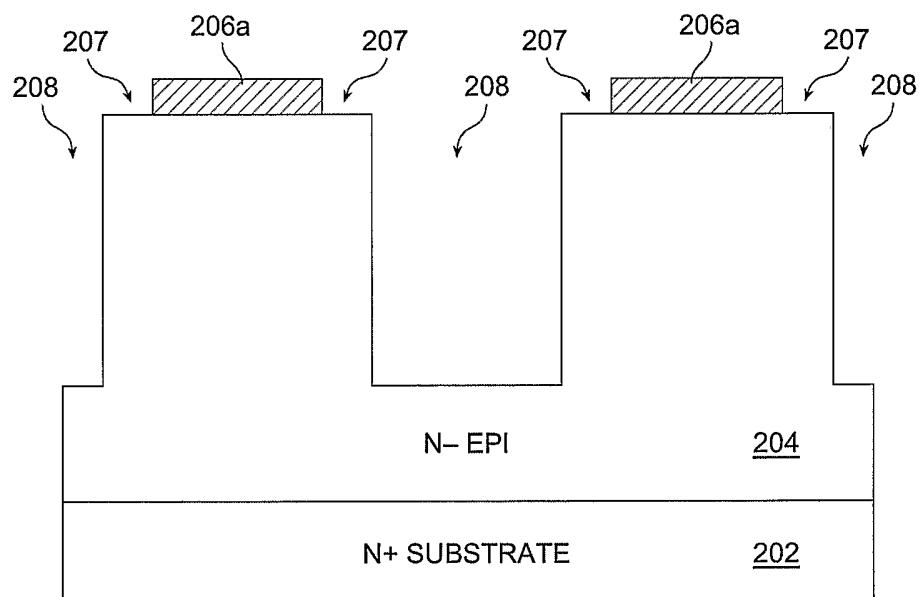


FIG. 2C

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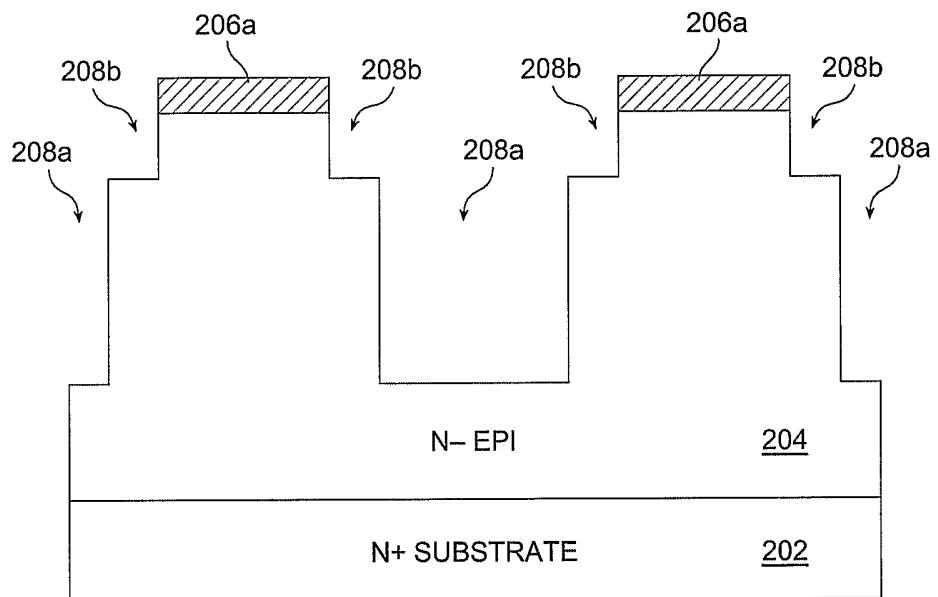


FIG. 2D

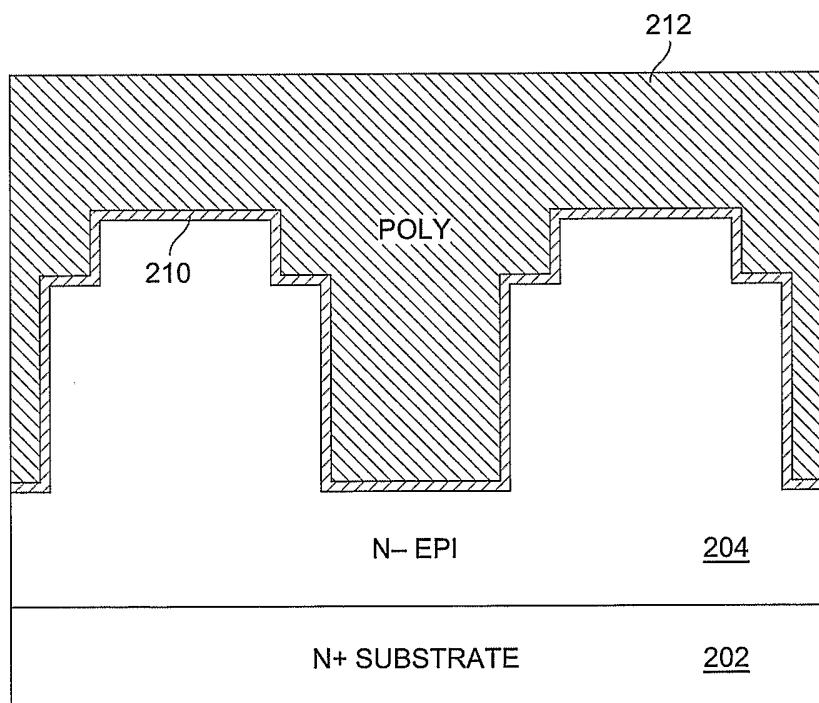


FIG. 2E

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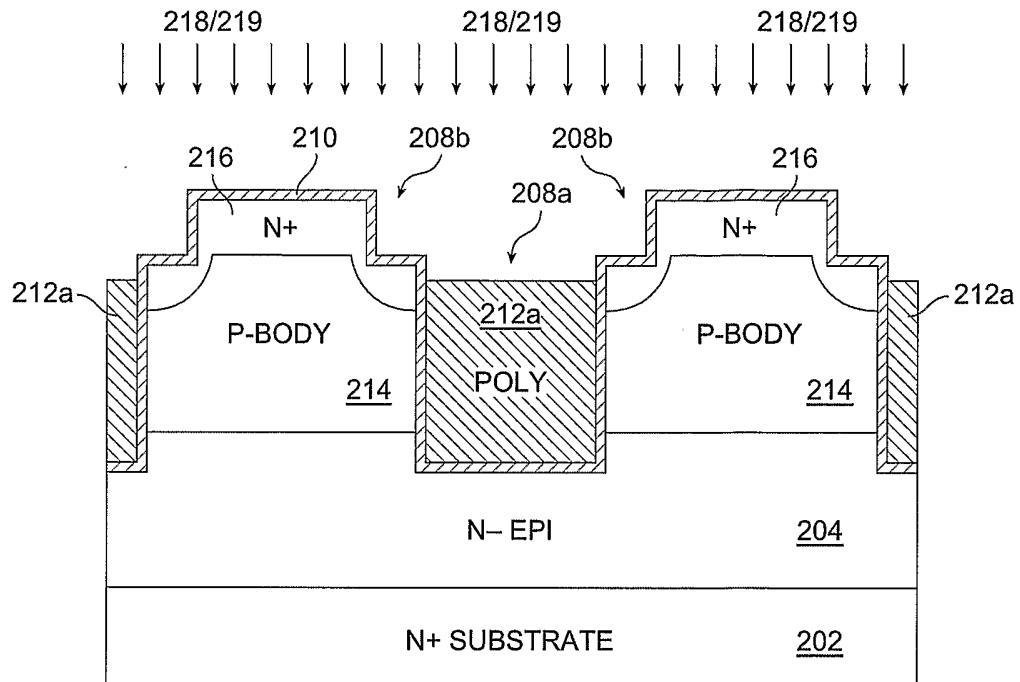


FIG. 2F

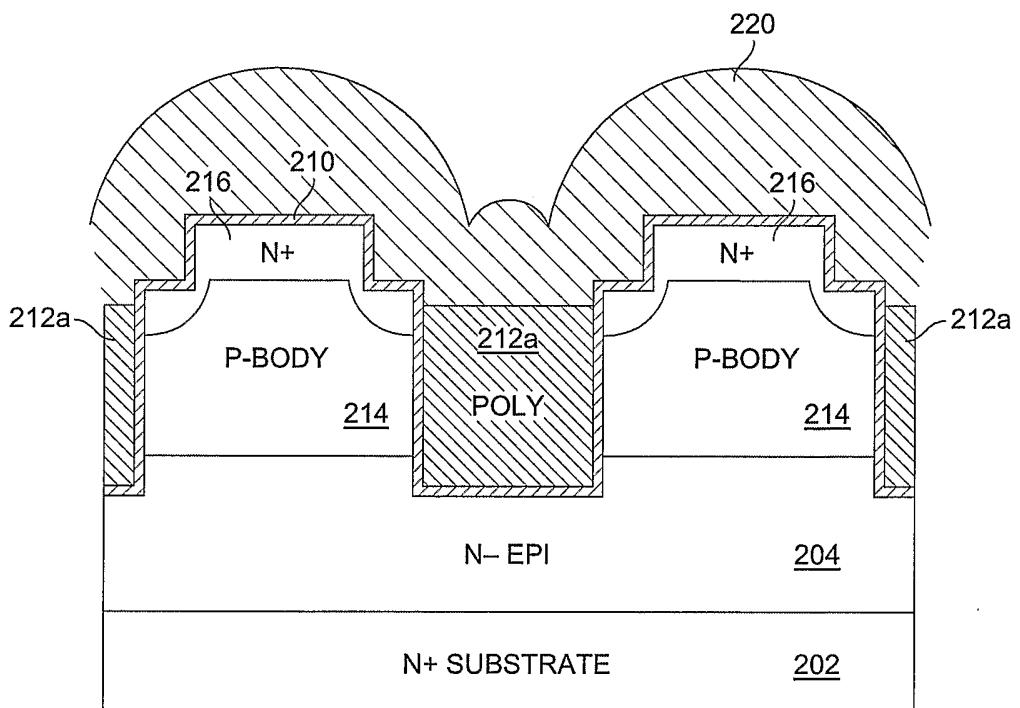


FIG. 2G

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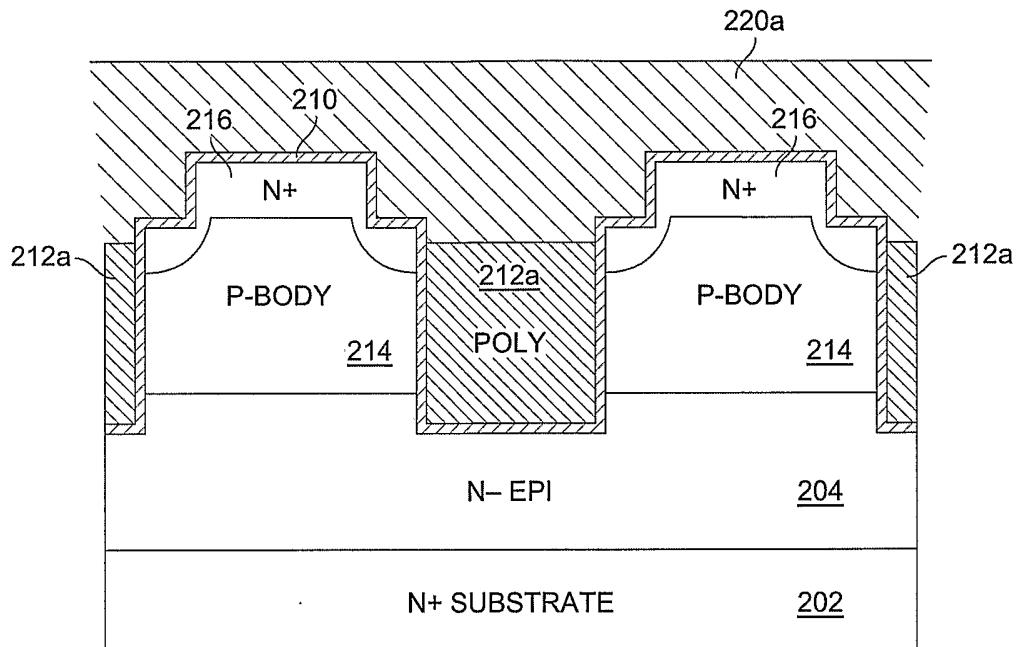


FIG. 2H

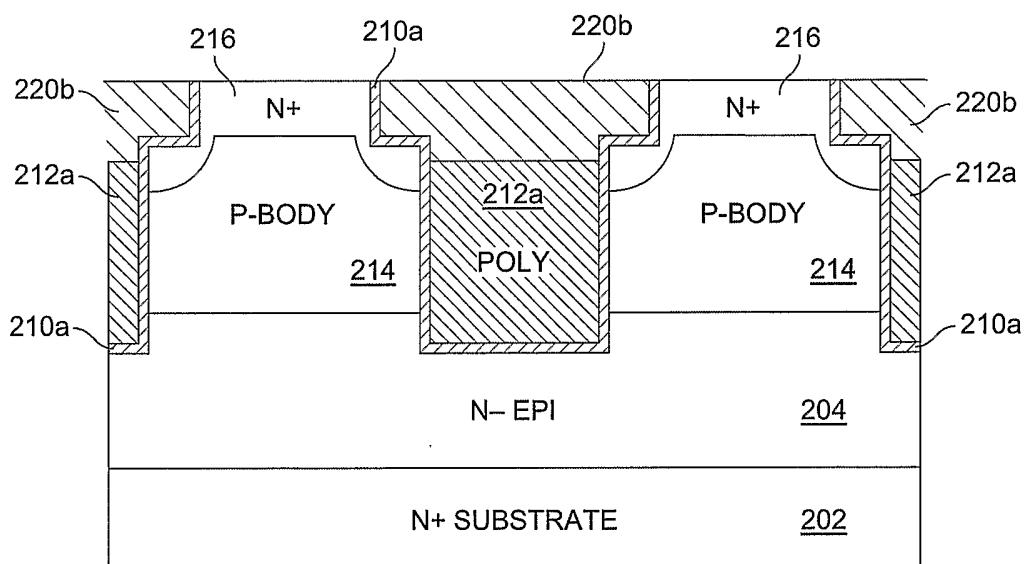


FIG. 2I

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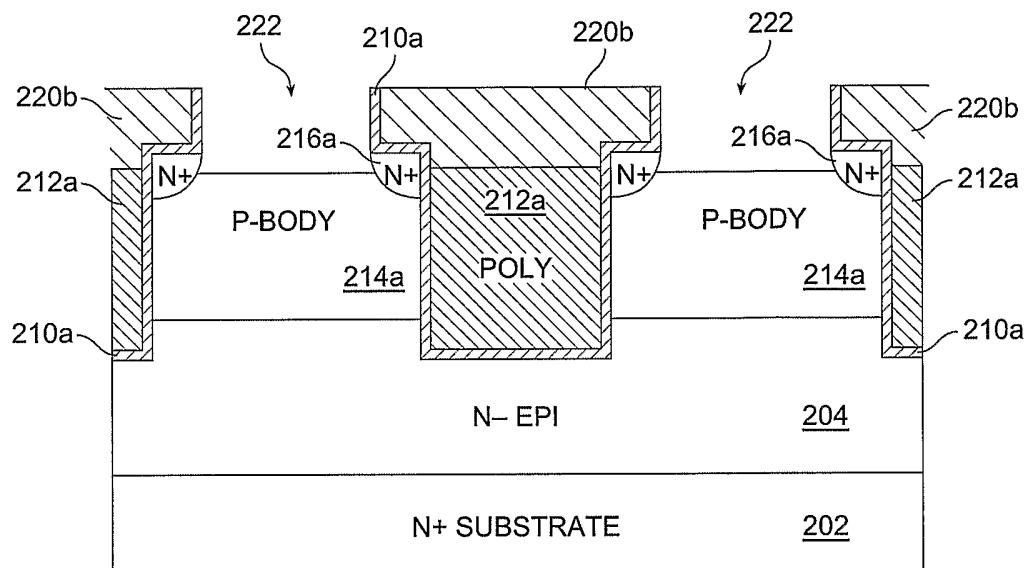


FIG. 2J

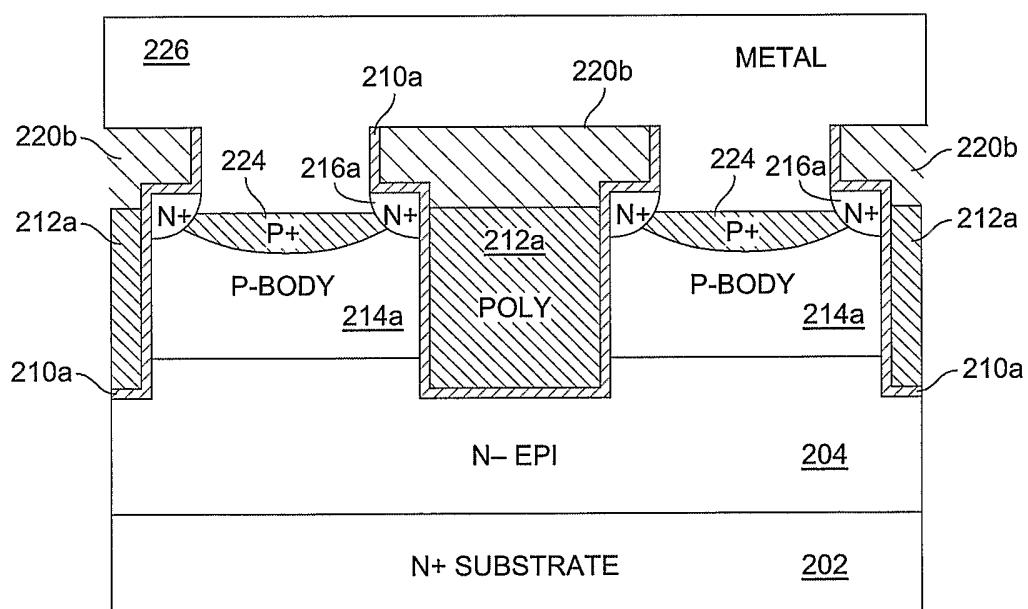


FIG. 2K

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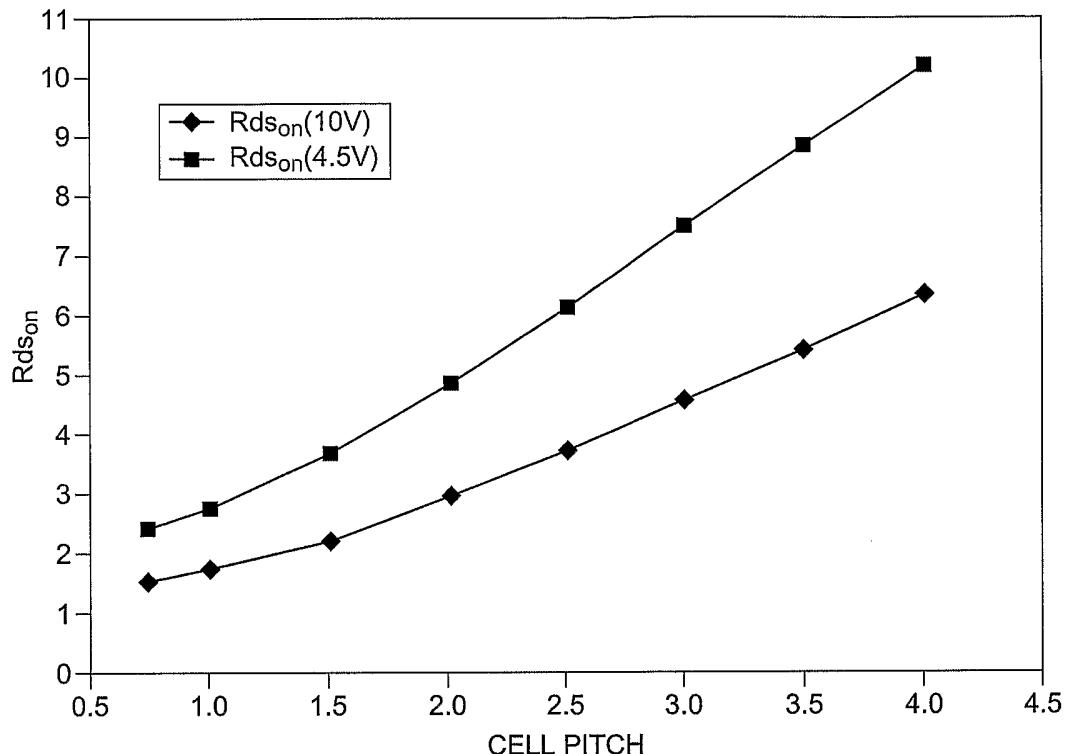


FIG. 3

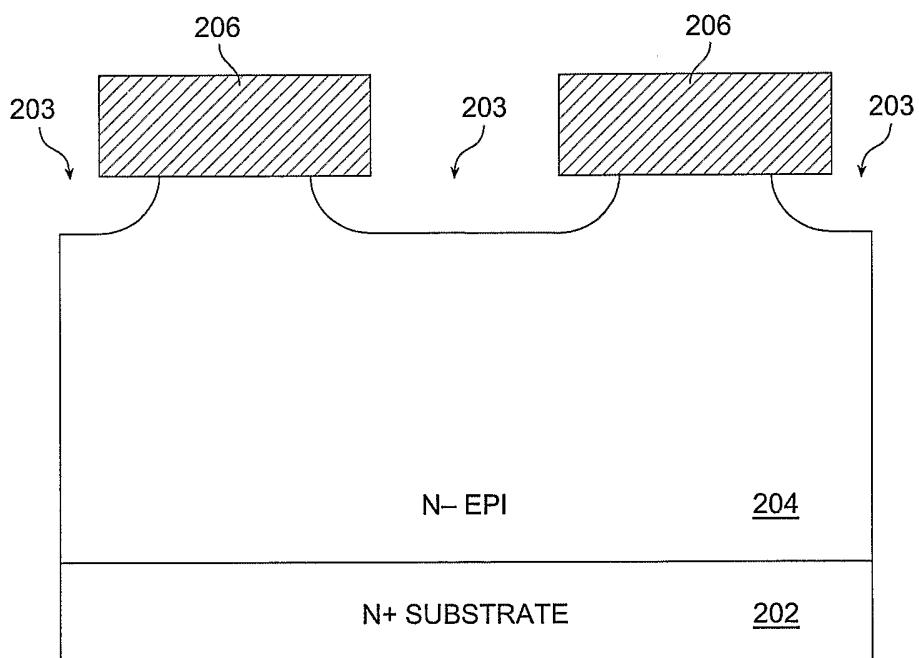


FIG. 4A

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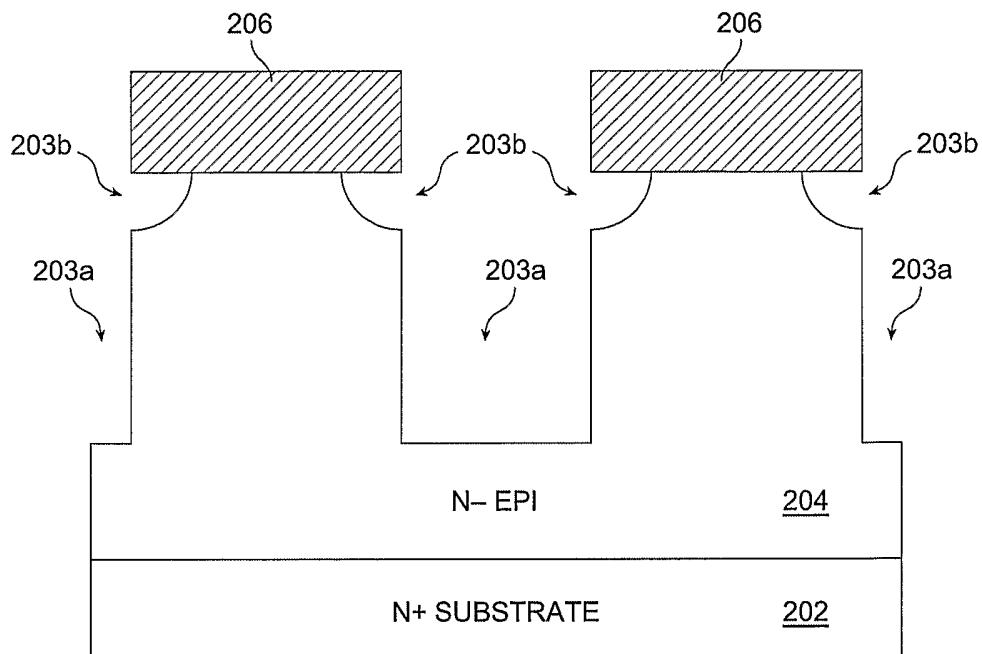


FIG. 4B

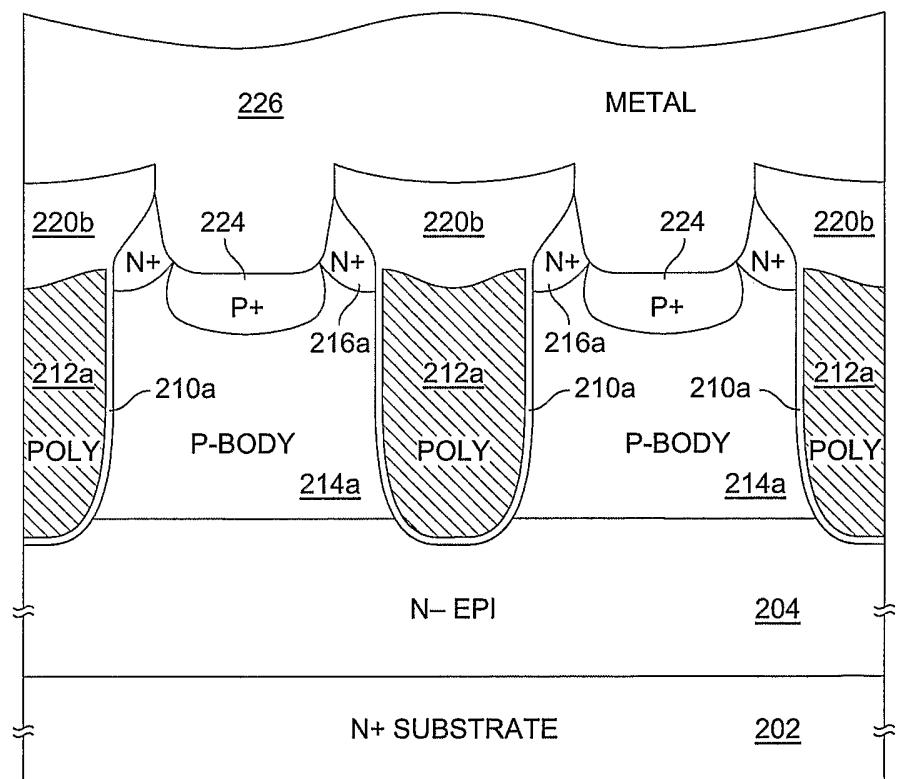


FIG. 5