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(54) PACKAGE FOR PUSH-PULL SEMICONDUCTOR DEVICES

(71) We, VARIAN ASSOCIATES, INC., of 611 Hansen Way, Palo Alto, California 94303, United States of America, a corporation organized under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

The invention relates to semiconductor devices and more particularly to the packaging of two or more such devices within one package.

In high frequency transistor packages the inherent inductance and capacitance caused by bonding wires and metallic pads contribute to the bandwidth, power loss, and ultimate impedance matching capability of the device. In the past, these devices have been constructed by placing the input and output pads in a spaced relationship with a ground plane so that the circuit exhibits a transmission line characteristic with respect to the ground plane.

U.S. Patent 3,713,006, which issued to Litty et al on January 23, 1973, is an example of a packaging technique for RF and microwave transistors which uses a number of transistors formed on a common die which are wired in parallel to provide a high power device. In order to achieve higher and higher power outputs, the approach has been to wire more and more transistors in parallel. The disadvantage of this is that the parasitic reactances associated with the transistor die and associated packaging leads cause the impedance levels to decrease and thus become an important part of the equivalent input and output circuit.

The bandwidth, internal power loss, input and output impedance levels, and impedance matching characteristics are all related to parasitic reactances created by the

lead bonds within the package and the parasitic elements associated with the transistor die.

In U.S. Patent 3,969,752, which issued to Martin et al on July 13, 1976, a compensating circuit is formed by a shunt reactance which is equal to the shunt parasitic capacitance at the output of the transistor die. The shunt reactance resonates with the parasitic capacitance to thereby cancel out the reactance characteristic in the equivalent circuit. The reactance branch which includes a capacitance in series with an inductance is connected in parallel with the shunt die capacitance. The series capacitance is necessary in order to block the DC currents from the ground plane which otherwise would short out the transistor output through the inductance to ground. The inductance is provided by either a lumped tuning wire or a high impedance transmission line connected from the capacitance to the transistor die of the device. In either case, the prior circuit is necessarily complicated by the fact that bond wires must be used in order to connect the various elements of the circuit together. It is very difficult to always attain the same length of bond wire in a manufacturing process and therefore this circuit tends to be very difficult to reproduce in mass production. Furthermore, the series capacitor introduces further loss characteristics which degrade the efficiency of the transistor circuit. The necessity of having a capacitor introduces one more potential element to fail and thus decreases the overall reliability of the device.

According to the invention there is provided a common package for semiconductor devices comprising: a dielectric member, first and second adjacent input conductors on said member, first and second adjacent output conductors on said member, a common ground conductor adjacent to said input and output conductors and at least one

dielectric member for supporting said conductors whereby each of said first and second input conductors and each of said first and second output conductors form a portion of an electrical circuit including said semiconductor devices and further including first and second active semiconductor devices connected to the ground conductor, and respectively, between said first input conductor and said first output conductor, and between said second input conductor and said second output conductor, each of said active semiconductor devices defining a discrete path for the transfer of high frequency signals from the corresponding input conductor to the corresponding output conductor.

When the semiconductor devices are mounted on the dielectric member and connected to operate in push-pull, the collectors of the semiconductors are always at substantially the same DC level. It is therefore unnecessary to provide a DC blocking capacitor in the output reactance circuit used to compensate for the parasitic output capacitance of the semiconductors.

An inductance may be connected across the two collectors of the push-pull semiconductors to act as a compensating reactance thereby to resonate with the parasitic output capacitance to minimize the effects thereof. This inductance may be formed of a single strip of metallic material between the collector pads, which material may be formed at the same time as and of the same material as the collector pads.

The circuit has the advantage that only a relatively small change in existing circuit packaging manufacturing techniques is necessary to practice the invention. Furthermore, these changes result in an overall reduction in the complexity of the circuit to achieve overall improved results.

The circuit has the advantage of achieving higher input and output impedance levels. More specifically, for a given amount of transistor die area the circuit achieves four times the input impedance and also four times the output impedance by using the push-pull approach of the invention as opposed to the conventional prior art parallel transistor approach.

The reduced series inductance because of the close proximity of the leads within the package and the increase in impedance levels achieves higher power levels and wider bandwidths with the packaging technique of the present invention.

The invention has the further advantage that the package allows DC connections for the base, emitter and collector to be made at points of RF ground. This makes the DC bypassing of the circuitry much less complicated. This means that the DC bias for the base can be connected at the point of RF

ground on the transformer.

The following is a detailed description of the preferred embodiments of the invention as illustrated in the accompanying drawings, which also illustrate the subject matter of divisional application 8021605 (Serial No. 1598842) and in which

Figure 1 is a plan view of a first embodiment of the present invention;

Figure 2 is an equivalent circuit of the transistor package of *Figure 1* illustrating the parasitic reactances associated with the circuit and an output shunt inductance branch;

Figure 3 is an equivalent circuit of a prior transistor package utilizing parallel transistors;

Figure 4 is a schematic diagram of a typical push-pull amplifier circuit utilizing the transistor package of the present invention; and

Figure 5 is a plan view of a second embodiment of the invention.

Referring now to *Figure 1* the transistor package is comprised of a ceramic wafer 10 upon which discrete metallized areas or pads are plated in accordance with known metallization techniques. These areas include a pair of input areas 12, 14. Input terminals 16, 18 are attached to the metallized input areas 12, 14, respectively.

A pair of output areas 20, 22 are also deposited on the ceramic wafer 10. The pair of output areas are aligned with the respective input areas 12, 14. Output leads 24, 26 are attached to the output areas 20, 22, respectively. A common ground plane is provided and in one embodiment is comprised of a pair of metallized ground areas or portions 30, 32, deposited on the wafer 10, having facing edges parallel to the facing edges of the pairs of input and output areas.

While not essential to the present invention, a further metallized ground area 34 is deposited on the wafer, the area passing between the input and output areas and making electrical connection to the parallel ground areas 30 and 32.

Ground terminals 36, 38 extend parallel to and on each side of the pair of input terminals and the pair of output terminals and are affixed to the pair of ground areas 30, 32.

A bridge 40, passing over the pair of metallized output areas 20, 22, is affixed to each of the ground terminals 36, 38.

It is understood that the ground areas need not be metallized on the same wafer as the input and output pads. The ground plane may be, for example, a metal plate spaced from and parallel to the metallized areas, or any other arrangement that will result in the creation of transmission line characteristics at the operating frequency of the device.

The metallized output area 20 further includes a portion or strip of metallized area 42 extending between the first metallized input area 12 and the output area 20. This thin strip of metallized area extends to and forms a bridge with a second portion extending between the second input area 14 and the second output area 22. The first portion 42 and the second portion 44 are in alignment with each other with a space 46 therebetween such that the space can be bridged by inductance wires 48. In an alternative embodiment, the space 46 is connected as shown by the dotted lines such that the first and second portions 42 and 44 comprise a continuous metallized strip without bond wires. In either case, a parallel inductance is provided across the first and second output areas.

A transistor die 50, comprised of a plurality of individual transistor cells 50a-50d, is attached to the metallized area 20 to form a first transistor. The transistor die 50 is produced by well known methods and the body of the die constitutes the common collector of all the transistor cells 50a-50d such that the common collector region is placed in electrical contact with the output area 20.

A second transistor 52, comprised of individual cells 52a-52d is attached in a similar manner to the output area 22. Common emitter and base regions are formed within each cell 50a-50d and 52a-52d which in turn are interconnected so as to form a plurality of common base sites and common emitter sites in an alternating pattern along the center line of the transistor dies 50, 52.

A split capacitor is attached to the ground area 34 separating the input and output areas. A first capacitive element has a first plate 54 and a second plate 56. The first plate 54 of the first capacitor is connected to the input area 12 via leads 68 and the second plate 56 of the capacitor is attached to the emitter sites on the transistor die 50 via leads 64. The emitter sites are also connected to points on the bridge 40 by emitter lead bonds 66.

The first plate 54 of the first capacitor is also connected to the base sites on the transistor die 50 by lead bond wires 70.

A second capacitive element has a first plate 58 and a second plate 60. The first plate 58 of the second capacitor is connected to the input area 14 via leads 69 and the second plate 60 is attached to the emitter sites on the transistor die 52 via leads 65. The emitter sites are also connected to points on the bridge 40 by emitter lead bonds 67.

A common emitter configuration has been illustrated. It should be understood that the present invention is not limited to

this configuration and is easily modified to a common base configuration by changing the lead bond connections appropriately.

Referring now to Figure 2, a schematic diagram of the equivalent circuit of the transistor package shown in Figure 1 is illustrated. The A input corresponds to the input terminal 16. The parasitic input inductances of the lead bond wires 68, 70 are illustrated by inductances 68, 70. The capacitance C1 is the input capacitance 54, 56 shown in Figure 1. The parasitic capacitance C3 of transistor 50 is shown in phantom across the emitter and collector of transistor 50.

A similar circuit is shown for the transistor 52. The value of the input capacitors C1 and C2 is chosen so as to reduce the Q and increase the magnitude of the input impedance over the operating frequency band of the circuit.

The output inductance formed by the conductive strip 42, 44 of Figure 1 is illustrated in the schematic diagram by inductance L1 which appears across the collectors of transistors 50, 52. The value of L1 is such that its reactance is equal to the combined capacitive reactance of capacitors C3 and C4 at the operating frequency. Thus the capacitance C3 and C4 and the inductance L1 will resonate thereby cancelling the effects of the total shunt capacitance contributed by C3 and C4.

It should be apparent from Figure 2 that a DC blocking capacitor in series with the inductance L1 is not necessary because the collectors of transistors 50 and 52 are at substantially the same DC output level.

Referring now to Figure 3, a schematic diagram of the prior art parallel transistor approach is shown. In this package, an inductor L3 is placed as close to the transistor die as possible to resonate out the parasitic capacitance C6 at the output. This inductance must be DC blocked from ground, otherwise it would cause a short across the output. Therefore a DC blocking capacitor C6 is wired in series with the inductance L3. By connecting two smaller transistors in a push-pull relationship, DC isolation is not necessary on the output because the collectors of the two transistors are at substantially the same DC potential. This eliminates the bond wires which were necessary to connect the series capacitor. Therefore the reliability and reproducibility of the circuit is much greater because it is possible to form the inductance L1 by means of a continuous conductive strip metallized on the wafer. The actual value of the inductance L1 depends upon the values of C3 and C4 for the particular transistor fabricated and the frequency of operation. An approximate value would be an inductance reactance of 16 ohms at 300 megahertz,

at a power level of about 125 watts.

The circuit of Figure 2 wired in a push-pull circuit is shown in Figure 4 as circuit 82 with input transformer 80 and output transformer 84. This circuit has certain advantages over connecting the same transistors in a parallel arrangement as was done in the prior art. In order to wire two discrete transistors in parallel it is necessary to go through some printed inductance which reduces the high frequency performance by making the high frequency cut-off lower. The advantage of the push-pull arrangement of Figure 4 is that higher input and higher output impedance levels are possible for a given amount of transistor die utilized. Furthermore greater power levels are possible than could be achieved by tying two single discrete devices in parallel. By placing the two transistors in the same package shorter connecting leads are made possible further improving the frequency response characteristics.

Referring now to Figure 5 a second embodiment of the invention is shown. In Figure 5 the transistor package is comprised of two ceramic wafers providing two separate planes upon which discrete metallized areas or pads are plated. The lower ceramic wafer 100 has plated thereon a ground plane 102 which completely surrounds a pair of inner output areas 104, 106. The inner output areas 104, 106 are connected by a thin portion or strip of metallized area 108 extending between the first area 104 and the second area 106. This thin strip of metallized area comprises a parallel inductance across the first and second inner areas 104, 106.

An upper ceramic frame 110 is provided upon which a pair of input areas 112, 114 are plated. Input terminals 116 and 118 are attached to the metallized input areas 112, 114, respectively.

A pair of output areas 120, 122 are also deposited on the ceramic frame 110. Output leads 124, 126 are attached to the output areas 120, 122, respectively.

The common ground plane 102 is comprised of a pair of metallized ground areas generally designated by the numerals 130, 132, deposited on the lower ceramic wafer 100, extending parallel to and on each side of the inner areas 104, 106.

While not essential to the present invention, a further metallized ground area designated by the numeral 134, is deposited on the lower wafer 100, the area passing between the input and inner output areas and making electrical connection to the parallel ground areas 130, 132. In the embodiment shown in Figure 5, the ground areas just described are actually all interconnected to form a continuous ground plane 102 shaped in the form of a rectangle with

an opening 135 at its center.

A transistor die 150, comprised of a plurality of individual transistor cells, is attached to the metallized inner area 104 to form a first transistor. The body of the die constitutes the common collector of all the transistor cells such that the common collector region is placed in electrical contact with the inner area 104.

A second transistor 152 is attached in a similar manner to the inner area 106. Emitter and base regions are formed within each cell which in turn are interconnected so as to form a plurality of common base sites and common emitter sites in an alternating pattern along the center line of the transistor dies 150, 152.

A split capacitor is attached to the ground area 134. A first capacitive element has a first plate 154 and a second plate 156. The first plate 154 is connected to the input area 112 via leads 168 and the second plate 156 is attached to the base sites on the transistor die 150 via leads 164. The base sites are also connected to points on the common ground plane via base lead bonds 166. This results in a grounded base configuration. The first plate 154 of the first capacitor is also connected to the emitter sites on the transistor die by lead bond wires 170.

A second capacitive element has a first plate 158 and a second plate 160. The first plate 158 of the second capacitor is connected to the input area 114 via leads 169 and the second plate 160 is attached to the base sites on the transistor die 152 via leads 171. The base sites are also connected to points on the common ground plane by base lead bonds 167.

A common base configuration has been illustrated. It should be understood that the described embodiment of the invention is not limited to this configuration and is easily modified to a common emitter configuration by changing the lead bond connections appropriately.

The equivalent circuit of the transistor package shown in Figure 5 is identical to that shown in Figure 2 with the exception that the base and emitter connections are reversed to thereby provide a common grounded base configuration.

The two embodiments of the invention have been described with respect to transistor dies having three active areas, however, it should be understood that the invention can be practiced utilizing any semiconductor devices and is not limited to devices having three active areas.

WHAT WE CLAIM IS:-

1. A common package for semiconductor devices comprising: first and second adjacent input conductors, first and second adjacent output conductors, a common ground conductor adjacent to said input and

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output conductors and at least one dielectric member for supporting said conductors, whereby each of said first and second input conductors and each of said first and second output conductors form a portion of an electrical circuit including said semiconductor devices and further including first and second active semiconductor devices connected to the ground conductor and, respectively, between said first input conductor and said first output conductor, and between said second input conductor and said second output conductor, each of said active semiconductor devices defining a discrete path for the transfer of high frequency signals from the corresponding input conductor to the corresponding output conductor.

2. A package as claimed in claim 1 comprising a first metallized strip extending from and electrically connected to the first output conductor and a second metallized strip extending from and electrically connected to the second output conductor, the first and second strips being in alignment with each other and a space therebetween such that said space can be bridged by an inductance wire bonded to said first and second strips thereby to provide a parallel inductance across said first and second output conductors.

3. A package as claimed in claim 1 or claim 2 wherein said output conductors are connected by an inductance.

4. A package as claimed in claim 3 when dependent on claim 1 wherein said inductance comprises conductive strip extending from said first output conductor to said second output conductor.

5. A package as claimed in claim 4 wherein said conductive strip is located between said input conductors and said output conductors.

6. A package as claimed in any one of claims 1 to 5 wherein said ground conductor passes between said input and output conductors.

7. A package as claimed in any one of claims 1 to 6 wherein the ground conductor comprises portions extending parallel to and on each side of said output conductors.

8. A package as claimed in any one of claims 1 to 7 comprising first and second adjacent output contact pads connected respectively to said first and second output conductors.

9. A package as claimed in claim 7 and claim 8 wherein said ground conductor passes between said output conductors and said output contact pads.

10. A package as claimed in claim 7 further comprising a conductive bridge passing over said output conductors and making electrical contact with said portions.

11. A package as claimed in any one of

the preceding claims wherein said ground conductor is mounted on a different dielectric member from said input conductors.

12. A package as claimed in claim 11 when dependent on claim 9 wherein said output conductors are mounted on the same dielectric member as that on which the ground conductor is mounted.

13. A package as claimed in claim 11 or claim 12 when dependent on claim 4 or claim 5 wherein said conductive strip is mounted on the same dielectric member as that on which the ground conductor is mounted.

14. A package as claimed in any one of the preceding claims and comprising a first die of semiconductor material having at least first, second and third active regions therein forming a first transistor constituting said first active device, a second die of semiconductor material having at least first, second and third active regions therein forming a second transistor constituting said second active device, means electrically connecting said first die to said first output conductor such that the first active region thereof makes contact with said output conductor, means electrically connecting said second die to said second output conductor such that said first active region thereof makes contact with said second output conductor, a first electrical connection to said third active region of said first transistor in electrical contact with said common ground conductor, a second electrical connection to said third active region of said second transistor in electrical contact with said common ground conductor, a third electrical connection between said first input conductor and said second active region of said first transistor, and a fourth electrical connection between said second input conductor and said second active region of said second transistor.

15. A package as claimed in claim 14 in which there are more than one of said second and third active regions in each of said semiconductor dies.

16. A package as claimed in claim 14 or 15 wherein said first, second and third active regions of said semiconductor dies are transistor collector, base and emitter regions, respectively.

17. A package as claimed in claim 15 wherein said first, second and third active regions of said semiconductor dies are transistor collector, emitter and base regions, respectively.

18. A package as claimed in claim 14 when dependent on claim 6 comprising a first capacitive element on said ground conductor, said element having first and second plates, and wherein said third electrical connection includes means for connecting said first plate to said first input

conductor and wherein there are also means for connecting said second plate to said second active region of said first die.

19. A package as claimed in claim 18
5 further comprising a second capacitive element on said ground conductor, said element having third and fourth plates and wherein said fourth electrical connection
10 includes means for connecting said third plate to said second input conductor and wherein there are also means for connecting said fourth plate to said second active region of said second die.

20. A common package for semiconductor devices substantially as hereinbefore described with reference to and as illustrated in Figures 1 to 4 or Figure 5 of the accompanying drawings.

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FIG.1

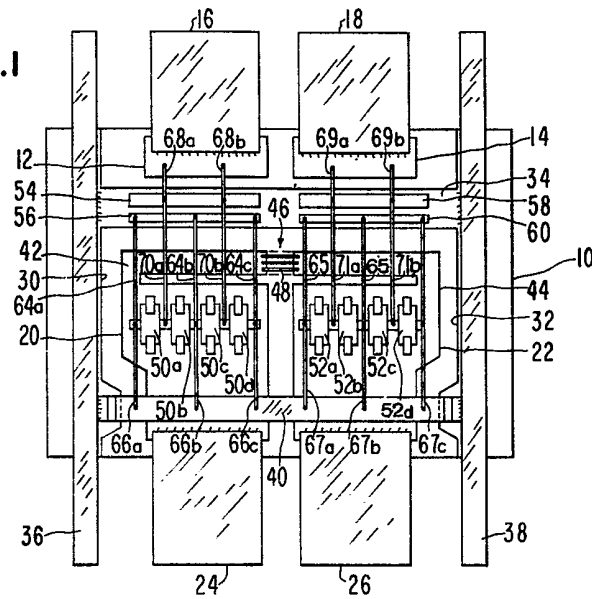


FIG.2

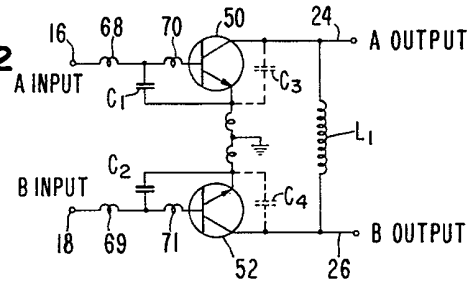


FIG.3 PRIOR ART (3,969,752 - MARTIN ET. AL.)

