The present invention provides a stabilized fine textured metal microstructure that constitutes a durable activated surface 310 usable for bonding a 3D stacked chip. A fine-grain layer that resists self anneal enables metal to metal bonding at moderate time and temperature and wider process flexibility.
Improved metal to metal bonding for stacked (3D) integrated circuits

BACKGROUND

0001 The present invention relates generally to three dimensional (3D) integrated circuits, and more particularly to enabling the metal-to-metal bonding of integrated circuit substrates at low temperature and pressure.

0002 The semiconductor industry continues to drive toward greater functionality and speed of integrated circuits. For the most part, such improvements have been achieved by scaling the feature size such that more smaller devices can fit in a given area. But such scaling cannot continue indefinitely because devices are now approaching atomic dimensions. Furthermore, as the density has increased, so has the complexity and length of the interconnect circuitry, causing increases in both circuit resistance-capacitance (RC) delay and power consumption. Three-dimensional integrated circuits - that is, stacked chips bonded together - provides an opportunity to overcome these limitations.

0003 Figure 1 illustrates a 3D stack 100 in which two semiconductor die are bonded together. Each die may be one of a plurality of dice on a whole or partial semiconductor wafer, such that 3D stack 100 can represent any combination such as wafer to wafer, die to wafer, or die to die. A first die 110 includes a semiconductor substrate 106 in which at least one semiconductor device 101 formed and interconnect wiring layer 102, and a second die 120 includes one or more TSVs (through substrate vias) 121 for passing power or signals entirely through the second die 120 to the devices 101 of the first die. The interconnect wiring 102 is embedded in back end of the line (BEOL) dielectric layers 103, formed on substrate 106. The interconnect wiring and TSVs include a conductive core, which can be formed of copper. The core is typically separated from the surrounding materials (e.g., the substrate wafer or dielectric layers) by liner and barrier layers.
The wiring and TSVs are conventionally formed by plating copper onto a seed layer that has been deposited such as by PVD or ALD. The grain size of the plated copper depends on the plating conditions and the thickness of the deposition. This microstructure is known to "self-anneal", that is, the thermodynamics favor grain growth, even at room temperature, and even though this grain growth induces a tensile stress. See Lee and Wong, "Correlation of stress and texture evolution during self- and thermal annealing of electroplated Cu films", J.Appl.Phys 93:4 3796-3804. Such stresses can cause distortions such as warpage of a silicon wafer. Typical semiconductor processing includes a thermal anneal to accelerate the atomic rearrangement and bring the plated copper to an equilibrium state.

Controlling the anneal enables further high fidelity processing such as alignment and bonding of two substrates to form the 3D stacked structure of Figure 1. First die 110 (after completing BEOL processing to form layer 103 with interconnect wiring 102) and second die 120 can be bonded by thermocompression bonding between a plated metal (e.g., 105) on the bonding surface 104 of the first die and a plated metal (e.g., 125) on the bonding surface 124 of the second die. This method may be used in die to die, or die to wafer, as well as for wafer to wafer bonding for 3D applications. The facing surfaces of the two die can be formed with metal regions, for example, a mirror image pattern of copper regions as depicted in Figure 2. These metal regions can constitute part of the circuitry of the final 3D stack, or they can be created strictly as bonding regions. Metal bonding to form the 3C integrated circuit stack can be achieved by holding the stack together at temperature of at least 350-400C for at least 30 to 60 minutes.

Unfortunately, such conditions can exceed the thermal budget of delicate integrated circuitry which cannot be exposed, or at least not for extended time, to high temperature. Farrens reports in "Wafer and Die Bonding Technologies for 3D Integration", MRS Fall 2008 Proceedings E, that lower temperature atomic diffusion of all fee metals is primarily along grain boundaries. Bonding a 3D stack at lower temperatures would permit a wider selection of devices and materials,
but has not been possible because, as noted above, conventional processing promotes grain growth such that a plated copper surface has a very low concentration of grain boundaries. Even without a thermal anneal, thermodynamics drives grain growth and within a very short time converts the surface microstructure of plated copper such that metal to metal bonding at temperature below 350°C is impractical.

0007 A need remains to achieve reliable metal bonding in reasonable time at less stressful conditions.

BRIEF SUMMARY

0008 The present invention enables metal to metal bonding at lower bond temperature and time combination, enabling a lower thermal budget.

0009 According to a first embodiment, metal to metal bonding can be enabled by electroless plating a metal surface to form a bonding layer wherein an average grain size of said bonding layer is smaller than an average grain size of said metal surface. According to a further embodiment, the metal surface can be oxidized by exposure to H₂O₂, TEAH or TMAH to create a roughened surface prior to such electroless plating.

0010 In a first aspect of the invention, a custom electroless plating solution includes a reducing agent poison. In another aspect of the invention, a custom electroless plating solution includes a deposition poison. In another aspect of the invention, a plating solution includes a contaminant species that inhibits grain growth in a deposited layer.

0011 According to another embodiment is provided a 3D stacked structure that includes a first die bonded to a second die by a metallic bond. The first die includes metal wiring structure formed within a one or more dielectric layers disposed on a semiconductor substrate within which at least one semiconductor device has been formed, and the second die includes a semiconductor substrate
having at least one contact pad. The metallic bond is at an interface between said metal structure and said contact pad. A species that inhibits plating other than oxygen is present at the interface at a concentration substantially higher than the concentration of such species within either of said metal structure or said contact pad.

BRIEF DESCRIPTION OF SEVERAL VIEWS OF THE DRAWINGS

0012 Exemplary embodiments may best be understood by reference to the detailed description in conjunction with the accompanying figures. The Figures are provided for illustration and are not drawn to scale.

0013 Figure 1 depicts a 3D integrated circuit.

0014 Figure 2 illustrates the bonding surfaces of two substrates comprising a 3D integrated circuit structure wherein the surfaces have mirror image metal regions within a field of non-conductive material.

0015 Figures 3A and 3B illustrate a discontinuous seed layer according to various embodiments of the invention.

0016 Figure 4A, 4B and 4C illustrate pre-treating a bonding surface according to embodiments of the invention.

0017 Figure 5 illustrates an incompletely polished surface amenable to treatment by embodiments of the invention.

DETAILED DESCRIPTION

0018 It will be understood that when an element as a layer, region or substrate is referred to as being "on" or "over" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or "directly over" another element, there are no intervening elements present. Similarly, when an element is
referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present. Additionally, to the extent a feature is described to be horizontal or vertical, that orientation is with respect to a generally planar major surface of the substrate which can be in the form of a wafer or disk.

The present invention promotes metal to metal bonding at lower temperature by forming a layer of fine textured structure on the bonding surface. Fine metal grains can be deposited and arranged to create a layer of fine textured structure capable of metal to metal surface bonding at a reduced temperature, that is, at a temperature lower than the temperature normally required for metal to metal bonding. A plating step ordinarily is conducted in such a manner so that clean surfaces are maintained to enable even metal deposition and growth. Even if a fine metal grain structure could be formed on such a plated surface, the microstructure is not durable because thermodynamics drives the fine grains to "self-anneal", that is, to join together to form larger grains constituting a lower energy state. The present invention provides a stabilized fine textured metal microstructure that constitutes a durable activated surface even after significant passage of time. Such a fine textured structure can enable metal bonding at lower thermal budget and can be achieved in various ways.

Figure 2 illustrates a possible arrangement of the bonding surfaces of the 3D stack 100 of Figure 1. The material of substrate 106 and 126 can be any semiconductor material including but not limited to group IV semiconductors such as silicon, silicon germanium, or germanium, a III-V compound semiconductor, or a II-VI compound semiconductor. Furthermore, substrates 106 and 126 can be bulk silicon or can comprise layers such as, silicon/silicon germanium, silicon on insulator (SOI), ETSOI (extremely thin semiconductor on insulator), PDSOI (partially-depleted semiconductor on insulator) or silicon germanium-on-insulator. The insulator layers of these can be referred to as a buried oxide (BOX) layer.
which can be any insulating oxide such as, e.g., silicon dioxide, or even an epitaxial oxide such as Gadolinium(III)-oxide \( \text{(Gd}_2\text{O}_3 \).}

0021 Bonding surface 104 of die 110 can be the top of BEOL layer 103. As such, surface 104 can include exposed regions of metal 105 which could be the topmost portion of interconnect wiring 102, or they could be pads formed exclusively as bonding structure which does not electrically connect to any devices. The remaining portion of surface 104 would be dielectric material such as oxide. Metal regions 105 can be laid out to align with metal regions 125 on the bonding surface 124 of die 120.

0022 Surface 124 includes metal regions 125 surrounded by a field. It should be understood that Figure 2 can represent bonding surfaces for die to die, die to wafer, or wafer to wafer bonding. Metal regions of the bonding surfaces can be as depicted in Figure 2, with small isolated metal regions in a dielectric (or other non-metal) field, or could be more of a checkerboard or mixed line pattern. The metal regions 105 and 125 can be made from a material selected from the group consisting of copper, nickel, copper/nickel, copper/gold and copper/nickel/gold. One or more layers, e.g. a barrier layer, may separate metal regions from surrounding material but are not shown. The field material surrounding regions 125 depends on the design of die 120 and stack 100. For example, if vias 121 were etched into substrate 126 from the side opposite surface 124, but not all the way through the substrate, and then exposed by thinning the substrate to expose the remote ends 125 of vias 121, then the field could be the material of substrate 126 or it could be another material such as a passivation material. Another option is that die 120 has a BEOL layer (not shown), oriented "face to face" with BEOL layer 103, in which case the field of surface 124 could be predominantly dielectric material. It should be understood, that first and second die 110 and 120 may have similar or different structure or function, and they can be formed of similar materials such as both having a bulk silicon substrate, but there is no requirement that any analogous structure be of the same material. The metal of regions 125 can be different from that of 105, provided that they are capable of
combining to permit electron derealization, i.e., forming a metallic bond. A 3D stack can also have bonding surfaces that are primarily metal. For example US 7939369, the specification of which is hereby incorporated by reference, teaches a 3D structure joined by metal to metal bonding, where a metal plane constitutes the last layer of both die to be bonded so that each bonding surface is almost completely metal.

0023 Electroless plating according to embodiments of the present invention can be used to activate a bonding surface having isolated bonding regions (such as depicted by Figure 2), or one comprised primarily by metal, which is to say it is applicable to joining any two structures by forming a metallic bond. Ordinarily, an electroless solution composition is carefully controlled to promote deposition of a smooth and continuous layer, and is designed to maintain clean interfaces as the plating process proceeds. The plating solution and the process controls are designed to enable and promote continuous films to the thickness required from the plating solution to produce the correct film to meet design characteristics. For example a 1 micrometer thick film may be required for a process and the electroless chemistry is designed to produce a continuous film that will achieve a 1 micrometer thickness without significant internal imperfection. The standard electroless plating solution typically includes a source of metal ions; a reducing agent, such as formaldehyde for copper deposition; additives such as to keep the metal ions in solution or a pH buffer; and a very small concentration, such as a few ppm, of a deposition poison, such as lead (Pb) ions, to stop unwanted plating on the tank or transfer equipment.

0024 Figure 3B illustrates the top or bonding surface 304 of a structure 300, and Figure 3A illustrates a sideview of structure 300 along a cut at 3A. Structure 300 includes isolated metal regions 305 embedded within a non-metal material 303. Isolated metal regions 305 could be the surface, for example, of BEOL metallization, a contact pad, or a TSV. Metal regions 305 may be annealed to have large average grain size of e.g., 2.0 micron or more. According to the present invention, a thermodynamically-stable fine-textured metal layer (having
small average grain size such as <1.0 or even <0.6 micron or less) can be formed on a bonding surface by electroless plating. According to a first embodiment, an activated layer (such as a fine-textured layer) can be formed on metal regions by exposing bonding surface to a customized electroless plating solution that includes, in addition to the usual components, an inhibitor to interfere with metal deposition.

The inhibitor, which may also be referred to as a poison, can be selected from species known to inhibit or stop metal deposition. The selection and concentration of the inhibitor species depends on the resultant textured surface that is desired. For very fine grain textured surfaces, the inhibitor concentration is selected to surface adsorb and poison small regions on which initial fine grains will not form, at a rate comparable to deposition of fine grains on to regions. The chemistry can be tuned so that regions and have roughly equivalent surface area and have a mean diameter as small as tens of nanometers. The proper inhibitor concentration appreciates competitive surface adsorption rates of the inhibitor and metal which is desired to be plated, and can be tuned for plating onto a freshly plated surface or onto a stabilized or annealed metal surface. The electroless solution may include inhibitor at a concentration as low as 100 ppm to as high as several hundred thousand ppm dependent on the reactant constant of the inhibitor relative to the reactant constant of the plating system to deposit metal. For example, the solution could include cobalt (Co) ions in a concentration between 1000 and 10000 ppm, or about 5000 ppm.

Selection of an inhibitor species depends on the particular electroless chemistry, and can be, for example, one or more of arsenic, cobalt, manganese, chromium, lead, silver, nickel or other metals, metal oxides of any of the foregoing, and can also be compounds such as, e.g., acetone, ammonium peroxysulfate, cerium ammonium nitrate (CAN), 2-mercapto-5-benzimidazolesulfonic acid (MBIS), and bis-(3-sulfopropyl)-disulfide (SPS).

According to another embodiment, uniform metal deposition can be disrupted by interfering with the activity of the plating reducing agent. In that case, an inhibitor
to the reducing agent can promote unequal rates of metal ion reduction (ie, deposition) to produce a fine textured surface. The inhibitor concentration for such embodiment could be as low as 100 ppm or several hundred ppm to as high as tens of thousands ppm dependent on the reactant constant of the inhibitor relative to the reactant constant of the plating system to deposit metal. The reducing agent inhibitor could be a non-metal or a metal compound such as a metal ion oxide, or could be, for example, arsenic within the range of 100 to 100,000 ppm, or at a concentration of about 500 ppm.

0028 According to yet another embodiment, activated layer 310 can be formed on a bonding surface 304 by forming a dispersed seed layer. Such dispersed seed layer could be formed by exposing surface 304 to a customized seed solution that includes palladium (Pd) or other seeding catalyst along with a slightly higher concentration of an inhibitor that poisons portions of the exposed surface of metal region 305 and preferentially prohibits uniform seeding. An example of such inhibitor could be, e.g. lead (Pb) or thallium (Tl), at a concentration in the range of 50 to 500 ppm. In particular embodiments the inhibitor could be in the range of 350 to 500 ppm to form seeded regions 315 within a matrix of poisoned regions 314 constituting a discontinuous seed layer. Subsequent electroless deposition can form a fine textured and durable activated surface 310 on top of the discontinuous seed layer.

0029 The poison species will inhibit seed deposition on regions of the exposed metal, such that the seeded deposition that does occur will be a discontinuous layer. Optimally each region 315 is very small, such as just a few seed species, and region 314 has less total surface area than the aggregation of all regions 315. In a preferred embodiment, the bonding surface constitutes a finely dispersed composition, such as where the mean diameter of regions 315 (ie, the average width of a seed region) is greater than or at least the same order of magnitude as the average edge to edge distance between adjacent seed regions. Electroless deposition of layer 310, e.g., copper onto such 'dispersed seed layer' can maintain a fine grain structure for subsequent bonding because the seed layer
constitutes dispersed particles of seed rather than a continuous film. When subsequently bonded, the fine grained layer 310 may anneal with or into the opposite bond surface, but the finely dispersed seed layer will remain as a very thin layer wherein the poison is at substantially higher concentration than in the bulk of the bonded material. In embodiments, the poison concentration at the interface could be more ten times or even several orders of magnitude greater than its concentration in the bulk of the bonded metal structures. In other words, the interface will include a detectible plating poison at a concentration at least one order of magnitude higher than in the adjacent metal structures. In a preferred embodiment, the poison concentration at the interface is at least three orders of magnitude greater than in the bulk of metal regions 305.

According to yet another embodiment, Figure 4 depicts subjecting exposed metal 405 to surface pretreatment such as in H₂O₂, TEAH, TMAH, to promote non-uniform oxide growth 409. For example, a metal copper surface can be roughened by pre-treatment such as by H₂O₂, followed by a partial surface clean with hydroxyl amine. Subsequent plating a film onto such treated surface can create a durable activated layer with enhanced roughness and fine grain size.

Figure 5 illustrates yet another substrate 500 that can be treated according to any embodiment of this invention to form a stable activated bonding surface. Substrate 500 includes conductive pathways 522 plated to fill patterned openings in a top dielectric layer 503 where a layer 528 constitutes a current carrier for electrochemical deposition. CMP to remove excess metal can incompletely remove the barrier layer 528, exposing only small regions of dielectric 503. Surface pretreatment such as with H₂O₂ can promote non-uniform oxide growth on exposed metal 522 as illustrated in Figure 4. When subsequently subjected to electroless plating, the differential thickness of this oxide growth, which can preferentially form along copper grain boundaries, is removed and exposes a rough pristine metal surface. A fine-grained bonding layer can be deposited onto the rough surface. The roughness helps to stabilize an activated layer that can be formed with a high density of dislocations and fine grain structure.
In yet a further embodiment, a contaminant such as tin or silver is included in the electroless solution. Such contaminant is selected to co-deposit with the particular metal to be deposited, so that e.g., tin dispersed in copper is deposited onto a prepared seed layer. Such deposition can be onto a seed layer formed by conventional processing or preferably onto a finely dispersed seed layer as described above. The contaminant, which may constitute from a few ppm up to several percent such as 200 ppm to 1.5%, or within the range of 0.01% to 1% of a thinly deposited layer, can pin the grain boundaries of the deposited metal and thereby enable formation of a stable fine-textured bonding layer. By inhibiting or delaying grain growth, the deposited bonding layer can maintain a fine grained microstructure and enable metal to metal bonding at lower temperature, or in less time, or both.

It will be apparent to those skilled in the art having regard to this disclosure that other modifications of the exemplary embodiments beyond those embodiments specifically described here may be made without departing from the spirit of the invention. Accordingly, such modifications are considered within the scope of the invention as limited solely by the appended claims.
CLAIMS

What is claimed is:

1. A method to enable metal to metal bonding comprising:
   plating a metal surface to form a bonding layer wherein an average grain size of said bonding layer is smaller than an average grain size of said metal surface.

2. The method of claim 1 wherein said bonding layer is formed by electroless plating.

3. The method of claim 2 further comprising prior to said plating:
   oxidizing said metal surface by exposure to $\text{H}_2\text{O}_2$, TEAH or TMAH.

4. The method of claim 2 further comprising prior to said plating:
   forming a discontinuous seed layer.

5. The method of claim 4 wherein said discontinuous seed layer is formed by
   exposing said metal surface to a solution in which the concentration of a seed catalyst is less than the concentration of a poison species.

6. The method of claim 5 said seed catalyst is selected from palladium or thallium and said poison species is an ionic species of, or a compound comprising, arsenic, cobalt, manganese, chromium, lead, nickel, silver, or combinations thereof.

7. The method of claim 5 wherein said concentration of a poison species is between 50ppm and 500ppm.

8. The method of claim 2 wherein said electroless plating utilizes a plating solution that contains a one or more species selected from the group consisting of acetone, ammonium peroxydisulfate, cerium ammonium nitrate (CAN), 2-mercapto-5-benzimidazolesulfonic acid (MBIS), and bis-(3-sulfopropyl)-disulfide (SPS).

9. The method of claim 2 wherein said electroless plating utilizes a plating solution that contains a reducing agent inhibitor at a concentration between 100 to 1000ppm.
10. The method of claim 9 wherein said reducing agent inhibitor is arsenic.

11. The method of claim 2 wherein said electroless plating utilizes a plating solution that contains cobalt at a concentration between 1000ppm and 10000ppm.

12. The method of claim 2 wherein said electroless plating utilizes a plating solution that contains a contaminant that inhibits grain growth within said bonding layer.

13. The method of claim 12 wherein said contaminant is selected from tin or silver.

14. A method to form a metallic bond between a first metal structure and a second metal structure comprising:

    holding said first metal structure and said second metal structure together at less than 350°C to form said metallic bond at an interface, wherein said interface includes a poison species at a concentration at least one order of magnitude higher than a concentration of said poison species in either of said first metal structure and said second metal structure.

15. The method of claim 14 further comprising forming a dispersed seed layer on said first metal structure.

16. The method of claim 14 wherein said interface further comprises a contaminant that inhibits grain growth.

17. A 3D structure comprising a first die bonded to a second die, wherein the first die includes metal structure formed within a dielectric layer disposed on a semiconductor substrate within which at least one semiconductor device is formed, and the second die includes a semiconductor substrate and a metal contact pad, the 3D structure comprising:

    a metallic bond at an interface between said metal structure and said contact pad, the composition of said interface including a species other than oxygen that inhibits plating, the concentration of said impurity at the interface being at least one order of magnitude higher than the concentration of said species within either of said metal structure or said contact pad.
18. The structure of claim 17 wherein said species is Pb, Tl, or a combination including Pb or Tl.

19. The structure of claim 17 wherein the concentration of said species is at least three orders of magnitude higher than a concentration of said species in either of said metal structure or said contact pad.

20. The structure of claim 17, wherein a contaminant of the group consisting of arsenic, tin, cobalt, or silver is detectible at said interface.

21. The structure of claim 17 formed by the method of claim 1.

22. The structure of claim 17 formed by the method of claim 14.
INTERNATIONAL SEARCH REPORT

PCT/US2014/010442

A. CLASSIFICATION OF SUBJECT MATTER

HOIL 23/48(2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
HOIL 23/48; HOIL 21/768; HOIL 29/92; H01G 4/00; C23C 18/32; H01L 23/522; H01L 21/321; B05D 3/04; B32B 15/16

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: grain size, plating, metallic bond, poison species, inhibitor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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<th>Category</th>
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<td>US 2002-0192363 Al (ROBERT J. BAHN et al.) 19 December 2002 See abst ract, paragraphs [0008]- [0010], [0028]- [0032] and figures 1A-7.</td>
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<td>Y</td>
<td>US 2010-0289144 Al (MUKTA G. FAROOQ et al.) 18 November 2010 See abst ract, paragraphs [0046]- [0057] and figures 1-7.</td>
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☑ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
* "A" document defining the general state of the art which is not considered to be of particular relevance
* "E" earlier application or patent but published on or after the international filing date
* "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
* "O" document referring to an oral disclosure, use, exhibition or other means
* "P" document published prior to the international filing date but later than the priority date claimed

"P" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"R" document member of the same patent family

Date of the actual completion of the international search 09 May 2014 (09.05.2014)
Date of mailing of the international search report 09 May 2014 (09.05.2014)

Name and mailing address of the ISA/KR
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FormPCTVISA/210 (second sheet) (July 2009)
### Box No. II  Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. □ Claims Nos.:
   because they relate to subject matter not required to be searched by this Authority, namely:

2. ☑ Claims Nos.: 21-22
   because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
   - Claim 21 and claim 22 are related to the structure of claim 17 formed by the method of claim 1 and claim 14, respectively.
   - However, claims 1 and 14 are related to forming a metal bonding, not related to forming a 3D structure. In addition, the structure of claim 17 is not expected to be formed by the method of claim 1 or claim 14. Therefore, claims 21-22 do not clearly define the matter for which protection is sought.

3. □ Claims Nos.:
   because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

### Box No. III  Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☑ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. □ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fees.

3. □ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☑ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

### Remark on Protest
- □ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☑ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☑ No protest accompanied the payment of additional search fees.
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