(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
2 February 2017 (02.02.2017)

WIPO | PCT

(10) International Publication Number
WO 2017/019420 A1

(51) International Patent Classification:
G02F 1/1343 (2006.01) *G02F 1/1368* (2006.01)
G02F 1/1362 (2006.01)

(21) International Application Number:
PCT/US2016/043230

(22) International Filing Date:
21 July 2016 (21.07.2016)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
62/196,359 24 July 2015 (24.07.2015) US

(71) Applicants: **OREGON STATE UNIVERSITY** [US/US]; 312 Kerr Administration Building, Corvallis, OR 97331 (US). **AMORPHYX** [US/US]; 508 SW Jefferson Avenue, Corvallis, OR 97333 (US).

(72) Inventors: **COWELL, E., William**; 2156 Nw Christopher Pl., Corvallis, OR 97330-2203 (US). **NEWTON, John**; 41 Rihana Street, Orakei, Auckland, 1071 (NZ).

(74) Agents: **HAUN, Niels** et al.; Dann, Dorfman, Herrell And Skillman, P.C., 1601 Market Street, Suite 2400, Philadelphia, PA 19103-2307 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: IN-PLANE SWITCHING LIQUID CRYSTAL DISPLAY BACKPLANE USING AMORPHOUS METAL NON-LINEAR RESISTORS AS ACTIVE SUB-PIXEL DEVICES

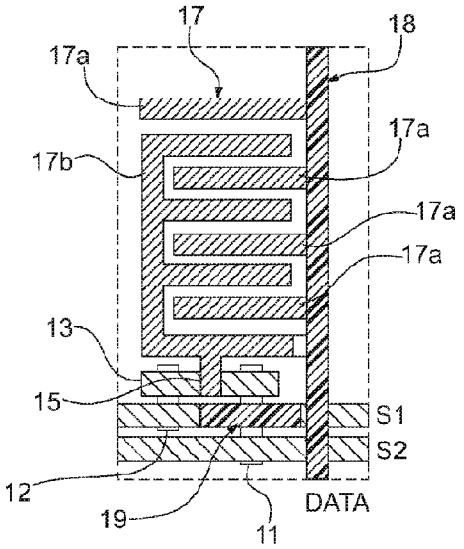

FIG. 2D

(57) **Abstract**: A physical layout for a circuit using amorphous metal non-linear resistors as active devices for an in-plane switching liquid crystal display sub-pixel is provided. The lower interconnect of the two amorphous metal non-linear resistors and the lower electrode of the storage capacitor may be concurrently deposited and patterned. The area of the storage capacitor is defined by the overlap of the data signal interconnect and the storage capacitor lower electrode, which is easily modified through the size of the lower electrode and/or the size of the data signal interconnect where it overlaps the lower electrode and does not degrade the aperture ratio of the pixel. Two embodiments of sub-pixel circuits are described. One, which employs a select line bridge, enables the use of full dot inversion of the image data. The second only allows row inversion of the image data.

WO 2017/019420 A1

In-Plane Switching Liquid Crystal Display Backplane Using Amorphous Metal Non-linear Resistors as Active Sub-pixel Devices

Field of the Invention

[0001] In one of its aspects, the present invention relates generally to the realization of a liquid crystal display backplane having a matrix of pixels used to modulate the polarization of a liquid crystal material parallel to the substrate within the pixel. Active devices of the present invention may include amorphous metal thin-film non-linear resistors which allow for the control of liquid crystal polarization in each pixel, and therefore, the pixel brightness.

Background of the Invention

[0002] A liquid crystal display (LCD) that employs an in-plane switching (IPS) sub-pixel circuit is presently considered state-of-the-art technology. IPS LCD has benefits in viewing angle and operational speed compared to a more traditional vertical alignment (VA) based LCD sub-pixel circuit. The primary distinction between IPS and VA LCD sub-pixel circuits is the relative location of the two electrodes (i.e., sub-pixel electrodes) between which an electric field is applied to polarize a liquid crystal material located between the two electrodes. The extent to which the liquid crystal material is polarized controls the amount of light that is transmitted through the backplane. The control of light transmission through the backplane is the means through which a digital image is created on an LCD. IPS based sub-pixel circuits have both electrodes located on one substrate (i.e., the backplane), whereas VA based sub-pixel circuits have one electrode on the backplane and one electrode on a second substrate (i.e., the color filter, CF). Present IPS LCD technology employs a thin-film transistor (TFT), located on the backplane, to control the magnitude of the electric field applied between sub-pixel electrodes that, in turn, controls the digital image on the IPS LCD.

[0003] The LCD backplane, which is a glass substrate onto which active devices, conducting layers and insulating layers are fabricated, controls an image on a liquid crystal display through precisely polarizing a liquid crystal material located between the backplane and another layer of glass. The second layer of glass, in certain

embodiments known as color filter glass (CF), is the location of color filters, one per sub-pixel, used to create color images. Presently, the preferred backplane active device is the thin-film transistor (TFT), which is a semiconductor based device comprised of sequentially deposited and patterned thin-film layers. Thin-film semiconductor materials used in TFTs have many limitations, including low carrier mobility, light and temperature sensitivity, and fabrication complexities, which create performance and manufacturing cost issues. Thus, new devices which overcome such limitations, such as those disclosed herein, represent an advance in the state of the art.

Summary of the Invention

[0004] Amorphous metal non-linear resistors (AMNR) may be particularly desirable for use in circuits of the present invention, because and AMNR does not employ semiconductor materials, and therefore, an LCD backplane based on AMNRs can overcome the performance and cost issues associated with TFT based LCD backplanes. (AMNRs are further described in published PCT application WO 2014074360 and U.S. Patent 9,099,230, the entire contents of which are incorporated herein by reference.) An AMNR based LCD backplane can therefore provide an important advance in the art. For example, the use of pixel electrodes that modulate the polarization of liquid crystal materials in the plane of the LCD backplane substrate, in-plane switching (IPS), has advanced the performance of LCDs in terms of picture quality. The use of AMNRs as the active devices in an IPS LCD backplane may provide high-performance LCDs that are manufactured with simple materials and processes, thereby reducing manufacturing costs.

[0005] Thus, in one of its aspects, the present invention relates to a sub-pixel circuit for in-plane switching in a liquid crystal display backplane, where the circuit may include AMNRs along with methods for the production of such circuit. In particular, an amorphous metal thin-film may be patterned to provide, in a single layer, electrical interconnects for each of two or more AMNRs and a lower electrode of a storage capacitor.

[0006] In an additional aspect, the present invention may provide a method of fabricating a sub-pixel circuit employing two AMNRs and a storage capacitor possessing an AMTF lower electrode deposited concurrently with the AMNR

amorphous metal interconnects. The sub-pixel circuit may be disposed on a substrate that supports the materials used to physically realize the circuit. In addition, the sub-pixel circuit may allow for the application of an electric field parallel to a substrate across a liquid crystal material disposed between two electrodes located in the same physical plane. Through the described exemplary method of fabrication, the present invention may provide interconnection of the described sub-pixel circuits into an addressable matrix of pixels that may be controlled independently to produce an image on an LCD. The exemplary manufacturing processes described herein may provide a means of LCD backplane fabrication capable of producing IPS based LCDs with reduced manufacturing costs relative to semiconductor based TFT backplane manufacturing costs. The reduction in manufacturing costs may result from fewer process steps, simpler process steps, and the elimination of semiconductor content.

Brief Description of the Drawings

[0007] The foregoing summary and the following detailed description of exemplary embodiments of the present invention may be further understood when read in conjunction with the appended drawings, in which:

[0008] Figure 1 schematically shows a lumped element model of an in-plane switching liquid crystal display sub-pixel circuit;

[0009] Figures 2A – 2D schematically show an exemplary process for forming a physical device corresponding to the model of Fig. 1, in which the device includes a dual select in-plane switching LCD sub-pixel circuit with two amorphous metal non-linear resistors and a storage capacitor formed with concurrently deposited and patterned an AMTF first layer;

[0010] Figures 3A – 3C schematically show cross-sectional views of the device of Fig. 2D, where Fig. 3B shows the cross-section across path A–B–C and Fig. 3C shows the cross-section across path 3C–3C;

[0011] Figures 4A – 4B schematically show the means through which individual sub-pixels may be connected to form a matrix of sub-pixels that may be addressed independently with row and column inversion;

[0012] Figures 5A – 5D schematically show an exemplary process for forming a dual select IPS LCD sub-pixel circuit without column inversion with two AMNRs and a storage capacitor formed with concurrently deposited and patterned AMTF first layer, with the exemplary process using four photolithographic patterning masks;

[0013] Figures 6A – 6B schematically show an exemplary implementation of an AMNR based IPS LCD sub-pixel circuit that does not enable column inversion, and a cross section through path A–B–C, with a storage capacitor formed between a data signal interconnect, the storage capacitor having an amorphous metal lower electrode; and

[0014] Figures 7A – 7B schematically show the means through which individual sub-pixels may be connected to form a matrix of sub-pixels that may be addressed independently with row inversion but without column inversion.

Detailed Description of the Invention

[0015] Referring now to the figures, wherein like elements are numbered alike throughout, exemplary devices and methods in accordance with the present invention are shown which may provide in-plane switching in a liquid crystal display backplane. Such devices and methods may typically include amorphous metal non-linear resistors (AMNRs), which may be described as a two terminal device possessing symmetric current-voltage (IV) characteristics. For example, Figure 1 schematically illustrates a non-limiting exemplary lumped element diagram of a sub-pixel circuit 8 where two AMNRs 5 may be used to precisely polarize a liquid crystal material LC through the application of an electric field to a capacitor 6. The area within the dashed line 8 denotes the physical elements of a sub-pixel. The capacitor 6 may include electrodes 2, 3 electrically connected to nodes A and B, with a dielectric comprised of the liquid crystal material LC disposed between the electrodes 2, 3. The electrodes 2, 3 may comprise indium tin oxide (ITO) disposed in the same physical plane on a backplane substrate, and nodes A and B may be the data and select nodes of the sub-pixel controlled by the sub-pixel circuit 8. A storage capacitor 7 may be electrically connected in parallel to the liquid crystal capacitor 6 to provide advantages to the operation of the sub-pixel circuit 8. The storage capacitor buffers the voltage located on the liquid crystal capacitor 6, thereby

reducing the voltage dependent capacitance and leakage effects existing for the liquid crystal capacitor 6.

[0016] Liquid crystal materials are long molecules that change orientation in response to an electric field applied across the liquid crystal material, i.e., liquid crystal materials are polarized through the application of an electric field. Polarization is, therefore, a physical process where the liquid crystal molecules are physically moved, or more precisely, rotated. A liquid crystal material, when repeatedly rotated in the same direction many times, experiences less resistance to rotation in the same direction. Less rotational resistance changes the magnitude of polarization of a liquid crystal material at the same applied electric field magnitude, which is an undesirable effect. To avoid a polarization magnitude change, the polarity of an electric field that is applied to a liquid crystal material may be regularly changed or, more precisely, inverted. Certain non-limiting embodiments of the described invention allow for the inversion of applied electric fields to an array of IPS LCD sub-pixels by both row and columns in the array. The inversion of sequential rows of an array in addition to the inversion of sequential columns in the array is referred to, by those skilled in the art, as dot inversion. In another non-limiting embodiment of the described invention, referred to those skilled in the art as row inversion, sequential rows in an array of IPS LCD sub-pixels are inverted while sequential columns are not.

[0017] Figures 2A – 3C schematically illustrate a non-limiting, exemplary process for fabricating an in-plane switching (IPS) LCD sub-pixel circuit corresponding to the circuit model shown in Fig. 1. (The area within the dashed box of Figs. 2A–2D corresponds to the outlined area in Fig. 1.) The exemplary process sequence presented in Figs. 2A – 3C may employ the patterning of four material layers which compares favorably to the present state of the art for high-volume manufacturing of high definition and ultra-high definition IPS LCD televisions which employs five patterning steps. Additionally, the exemplary process allows for the use of dot inversion with respect to the polarity of adjacent sub-pixels.

[0018] First, an amorphous metal thin film (AMTF) with thickness less than 50 nm may be deposited concurrently and patterned into a lower electrode 10 of the storage capacitor 7 and patterned into two AMNR lower interconnects 11, 12. The lower

interconnects 11, 12 may provide first and second row select lines for addressing the pixel within a matrix of pixels. The AMTF layer may be ultra-smooth with an RMS roughness less than 0.5 nm when deposited. The ultra-smooth, i.e., < 0.5 nm RMS, surface morphology of the AMTF electrode 10 and interconnects 11, 12 can provide the ability to precisely apply an electric field across the storage capacitor 7 comprising lower electrode 10 and/or AMNRs 5 comprising lower interconnects 11, 12. After the patterning of the AMTF to provide the electrode 10 and interconnects 11, 12, an unpatterned dielectric layer comprising, but not limited to, metallic oxides, metallic nitrides, semiconductor oxides or semiconductor nitrides, may be deposited onto the electrode 10 and interconnects 11, 12 to provide a tunnel barrier 32, Fig. 3B.

[0019] Subsequently a layer comprising, but not limited to, a thin film of crystalline metal or a stack of two or more thin films of crystalline metals, may be deposited onto the tunnel barrier 32. The deposited crystalline metal thin-film, or stack of crystalline metal thin-films, may then be patterned to form select line interconnects, S1, S2 and select interconnect node 13 (which corresponds to node A in Fig. 1) between the select lines S1, S2, Figs. 2B, 3B.

[0020] An insulating, dielectric layer 34 comprising, but not limited to, metallic oxides, metallic nitrides, semiconductor oxides or semiconductor nitrides, may be deposited onto the patterned select lines S1, S2 and interconnect node 13. The insulating layer 34 may function as the second layer of dielectric for the storage capacitor 7, as a passivation layer for the AMNRs 5, and as an inter-layer dielectric (ILD) located above the select lines S1, S2, and below subsequently deposited metal layers. A hole in the dielectric layer 34 may be subsequently patterned to provide a storage capacitor contact 14, a select interconnect node contact 15, and select line bridge contacts 16, Fig. 2C.

[0021] Finally, a top layer metal stack may be deposited onto the dielectric layer 34. A first layer 37 of the stack may include a transparent conducting oxide, e.g., indium tin oxide (ITO) layer 37. The ITO layer 37 may form the electrodes 17a, 17b of an IPS liquid crystal capacitor 17 corresponding to the liquid crystal capacitor 6 illustrated in Fig. 1. The subsequent layer(s) 36 of the metal stack may be sequentially deposited onto the ITO layer 37 and may comprise either a thin film of crystalline metal or a stack of two or more thin films of crystalline metals. The

crystalline metal thin film or the stack of two or more thin films of crystalline metals, in conjunction with the ITO layer 37, may provide a data signal interconnect 18 and the select line bridge 19, through which column inversion may be effected. Since the lower interconnects 11, 12 of the AMNRs 5 may provide first and second row select lines, the combination of row select by the AMNRs 5 and column inversion by the select line bridge 19 together can effect dot inversion in an IPS LCD. The contact between the data signal interconnect 18 and the ITO liquid crystal capacitor 17 may be made through the sequential deposition of the data signal interconnect 18 directly onto the ITO liquid crystal capacitor layer 37. Thus, correlating the structures in Figs. 2A–3C to those in Fig. 1, the storage capacitor 7 of Fig. 1 can be seen to be realized by the combination of the lower electrode 10, the tunnel barrier 32, the insulating layer 34, and the data signal interconnect 18 to provide storage capacitor 20, Fig, 3C. Likewise, one AMNR 5 of Fig. 1 can be seen to be realized by the combination of the interconnect 12, the tunnel barrier 32, the select line S1, and the select interconnect node 13, and the other AMNR 5 of Fig. 1 by the combination of the interconnect 11, the tunnel barrier 32, select line S2, and the select interconnect node 13.

[0022] In a certain embodiment of this invention, a process sequence to pattern the top layer metal stack may use, but is not limited to, a multi-tone exposure process. This process allows for the formation of the IPS liquid crystal capacitor 17, data signal interconnect 18, and the select line bridge 19 through one photolithographic mask.

[0023] In another embodiment of the described invention, the chemistries used to etch the ITO layer 37 and the subsequently deposited crystalline metal layer or layers 36 may be engineered to etch only the ITO or the crystalline metal layer(s). The described etch chemistries, therefore, may be defined as selective to the layer that is being etched by them. The use of selective etch chemistries may enhance the effectiveness of multi-tone photolithographic patterning techniques and may also allow for the use of two separate masking layers.

[0024] Figures 3A – 3C schematically illustrate cross sectional views of the device of Fig. 2D. The cross sectional view along the path A–B–C shows the path of the select line bridge 19 over the AMNR 5 comprising select line S2 and the select

interconnect node 13. As the ITO is more resistive than crystalline metals, it can be important to have the crystalline metal or crystalline metal stack 36 incorporated into the select line bridge 19 to keep the select line resistance low. Two contact holes 16 in the ILD (dielectric layer 34) provide the means through which the select line bridge 19 may be connected to the select line S1. The cross sectional view through points 3C–3C illustrate the means by which one of the ITO electrodes 17b of the liquid crystal capacitor 17 may be connected to the storage capacitor 20. The ITO/storage capacitor contact 14 may be patterned through both the ILD 34 and the tunnel barrier 32 allowing contact between the ITO of the liquid crystal capacitor electrode 17b and the storage capacitor lower electrode 10.

[0025] Storage capacitor area may be defined by the overlap between the storage capacitor AMTF lower electrode 10 and the data signal interconnect 18. Storage capacitor area may, therefore, be easily modulated by the dimensions of the AMTF lower electrode 10 and/or the dimensions of the data signal interconnect 18 where it overlaps the AMTF lower electrode 10. Additionally, the storage capacitor 20, will not significantly decrease the amount of light that is transmitted through the IPS LCD sub-pixel as it is located underneath the data signal interconnect 18. The percentage of light transmitted through an IPS LCD sub-pixel is an important consideration to sub-pixel design. Therefore, the fabrication sequence described in this disclosure that creates a storage capacitor 20 within an AMNR based IPS LCD sub-pixel provides an important contribution to light transmission.

[0026] IPS LCD sub-pixels using AMNRs, as described herein, may be connected into an array as shown in Figs. 4A – 4B; the area of the dashed line of Fig. 4A corresponds to the area of the dashed line in Fig. 2D, and the area of the dashed line of Fig. 4B corresponds to the area of the dashed line in Fig. 1. The polarity of the sequential pairs of select lines, e.g., $S1_i$ and $S2_i$, then $S1_{i+1}$ and $S2_{i+1}$, may alternate between positive and negative polarity, giving rise to row inversion. Through the use of the select line bridge 19, sequential data signal columns D_i, D_{i+1} may have alternating polarity across row of sub-pixels, giving rise to column inversion. The combination of row inversion and column inversion leads to dot inversion. The polarity of the data signals applied to the liquid crystal capacitors 17 is shown as + and – in Fig. 4B, providing a schematic representation of dot inversion. Dot

inversion (a current best practice in IPS LCD televisions) is readily achieved using AMNR based sub-pixels using four patterning steps by the invention described herein.

[0027] In certain embodiments of the described invention, row inversion without column inversion, i.e., no dot inversion, provides sufficient image quality for an IPS LCD. Figures 5A – 5D schematically illustrate an exemplary, non-limiting sequence of fabrication process steps used to create an AMNR based IPS LCD sub-pixel without column inversion. The area of the dashed line of Figs. 5A–5D corresponds to the area of the dashed line in Fig. 1.

[0028] First an amorphous metal thin film (AMTF) with thickness less than 50 nm is deposited and patterned into a storage capacitor lower electrode 510 and two AMNR lower interconnects 511, 512 , one for select line S25 and one for select line S15. Without the need for column inversion, in certain embodiments of the described invention, select line S15 and select line S25 may be positioned on opposite sides of the IPS LCD sub-pixel and, therefore, there is no need for a select line bridge. Removal of the select line bridge reduces the number of contact holes in the sub-pixel from 4 contacts to 3 contacts, which may be an advantage. After the described patterning of the AMTF, an unpatterned dielectric layer comprised of, but not limited to, metallic oxides, metallic nitrides, semiconductor oxides or semiconductor nitrides, may be sequentially deposited onto the patterned AMTF interconnects 511, 512 and storage capacitor lower electrode 510 to provide a tunnel barrier 532 thereover, Fig. 6B.

[0029] Subsequently a layer comprised of, but not limited to, a thin film of crystalline metal or a stack of two or more thin films of crystalline metals, may be deposited onto the tunnel barrier 532. The layer of deposited crystalline metal thin-film, or stack of crystalline metal thin-films, may then be patterned to form the select line interconnects, S15 and S25, and the select interconnect nodes 513 between the select lines which corresponds to node A in Fig. 1. There may be two select interconnect nodes in a sub-pixel that does not provide dot inversion.

[0030] An insulating, dielectric layer 534 comprised of, but not limited to, metallic oxides, metallic nitrides, semiconductor oxides or semiconductor nitrides, may be sequentially deposited onto the patterned interconnect lines S15, S25 and

interconnect node 513, Fig. 6B. The insulating layer 534 may function as the second layer of dielectric for the storage capacitor 520, as a passivation layer for the AMNR interconnects 511, 512, and as an inter-layer dielectric (ILD) located above the select lines, S15 and S25, and below subsequently deposited metal layers. Holes in the ILD may subsequently be patterned as a storage capacitor contact 514 and select interconnect node contacts 515.

[0031] Thereafter, a top layer metal stack may be deposited onto the ILD. The first layer 537 of the stack may be a transparent conducting oxide, i.e., indium tin oxide (ITO). The ITO layer 537 may provide the electrodes 517a, 517b of an IPS liquid crystal capacitor 517 corresponding to the liquid crystal capacitor 6 illustrated in Fig. 1. The subsequent layer(s) of the metal stack 536 may be sequentially deposited onto the ITO layer 537 and may be comprised either a thin film of crystalline metal or a stack of two or more thin films of crystalline metals. The crystalline metal thin film 536 or the stack of two or more thin films of crystalline metals, in conjunction with the ITO layer 537, may provide a data signal interconnect 518. The contact between the data signal interconnect 518 and the ITO liquid crystal capacitor 517 may be made through the sequential deposition of the data signal interconnect layer 536 directly onto the ITO liquid crystal capacitor layer 537.

[0032] In a certain embodiment of this invention, a process sequence to pattern the top layer metal stack may use, but is not limited to, a multi-tone exposure process. This process allows for the formation of the IPS liquid crystal capacitor 517 and the data signal interconnect 518 through one photolithographic mask.

[0033] In another embodiment of the described invention, the chemistries used to etch the ITO layer 537 and the subsequently deposited crystalline metal layer or layers may be engineered to etch only the ITO or the crystalline metal layer(s). The described etch chemistries may, therefore, be defined as selective to the layer that is being etched by them. The use of selective etch chemistries may enhance the effectiveness of multi-tone photolithographic patterning techniques and also allows for the use of two separate masking layers.

[0034] Storage capacitor area may be defined by the overlap between the storage capacitor AMTF lower electrode 510 and the data signal interconnect 518. Storage capacitor area may be therefore, easily modulated by the dimensions of the AMTF

lower electrode 510 and/or the area of the data signal interconnect 518 where it overlaps with the AMTF lower electrode 510. Additionally, the storage capacitor 520, will not significantly decrease the amount of light that is transmitted through the IPS LCD sub-pixel as it is located underneath the data signal interconnect 518. The percentage of light transmitted through an IPS LCD sub-pixel is an important consideration to sub-pixel design. Therefore, the fabrication sequence described in this disclosure that creates a storage capacitor within an AMNR based IPS LCD sub-pixel provides an important contribution to light transmission.

[0035] The layout and cross section provided in Figs. 6A – 6B illustrate that a storage capacitor 520 formed by the overlap between a lower AMTF layer containing components 510, 511, 512 and a data signal interconnect 518 is analogous between the AMNR based IPS LCD sub-pixel that enables dot inversion (e.g., Figs. 4A, 4B) and the AMNR based IPS LCD sub-pixel that only enables row inversion, Fig. 5D. The connection between the select signal ITO electrode 517b of the liquid crystal capacitor 517 and the storage capacitor lower electrode 510 may be made through a contact 514 through the ILD layer 534 and the tunnel barrier layer 532, Fig. 6B.

[0036] Figs. 7A – 7B provide a schematic representation of an array of AMNR based IPS LCD sub-pixels that enables row inversion but not dot inversion. There are no select line bridges in the exemplary array, and the select lines $S1_i$, $S2_i$ for a sub-pixel are located on opposite sides of the sub-pixel. The polarities of the sub-pixels is represented as + and – in the circuit diagram array.

[0037] These and other advantages of the present invention will be apparent to those skilled in the art from the foregoing specification. Accordingly, it will be recognized by those skilled in the art that changes or modifications may be made to the above-described embodiments without departing from the broad inventive concepts of the invention. It should therefore be understood that this invention is not limited to the particular embodiments described herein, but is intended to include all changes and modifications that are within the scope and spirit of the invention as set forth in the claims.

Claims

What is claimed is:

1. An in-plane switching liquid crystal sub-pixel circuit, comprising:
   first and second amorphous metal non-linear resistors each having a respective lower electrode interconnect comprising an amorphous metal thin film;
   a storage capacitor having a lower capacitor electrode comprising an amorphous metal thin film,
   wherein the lower electrode interconnects and lower capacitor electrode are disposed within the same plane.
2. The sub-pixel circuit of claim 1, wherein the amorphous metal thin film of the lower electrode interconnects and of the lower capacitor electrode have a thickness of about 50 nm or less.
3. The sub-pixel circuit of any one of the preceding claims, comprising a dielectric layer disposed over the lower electrode interconnects and lower capacitor electrode, and wherein the storage capacitor comprises a data signal interconnect disposed above the lower capacitor electrode with a portion of the dielectric layer disposed therebetween, whereby the data signal interconnect, the lower capacitor electrode, and the portion of the dielectric layer cooperate to provide the storage capacitor.
4. The sub-pixel circuit of claim 3, comprising two liquid crystal capacitor electrodes disposed in a plane over the dielectric layer, wherein the liquid crystal capacitor electrodes and data signal interconnect are disposed in the same plane.
5. The sub-pixel circuit of claim 4, comprising an upper contact electrically connected between the amorphous metal non-linear resistors, the upper contact electrically connected to a selected one of the liquid crystal capacitor electrodes.
6. The sub-pixel circuit of any one of claim 3–5, comprising:
   at least one select line comprising a crystalline metal disposed over the dielectric layer, the at least one select line having first and second segments with a gap disposed therebetween, with the lower electrode of a selected one of the amorphous metal non-linear resistors disposed in the gap between the first and second segments; and
   an interconnect bridge electrically connected to the first and second segments

of the select line, the bridge disposed above the lower electrode of the selected amorphous metal non-linear resistor.

7. The sub-pixel circuit of claim 6, wherein the interconnect bridge extends from the first and second segments into the plane of the liquid crystal capacitor electrodes.
8. An array of the sub-pixel circuits of any one of the preceding claims, comprising a tunnel barrier layer disposed over the lower electrode interconnects of the first and second amorphous metal non-linear resistors.
9. An array of the sub-pixel circuits of any one of the claims 6–8 arranged in a row/column matrix and configured to independently control the electric field applied to each sub-pixel liquid crystal capacitor that, along a matrix row, alternates the position of the interconnect bridge from the select line physically located below the liquid crystal capacitor electrodes to the select line physically located above the liquid crystal capacitor, then back to the select line physically located below the liquid crystal capacitor.
10. An array of the sub-pixel circuits of any one of claims 1–8 arranged in a row/column matrix configured to independently control the electric field applied to each sub-pixel liquid crystal capacitor.

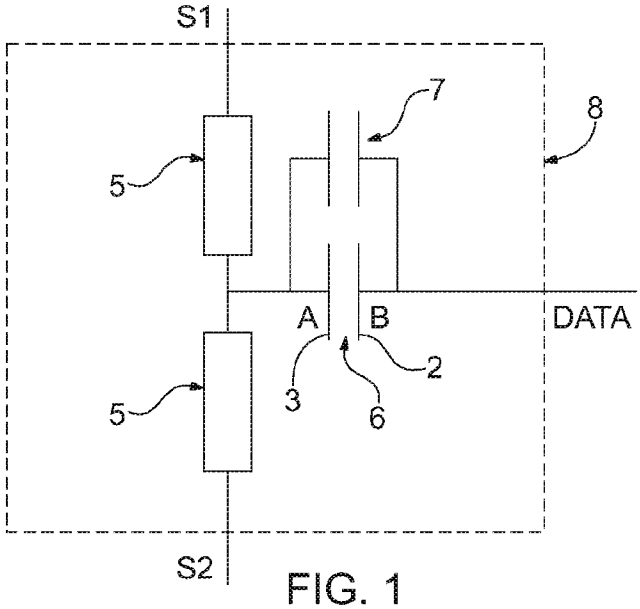

FIG. 1

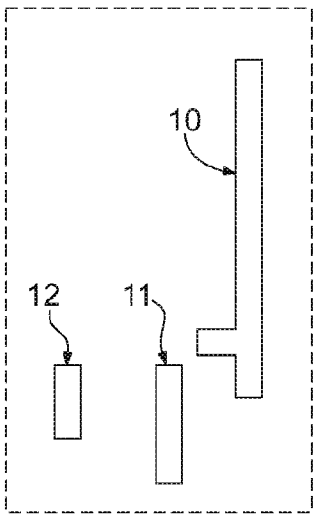

FIG. 2A

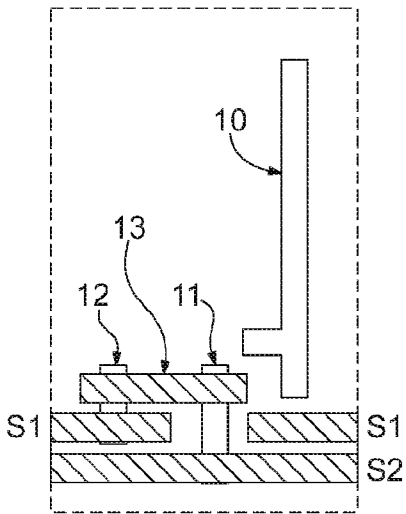

FIG. 2B

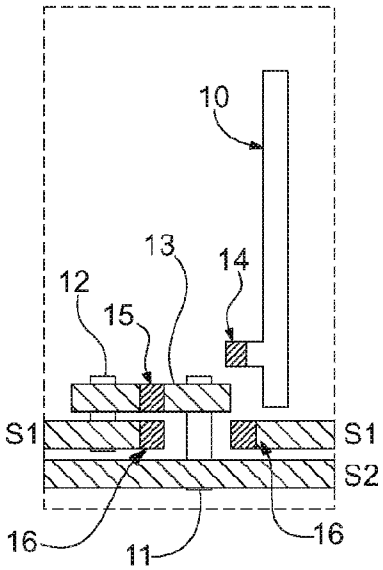
10
13
14
12
15
S1
S1
S2
16
11
16

FIG. 2C

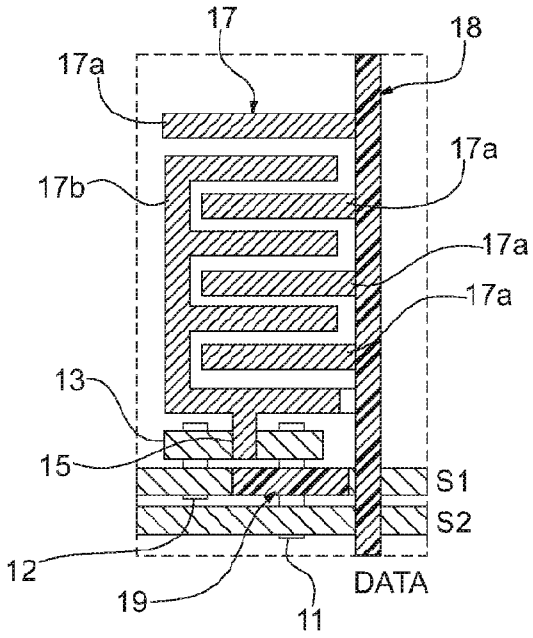
17
18
17a
17a
17b
17a
17a
13
15
S1
S2
12
19
11
DATA

FIG. 2D

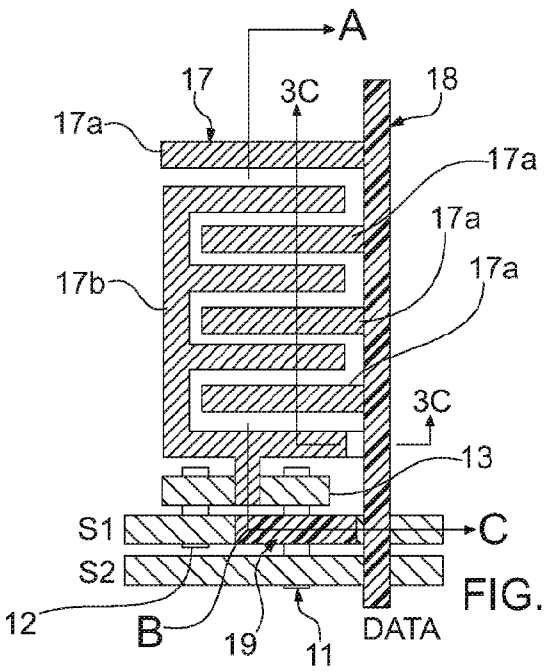

FIG. 3A

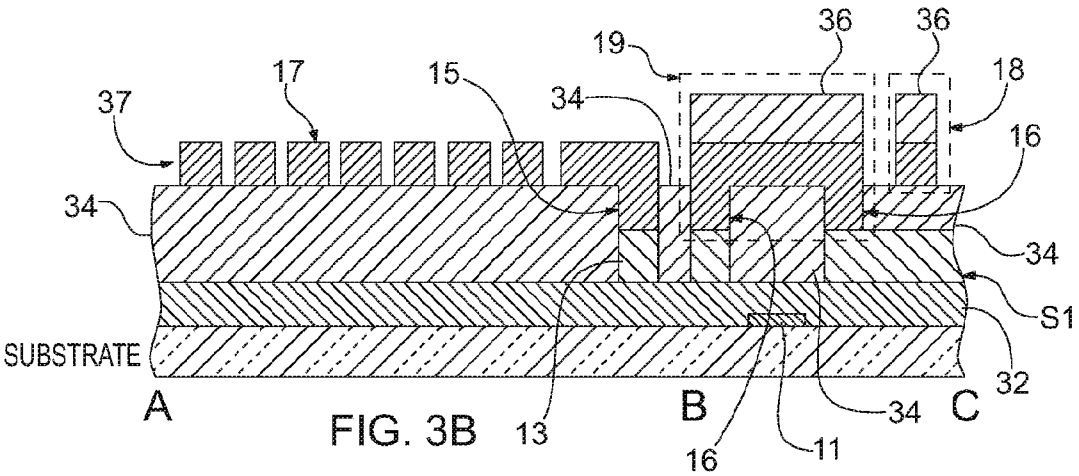

FIG. 3B

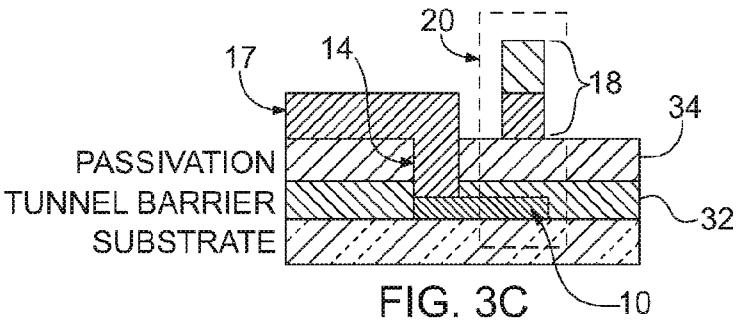

FIG. 3C

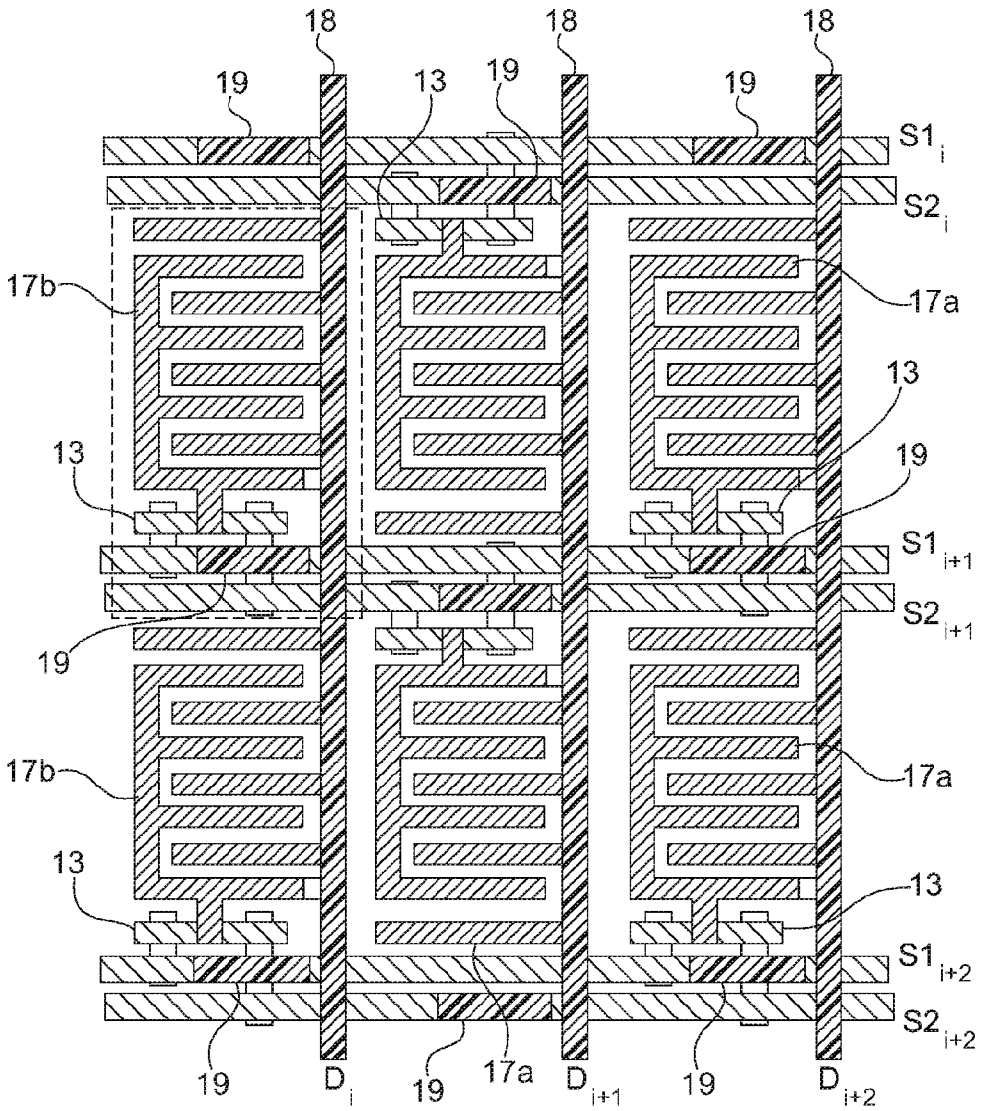
18
18
18
19
13
19
19
S1 i
S2 i
17b
17a
13
13
19
S1 i+1
S2 i+1
19
17b
17a
13
13
S1 i+2
S2 i+2
19
D i
19
17a
D i+1
19
D i+2

FIG. 4A

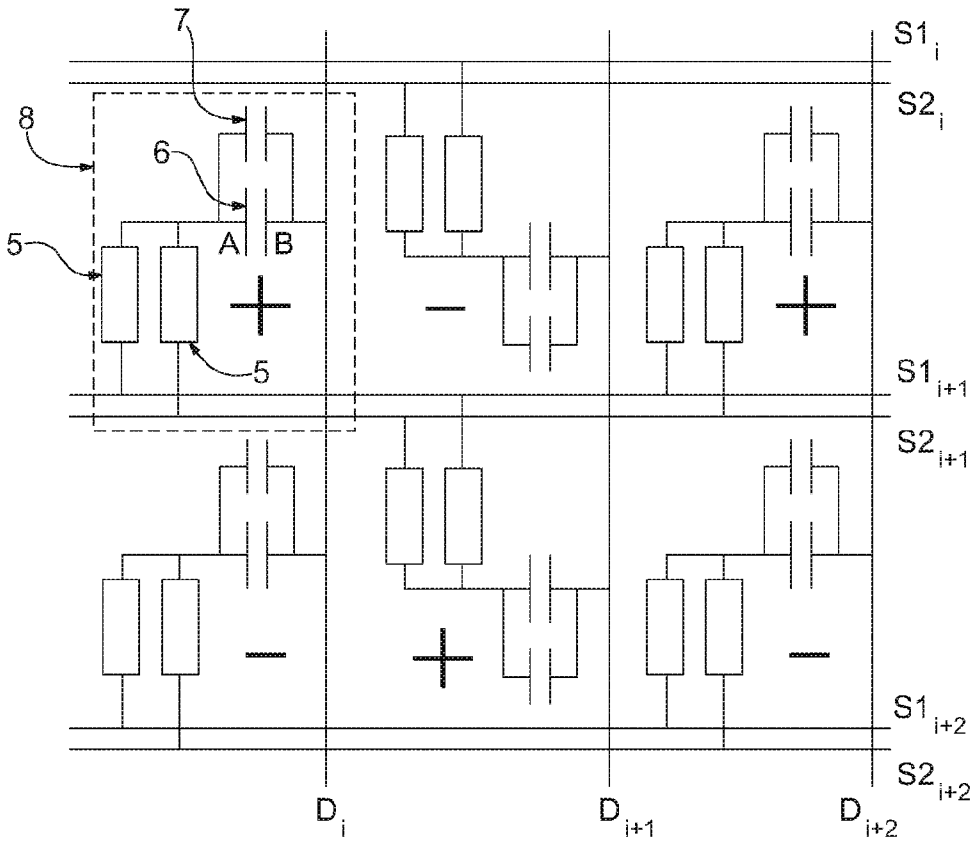

FIG. 4B

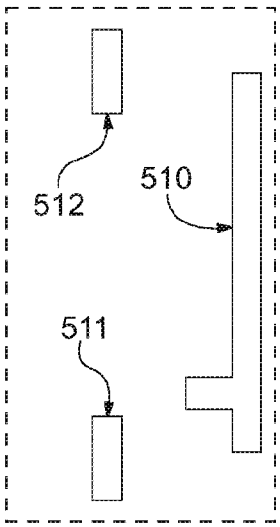

FIG. 5A

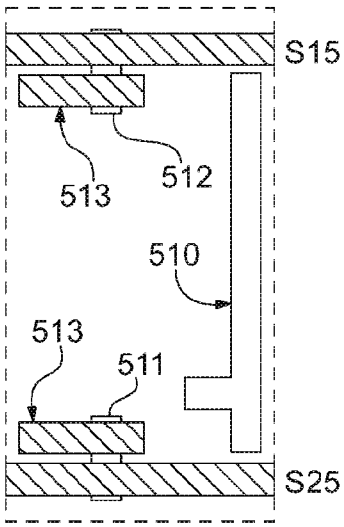

FIG. 5B

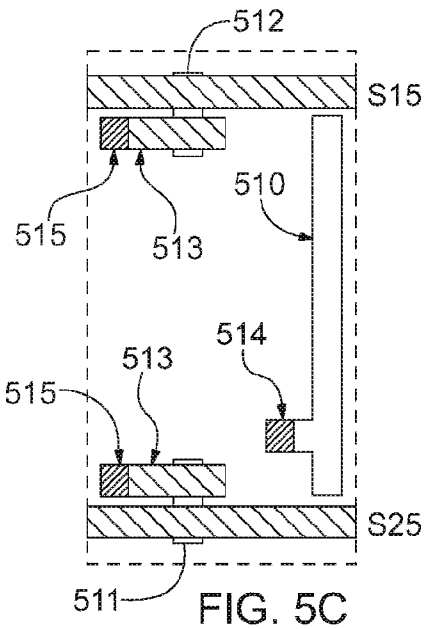

FIG. 5C

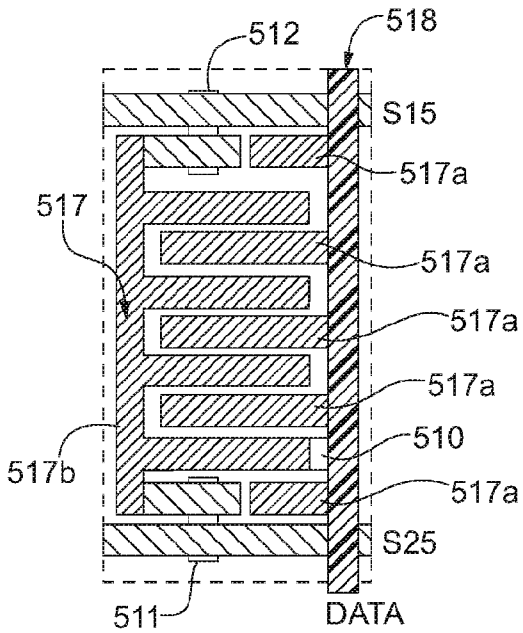

FIG. 5D

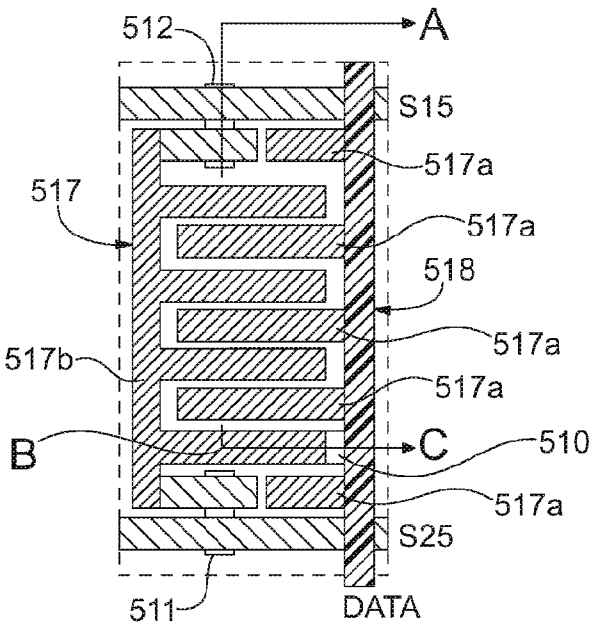
512
A
S15
517a
517
517a
518
517a
517b
517a
B
C
510
517a
S25
511
DATA

FIG. 6A

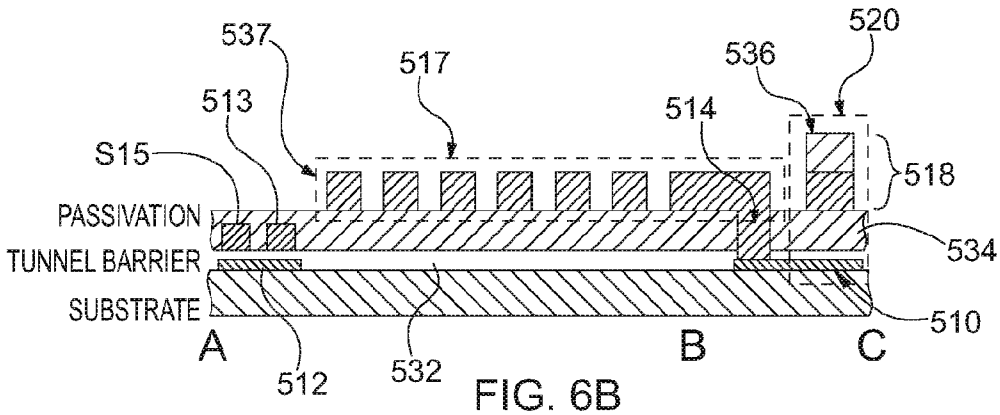
537
517
536
520
513
514
S15
518
PASSIVATION
534
TUNNEL BARRIER
SUBSTRATE
510
A
B
C
512
532

FIG. 6B

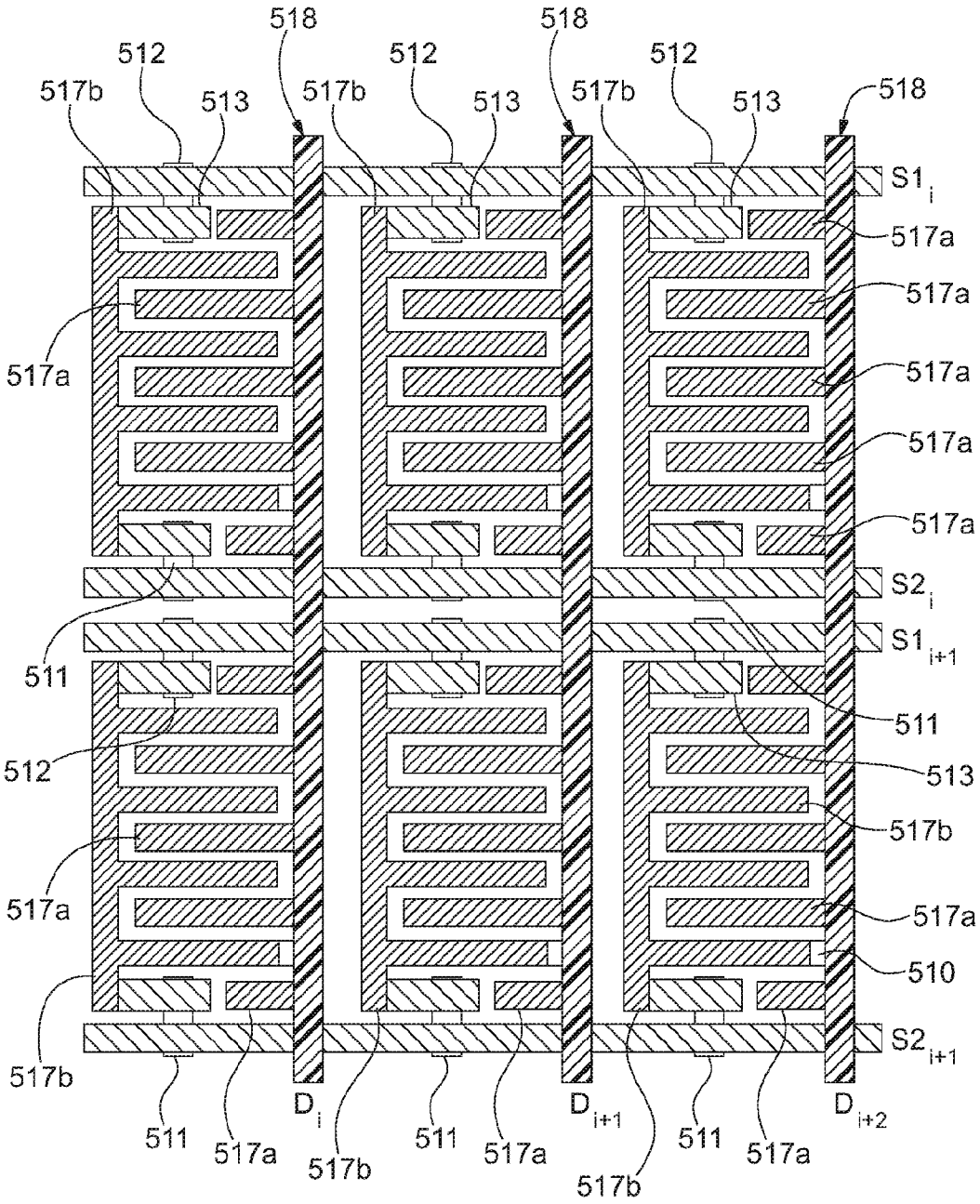
518
512
517b
513
518
512
517b
513
518
512
517b
513
518
S1i
517a
517a
517a
517a
517a
517a
S2i
S1i+1
511
511
512
513
517b
517a
517a
510
517b
S2i+1
511
517a
517b
511
517a
517b
511
517a
Di
Di+1
Di+2

FIG. 7A

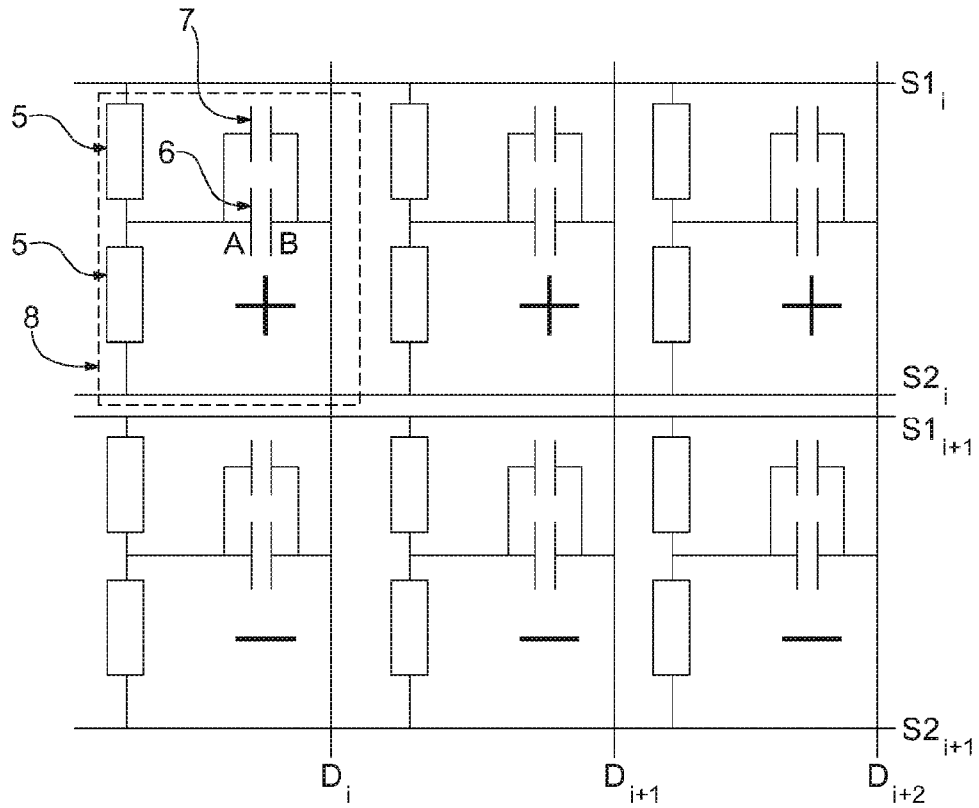

FIG. 7B

PCT/US2016/043230

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 7
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
Claim 7 is considered to be unclear, because it refers to a claim, which does not comply with PCT Rule 6.4(a).

3. ☒ Claims Nos.: 6,8-10
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required addtional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/043230

A. CLASSIFICATION OF SUBJECT MATTER

G02F 1/1343(2006.01)i, G02F 1/1362(2006.01)i, G02F 1/1368(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G02F 1/1343; G09G 5/02; H01C 1/012; G02F 1/1333; G06F 3/038; H01L 21/00; G02F 1/1362; G02F 1/1368

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: IPS LCD, sub-pixel, amorphous metal non-linear resistor, storage capacitor, liquid crystal capacitor electrode

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2011-0261028 A1 (JOON-CHUL GOH et al.) 27 October 2011 See paragraphs [0021], [0046]-[0049]; claim 6; and figure 1.	1-5
A	US 2009-0316061 A1 (YU-CHIEN KAO) 24 December 2009 See paragraphs [0022]-[0026]; and figure 4.	1-5
A	US 2010-0123744 A1 (JUN IBA et al.) 20 May 2010 See paragraphs [0031]-[0035], [0125]; claim 1; and figure 1	1-5
A	US 2014-0293166 A1 (INNOLUX CORPORATION) 02 October 2014 See paragraphs [0017]-[0024]; claims 1, 6; and figures 1-2.	1-5
A	WO 2014-074360 A1 (THE STATE OF OREGON ACTING BY AND THROUGH THE STATE BOARD OF HIGHER EDUCATION ON BEHALF OF OREGON STATE UNIVERSITY) 15 May 2014 See paragraphs [0016]-[0020]; and figure 1A.	1-5

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 October 2016 (24.10.2016)	**24 October 2016 (24.10.2016)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
LEE, Dong Yun
Telephone No. +82-42-481-8734

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2016/043230

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2011-0261028 A1	27/10/2011	KR 10-2011-0117998 A	28/10/2011
		US 8803855 B2	12/08/2014
US 2009-0316061 A1	24/12/2009	TW 201001036 A	01/01/2010
		TW I372932 B	21/09/2012
		US 8149344 B2	03/04/2012
US 2010-0123744 A1	20/05/2010	JP 2010-123338 A	03/06/2010
		US 8378937 B2	19/02/2013
US 2014-0293166 A1	02/10/2014	CN 102053410 A	11/05/2011
		CN 102053410 B	21/11/2012
		JP 2011-096249 A	12/05/2011
		JP 5697939 B2	08/04/2015
		US 2011-0102692 A1	05/05/2011
		US 8804058 B2	12/08/2014
WO 2014-074360 A1	15/05/2014	CN 105264618 A	20/01/2016
		JP 2016-502268 A	21/01/2016
		KR 10-2015-0084879 A	22/07/2015
		TW 201432735 A	16/08/2014
		US 2014-0368310 A1	18/12/2014
		US 9099230 B2	04/08/2015