(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
20 September 2001 (20.09.2001)

PCT

(10) International Publication Number
WO 01/69658 A2

(51) International Patent Classification[7]: H01L

(21) International Application Number: PCT/US01/07175

(22) International Filing Date: 6 March 2001 (06.03.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/524,262 13 March 2000 (13.03.2000) US

(71) Applicant (*for MC only*): **PHILIPS SEMICONDUCTORS, INC.** [US/US]; 811 East Arques Avenue, Sunnyvale, CA 94088 (US).

(71) Applicant (*for AT, BE, CH, CN, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, JP, KR, LU, NL, PT, SE, TR only*): **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL]; Groenewoulseweg 1, NL-5621BA Eindhoven (NL).

(72) Inventor: **MITCHELL, Todd**; 15918 Alsace, San Antonio, TX 78232 (US).

(74) Agents: **GALLENSON, Mavis, S.** et al.; Ladas & Parry, Suite 2100, 5670 Wilshire Boulevard, Los Angeles, CA 90036-5679 (US).

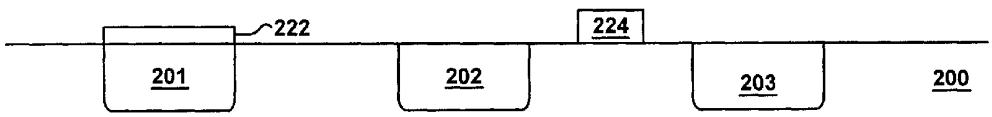
(81) Designated States *(national)*: CN, JP, KR.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: ONE-TIME PROGRAMMABLE ANTI-FUSE ELEMENT AND METHOD



(57) Abstract: The present invention is drawn to a method and a system for creating a one time programmable anti-fuse element. No amorphous silicon is used as in the prior art approach. Rather, a side wall spacer etch blocking mask is used to form a poly diode as the one time programmable anti-fuse element. In particular, in creating the one time programmable anti-fuse element, the present invention uses steps from existing standard process flow typically used for fabricating a standard semiconductor device such as a transistor. As such, these steps can be performed concurrently with the process flow of a standard semiconductor device. Thus, advantageously, the present invention does not perturb the existing process flow in creating the poly diode as the one time programmable anti-fuse element. Moreover, a forward biased current can be driven through the poly diode to destroy ("blow") it as the one time programmable anti-fuse element. As an added bonus, when compared to the blown prior art anti-fuse element, the blown anti-fuse element is harder to detect. Thus, advantageously, the anti-fuse element of the present invention is well suited for security applications.

WO 01/69658 A2

ONE-TIME PROGRAMMABLE ANTI-FUSE ELEMENT AND METHOD

FIELD

The present disclosure relates to a one time programmable anti-fuse element and method. Specifically, the present invention relates to forming a one time programmable anti-fuse element on a semiconductor substrate.

BACKGROUND

In a conventional one time programmable anti-fuse element, a specified amount of current is passed through the element in order to "blow" (destroy) the element. This destruction is irreversible, thus the term "one time programmable." By "blowing" the one time programmable anti-fuse element, conductive pathways can be selectively formed.

One time programmable anti-fuse elements can be used in security applications such as setting private individuals preferences in electronic equipments (e.g., a C.D. player). A blown anti-fuse element is less detectable offers better security because private information entered by the user becomes more difficult to detect.

In creating a one time programmable anti-fuse element, a prior art approach uses an amorphous silicon based process to form the one time programmable anti-fuse element. However, several problems are associated with conventional amorphous silicon based process used to form the one time programmable anti-fuse element.

Specifically, the use of amorphous silicon necessitates at least three steps that are not typically performed by an existing standard process flow for creating a standard semiconductor device such as a transistor. These steps are a sputtering step, a masking step, and a etching step that do not ordinarily occur in an existing standard semiconductor device formation process flow. Each of these steps requires its own stepper. As a result, performing these steps perturbs the standard process flow. As such, producing one time programmable anti-fuse elements becomes costly and error-prone. Moreover, in a conventionally formed one time programmable anti-fuse element, one can readily determine whether the element has been blown or is intact, thus making the prior art anti-fuse element less suitable for security applications.

Referring now Figure 1, the prior art approach of creating a one time programmable anti-fuse element is depicted in its side sectional view. A semiconductor substrate 100, such as, for example, silicon, is used as the foundation of the one time programmable anti-fuse element to be created. An oxide layer 110 has been shown deposited on substrate 100. An amorphous silicon 111 has been formed on oxide layer 110. Amorphous silicon 111 functions as the one time programmable anti-fuse element. A metallic layer 122 touches one end of amorphous silicon 111 while another metallic layer 124 touches the other end of amorphous silicon 111.

Continuing with Figure 1, another metallic layer 140 is separated from amorphous silicon 111 by inter-metallic oxide 130 (IMO 130). At the same time, two contact via etches 143-144 allow metallic layer 140 to connect to amorphous silicon 111. In particular, contact via etches 143-144 are filled with conducting material such as, for example, tungsten, copper, or titanium.

Continuing still with Figure 1, the structure as shown in Figure 1 constitutes a one time programmable anti-fuse element because a current can be forced through amorphous silicon 111 to "blow the anti-fuse." Specifically, as current flows into amorphous silicon 111, the current changes the phase of amorphous silicon 111 and the aerial property of amorphous silicon 111 so that amorphous silicon 111 goes from a high electric resistance phase to a low electric resistance phase. In other words, amorphous silicon 111 goes into a conductive phase.

Still referring to Figure 1, substrate 100 and oxide layer 110 are deposited as in typically standard process flow. However, amorphous silicon 111 requires a different process chamber and additional steppers. In the process, amorphous silicon is blanket deposited with part of the layer etched away. Then, IMO is deposited. This process flow uses sputtering of amorphous silicon that requires special masking and special etching. Unfortunately, these three steps are normally not in the standard process flow typically used in creating a standard semiconductor device such as a transistor. Thus, the prior art approach cannot be implemented without perturbing the standard process flow.

Thus, a need exists for a one time programmable anti-fuse element whose formation does not require process steps foreign to a standard semiconductor device formation process flow. Furthermore, a need exists for a one time programmable anti-fuse element that can be produced without using amorphous silicon. Further still, a need exists for a one time programmable anti-fuse element whose condition (e.g., blown or intact) is difficult to detect.

Fortunately, as will be explained, the present invention answers all of the needs discussed above. Furthermore, the present invention offers advantages not available in the prior art approach.

SUMMARY:

The present invention provides a one time programmable anti-fuse element whose formation does not require process steps foreign to a standard semiconductor device formation process flow. Furthermore, the present invention provides a one time programmable anti-fuse element that can be produced without using amorphous silicon. Further still, the present invention provides a one time programmable anti-fuse element whose condition (e.g., blown or intact) is difficult to detect.

In one embodiment of the present invention, a method is provided for creating a one time programmable anti-fuse element. Specifically, a first doped region of a poly silicon region is formed above a shallow trench isolation (STI) region. A second doped region of the poly silicon region is also formed above the STI region. A dielectric material is deposited above the poly silicon region. In addition, a side wall spacer etch blocking mask is used to complete the formation of said poly silicon region. These steps can be performed using a standard process flow of forming a standard semiconductor device, while not perturbing the standard process flow. As such, these steps also can be performed concurrently with the formation of a standard semiconductor device, while not perturbing the standard process flow.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having

read the following detailed description of the preferred embodiments which are illustrated in the various drawing figures.

BRIEF DESCRIPTION OF THE FIGURES:

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and together with the description, serve to explain the principles of the invention:

Figure 1 depicts the side sectional view of a one time programmable anti-fuse element according to a prior art approach.

Figure 2A depicts the side sectional view of one fabrication phase of forming a one time programmable anti-fuse element concurrently with the formation of a semiconductor device in accordance with one embodiment of the present invention.

Figure 2B depicts the side sectional view of another fabrication phase of forming the one time programmable anti-fuse element concurrently with the formation of the semiconductor device in accordance with the embodiment in Figure 2A.

Figure 2C depicts the side sectional view of another fabrication phase of forming the one time programmable anti-fuse element concurrently with the formation of the semiconductor device in accordance with the embodiment in Figure 2A.

Figure 2D depicts the side sectional view of another fabrication phase of forming the one time programmable anti-fuse element concurrently with the formation of the semiconductor device in accordance with the embodiment in Figure 2A.

Figure 2E depicts the side sectional view of another fabrication phase of forming the one time programmable anti-fuse element concurrently with the formation of the semiconductor device in accordance with the embodiment in Figure 2A.

Figure 2F depicts the side sectional view of another fabrication phase of forming the one time programmable anti-fuse element concurrently with the formation of the semiconductor device in accordance with the embodiment in Figure 2A.

Figure 2G depicts the side sectional view of another fabrication phase of forming the one time programmable anti-fuse element concurrently with the formation of the semiconductor device in accordance with the embodiment in Figure 2A.

Figure 2H depicts the side sectional view of another fabrication phase of forming the one time programmable anti-fuse element concurrently with the formation of the semiconductor device in accordance with one embodiment in Figure 2A.

Figure 3 is a flow chart outlining the steps performed in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

Reference will now be made in detail to the preferred embodiments of the invention, a method for forming and an apparatus of a one time programmable anti-fuse element, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one ordinarily skilled in the art that the present invention may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the current invention.

Figures 2A to 2H depict side sectional views of one embodiment of the present invention in progressive stages of forming a one time programmable anti-fuse element. Because these stages can also be used without perturbation to the process flow for creating a standard semiconductor device such as a transistor, the formation of the transistor is shown concurrently in the same progressive stages.

However, as understood herein, the one time programmable anti-fuse element does not need to be formed concurrently with a standard semiconductor device such the transistor shown. The illustrated concurrent formations of the one time programmable anti-fuse element and the transistor are meant to highlight one advantageous feature of the present invention. That is, the one time programmable anti-fuse element can be formed using the standard process flow of forming a standard semiconductor device, while not requiring process steps foreign to the standard process flow.

Also, as will be described, in contrast to the prior art approach, the present embodiment does not use amorphous silicon to form the one time programmable anti-fuse element. Rather, the present embodiment uses a poly diode to form the one time programmable anti-fuse element. As an added benefit not found in the prior art approach, once the poly diode is blown, the damage to the poly diode is harder to detect than the damage done to the amorphous silicon based anti-fuse device of the prior art. Thus, the present embodiment is better suited for security applications.

Advantageously, although not necessary, the poly diode can be formed concurrently with the existing process flow for fabricating a standard semiconductor device such as a transistor. For this reason, each of Figures 2A to 2H depicts concurrent formation of a standard semiconductor device (e.g., a transistor) side by side with the illustrated formation of the one time programmable anti-fuse element (the poly diode).

The concurrent formations to be shown highlight the fact that forming the poly diode as the one time programmable anti-fuse element does not perturb the standard process for forming a standard semiconductor device.

Referring now to Figure 2A, a side sectional view of one embodiment of the present invention is depicted. Three shallow trench isolation (STI) regions 201-203 are formed within semiconductor substrate 200 that can be, for example, silicon. STI regions 201-203 are typically filled with an oxide using high density plasma deposition process.

Referring still to Figure 2A, in the present embodiment, the present poly diode will be formed above STI region 201. STI regions 202-203 are typically used to isolate neighboring electrical devices. A poly silicon region 222, which will become a part of a poly diode as a one time programmable anti-fuse element, is formed above STI region 201. The formation of poly silicon region 222 is adapted to be formed concurrently with the same process flow that is used to form poly silicon region 224, which will become a part of a standard semiconductor transistor. Specifically, poly silicon region 224 will be used as a gate of the standard semiconductor transistor.

In Figure 2A, the concurrent formations of poly silicon regions 222 and 224 are shown to highlight the fact that the same process flow can be used without perturbation to the process flow.

Referring now to Figure 2B, spacer oxide regions 231-232 and 234-235 are deposited. Also, poly silicon region 222 includes a first doped region shown as a n-doped region 213, and a second doped region shown as a p-doped region 217. As such, poly silicon region 222 is adapted to be used as a poly diode. However, as understood herein, the first and second doped regions need not be doped, respectively, with n-type and p-type dopants. For example, in an alternative embodiment, the first and second doped regions are doped, respectively, with p-type and n-type dopants. More generally, the first and second doped regions are doped, respectively, with dopants of a first conducting type and a second conducting type.

In Figure 2B, spacer oxide regions 231-232 are deposited beside the ends of poly silicon region 222. Also, oxide region 233 are deposited above poly silicon region 222 to cover both n-doped region 213 and p-doped region 217 such that two contact surfaces 281-282 are partially exposed. Concurrently, spacer oxide regions 234-235 have been deposited beside ends of poly silicon region 224 that will become a part of the transistor. The concurrent depositions of spacer oxide regions 231-232 (adjacent to poly silicon regions 222) and 234-235 (adjacent to poly silicon region 224) are shown to highlight the fact that these two depositions use the same process flow without perturbation to the process flow. Thus, as understood herein, spacer oxide regions 231-232 and 234-235 need not be deposited concurrently.

Referring now to Figure 2C, a titanium layer 250 is deposited. As for poly silicon region 222, titanium layer 250 covers substrate 100, spacer oxide regions 231-232, oxide region 233, and contact surfaces 281-282. Concurrently, as for poly silicon region 224, as a part of the standard semiconductor transistor, titanium layer 250 covers spacer oxide regions 234-235 and poly silicon region 224. The concurrent depositions of titanium layer 250 above poly silicon regions 222 and 224 are shown to highlight the fact that these two depositions use the same process flow without perturbation to the process flow. Thus, as understood herein, titanium layer 250 need not be deposited concurrently for both poly silicon regions 222 and 224. Specifically, even in the absence of a semiconductor device, titanium layer 250 can still be deposited above silicon region 222 for forming a one time programmable anti-fuse element.

Referring now to Figure 2D, rapid thermal annealing (RTA) is applied to portions of titanium layer 250. RTA causes the formation of silicide where portions of titanium layer 250 do not touch oxide. Specifically, the silicide formation occur everywhere except at chemically unreacted portions 251-255 of titanium layer 250 that touch, as shown respectively, oxide 231-235. Silicide portions that are formed by RTA have low electrical resistance. As will be described in Figure 2E, these silicide portions are to be used as electrical contacts.

In Figure 2D, RTA is applied for both poly silicon regions 222 and 224 to highlight the fact that forming the one time programmable anti-fuse element in accordance with the present embodiment does not introduce processing steps foreign to the standard process flow for forming a standard semiconductor device such as the transistor being formed here. However, as understood herein, even without the transistor being formed here, RTA can still be applied for forming the one time programmable anti-fuse element.

Referring now to Figure 2E, chemically unreacted portions 251-255 of titanium layer 250 are etched away, leaving only silicide portions 261-267 of titanium layer 250 as shown. As for the one time programmable anti-fuse element being formed, silicide portion 262 sits above contact surface 281 to form the electrical contact for n-doped region 213, whereas silicide portion 263 sits above contact surface 283 to form the electrical contact for p-doped region 217. As for the semiconductor transistor being formed concurrently using the standard process flow, silicide portions 265-267 become, respectively, the electrical contacts for drain, gate, and source of the semiconductor transistor.

In Figure 2E, the concurrent etchings of titanium layer 250 above poly silicon regions 222 and 224 are shown to highlight the fact that these two etchings use the same process flow without perturbation to the process flow. However, as understood herein, titanium layer 250 need not be etched concurrently for both poly silicon regions 222 and 224. Specifically, even in the absence of the transistor being formed here, titanium layer 250 can still be etched above silicon region 222 for forming a one time programmable anti-fuse element.

Referring now to Figure 2F, inter-metallic oxide (IMO) 270 is deposited as shown. Also as shown, concurrently with the formation of contact via etches 273-275 within IMO 270, contact via etches 271-272 have been formed within IMO 270. The concurrent formations of contact via etches 271-272 (for the one time programmable anti-fuse element) and 273-275 (for the transistor being formed) are shown to highlight the fact that these two depositions use the same process flow without perturbation to the process flow. Thus, as understood herein, contact via etches 271-272 for the one time programmable anti-fuse element need not be formed concurrently with contact via etches 273-275 for the transistor being formed. Specifically, even in the absence of the transistor being formed here, contact via etches 271-272 can still be formed above silicon region 222 for forming the one time programmable anti-fuse element.

Referring now to Figure 2G, contact via etches 271-275 are filled, respectively, with conducting plugs such as, for example, tungsten plugs 291-295. Moreover, planarization such as, for example, chemical mechanical polishing (CMP) is performed so that the exposed surface of IMO 270 is level with the exposed ends of tungsten plugs 291-295. Thus, because the planarization is a part of the standard process flow for creating the standard semiconductor transistor, tungsten plugs 291-292 are put in place without perturbing the process flow of forming the semiconductor transistor (or any other standard semiconductor devices).

In Figure 2G, planarization is applied for tungsten plugs 291-292 (for poly silicon regions 222) and 293-295 (for poly silicon region 224) to highlight the fact that forming the one time programmable anti-fuse element in accordance with the present embodiment does not introduce processing steps foreign to the standard process flow for forming a standard semiconductor device such as the transistor being formed here. However, as understood herein, even without the transistor being formed here, planarization can still be applied for forming the one time programmable anti-fuse element.

Referring now to Figure 2H, a metallic layer 290 is deposited above IMO 270. Specifically, metallic layer 290 connects electrically to poly silicon region 222 through both tungsten plugs 291-292 and silicide contacts 262-263. Also, metallic layer 290 connects electrically to drain, gate, and source of the semiconductor transistor through, respectively, tungsten plugs 293-295. Thus, formation of the electric paths from metallic layer 290 to poly silicon region 222 does not perturb the existing standard process flow for forming the standard semiconductor transistor (or any other standard semiconductor device).

As understood herein, concurrent electric paths formations for both poly silicon regions 222 and 224 are shown to highlight the fact that forming the one time programmable anti-fuse element in accordance with the present embodiment does not introduce processing steps foreign to the standard process flow for forming a standard semiconductor device such as the transistor being formed here. Even without the transistor being formed here, the electric paths from metallic layer 290 to poly silicon region 222 can still be formed using the same process flow.

Referring still to Figure 2H, poly silicon region 222 as a diode, with its electrical contacts to metallic layer 290 as shown, functions as a one time programmable anti-fuse element. Specifically, poly silicon region 222 can be programmed by driving a forward biased electric current through poly silicon region 222 from metallic layer 290. The forward biased electric current travels from metallic layer 290 through tungsten plug 291 and silicide contact 262 to enter n-doped region 213. Furthermore, the forward biased electric current travels to p-doped region 217, through silicide contact 263 and tungsten plug 292 to reach metâllic layer 290. As the electric current travels through poly silicon region 222, poly silicon region 222 is "blown" (i.e., destroyed) as a one time programmable anti-fuse element, thereby forming conducting path from n-doped region 213 to p-doped region 217.

Advantageously, in the process of forming poly silicon region 222 as a one time programmable anti-fuse element, no perturbation is introduced to the standard process flow for forming the standard semiconductor transistor (or any other standard semiconductor devices). Moreover, the damage to the blown one time programmable anti-fuse element is not readily detectable, thus making the element well suite for security applications.

Figure 3 is a flow chart outlining steps performed in accordance with one embodiment of the present invention.

In step 305, STI regions are formed in a semiconductor substrate. Standard semiconductor device such as a transistor is typically fabricated in the region between two STI regions. Nevertheless, according to the present embodiment, a one time programmable anti-fuse element will be formed using a poly silicon region above one of the STI regions.

In step 310, a n-doped region of the poly silicon region on the STI region is formed using the standard process flow typically used for creating a standard semiconductor device such as a transistor.

In step 315, a p-doped region of the poly silicon region is formed using the standard process flow. With its n-doped and p-doped regions, the poly silicon region is adapted to be used as a diode.

In step 320, a dielectric material is deposited above the poly silicon region using the standard process flow.

In step 325, a side wall spacer etch blocking mask from the standard process flow is used to cover the sides of the poly silicon region. Also, using the standard process flow, an oxide block partially covers the top surface of the poly silicon region.

In step 330, a titanium layer is deposited using the standard process flow to cover the poly silicon region, its side oxide block, and its side wall spacer etch blocking mask.

In step 335, RTA of the standard process flow is performed to the titanium. Portions of the titanium undergo chemical reaction. Specifically, portions of the titanium layer that touch the semiconductor substrate and/or the poly silicon region undergo chemical reaction that causes the formation of silicide.

In step 340, portions of the titanium layer that do not react with the substrate or the poly silicon region (i.e., the non-silicide portion of the titanium layer) are etched away using the standard process flow. After the etching process, silicide contacts remain on ends of the poly silicon region.

In step 345, IMO is deposited above the poly silicon region using the standard process flow.

In step 350, using the standard process flow, contact via etches are formed in the IMO so that, thereafter, silicide contacts of the poly diode are exposed.

In step 355, contact via etches reaching the poly diode are filled with tungsten plugs using the standard process flow.

In step 360, IMO and tungsten plugs are planarized using the standard process flow. Typically, the planarization is implemented with CMP.

In step 365, using the standard process flow, a metallic layer is deposited above IMO and the tungsten plugs. In so doing, electrical conducting paths are formed from the metallic layer to the poly silicon region as a poly diode. At this point, the poly diode can be used as a one time programmable anti-fuse element.

In step 370, poly diode is "blown" as a one time programmable anti-fuse element. In particular, a forward biased current is driven from the metallic layer through the poly diode to "blow the poly diode as the anti-fuse element." Advantageously, in contrast to the damage of a blown anti-fuse element of the prior art approach, the damage of the blown anti-fuse in the present embodiment is difficult to detect.

Referring still to the flow chart in Figure 3, the steps implemented (in creating the poly diode as the one time programmable anti-fuse element) do not perturb the existing process flow for a standard semiconductor device (e.g., a transistor). As such, these steps can be implemented concurrently with the fabrication process flow for a standard semiconductor device (e.g., a transistor) such that no perturbation of the process flow is introduced. Thus, advantageously, the existing process flow in forming a standard semiconductor device can also be used in creating a poly diode of the present invention as a one time programmable anti-fuse element. Also advantageously, as an added benefit, the blown anti-fuse element of the present invention, unlike the prior art anti-fuse element made of amorphous silicon, is very difficult to detect. Thus, the one time programmable anti-fuse element of the present invention is well suited for security applications.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are p possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the are to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. The scope of the invention is intended to be defined by the Claims appended hereto and their equivalents.

CLAIMS

What is claimed is:

1. A method for creating a one time programmable anti-fuse element, said method comprising the steps of:

b) forming a first doped region of a poly diode above a shallow trench isolation (STI) region;

c) forming a second doped region of said poly diode;

d) depositing a dielectric material above said poly diode; and

e) using a side wall spacer etch blocking mask to complete the formation of said poly diode, wherein said steps b) through e) are adapted to be performed with the standard process flow of forming a standard semiconductor device while not perturbing the standard process flow.

2. The method of Claim 1 further comprising the step of:

a) forming the shallow trench isolation (STI) region, wherein said steps a) through e) are adapted to be performed with the standard process flow of forming a standard semiconductor device while not perturbing the standard process flow.

3. The method of Claim 1 or 2 further comprising the steps of:

f) depositing a titanium layer above said poly diode;

g) performing a rapid thermal annealing (RTA) of said titanium layer, said titanium layer forming a first silicide contact above said first doped region and a second silicide contact above said second doped region; and

h) removing portions of said titanium layer which do not react with said semiconductor substrate and said poly diode, thereby exposing portion of said semiconductor substrate strapping said poly diode, and exposing portion of said poly diode, wherein at least said steps b) through h) are adapted to be performed with the standard process flow of forming a standard semiconductive device while not perturbing the standard process flow.

4. The method of Claim 3, further comprising the steps of:

i) depositing an inter-metal oxide (IMO) above said poly diode and said semiconductor substrate;

j) forming a first contact via etch in said IMO to expose said first silicide contact above said poly diode;

k) forming a second contact via etch in said IMO to expose said second silicide contact above said poly diode, wherein at least said steps b) through k) are adapted to be performed with the standard process flow of forming a standard semiconductor device while not perturbing the standard process flow.

5. The method of Claim 4 further comprising the steps of:

l) planting a first tungsten plus into said first contact via etch;

m) planting a second tungsten plug into said second contact via etch;

n) forming a flat surface on said IMO and said first and second tungsten plugs, said flat surface adapted to be covered by a metallic layer, wherein at least said steps b) through n) are adapted to be performed with the standard process flow of forming a standard semiconductor device while not perturbing the standard process flow.

6. The method Claim 5, wherein said flat surface is formed by performing chemical mechanical polishing (CMP) on said IMO and said first and second tungsten plugs.

7. The method of Claim 5 or 6 further comprising the steps of:

o) depositing a conducting metallic layer above said IMO and exposed parts of said first and second tungsten plugs, thereby creating a first conducting path connecting said conducting metallic layer to said poly diode through said first silicide contact, and thereby creating a second conducting path connecting said conducting metallic layer to said poly diode through said second silicide contact, wherein at least said steps b) through o) are adapted to be performed with the standard process flow of forming a standard semiconductor device while not perturbing the standard process flow.

8. The method of Claim 7, wherein said first conducting path connects said conducting metallic layer to said poly diode also through said first tungsten plug and said second conducting path connects said conducting metallic layer to said poly diode also through said second tungsten plug.

9. The method of Claim 7 or 8 further comprising the steps of:

p) programming said poly diode as a one time programmable anti-fuse element by driving a forward biased electric current through said poly diode from said conducting metallic layer, wherein said forward biased electric current travels from said conducting metallic layer through said first tungsten plug to said first doped region of said poly diode, and further travels to said second doped region of said poly diode through said second tungsten plug to said conducting metallic layer, and wherein at least said steps b) through p) are adapted to be performed with the standard process flow of forming a standard semiconductor device while not perturbing the standard process flow.

10. The method of Claim 9, wherein said forward biased electric current also travels through said first silicide contact when traveling to said first doped region of said poly diode, and also travels through said second silicide contact when further traveling to said second doped region of said poly diode.

11. The method of Claim 9 or 10, wherein damage of said blown poly diode is harder to detect when compared to a blown one time programmable anti-fuse element made from amorphous silicon.

12. The method of Claim 1 or 2, wherein at least said steps b) through e) are adapted to be performed concurrently with the formation of said standard semiconductor device, while not perturbing the standard process flow of forming said standard semiconductor device.

13. The method of any one of the preceding claims, wherein said first doped region is a n-doped region, and wherein said second doped region is a p-doped region.

14. A one time programmable anti-fuse element comprising:

a poly diode disposed above a STI region of a semiconductor substrate, wherein said poly diode does not use amorphous silicon;

a metallic layer coupled to a first doped region and a second doped region of said poly diode, wherein a first electrically conducting path is created between said metallic layer and said first doped region, and wherein a second electrically conducting path is created between said metallic layer and said second doped region; and

an IMO disposed between said poly diode and said metallic layer.

15. The one time programmable anti-fuse element of Claim 14, wherein said poly diode, said metallic layer and said IMO are adapted to be formed concurrently with the process flow for forming a standard semiconductor device while not perturbing the process flow.

16. The one time programmable anti-fuse element of Claim 14 or 15, wherein said first doped region of said poly diode couples to said metallic layer through a first silicide contact and a first tungsten plug to form said first electrically conducting path between said first doped region and said metallic layer, and wherein said second doped region of said poly diode couples to said metallic layer through a second silicide contact and a second tungsten plug to form said second electrically conducting path between said second doped region and said metallic layer.

17. The one time programmable anti-fuse element of any one of Claims 14 to 16, wherein a current is driven in a forward biased direction relative to said poly diode to program said one time programmable anti-fuse element, said current traveling from said metallic layer to said first doped region, continuing to said second doped region, and back to said metallic layer, thereby blowing said poly diode as said one time programmable

anti-fuse element to create a conducting path from said metallic layer to said first doped region, through said poly diode, and back to said metallic layer from said second doped region.

18. The one time programmable anti-fuse element of Claim 17, wherein damage of said blown poly diode is harder to detect when compared to a blown one time programmable anti-fuse element made from amorphous silicon.

19. The one time programmable anti-fuse element of any one of the Claims 14 to 18 wherein said first doped region is a n-doped region, and wherein said second doped region is a p-doped region.

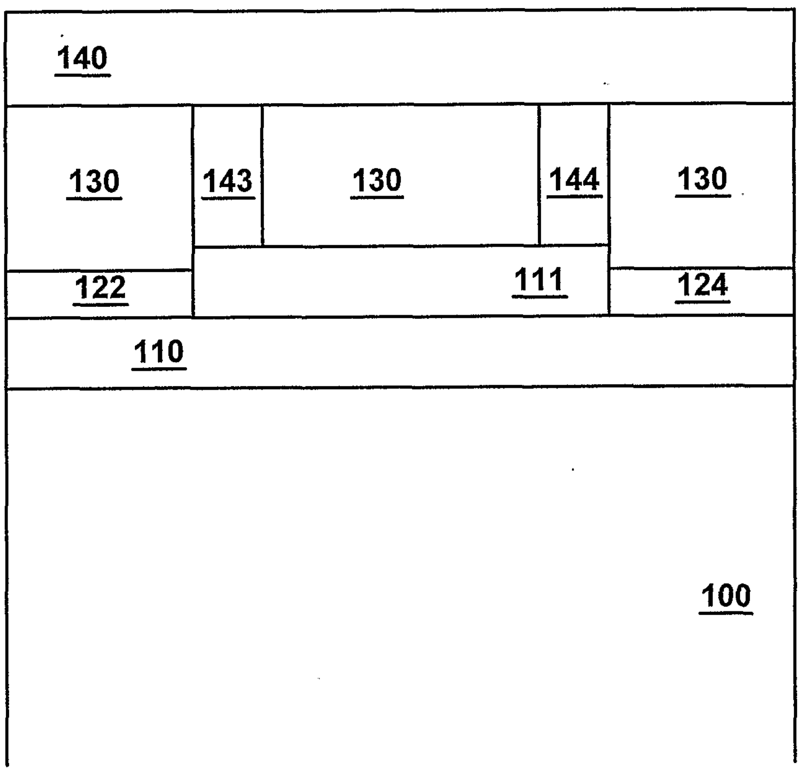


FIG. 1 (Prior Art)

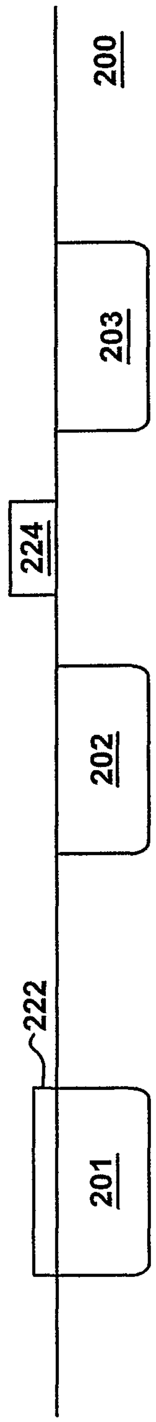


FIG. 2A

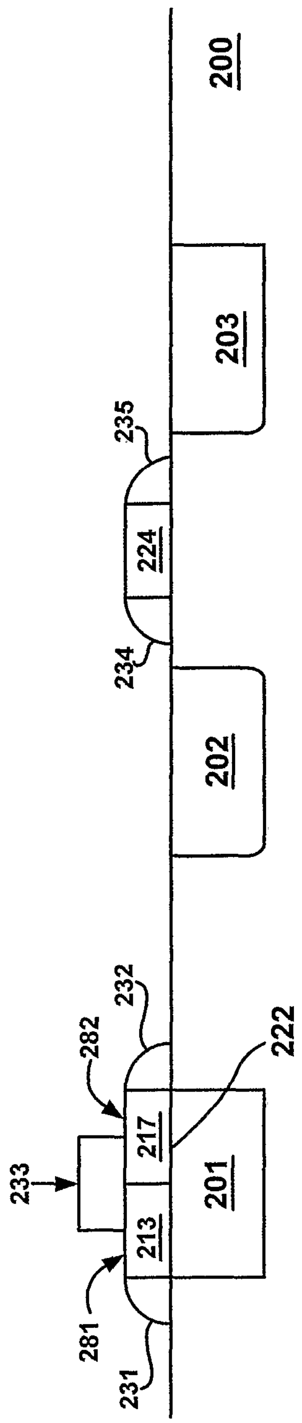


FIG. 2B

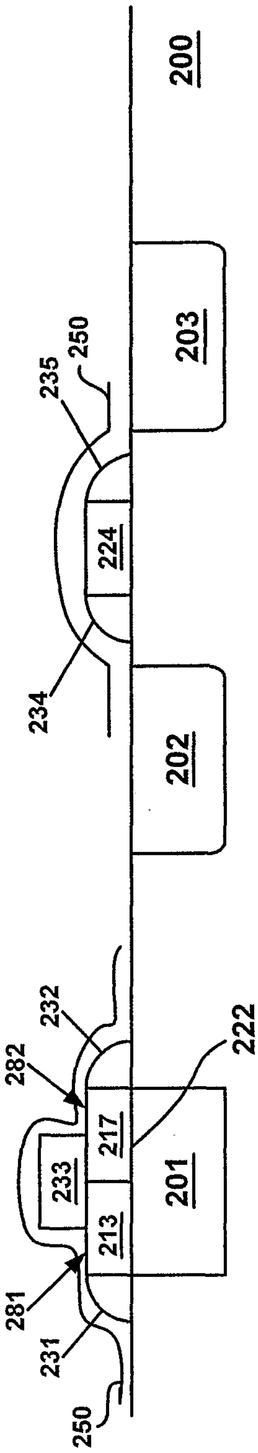

200
203
250
235
224
234
202
232
282
222
233
217
201
213
281
231
250

FIG. 2C

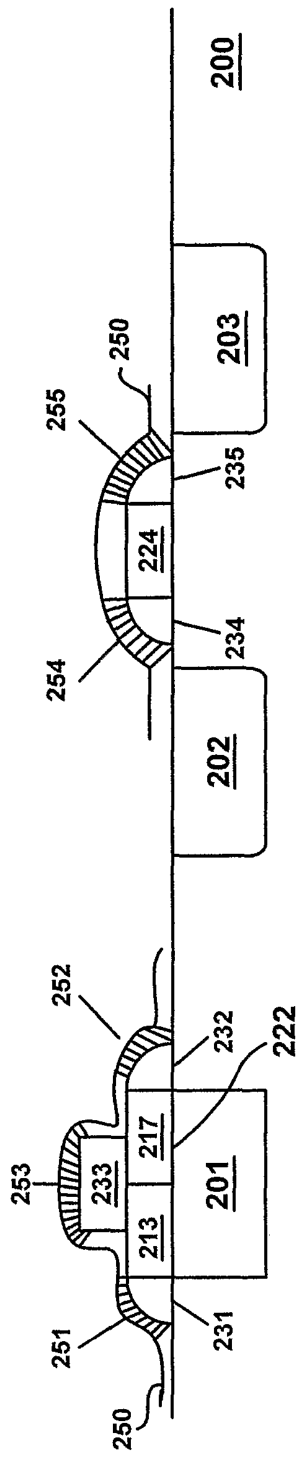

200
203
250
255
235
224
234
254
202
252
232
222
217
233
253
213
201
251
231
250

FIG. 2D

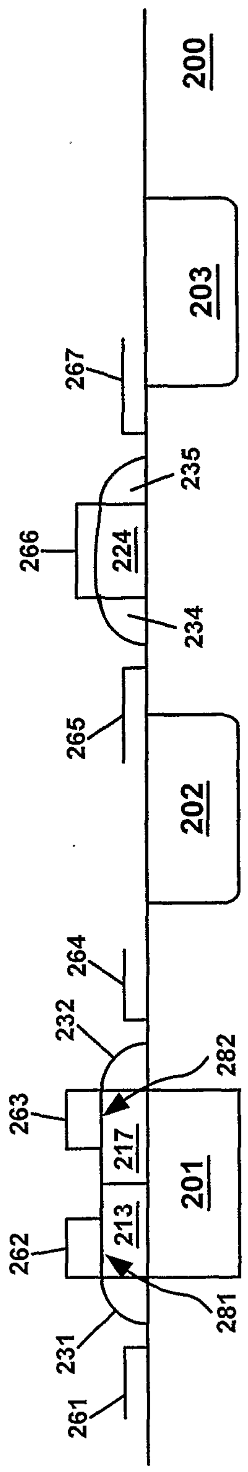

200
203
267
235
266
224
234
265
202
264
232
282
263
217
201
213
262
281
231
261

FIG. 2E

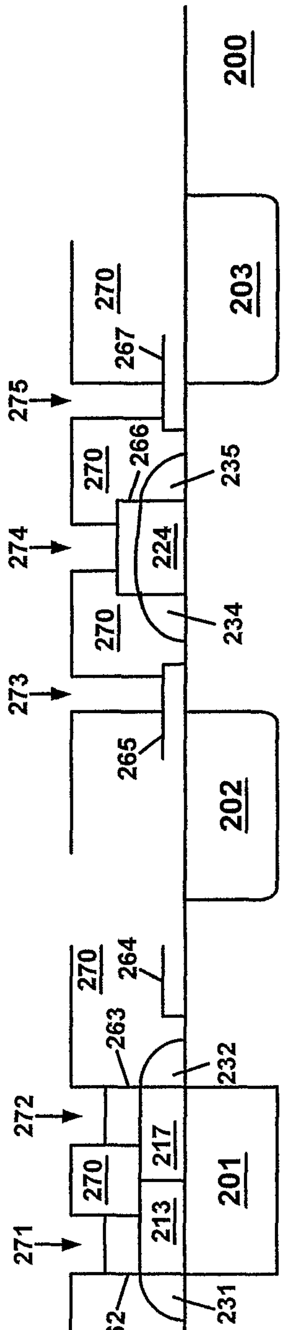

200
203
270
267
275
270
266
235
224
274
270
234
273
265
202
270
264
263
232
272
270
217
201
271
213
231
262
270
261

FIG. 2F

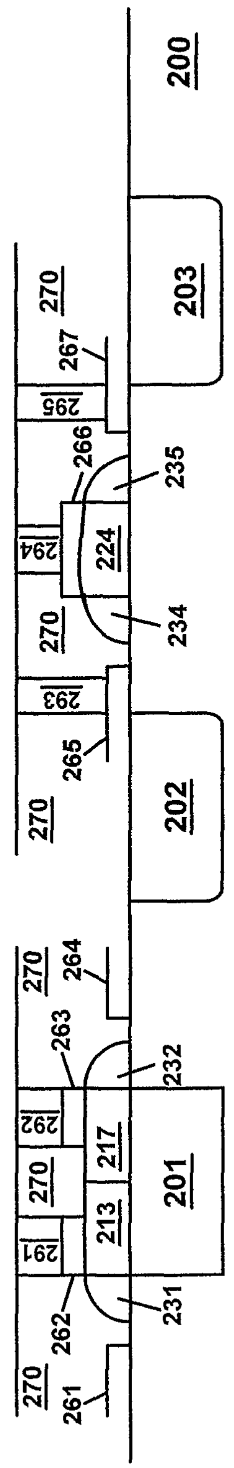

200
203
270
267
295
266
235
224
294
234
270
293
265
270
202
264
270
263
232
292
217
270
201
213
291
262
231
270
261

FIG. 2G

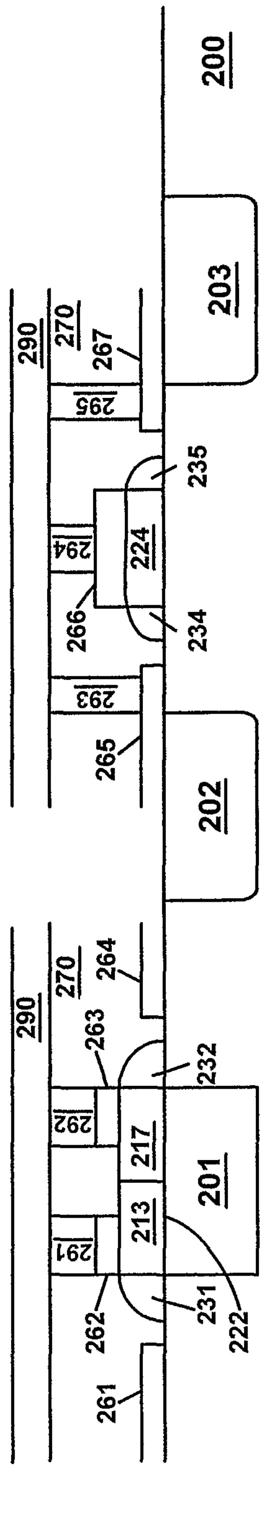

200
203
290
270
267
295
235
224
294
266
234
293
265
202
264
270
290
263
232
292
217
201
213
291
262
231
222
261

FIG. 2H

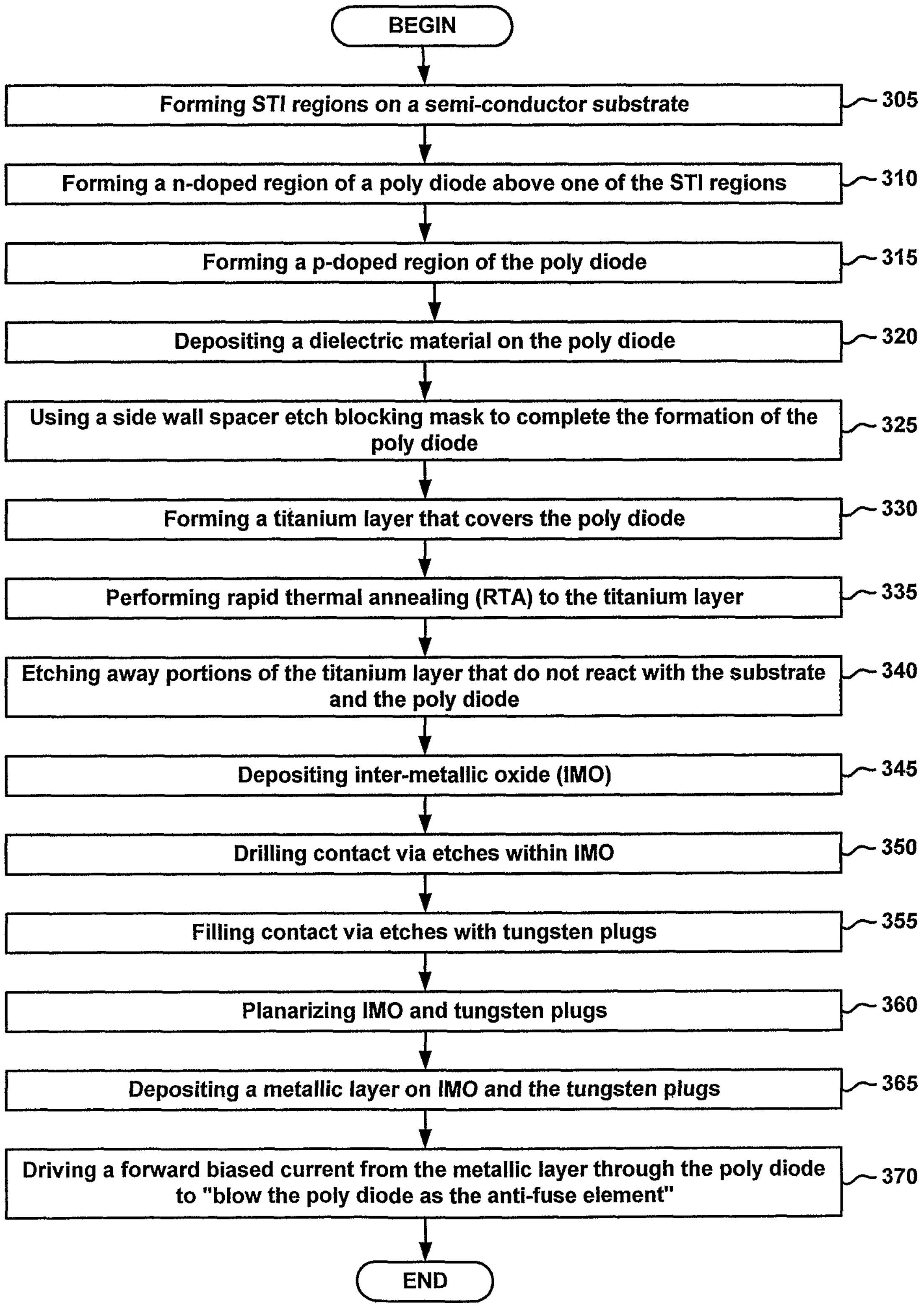

BEGIN
Forming STI regions on a semi-conductor substrate
305
Forming a n-doped region of a poly diode above one of the STI regions
310
Forming a p-doped region of the poly diode
315
Depositing a dielectric material on the poly diode
320
Using a side wall spacer etch blocking mask to complete the formation of the poly diode
325
Forming a titanium layer that covers the poly diode
330
Performing rapid thermal annealing (RTA) to the titanium layer
335
Etching away portions of the titanium layer that do not react with the substrate and the poly diode
340
Depositing inter-metallic oxide (IMO)
345
Drilling contact via etches within IMO
350
Filling contact via etches with tungsten plugs
355
Planarizing IMO and tungsten plugs
360
Depositing a metallic layer on IMO and the tungsten plugs
365
Driving a forward biased current from the metallic layer through the poly diode to "blow the poly diode as the anti-fuse element"
370
END

FIG. 3