

(12) PATENT
(19) AUSTRALIAN PATENT OFFICE

(11) Application No. AU 199648063 B2
(10) Patent No. 713906

(54) Title
Data clock recovery circuit

(51)⁶ International Patent Classification(s)
H04L 007/033

(21) Application No: 199648063 (22) Application Date: 1996 .03 .13

(30) Priority Data

(31) Number	(32) Date	(33) Country
P9500648	1995 .03 .31	ES

(43) Publication Date : 1996 .10 .10
(43) Publication Journal Date : 1996 .10 .10
(44) Accepted Journal Date : 1999 .12 .16

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(56) Related Art
JP 56-035561
GB 2280555
JP 06-132818



AU9648063

(12) PATENT ABRIDGMENT (11) Document No. AU-B-48063/96
(19) AUSTRALIAN PATENT OFFICE (10) Acceptance No. 713906

- (54) Title
DATA CLOCK RECOVERY CIRCUIT
- International Patent Classification(s)
(51)⁶ **H04L 007/033**
- (21) Application No. : **48063/96** (22) Application Date : **13.03.96**
- (30) Priority Data
- | (31) Number | (32) Date | (33) Country |
|-----------------|-----------------|-----------------|
| P9500648 | 31.03.95 | ES SPAIN |
- (43) Publication Date : **10.10.96**
- (44) Publication Date of Accepted Application : **16.12.99**
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- (56) Prior Art Documents
JP 56-035561
GB 2280555
JP 06-132818
- (57) Claim

ABSTRACT

DATA CLOCK RECOVERY CIRCUIT

Based on a phase locked loop (PC1, CP1, VCXO) which receives an incoming data signal (DS) and generates a recovered clock signal (RC). In the event that this incoming data signal (DS) includes low frequency cycling, false phase locking can occur, consequently leading to impaired operation.

To avoid this, according to the invention, there is also included a false locking detector (FLD) to which is applied the incoming data signal (DS) and the recovered clock signal (RC) and the output of which, which is added in an adder circuit (ADD) to that coming from the first loop, produces voltage pulses when both signals are not at the same frequency, provoking a non-locked state. Only when the frequency is correct, does the false locking detector (FLD) not alter loop operation.

(Figure 4)



AUSTRALIA

Patents Act 1990

ORIGINAL
COMPLETE SPECIFICATION
STANDARD PATENT

Invention Title:

"DATA CLOCK RECOVERY CIRCUIT"

The following statement is a full description of
this invention, including the best method of
performing it known to us:-

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This invention relates to a clock recovery circuit for an NRZ type data signal, starting from the data signal itself and in particular to systems based on time
5 compression multiplexing, TCM, in which half of the frame is employed for transmitting data in one direction, from a ventral office to a number of network terminating equipments, while the other half is used to transmit data in the other direction, from the network terminating equipments to the central office.

The data signal received in the network terminating equipments, the clock of which it is intended to recover, is only active during one half of the frame.

10 In digital transmission communications systems, it is often necessary to regenerate the waveform of a data signal in order to ensure its integrity.

To do this, the data clock signal is recovered in some way and used to sample the data signal at the moment of least probability of error (in the centre of the data
15 cycle).

Frequently the recovery of the clock signal is done by means of a phase-locked loop or PLL circuit which, by comparing the incoming data signal with another
20 generated in a voltage-controlled oscillator, obtains an error signal that is applied to this voltage-controlled oscillator so that both signals maintain a constant phase relationship.

The difficulties in applying this technique depend on the nature of the data signals from which it is intended to recover the clock signal.

In the article "Monolithic chip retimes data at 622 Mb/s" by Benny Lai and Richard C. Walker, published in the review "Microwaves & RF" of March, 1992, on
25 pages 202 to 205, a clock recovery circuit of this type is shown, formed by a phase/frequency detector, a charge pump and a voltage-controlled oscillator with a nominal centre frequency of 622 Mb/s with a range of $\pm 10\%$.

The phase loop so formed permits data clock recovery and, consequently, regeneration of the incoming data signal using a local oscillator which has a nominal
30 frequency very close to that of the data clock signal.

However, when the data signal employs time compression multiplexing, TCM,

its spectrum includes, besides a tone whose frequency is equal to the clock frequency, tones which are above and below the actual clock frequency tone by an amount equal to the frame frequency.

In the case where the frame frequency is very low compared to the data clock frequency, these tones lie with within the locking range of the PLL, meaning that there is a possibility that the PLL in question
 5 erroneously locks in to one of them. This situation would be catastrophic for the receive and, therefore, for the communications system of which it forms part.

The present invention avoids the above situation and thereby permits the PLL of the clock recovery circuit to lock in only to the frequency corresponding to the received signal data clock.

According to a first aspect of the present invention there is provided a clock recovery circuit for an
 10 incoming data signal comprising a first phase locked loop and a second phase locked loop, said first phase locked loop including a first phase comparator, a first charge pump and a voltage controlled oscillator, and said second phase locked loop including said voltage controlled oscillator and a false
 15 locking detector, wherein the false locking detector is adapted to receive the incoming data signal and a signal derived from the output of the voltage controlled oscillator, and to produce an output signal for summation with an output signal of said first charge pump for control of the voltage controlled oscillator.

Preferably, the clock recovery circuit includes a first phase comparator, a first charge pump and a
 20 voltage-controlled oscillator forming a phase-locked loop, also has a false locking detector which receives the incoming data signal and a signal obtained from the voltage-controlled oscillator output signal, and which generates, in turn, a signal that is also applied to the voltage-controlled oscillator.

In this way, in the event of false locking occurring, the output signal of the false locking detector takes a
 25 value that is added to that produced in the first loop in order to shift the voltage-controlled oscillator frequency from the value at which it was locked to the PLL. If the latter is locked in to the correct value, the false locking detector produces no signal, and so the PLL remains locked in to the existing frequency.

Preferably the false locking detector includes a second phase comparator which feeds a second charge
 30 pump in such a way that the output signal of this second charge pump is added to that coming from the first charge pump in order to provide a signal for voltage-controlled oscillator. It is also preferable that the clock recovery circuit has discharge circuits which discharge, respectively, the capacitors of the first and second charge pumps when the output signal of the second charge pump reaches a determined value close to its saturation value.



It is also preferable that the second phase comparator operates in such a way that its output signal takes a non-zero level when the difference in times between the data transitions and the activating edges of the recovered clock signal exceed a determined value.

Thus, in accordance with a preferred embodiment of the invention, in the event of false locking of the clock recovery circuit to a frequency other than that of the data clock, an additional signal is produced by a false locking detector that acts to release the PLL that has been formed. Only when the latter is locked in to the correct frequency will the false locking detector generate no output signal, whereby the PLL remains locked into this frequency, avoiding in this way the circumstances that would produce incorrect operation of the system.

10 Additional features of the invention will now be explained in more detail by way of example with reference to the accompanying drawings, in which:

-figure 1 shows a clock recovery circuit based on a conventional PLL according to the state of the art,

-figure 2 shows the basic configuration of a charge pump,

15 -figure 3 shows a timing diagram of the data signal received by the clock recovery circuit and of the recovered clock signal,

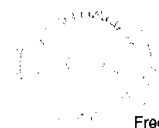
-figure 4 shows, in accordance with the invention, a clock recovery circuit with a PLL structure which includes a false locking detector,

20 -figure 5 shows a clock recovery circuit like that above to which has been added a level detector and discharging circuits for the capacitors of the charge pumps, and

-figure 6 shows the complete circuits of an implementation of the recovery circuit according to the invention.

Referring to the drawings, the implementation described below of a clock recovery circuit according to this invention is applied in an optical fibre digital communications system that employs time compression multiplexing, TCM, techniques, such that one half of the frame is used to transmit data from a central office to a number of network terminating equipments which the other half is used for sending data from the network terminating equipments to the central office.

25 The bit rate of the data signal, and consequently the frequency of the data clock, is 51.84 Mb/s. The master oscillator is located in the central office and therefore each network terminating equipment has a clock recovery circuit in order to



achieve perfect reception of the data transmitted by the central office, and to transmit its own data at the rate set by the same clock.

5 The transmission from the central office to the network terminating equipments, or downstream connection, lasts for 250 μ s per frame and has the same duration for the opposite direction, or upstream connection. This results in a frame frequency of 2 kHz.

10 The network terminating equipments only receive the part corresponding to the downstream connection, whereby this signal is equivalent to a continuous data signal multiplied by a 2 kHz square wave. In the spectrum of the resulting signal there appears a fundamental tone at 51.84 MHz and, close to this, two other tones at 51.842 MHz and 51.838 MHz, respectively, resulting from the first harmonic of the frame frequency. There also appear the components due to all the odd multiples of the 2 kHz square wave signal.

15 The clock recovery circuit, as mentioned above, is based on a phase-locked loop, or PLL, with a determined capture range which in this case is very small (around $\pm 0.01\%$), as the voltage-controlled oscillator included in it is of the crystal type or VCXO with a very high stability. For this reason, all signals higher than the third harmonic of the 2 kHz square wave lie outside the PLL locking range.

20 The fundamental PLL is that shown in figure 1; it is a digital PLL consisting of a voltage-controlled oscillator VCXO, a first phase comparator PC1 formed by digital logic gates, and a first charge pump CP1 that acts to filter the digital pulses produced by the first phase comparator PC1. The output from this charge pump CP1 is applied to the voltage-controlled oscillator VCXO the nominal centre frequency of which, with 25 2.5 V at its input, is 51.84 MHz, the admissible tolerance for the maximum and minimum input voltages, respectively, being $\pm 0.01\%$.

30 Figure 2 shows the conceptual diagram of a charge pump which is formed by a capacitor C that is charged or discharged with a current I1 or I2, respectively, depending on the state of the switches SW1 and SW2. This is equivalent to an integration or lowpass filtering of digital signals with determined levels.

Figure 4 shows the block diagram of the clock recovery circuit according to the invention, in which is added, with respect to figure 1, a false locking detector FLD

which receives the input data signal DS and the recovered clock signal RC and generates an output signal that is added to that coming from the first charge pump CP1, such that the sum signal, obtained in an adder circuit ADD, is applied to the voltage-controlled oscillator VCXO in order to alter its frequency of oscillation.

The operation of the false locking detector FLD is based on determining the difference in time between a transition of the incoming data signal and the closest activating edge of the recovered clock. Figure 3 shows, in the time domain, the incoming data signal DS and the recovered clock RC, considering the rising edge of the latter as the activating edge.

In this case, the activating edge of the clock reaches the false locking detector FLD with a delay T_e with respect to a transition of the incoming data signal DS. If the value of the difference in time T_e corresponds to a lag of more than T_2 or to a lead of more than T_1 , the false locking detector FLD would generate an output signal in the form of pulses; this is equivalent to considering the loop to be out of lock or in a false lock state. This signal generated by the false locking detector, the DC component of which is finally applied to the voltage-controlled oscillator VCXO, tends to shift the loop away from the frequency at which it had erroneously become locked.

In the opposite case, the false locking detector FLD does not generate any signal since it is considered to be locked in to the correct frequency, and consequently the loop can remain at this frequency.

The false locking detector FLD, as shown in figure 5, is formed in turn by a second phase comparator PC2 and a second charge pump CP2. The second phase comparator PC2, as was mentioned above, produces an output consisting of a series of pulses which it sends to the second charge pump CP2 which in this case has only charging current.

To prevent the PLL becoming blocked in the event of its not being correctly locked in and the second charge pump CP2 reaching its maximum value, a level detector LD is attached to its output, the function of which is to activate two discharging circuits DC1, DC2 which discharge the capacitors of the first and second charge pumps CP1, CP2. This permits resetting of the clock recovery circuit, which starts a new sweep in an attempt to lock in to the data clock.

Finally, figure 6 shows the detailed electric circuit diagram of the implementation made of the clock recovery circuit according to the invention.

5 The first phase comparator PC1, of a type that is very common in digital PLLs, receives the incoming data signal DS and the recovered clock signal RC and generates at its output two signals the high and low levels of which, respectively, have the same duration in the event that the signals applied to its input maintain a constant phase relationship. This first phase comparator PC1 requires the upright and inverted clock signals, for which reason the clock signal coming from the voltage-controlled
10 oscillator VCXO is applied to one of the inputs of two identical exclusive-OR gates, the other input being a logical "1" and "0", respectively.



The first charge pump CP1, gradually charges and discharges its capacitor, depending on the times for which the outputs of the first phase comparator PC1 remain high and low, respectively. In the event that the PLL is locked in, the charge mentioned remains constant.



The adder circuit ADD is formed by two different operational amplifiers in a conventional arrangement for summing signals.



20 The false locking detector FLD is formed, as shown in figure 6, by a second phase comparator PC2 consisting of three NAND gates and a D-type bistable, and by a second charge pump CP2 formed by a diode, a resistor and a capacitor. In the event of a positive-going transition of the incoming data signal DS arriving at a moment other than when the clock signal applied to its input has a low level, a pulse is generated that slightly increases the charge on the capacitor of the second charge pump CP2. The output signal from this second charge pump CP2 is applied to the
25 adder ADD. The increase in voltage that is applied to the voltage-controlled oscillator VCXO via the false locking detector FLD pulls the PLL out of its locked state, making it immediately seek a new frequency that satisfies the loop equations.

30 The clock recovery circuit also has, as already mentioned, the first and second discharge circuits DC1, DC2 which discharge the capacitors included in the first and second charge pumps CP1, CP2 when the output voltage of the second charge pump CP2 reaches a preset value of 2.5 V. In this way the loop is reset and recommences the locking process starting with the initial conditions. This is necessary because the

second charge pump CP2 only supplies current in one direction and cannot reduce its output voltage spontaneously,. Otherwise the loop would saturate and would never be able to lock in.

- 5 The level detector LD is formed by a differential amplifier which receives, at one of its inputs, the voltage produced by the second charge pump CP2 and, at the other, the 2.5V reference voltage. When the output voltage from this second charge pump CP2 attains this voltage, and in order to avoid the negative feedback produced through the second discharge circuit, the reference voltage is also reduced sharply
- 10 through a resistor and a transistor which comes into conduction between the resistor mentioned and ground. In this way a comparator with hysteresis is formed which avoids output signal switching when the input voltage applied to its non-inverting input is close to the reference voltage.



Claims

1. A clock recovery circuit for an incoming data signal comprising a first phase locked loop and a second phase locked loop, said first phase locked loop including a first phase comparator, a first charge pump and a voltage controlled oscillator, and said second phase locked loop including said
5 voltage controlled oscillator and a false locking detector, wherein the false locking detector is adapted to receive the incoming data signal and a signal derived from the output of the voltage controlled oscillator, and to produce an output signal for summation with an output signal of said first charge pump for control of the voltage controlled oscillator.

10
2. A clock recovery circuit as claimed in claim 1 wherein an output signal of said first charge pump is increased or decreased depending on output pulses from said first phase comparator.

15
3. A clock recovery circuit as claimed in claim 1 or 2 wherein the false locking detector further comprises a second phase comparator and a second charge pump, the second charge pump being adapted receive an input signal from said second phase comparator and to produce an output signal for summation with the output signal of said first charge pump for control of the voltage controlled oscillator.

20
4. A clock recovery circuit as claimed in claim 3 wherein the circuit includes a plurality of discharge circuits for discharging the capacitors of said first and second charge pumps, when the output signal of the second charge pump reaches a predetermined value.

25
5. A clock recovery circuit as claimed in claim 3 wherein the output signal of said second phase comparator adopts a high level when the difference in times between transitions of the data clock signal and the activating edges of the recovered data clock signal exceeds a determined value.

6. A clock recovery circuit substantially as hereinbefore described with reference to figures 2 to 6 of the accompanying drawings.

Dated this 18th day of October 1999

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Freehills Patent Attorneys

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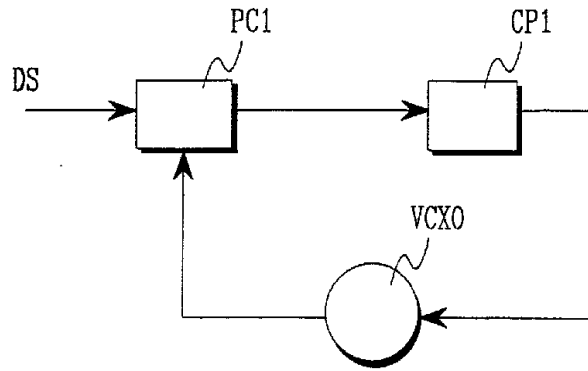


Fig. 1

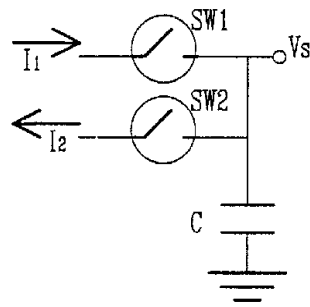


Fig. 2

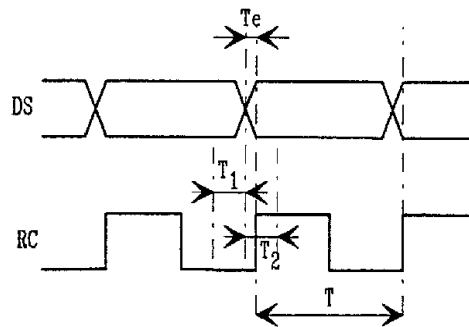


Fig. 3



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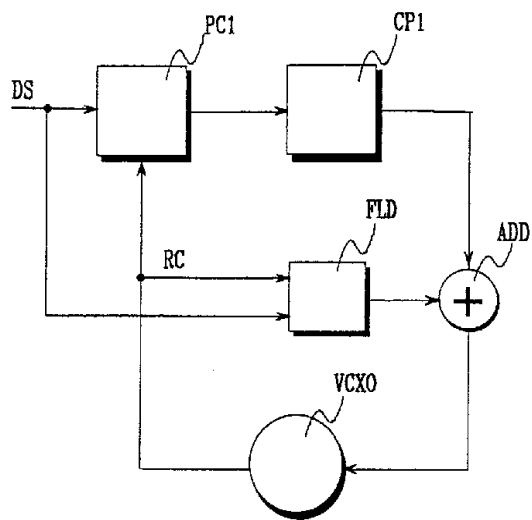


Fig. 4

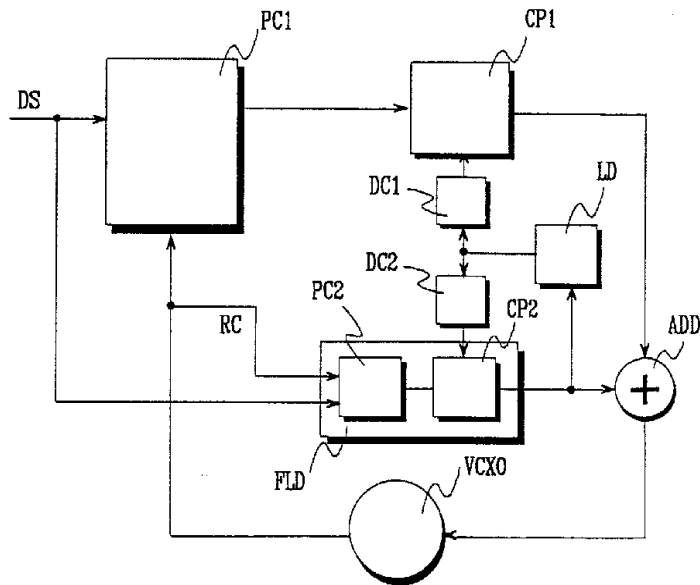


Fig. 5

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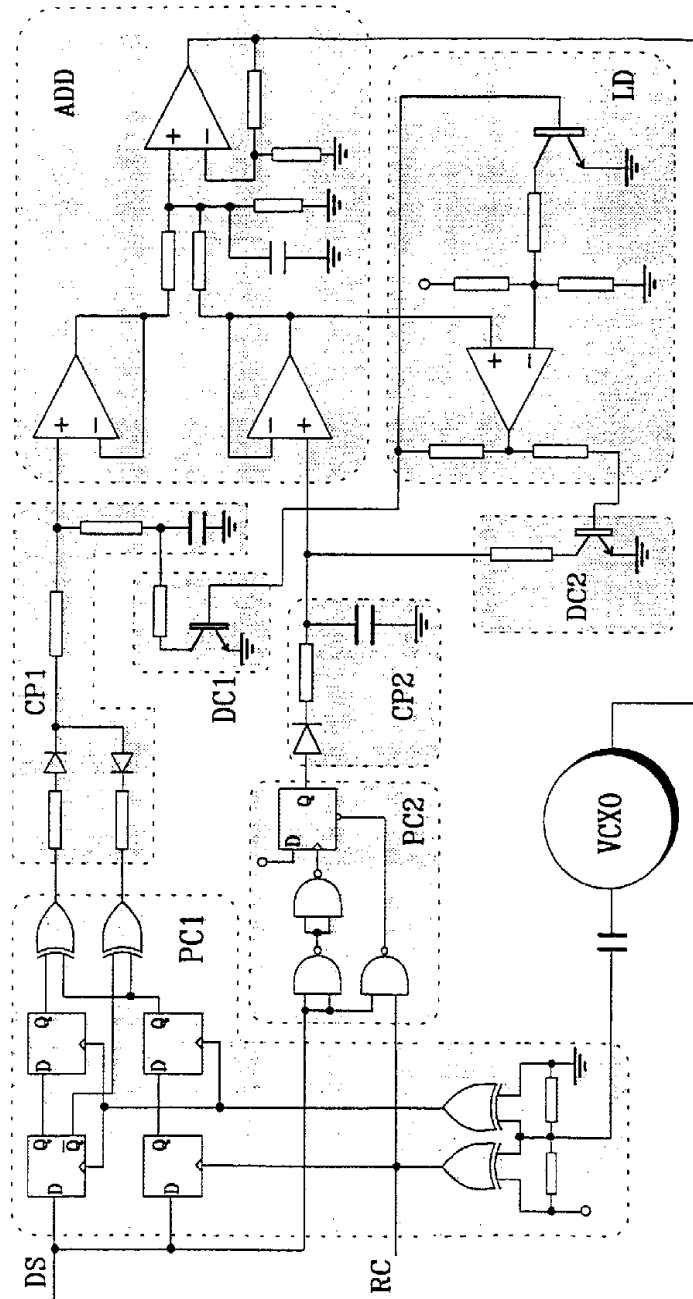


Fig. 6