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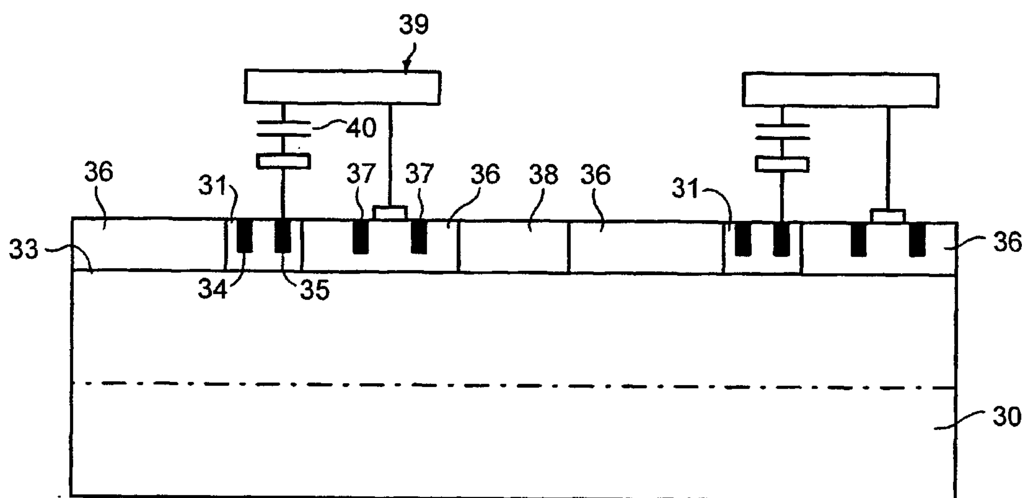
(54) Title: A MONOLITHIC SEMICONDUCTOR DETECTOR



(57) **Abstract:** A semiconductor radiation detector comprising a semiconductor substrate (30) on a front face of which are provided a first semiconductor well (31) and a second semiconductor well (36). The first well (31) forms a diode with the semiconductor substrate (30) and acts as a collector for collecting signals due to incident radiation. The second well (36) contains readout circuitry (37) that is connected to the collector (31), wherein a biasing contact (34) is provided for biasing the diode and the readout circuitry (37) is ac coupled to the collector (31).

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

A MONOLITHIC SEMICONDUCTOR DETECTOR

The present invention relates to a monolithic semiconductor detector. The invention further relates to a cryogenic semiconductor detector and a method of increasing the charge collection depth in such a detector.

Semiconductor detectors for detecting ionising particles and ionising radiation are currently used in a wide variety of applications, for example in high energy physics experiments, in the medical field for detecting X-rays and γ-rays, and in a number of industrial control processes. Such detectors are described in the book "Radiation Detection and Measurements" by G F Knoll, published by J Wiley & Sons.

One of the simplest known radiation detectors is shown in Figure 1. This comprises a p-n diode 10, which is created on a semiconductor substrate 11 between two contacts or terminals 12. Connected to the diode's terminals 12 are a dc bias circuit 13 for biasing the diode junction 14 and readout circuitry 15 for converting signals received at the terminals 12 into a format that is readable. Typically the readout circuitry includes an amplifier 16 and a meter 17.

In use, a voltage is applied to the terminals 12, so that the diode is reverse biased. This causes depletion of the semiconductor substrate 11. Ionising radiation that is incident on the depleted substrate 11 creates electron-hole pairs. Due to the electric field in the substrate 11, the electrons and holes so created are accelerated and travel through the substrate in opposite directions. This

causes charge to be induced on the terminals of the diode. The readout electronics 15 connected to the diode terminals 12 are then used to amplify the charge to transform it into an appropriate format for readout.

5 In some detectors of the type shown in Figure 1, the capacitance at the input of the first amplification stage of the readout circuitry is high. This is disadvantageous because it has a detrimental effect on the signal to noise ratio.

A further disadvantage of the detector of Figure 1 is that generally speaking the
10 semiconductor material that is used has to be of a high purity in order to obtain a sufficiently large collection depth. This means that the material has to contain few doping impurities and few impurities which create charge traps. A low doping level helps depletion of the substrate. Charge traps need to be minimized to prevent the charge created by the ionising radiation from being
15 trapped before it reaches the collection electrodes or the back side of the substrate. Typically very pure silicon is used, having, for example, an impurity density in the range of 10^{12} to 10^{13} cm^{-3}. For some applications, however, for example the detection of visible light, the ionising radiation does not penetrate far into the substrate and therefore lower purity material can be used. This is
20 because the required charge collection depth is not very high. Nevertheless, a limitation in the development of many radiation detectors is that to achieve a sufficient charge collection depth a high purity semiconductor must be used in the fabrication process. This excludes the possibility of fabricating detectors using commercial processes that are based on low purity materials.

25

Monolithic semiconductor detectors that have integrated detector electronics and readout electronics on the same piece of semiconductor have received much interest in the past few years. This is because monolithic devices, which use only one chip instead of two, are more robust, ultimately cheaper and thinner. In addition, the capacitance at the input of the first amplification stage of a monolithic detector is typically small. This is advantageous because it increases the signal to noise ratio and reduces the requirements on the readout circuitry. As with the detectors of Figure 1, however, in order to achieve sufficient charge collection depth monolithic detectors typically have to be made from a high purity semiconductor. This excludes the possibility of using standard commercial processes that are based on low purity materials.

Some successful results have, nevertheless, been obtained by fabricating monolithic detectors using a standard complementary metal oxide semiconductor (CMOS) process developed on a high purity substrate. CMOS is a well-known process that involves forming series combinations of n-type (NMOS) and p-type (PMOS) transistors on a semiconductor substrate. Digital static CMOS circuitry consumes no standing power because when such circuitry is in use, either an NMOS transistor or a PMOS transistor within the current path is off, thereby preventing static current flow.

Figure 2 shows a CMOS monolithic detector that was proposed by Sherwood Parker in the paper "A proposed VLSI Pixel Device for Particle Detection", Nucl. Instr. and Meth. A 275,494 (1989). This detector has an n-type substrate 20 on a front face of which are provided two n-type wells 21 on opposing sides of a p-type electrode 22. The p-type electrode 22 forms a diode with the n-type

substrate 20 and acts as a collector for collecting ionised charge due to incident radiation. A reverse bias on the p-type electrode 22 depletes the substrate 20. Contained in the n-type wells 21 is readout circuitry for converting signals due to charge collected in the p-type electrode 22 into a readable format, which readout circuitry is connected to the collection electrode 22.

The n-wells 21 of the device of Figure 2 act as Faraday cages for the readout circuitry so that transients in the circuitry cannot couple into the detecting element 22. The n-type wells 21 additionally provide an electric field that guides signal charge produced due to ionising radiation towards the p-type collection electrode 22. In order to fully deplete the substrate 20, however, and to divert the charge flow-lines into the collection electrode 22, a large potential difference is applied between the electrode 22 and the n-type wells 21 and the area of the collection electrode 22 must be relatively large. This is disadvantageous because the readout circuitry, which is connected to the collection electrode 22, is exposed to the large potential difference which may cause damage. In addition, the space available for accommodating such readout circuitry is limited.

In order to overcome the problems associated with the requirement for a high voltage in the well of the detector of Figure 2, another radiation detector that is fabricated using a CMOS process was developed. This is shown in Figure 3. In this case a p-n junction detecting element is formed by a homogenous N+ implant 23 on the backside of a p-type substrate 24. On the N+ implant 23 is provided a metal contact 25 that allows a bias voltage to be applied to the diode. On the front of the substrate 24 are provided collection electrodes 26 that are p-

type diffusion contacts. Adjacent to the p-type collection electrodes 26 are N-wells 27, which contain readout circuitry.

By applying a voltage to the contact 25 so as to reverse bias the junction, the substrate 24 can be depleted. Ionising radiation that is incident on the depleted substrate 24 creates electron-hole pairs. Due to the electric field in the substrate 24, the electrons and holes so created are accelerated and travel through the substrate 24 in opposite directions. This causes charge to be induced on the collection terminals 26. The readout electronics in the N wells 27 are then used to amplify the charge to transform it into an appropriate format for readout.

An advantage of the detector of Figure 3 is that the high field region of the diode is separated from the front circuit. In this way, the bias required on the wells 27 to divert the flow of charge from the rest of the circuit to the collection electrodes 26 is reduced. This allows low voltages and therefore a direct dc connection between the collection electrode 26 and the readout circuitry in the N-wells 27.

A disadvantage of the detector of Figure 3 is that the region between the junction on the back of the device and the collection electrodes 26 on the front needs to be fully depleted to avoid shorting all the collection electrodes 26 together. A further disadvantage of this structure is that if an n-well is used only PMOS transistors can be implemented for the readout circuitry local to each detecting element, although on the perimeter of the device, outside of the detecting area, CMOS circuitry could be used. A yet further disadvantage of this detector is that the substrate has to be patterned on both sides. This is

difficult to do in practice and so makes the fabrication process more complicated.

An object of the invention is to provide a monolithic semiconductor radiation detector that overcomes at least one of the afore-mentioned disadvantages of the prior art.

Another object of the invention is to provide a method of increasing the charge collection depth in a semiconductor radiation detector.

According to a first aspect of the present invention there is provided a semiconductor radiation detector comprising a semiconductor substrate on a front face of which are provided a first semiconductor well and a second semiconductor well, the first well forming a diode with the semiconductor substrate and acting as a collector for collecting signals due to incident radiation, and the second well containing readout circuitry that is connected to the collector, wherein a biasing contact is provided for biasing the diode and the readout circuitry is ac coupled to the collector.

An advantage of this detector is that in use the readout circuitry is isolated from the dc voltage that is applied to bias the detector. This allows use of a sufficiently high bias to attract the charge from underneath the second well to the collecting well, so that the charge which ends up on the second well is minimized. In this way the collection of charge is improved without applying

high voltage directly to the circuit in the second well, and radiation is detected even when it is incident in the region covered with the readout circuitry.

Preferably, the ac coupling is done by connecting the readout circuitry to the
5 collector using a capacitor. The capacitor may be formed by metal interconnects or between a diffusion and a metal interconnect.

The semiconductor substrate may by n-type or p-type. Where the substrate is n-type, the first well that forms the diode is a p-type well and the well that
10 contains the readout circuitry can be n-type or p-type. Where the substrate is p-type, the first well which forms the diode is n-type and the well that contains the readout circuitry can be p-type or n-type.

As will be appreciated, if the first and second wells are of the same type of
15 semiconductor material, they need to be isolated from each other. This is because they will be biased at very different potentials.

The first and second wells may be defined using a CMOS process.

20 The biasing contact may comprise a P+ implant when the first well is n-type or a N+ implant when the first well is p-type. The biasing contact may comprise PMOS transistors when the first well is n-type or NMOS transistors when the first well is p-type.

According to another aspect of the invention, there is provided a method of fabricating a radiation detector in which the first aspect of the invention is embodied, the method comprising using CMOS processing techniques.

5 According to a further aspect of the present invention, there is provided a radiation detecting system comprising a radiation detector as defined in the first aspect of the present invention and a cooling system for cooling the radiation detector.

10 Preferably, the cooling system is adapted to cool the detector to cryogenic temperatures.

An advantage of using CMOS processing techniques to fabricate the detector in this aspect of the invention is that CMOS devices can operate at low, cryogenic 15 temperatures so that no special processing techniques are required. In addition, the overall power consumption is relatively low, which means that the cooling system does not have to work as hard to maintain the desired temperature.

According to another aspect of the present invention there is provided a method 20 of increasing the charge collection depth in a semiconductor radiation detector, comprising cooling the semiconductor radiation detector.

An advantage of this method is that relatively low purity semiconductors can be used in the radiation detector when, previously, high purity material would have

been required. Where large areas of detectors are needed this can represent a substantial cost saving.

Preferably, the detector is cooled to a temperature in the range of 50K to 200K.

5

A method and detector in which the present invention are embodied will now be described by way of example only and with reference to the following drawings of which:

10 Figure 4 is a cross-section of a semiconductor device,

Figure 5 is a cross section through a test device,

Figure 6 shows a charge spectra for the device of Figure 5 taken at room temperature, and

Figure 7 shows charge spectrum for the device of Figure 5 taken at 77K

15 for various applied bias voltages.

The semiconductor device of Figure 4 is a CMOS device that comprises a p-type substrate 30 on a front face of which are a series of alternating N-wells and P-wells. Well 31 is an N-well that forms a diode with the p-type substrate 30

20 and acts as a collector for collecting charge generated in the substrate 30 due to ionising radiation. Located within the N-well 31 remote from the boundary 33 with the p-type substrate 30 is a heavily doped P+ implant 34 that is used as a high voltage biasing-electrode for biasing the diode. This implant 34 forms a diode with the N-well 31 which in turn forms a diode with substrate 30. In this

way, by applying a voltage to implant 34, the diode that is formed by the N-well 31 and the substrate 30 can be biased. The P+ implant 34 additionally acts as a sink for detector leakage current. Also provided in the N-well 31, but separately from the high voltage electrode 34, is a heavily doped N+ implant 35 that is used as a contact for measuring charge collected in the N-well 31.

On opposing sides of the N-well 31 are provided P-wells 36. The N+ implant 35 in the N-well is connected to readout circuitry 37 located in one of the P-wells 36. This circuitry is used for converting signals received at the N+ implants 35 into a format that is readable. Adjacent to each of the P-wells 36 and on the substrate 30 are further N-wells 38 that contain additional readout circuitry (not shown).

Connected between the contact 35 in well 31 and the readout circuitry 37 in well 36 is an ac coupling circuit 39 that comprises a capacitor 40. This can be implemented using the capacitance between metal interconnects or between a diffusion and a metal interconnect. This circuit acts as an isolation circuit between the well potential and the readout circuitry and allows charge collected at the contact 35 to be passed into the readout circuitry.

In use a high voltage is applied to the biasing electrode 34. This causes depletion in the diode that comprises the N-well 31 and the p-type substrate 30. The wells that contain the readout circuitry are in contrast biased using a low voltage in order to help prevent charge being collected in them.

In the presence of ionising radiation, electron hole pairs are created in the depleted substrate, which causes a flow of charge towards the N-well 31. In order to divert the flow of charge towards the collector 31 and away from the readout circuitry 37 in adjacent wells 36 and 38, it is necessary to ensure that
5 there is a sufficiently large difference between the potential applied to the N-well 31 and wells 36 and 38. In this way the loss of signal charge can be minimised. As mentioned previously, in the past this need to apply high voltages to the diode caused problems. However, because of the provision of the ac coupling circuit in the device of Figure 4, the readout circuitry 37 is
10 isolated from the high bias voltage and so damage to it is avoided.

Once charge is collected in the N-well 31, it is transferred through the contact 35 via the ac coupling circuit to the readout circuitry 37.

15 As an alternative to a P+ implant 34 in the N-well 31 to bias the N-well 31, it is possible that a circuit including PMOS transistors could be used. In this case, care needs to be taken to separate the part of the circuit biased near the high voltage from the rest of the circuit. In either case, care has to be taken to appropriately bias the wells containing the readout circuitry and the read-out
20 circuitry itself.

When either a P+ implant 34 or PMOS transistors are used in the detector of Figure 4, collection by N-wells other than the collection electrodes 31 should be minimised and punch through due to potential barrier lowering should be
25 avoided. In addition, breakdown should be avoided between the collection electrode 31 and the wells 36 and 38 that contain the readout circuitry 37. In

order to do this, for example, a guard ring structure could be used or a very gradual junction between the adjacent P-wells and the collection electrode could be formed.

5 Whilst a detector manufactured using a CMOS process has been described, it will be understood that the wells of the detector could contain other devices, such as, for example, bi-polar transistors.

The advantages of the device of Figure 4 can be improved by cooling it to 10 cryogenic temperatures of, for example, 77K. It has been found that this increases the charge collection depth of the device and so its overall sensitivity. This method of increasing the charge collection depth can of course be applied to any radiation detector. Figures 6 and 7, for example, show charge spectra taken from the radiation detector of Figure 5.

15

Figure 5 shows a radiation detector that comprises a diode formed by an n-type diffusion 41 on a p-type substrate 43 in a commercial CMOS process. The substrate 43 is of a low resistivity, for example, 1ohm cm and is covered with a p-type epitaxial layer 45 that is less doped than the substrate. The n-type 20 diffusion 41 creating the diode is that which is normally used for the N-well of the CMOS process. On the n-type diffusion is provided an electrode 47 for applying a biasing voltage to the diode. The diode area is of the order of 500 by 300 micrometres squared.

It has previously been thought that a low purity device such as that of Figure 5 would not be suitable for collecting charge created due to ionising radiation with a large penetration depth. Indeed, when this device was illuminated with electrons from a ^{90}Sr source at room temperature, no charge generated by the ionising radiation was detected. This can be seen from Figure 6, which shows a charge spectrum for the detector taken when the applied bias was 9.0V. This spectrum is merely the signal noise level. Charge due to ionising radiation with a large penetration depth was however detected when the sample was cooled to 77K.

Figure 7(a) shows various spectra that were collected at 77K when the detector of Figure 5 was illuminated with electrons from a ^{90}Sr source. Curve A is the spectrum for an applied voltage of 0V; curve B is the spectrum for 2.25V; curve C is the spectrum for 4.5V and curve D is the spectrum for 9.0V.

Curve A corresponds substantially to the measurement noise level, as would be expected. This curve remains the same when the electron source is removed. However, as the applied voltage bias is increased, the collected signal increases indicating an increase in the depth over which charge is collected. Plot D shows the greatest increase.

Figure 7(b) shows curve D together with a best-fit plot E for the pedestal noise and the best-fit Landau distribution F of the collected charge. The noise level does not allow the Landau peak in plot D to be seen, but using a suitable best-fit calculation the number of electrons was estimated to be about 8000, which corresponds to a vertical charge collection depth of 110μm. This means that

charge can be detected deep in the substrate of the detector, despite the use of relatively low purity material.

Cooling of a radiation detector in order to increase the charge collection depth
5 provides the possibility of producing detectors from relatively low purity material. Additionally, cooling makes it possible to integrate particle detectors and readout circuitry on a single substrate using a commercial FET process, for example a CMOS or JFET process.

10 A skilled person will appreciate that variations of the disclosed arrangements are possible without departing from the invention. Accordingly, the above description of a specific embodiment is made by way of example and not for the purposes of limitation. It will be clear to the skilled person that minor modifications can be made without significant changes to the operation
15 described above.

CLAIMS

1. A semiconductor radiation detector comprising a semiconductor substrate on a front face of which are provided a first semiconductor well and a second semiconductor well, the first well forming a diode with the semiconductor substrate and acting as a collector for collecting signals due to incident radiation, and the second well containing readout circuitry that is connected to the collector, wherein a biasing contact is provided for biasing the diode and the readout circuitry is ac coupled to the collector.

2. A detector as claimed in claim 1 wherein the ac coupling is done by connecting the readout circuitry to the collector using a capacitor.

3. A detector as claimed in claim 2, wherein the capacitor is formed by metal interconnects or between a diffusion and a metal interconnect.

4. A detector as claimed in any one of claims 1 to 3, wherein the semiconductor substrate is n-type or p-type.

5. A detector as claimed in claim 4 wherein, when the substrate is n-type, the first well that forms the diode is a p-type well and the well that contains the readout circuitry is n-type or p-type.

6. A detector as claimed in claim 4, wherein, when the substrate is p-type, the first well which forms the diode is n-type and the well that contains the readout circuitry is p-type or n-type.

7. A detector as claimed in any one of the preceding claims, wherein the first and second wells are defined using a CMOS process.

8. A detector as claimed in any one of the preceding claims, wherein the
5 first and second wells include bi-polar transistors.

9. A detector as claimed in any one of the preceding claims, wherein the first and second wells include field effect transistors.

10 10. A detector as claimed in any one of claims 1 to 4 or claim 6, wherein the biasing contact comprises a P+ implant when the first well is n-type.

11. A detector as claimed in claim 10, wherein the biasing contact comprises PMOS transistors.

15

12. A detector as claimed in any one of claims 1 to 5, wherein when the first well is p-type, the biasing contact comprises a N+ implant.

13. A detector as claimed in claim 12, wherein the biasing contact comprises
20 NMOS transistors.

14. A detector as claimed in any one of claims 1 to 7, wherein the biasing contact is a Schottky diode.

25 15. A method of fabricating a radiation detector as claimed in any one of claims 1 to 14, the method comprising using CMOS processing techniques.

16. A method of fabricating a radiation detector as claimed in any one of claims 1 to 14, the method comprising using FET processing techniques.

17. A method of fabricating a radiation detector as claimed in any one of claims 1 to 14, the method comprising using bi-polar processing techniques.

18. A radiation detecting system comprising a radiation detector as defined in any one of claims 1 to 14 and a cooling system for cooling the radiation detector.

19. A radiation detecting system as claimed in claim 16, wherein the cooling system is adapted to cool the detector to cryogenic temperatures.

20. A method of increasing the charge collection depth in a semiconductor radiation detector, comprising cooling the semiconductor radiation detector.

21. A method as claimed in claim 20, wherein the detector is cooled to a temperature in the range of 1.2K to 250K.

22. A method as claimed in claim 21, wherein the detector is cooled to a temperature in the range of 50K to 200K.

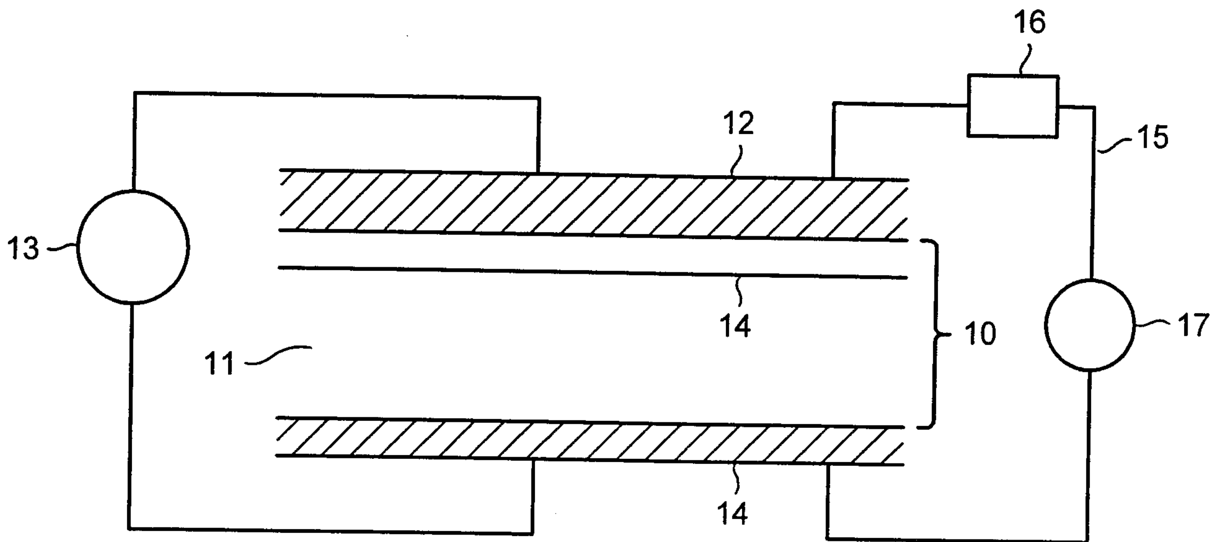

FIG. 1

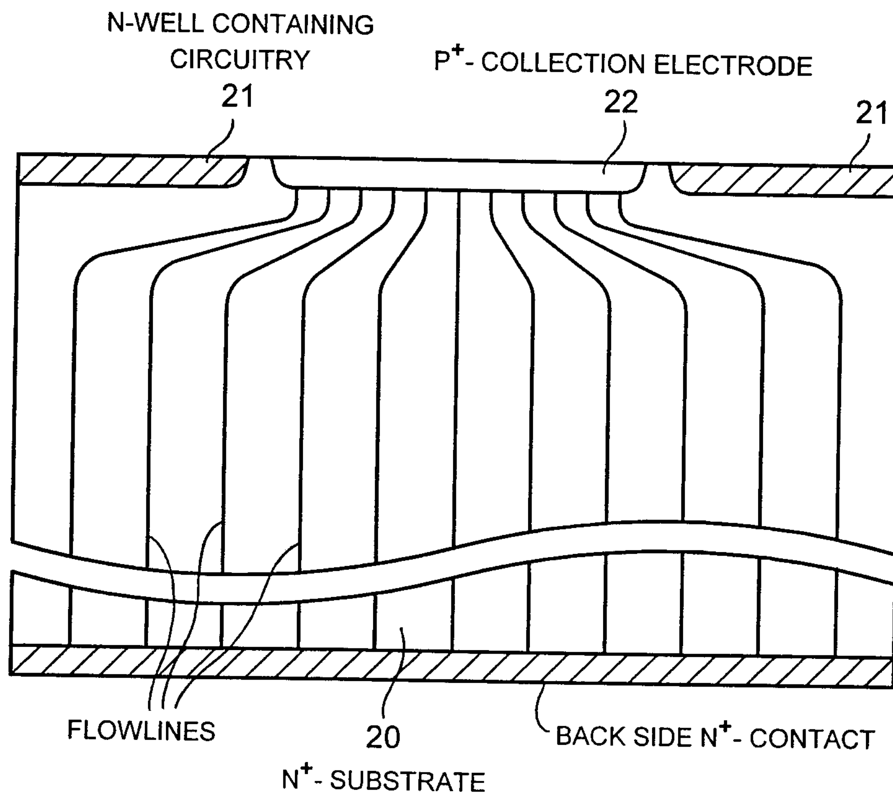

FIG. 2

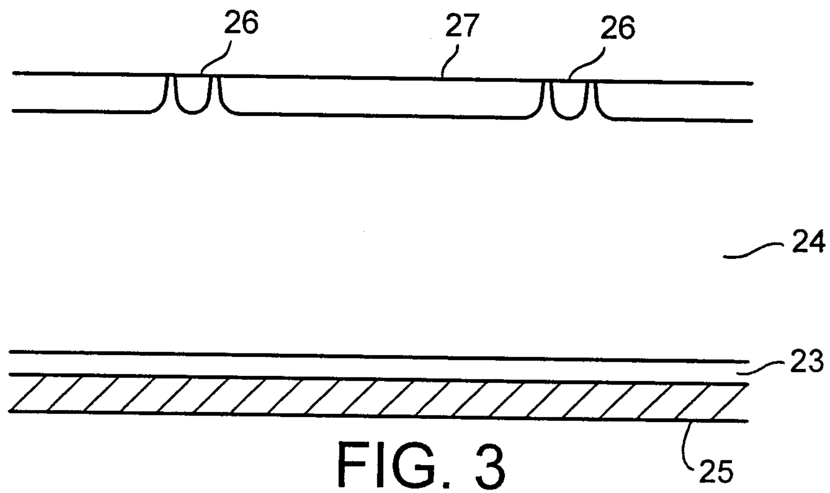

FIG. 3

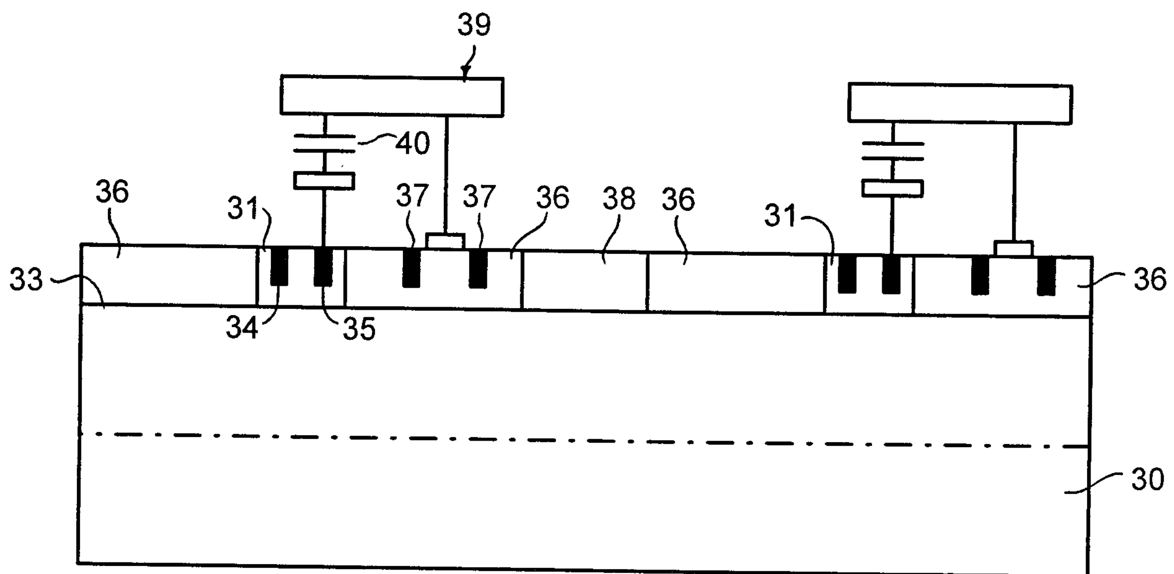

FIG. 4

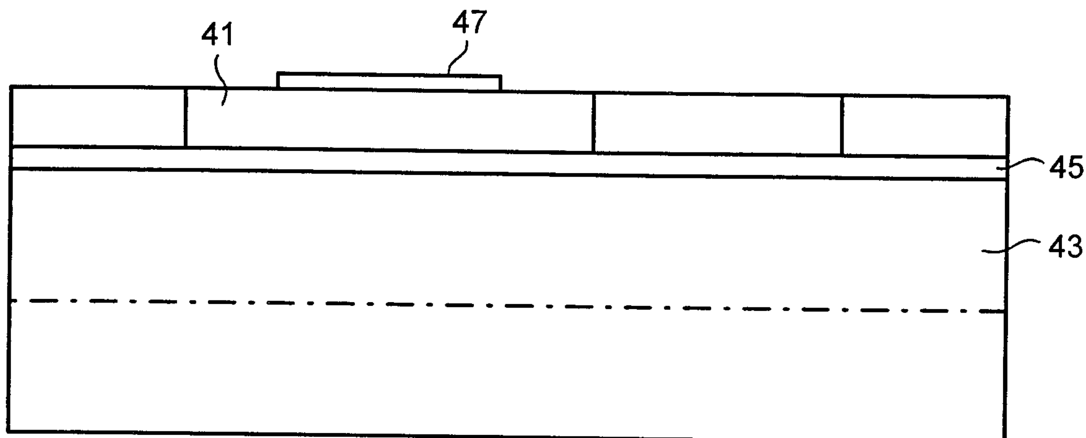

FIG. 5

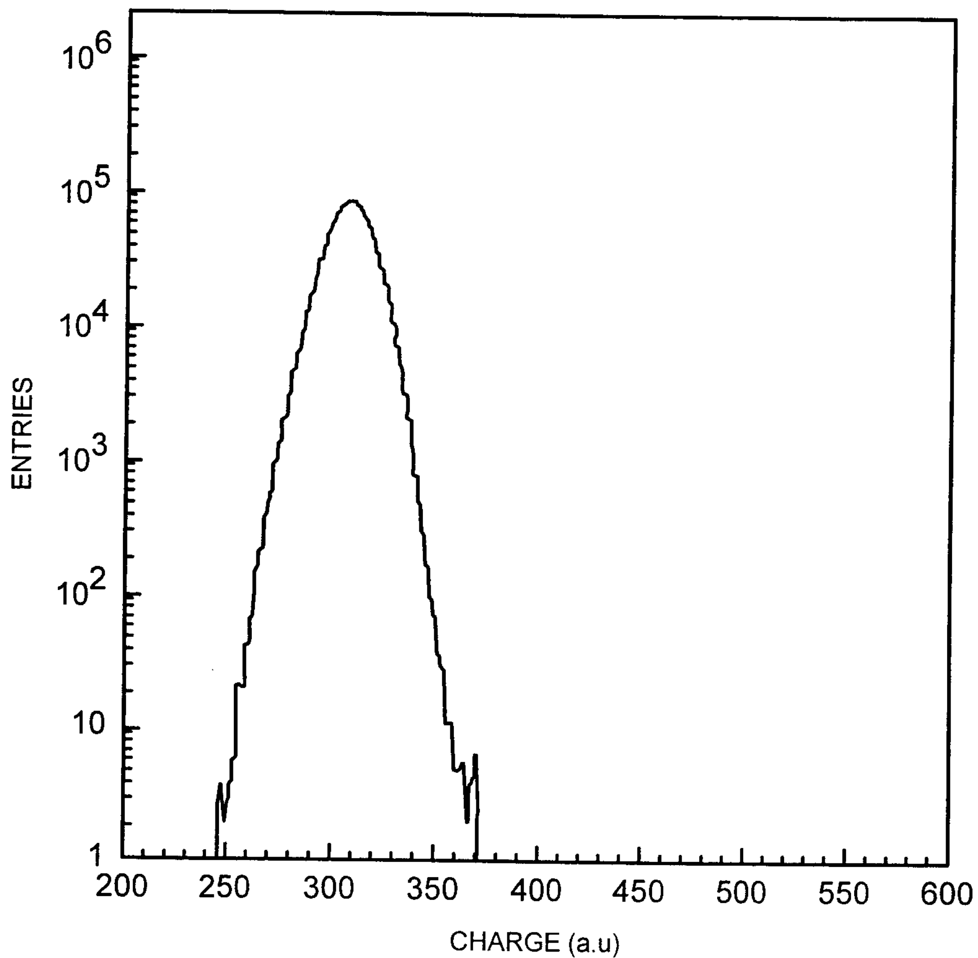

FIG. 6

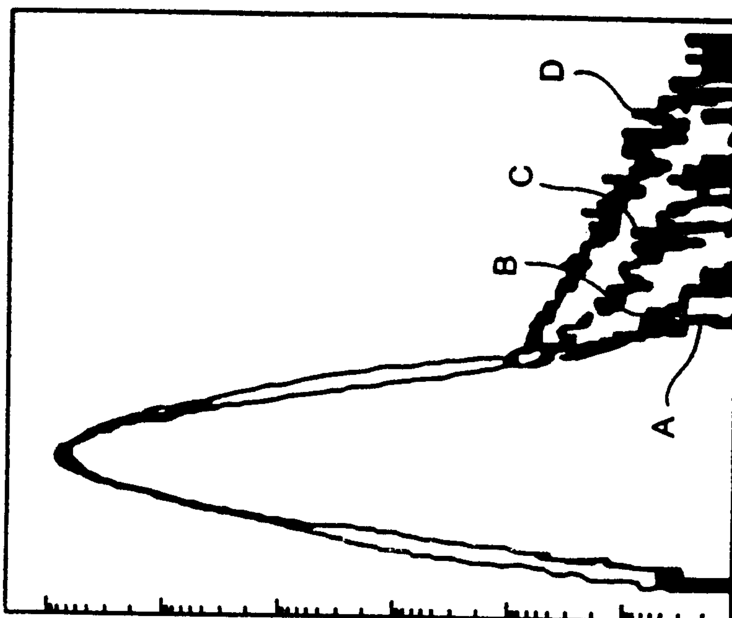

Figure 7(a)

CHARGE (a.u.)

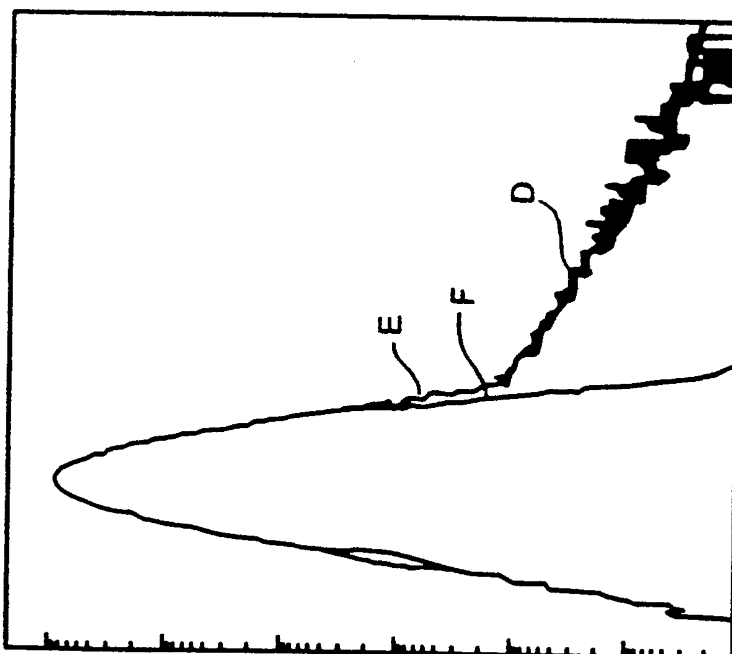

Figure 7(b)

ENTRIES

INTERNATIONAL SEARCH REPORT

International Application No
PCT/IB 00/00958

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L31/115 H01L27/144 G01T1/24

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L G01T

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

WPI Data, EPO-Internal, INSPEC, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	S. PARKER: "A proposed VLSI pixel device for particle detection" NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH, SECTION - A: ACCELERATORS, SPECTROMETERS, DETECTORS AND ASSOCIATED EQUIPMENT,NL,NORTH-HOLLAND PUBLISHING COMPANY. AMSTERDAM, vol. A275, no. 3, 1 March 1989 (1989-03-01), pages 494-516, XP002151764 cited in the application page 494-495 page 499 -page 502 ---	1-5,7,9, 15,16

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Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search	Date of mailing of the international search report
13 November 2000	20/11/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Visentin, A

2

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
Y	KEMMER J ET AL: "CONCEPTS FOR SIMPLIFICATION OF STRIP DETECTOR DESIGN AND PRODUCTION" NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH, SECTION - A: ACCELERATORS, SPECTROMETERS, DETECTORS AND ASSOCIATED EQUIPMENT,NL,NORTH-HOLLAND PUBLISHING COMPANY. AMSTERDAM, vol. A326, no. 1 / 02, 1 March 1993 (1993-03-01), pages 209-213, XP000367565 ISSN: 0168-9002 the whole document ---	1-5,7,9, 15,16
A	HUBBELING L ET AL: "MEASUREMENT OF SPATIAL RESOLUTION OF A DOUBLE-SIDED AC-COUPLED MICROSTRIP DETECTOR" NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH, SECTION - A: ACCELERATORS, SPECTROMETERS, DETECTORS AND ASSOCIATED EQUIPMENT,NL,NORTH-HOLLAND PUBLISHING COMPANY. AMSTERDAM, vol. A310, no. 1 / 02, 1 December 1991 (1991-12-01), pages 197-202, XP000274752 ISSN: 0168-9002 page 197 -page 198 ---	1,2,4
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A	ALLPORT P P ET AL: "FOXFET BIASSED MICROSTRIP DETECTORS" NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH, SECTION - A: ACCELERATORS, SPECTROMETERS, DETECTORS AND ASSOCIATED EQUIPMENT,NL,NORTH-HOLLAND PUBLISHING COMPANY. AMSTERDAM, vol. A310, no. 1 / 02, 1 December 1991 (1991-12-01), pages 155-159, XP000274747 ISSN: 0168-9002 the whole document ---	1,4,5,11
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