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ABSTRACT

**HETEROSTRUCTURE POWER TRANSISTOR WITH
AlSiN PASSIVATION LAYER**

5 A heterostructure semiconductor device includes a first active layer and a
second active layer disposed on the first active layer. A two-dimensional electron
gas layer is formed between the first and second active layers. An AlSiN passivation
layer is disposed on the second active layer. First and second ohmic contacts
electrically connect to the second active layer. The first and second ohmic contacts
10 are laterally spaced-apart, with a gate being disposed between the first and second
ohmic contacts.

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WE CLAIM:

1. A heterostructure power transistor comprising:

a first active layer;

5 a second active layer disposed on the first active layer, a two-dimensional electron gas layer forming between the first and second active layers;
a passivation layer comprising aluminum silicon nitride (AlSiN) disposed on the second active layer;

a gate;

10 first and second ohmic contacts that electrically connect to the second active layer, the first and second ohmic contacts being laterally spaced-apart, the gate being disposed between the first and second ohmic contacts.

2. The heterostructure power transistor of claim 1 further comprising a second
15 gate dielectric layer disposed on the passivation layer, the gate being disposed above the second gate dielectric layer.

3. The heterostructure power transistor of claim 2 wherein the second gate
20 dielectric layer comprises aluminum oxide (Al_2O_3).

4. The heterostructure power transistor of claim 2 further comprising an upper
passivation layer disposed over the second gate dielectric layer, the gate extending
vertically through the upper passivation layer to contact the second gate dielectric
layer.

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5. The heterostructure power transistor of claim 2 wherein the passivation layer has a first thickness and the second gate dielectric has a second thickness, the second thickness being larger than the first thickness.

5 6. The heterostructure power transistor of claim 2 wherein the first and second ohmic contacts extending vertically through the second gate dielectric layer and the passivation layer.

10 7. The heterostructure power transistor of claim 4 wherein the first and second ohmic contacts extending vertically through the upper passivation layer, the second gate dielectric layer, and the passivation layer.

8. The heterostructure power transistor of claim 1 wherein the passivation layer has a first thickness in a range of about 1-5 nanometers thick.

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9. The heterostructure power transistor of claim 2 wherein the second gate dielectric has a second thickness in a range of about 10-20 nanometers thick.

20 10. The heterostructure power transistor of claim 1 wherein the first and second ohmic contacts respectively comprise source and drain ohmic contacts.

11. The heterostructure power transistor of claim 4 wherein the upper passivation layer comprises SiN.

25 12. The heterostructure power transistor according to claim 1 wherein the first active layer comprises gallium nitride (GaN).

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13. The heterostructure power transistor of claim 1 wherein the second active layer comprises aluminum gallium nitride (AlGaN).

5 14. The heterostructure power transistor of claim 1 wherein the first and second active layers are defined as an isolated mesa.

15. The heterostructure power transistor of claim 1 wherein the gate comprises a nickel gold (NiAu) alloy.

10 16. The heterostructure power transistor of claim 10 wherein the gate includes a gate field plate that extends toward the drain ohmic contact.

17. The heterostructure semiconductor device of claim 1 wherein the gate
15 comprises a titanium gold (TiAu) alloy or a molybdenum gold MoAu alloy.

18. A method of fabricating a heterostructure semiconductor device comprising:
forming a first active layer on a substrate;

forming a second active layer on the first active layer, the first active layer and
20 the second active layer having different bandgaps such that a two-dimensional electron gas layer is formed therebetween;

forming a passivation layer comprising aluminum silicon nitride (AlSiN) on the second active layer, the passivation layer having a first thickness;

forming first and second ohmic contacts that each extend vertically through
25 the passivation layer, the first and second ohmic contacts being laterally spaced-apart and electrically connected to the second active layer; and

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forming a gate at a lateral position between the first and second ohmic contacts.

19. The method of claim 19 further comprising depositing a second gate
5 dielectric layer over the passivation layer, the second gate dielectric layer having a second thickness greater than the first thickness.

20. The method of claim 19 further comprising depositing an upper passivation
10 layer over the second gate dielectric layer.

21. The method of claim 19 further comprising annealing the second gate
dielectric layer.

22. The method of claim 19 wherein the second gate dielectric layer comprises
15 aluminum oxide.

23. The method of claim 18 wherein the first active layer comprises gallium
nitride.

20 24. The method of claim 18 wherein the second active layer comprises
aluminum gallium nitride.

25 25. The method of claim 18 wherein the passivation layer is formed in-situ with
the first and second active layers.

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26. The method of claim 18 further comprising growing, in-situ with the passivation layer, an AlN layer over the passivation layer.

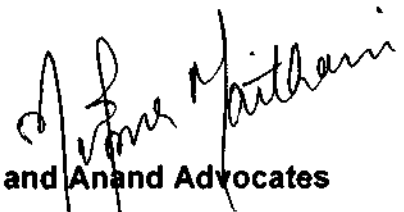
27. The method of claim 18 wherein the first thickness is in a range of about 1-5 nanometers thick.

28. The method of claim 19 wherein the second thickness is in a range of about 10-20 nanometers thick.

29. A heterostructure power transistor, substantially as herein described with reference to accompanying drawings and examples.

30. A method of fabricating a heterostructure semiconductor device, substantially as herein described with reference to accompanying drawings and examples.

Dated this 11th day of February 2014



Of Anand and Anand Advocates

Agent for the Applicant

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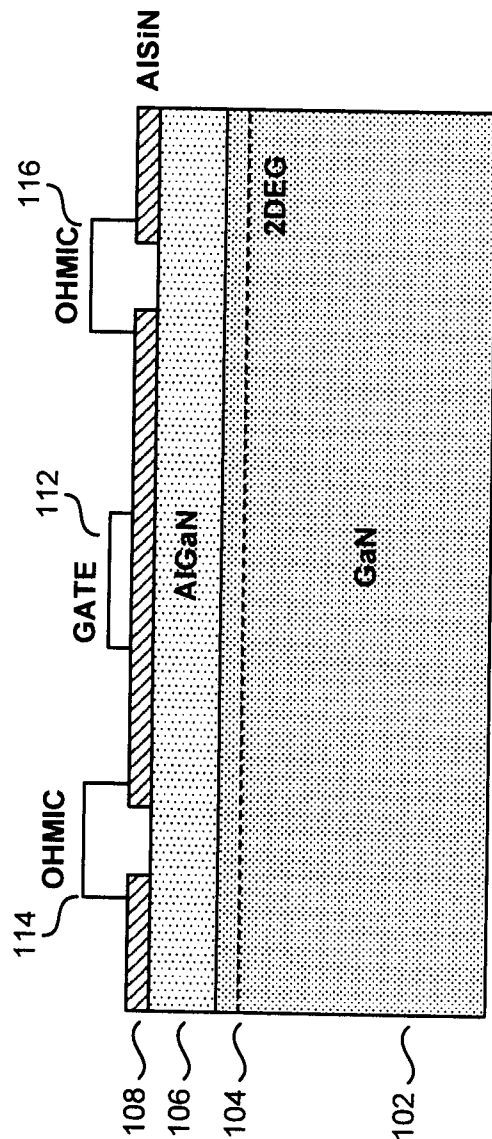


FIG. 1

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Archana Shanker
of Anand and Anand Advocates
Agent for the Applicant

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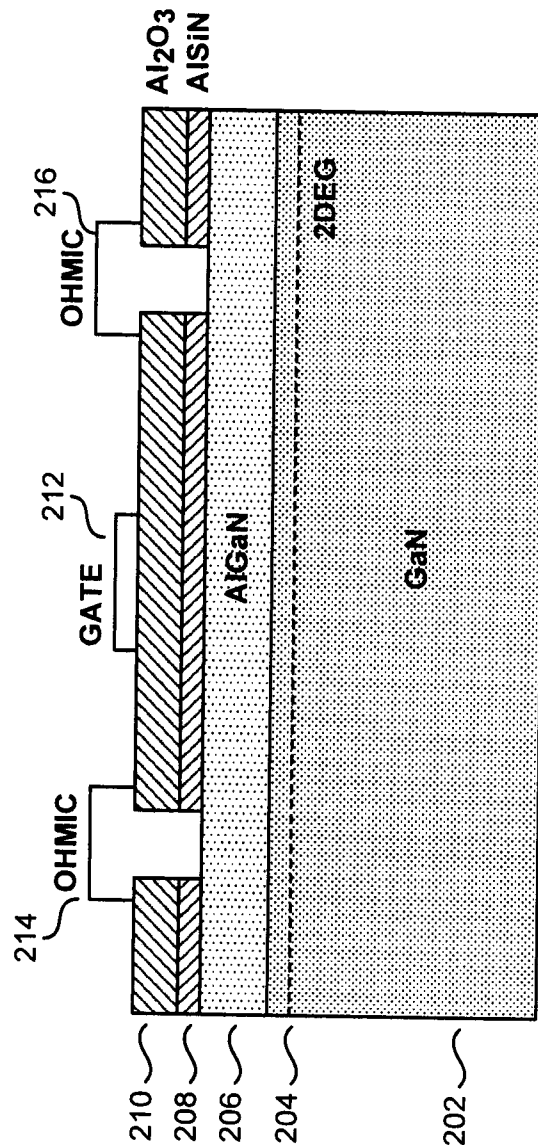


FIG. 2

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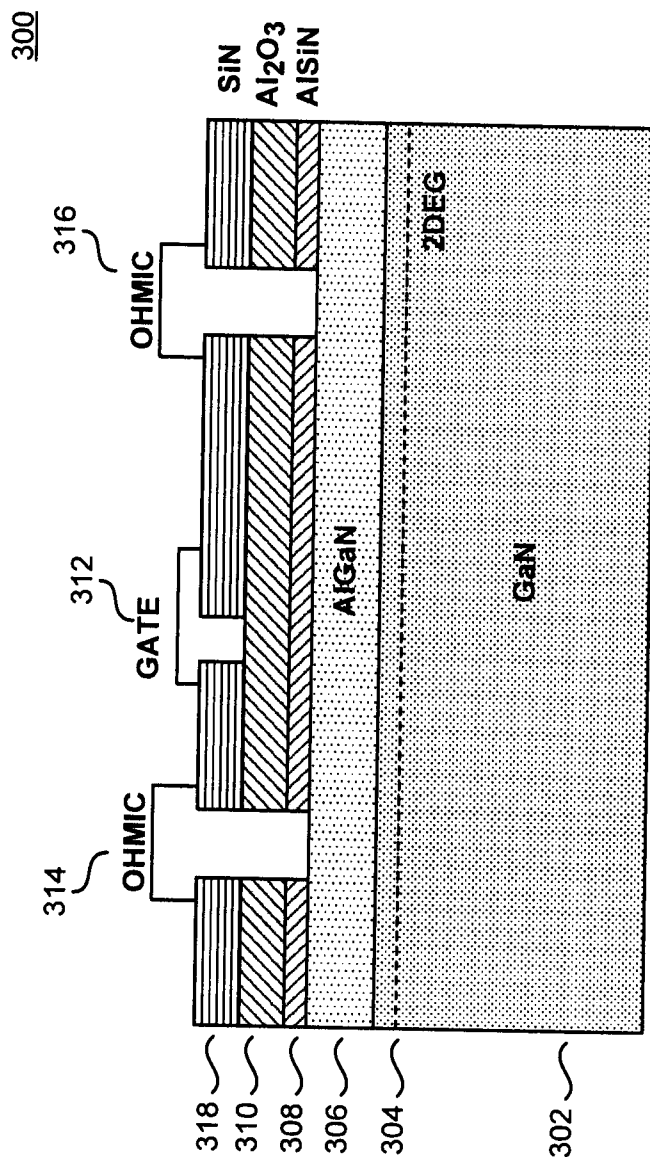


FIG. 3

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Archana Shanker
of Anand and Anand Advocates
Agent for the Applicant

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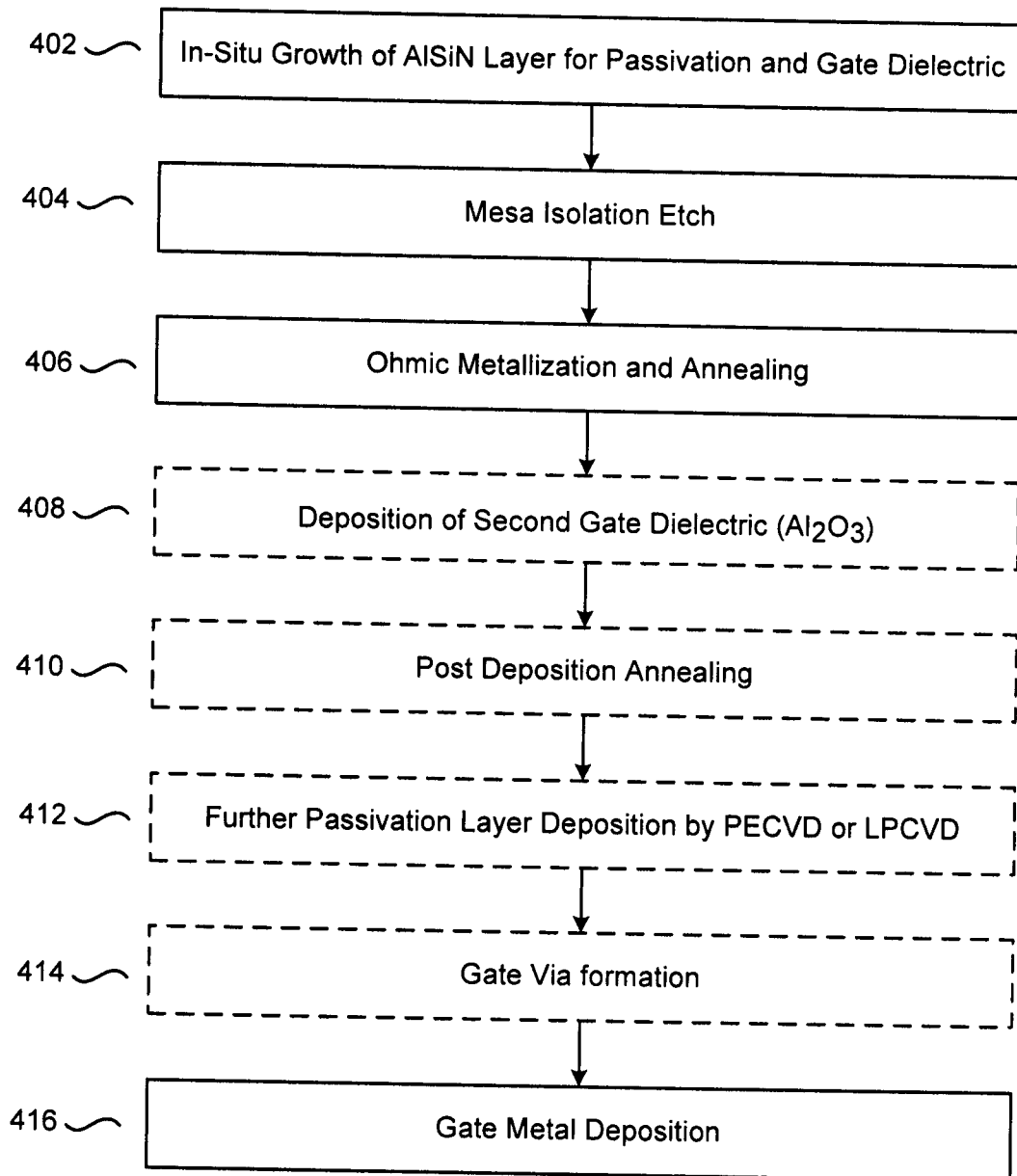


FIG. 4

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Archana Shanker
of Anand and Anand Advocates
Agent for the Applicant

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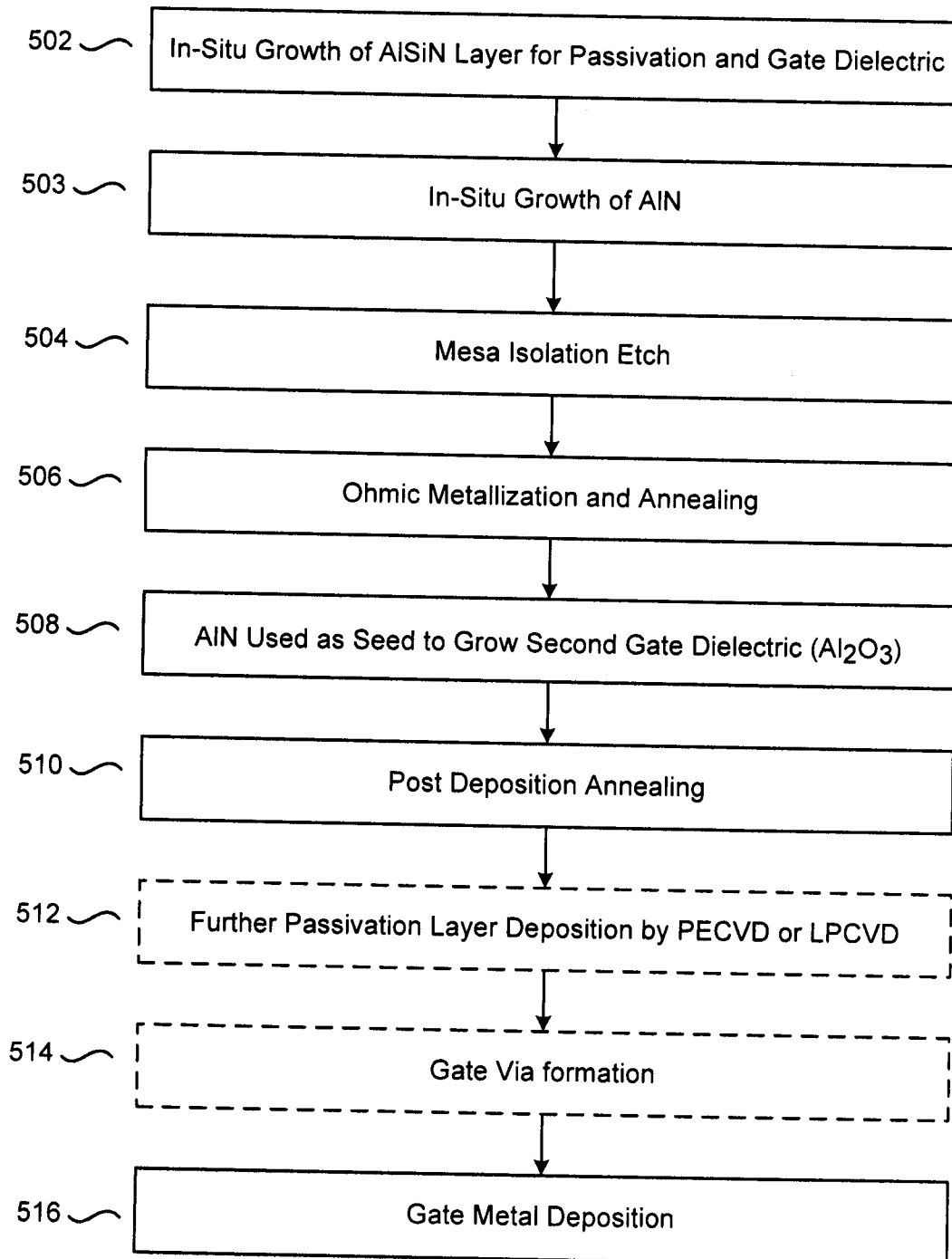


FIG. 5

Shanker

Archana Shanker
of Anand and Anand Advocates
Agent for the Applicant

HETEROSTRUCTURE POWER TRANSISTOR WITH AISIN PASSIVATION LAYER

5 TECHNICAL FIELD

[0001] The present invention relates generally to high-voltage field effect transistors (FETs); more specifically, to high-electron-mobility transistors (HEMTs) and heterostructure field-effect transistors (HFETs), and to methods of fabricating such power transistor devices.

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BACKGROUND

[0002] One type of high-voltage FET is a heterostructure FET (HFET), also referred to as a heterojunction or high-electron mobility transistor (HEMT). HFETs based on gallium nitride (GaN) and other wide bandgap III-IV direct transitional semiconductor materials, such as silicon carbide (SiC), are advantageously utilized in certain electronic devices due to their superior physical properties over silicon-based devices. For example, GaN and AlGaN/GaN transistors are commonly used in high-speed switching and high-power applications (e.g., power switches and power converters) due to the high electron mobility, high breakdown voltage, and high saturation electron velocity characteristics offered by GaN-based materials and device structures. Due to the HFETs physical properties, HFETs may change states substantially faster than other semiconductor switches that conduct the same currents at the same voltages and the wide bandgap may improve performance of the HFET at elevated temperatures.

20

25 [0003] GaN-based HFETs devices are typically fabricated by epitaxial growth on substrate semiconductor materials such as silicon, sapphire and silicon carbide formed into a thin disk or wafer. The fabrication steps for forming electronic devices (e.g., transistors) directly in the semiconductor material are frequently referred to as front-end-of-line (FEOL) processing. During FEOL processing of an HFET, the

wafer may be moved from various machines to build the various material layers of the device structure. But because GaN is a piezoelectric material, GaN-based HFET devices are susceptible to charge build-up (positive or negative) during FEOL processing. For example, charge build-up may result from the passivation process which involves deposition or growth of dielectric layers on the surface of a semiconductor. Passivation may be utilized to provide electrical stability by isolating the surface of the wafer from electrical and chemical conditions in the environment. For instance, exposure to air during fabrication of the HFET can cause surface reactions such as oxidation to occur which may impact the overall performance of the HFET device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Non-limiting and non-exhaustive embodiments of the present invention are described with reference to the following figures, wherein like reference numerals refer to like parts throughout the various views unless otherwise specified.

5 **[0005]** **FIG. 1** is a cross-sectional side view of an example semiconductor device having a passivation structure.

[0006] **FIG. 2** is a cross-sectional side view of an example semiconductor device having another passivation structure.

10 **[0007]** **FIG. 3** is a cross-sectional side view of an example semiconductor device having a further passivation structure.

[0008] **FIG. 4** is a flow diagram illustrating an example process flow for fabricating a semiconductor device structure.

[0009] **FIG. 5** is a flow diagram illustrating another example process flow for fabricating a semiconductor device structure.

15 **[0010]** Corresponding reference characters indicate corresponding components throughout the several views of the drawings. Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to
20 improve understanding of various embodiments of the present invention. Also, common but well-understood elements that are useful or necessary in a commercially feasible embodiment are often not depicted in order to facilitate a less obstructed view of these various embodiments of the present invention.

DETAILED DESCRIPTION

[0011] In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one having ordinary skill in the art that the specific detail need not be employed to practice the present invention. In other instances, well-known materials or methods have not been described in detail in order to avoid obscuring the present invention.

[0012] Reference throughout this specification to "one embodiment", "an embodiment", "one example" or "an example" means that a particular feature, structure or characteristic described in connection with the embodiment or example is included in at least one embodiment of the present invention. Thus, appearances of the phrases "in one embodiment", "in an embodiment", "one example" or "an example" in various places throughout this specification are not necessarily all referring to the same embodiment or example. Furthermore, the particular features, structures or characteristics may be combined in any suitable combinations and/or sub-combinations in one or more embodiments or examples. Particular features, structures or characteristics may be included in an integrated circuit, an electronic circuit, a combinational logic circuit, or other suitable components that provide the described functionality. In addition, it is appreciated that the figures provided herewith are for explanation purposes to persons ordinarily skilled in the art and that the drawings are not necessarily drawn to scale.

[0013] In the descriptions below, an example HFET is used for the purpose of explanation. However, it should be appreciated that embodiments of the present invention may be utilized with other types of FETs, such as a metal oxide

semiconductor FET (MOSFET) or metal insulator semiconductor FET (MISFET) devices.

[0014] As mentioned above, sheet charge may accumulate on the wafer of HFET devices during fabrication processing. To combat the effects of accumulated surface charge and to protect the HFET devices from other environmental conditions, one or more layers of dielectric material may be used as a passivation layer that protects the surface of the HFET.

[0015] In accordance with embodiments of the present invention, a GaN-based HFET device structure and method of fabricating the same is disclosed which utilizes a new material combination based on aluminum silicon nitride (AlSiN) to passivate a GaN surface of a HFET device. In one embodiment, the AlSiN layer functions both as a passivation layer and a gate dielectric in the HFET device. Compared with traditional passivation materials, the wider bandgap of AlSiN when used in the HFET structure described herein may minimize current collapse during switching, reduce gate leakage, and provide enhanced gate reliability and stability.

[0016] In one embodiment, the HFET device has first and second active layers with a two-dimensional electron gas layer forming therebetween. A passivation layer of AlSiN (e.g., AlSi_3N_4) is disposed on the second active layer. The AlSiN passivation layer may also serve as a first gate dielectric layer. (In the present disclosure, this dual function layer is also referred to as a passivation / first gate dielectric layer.) In a further embodiment, a second gate dielectric layer is disposed on the first gate dielectric layer. In one example, aluminum oxide (Al_2O_3) is utilized for the second gate dielectric layer. In other embodiments, one or more additional layers are formed over the second gate dielectric layer. A gate member is disposed above the AlSiN passivation layer. Ohmic contacts (source and drain) of the device extend down to the second active layer.

[0017] FIG. 1 illustrates a cross-sectional side view of an example semiconductor device 100, i.e., a HFET device, which includes a first active layer 102, also referred to as a channel layer, a second active layer 106, also called a barrier or donor layer, a passivation layer 108, a gate 112, and respective source and drain ohmic contacts 114 and 116. Respective source and drain ohmic contacts 114 and 116 are shown extending vertically down through passivation layer 108 to electrically connect to second active layer 106. As shown, source and drain ohmic contacts 114 & 116 are laterally spaced-apart, with gate 114 being disposed between source and drain ohmic contacts 116 & 118.

[0018] Further shown in FIG. 1 is an electrical charge layer 104 which is formed between the first active layer 102 and the second active layer 106. The electrical charge layer 104 is sometimes referred to as a two-dimensional electron gas (2DEG) layer 104. The 2DEG layer 104 defines a lateral conductive channel for the HFET device. The 2DEG layer 104 forms due to the bandgap difference between the two active layers. In particular, the 2DEG layer 104 forms due to the change in spontaneous and piezoelectric polarizations between the two active layers. Electrons trapped in a quantum well that results from the bandgap difference between the respective first and second active layer 102 and 106 are thus free to move laterally in two (horizontal) dimensions but are tightly confined in the third (vertical) dimension.

[0019] In the context of the present disclosure, the term "in-situ" refers to a process that is carried out within a single tool or reaction chamber without exposing the wafer to the environment outside the tool or chamber. Further, the term "ex-situ" may refer to a process that is not carried out in a single tool. In another embodiment, formation of passivation layer 108 may be carried out using metal-organic chemical vapor decomposition (MOCVD) after formation of the first and second active layers

102 and 106, respectively. In other words, the passivation layer 108 may be deposited in-situ with the first and second active layers 102 and 106, respectively.

[0020] It is appreciated that first active layer 102 is typically disposed over a substrate (not shown) formed of any one of a number of different materials, such as sapphire (Al_2O_3), silicon (Si), GaN, or silicon carbide (SiC). In one embodiment, first active layer 102 comprises an epitaxial GaN layer. To avoid possible problems with lattice mismatch and/or differences in thermal coefficients of expansion, one or more additional layers may be disposed between first active layer 102 and the underlying substrate. For example, an optional thin nucleation layer may be formed between the substrate and first active layer 102. In other examples, first active layer 102 may comprise different semiconductor materials containing various nitride compounds of other Group III elements. In addition, a thin (~ 1 nm) layer of AlN may be formed on top of first active layer 102 prior to formation of second active layer 106. First active layer 102 may be grown or deposited on the substrate.

[0021] The second active layer 106 is disposed on the first active layer 102. In the example of FIG. 1, second active layer 106 comprises aluminum gallium nitride (AlGa_N). In other examples, different Group III nitride semiconductor materials such as aluminum indium nitride (AlInN) and aluminum indium gallium nitride (AlInGa_N) may be used for second active layer 106. In other embodiments, the material of second active layer 106 may be a non-stoichiometric compound. In such materials, the ratios of the elements are not easily represented by ordinary whole numbers. For example, the second active layer 106 may be a non-stoichiometric compound of a Group III nitride semiconductor material such as $\text{Al}_x\text{Ga}_{1-x}\text{N}$, where $0 < x < 1$. In one implementation, second active layer 106 comprises AlGa_N (Al 25%) having a thickness of about 20 nanometers (nm) thick. A thin (~ 1 nm) termination layer of GaN may be optionally formed on top of second active layer 106 prior to formation of

passivation layer 108. The second active layer 106 may be grown or deposited on the first active layer 102.

[0022] As shown in FIG. 1, passivation layer 108 is disposed on second active layer 106. As discussed above, in one embodiment, passivation layer 108

5 comprises aluminum silicon nitride (AlSiN). In one example, the thickness of passivation 108 may be in an approximate range of 1-10 nanometers (nm) thick. Further, in one implementation passivation layer 108 is substantially 5-10% of aluminum (Al) to silicon nitride (SiN) and formed between 1-10 nm thick. As previously discussed, passivation layer 108 may be deposited in-situ with the first
10 and second active layers 102 and 106, respectively, and utilized to passivate the GaN-based active layers. In one example, passivation layer 108 has purity, density, and strength characteristics similar to a layer grown in-situ using MOCVD. For example, a layer grown in-situ generally has greater purity, higher strength, and higher density as compared to a layer grown ex-situ. Further, passivation layer 108
15 may also be utilized as a gate dielectric layer.

[0023] Passivation layer 108 separates gate 112 from second active layer 106. As shown, gate 112 is disposed atop passivation layer 108. In one embodiment, gate 112 comprises a gold nickel (NiAu) alloy. In another embodiment, gate 112 comprises a titanium gold (TiAu) alloy or molybdenum gold MoAu alloy. In
20 other examples, gate 112 may comprise a gate electrode and gate field plate. In operation, gate 112 controls the forward conduction path between respective source and drain ohmic contacts 114 & 116. In the example of FIG. 1, the portion of gate 112 which is above passivation layer 108 and extends laterally towards ohmic drain contact 116 serves as a gate field plate, which functions to alleviate the electric field
25 intensity at an edge (closest to ohmic drain contact 116).

[0024] Ohmic contacts 114 and 116 are disposed through passivation dielectric layer 108 to contact second active layer 106. Ohmic contact 114 is one example of a source contact, while ohmic contact 116 is one example of a drain contact. In one embodiment, ohmic contacts 114 and 116 may be formed by etching
5 openings in passivation layer 108, followed by a metal deposition and annealing steps.

[0025] As shown, FIG. 1 illustrates the device structure at a point in the fabrication process just after formation of gate 112 and ohmic metal contacts 114 and 116, which respectively comprise source and drain electrodes of GaN HFET
10 device 100. FIG. 1 shows ohmic metal contacts 114 and 116 formed directly on passivation layer 108. In other embodiments, ohmic metal contacts 114 and 116 may be formed in recesses which extend vertically downward into the second active layer 106. In still other embodiments, ohmic metal contacts 114 and 116 may be formed in recesses that extend vertically downward through second active layer 106
15 to contact the first active layer 102.

[0026] When semiconductor device 100 is configured for use as a power switch, gate 112 and ohmic contacts 114 and 116 are typically coupled through terminals to form electrical connections to external circuits. In operation, electric charge in 2DEG layer 104 flows laterally between ohmic contacts 114 and 116 to
20 become a current in an external circuit. The electric charge flow, and hence the current, may be controlled by a voltage from an external circuit that is electrically connected between the gate 112 and ohmic contact 114.

[0027] As used in this disclosure, an electrical connection is an ohmic connection. An ohmic connection is one in which the relationship between the
25 voltage and the current is substantially linear and symmetric for both directions of the current. For example, two metal patterns that contact each through only metal

are electrically connected. In contrast, ohmic contacts 114 and 116 are not electrically connected to each other in semiconductor device 100 because any connection between these two contacts is through a channel in the semiconductor material, which conduction path is controlled by gate 112. Similarly, gate 112 is not electrically connected to second active layer 106 since passivation layer 108 insulates gate 112 from the underlying active layers.

[0028] As discussed above, utilizing AlSiN as passivation layer 108 helps to alleviate the adverse effects of accumulated surface charge during the fabrication and/or handling of the device 100. In addition, utilizing AlSiN as passivation layer 108 in the HFET structure described herein may minimize current collapse during switching, reduce gate leakage, and provide enhanced gate reliability and stability. Further, passivation layer 108 may also be utilized as a gate dielectric layer.

[0029] FIG. 2 illustrates a cross-sectional side view of an example semiconductor device (HFET device) 200 which includes a first active layer 202, a second active layer 206, and a 2DEG layer 204 formed there between. Also shown are a passivation / first gate dielectric layer 208, a second gate dielectric 210, a gate 212, and respective source and drain ohmic contacts 214 and 216. Semiconductor device 200 shown in FIG. 2 is the similar to semiconductor device 100 of FIG. 1, except that HFET device 200 includes a second gate dielectric layer 210 atop passivation layer 218. Second gate dielectric layer 210 is disposed on passivation/first gate dielectric layer 208 and laterally surround respective source and drain ohmic contacts 114 and 116, as well as gate 112. Further, passivation / first gate dielectric layer 208 is similar to passivation layer 108, however is referred to as "passivation / first gate dielectric layer" to emphasize that the passivation layer 208 may also be utilized as one layer of multiple gate dielectric layers.

[0030] As shown, second gate dielectric layer 210 is disposed on passivation / first gate dielectric layer 208. In one example, second gate dielectric layer 210 comprises aluminum oxide (Al_2O_3). In still further examples, other oxide materials, such as ZrO , HfO , SiO_2 and GdO , may be utilized for the second gate dielectric layer 210. In one embodiment, second gate dielectric layer 210 has a thickness in the range of approximately 10-20 nm thick. In one embodiment, second gate dielectric layer 210 is thicker than passivation / first gate dielectric layer 208. For example, the thickness of passivation / first gate dielectric layer 208 may be in a range of approximately 1-10 nm. In one example fabrication process, second gate dielectric layer 210 may be deposited ex-situ from respective first and second active layers 202 & 206 utilizing atomic layer deposition (ALD).

[0031] As shown, passivation / first gate dielectric layer 208 and second gate dielectric layer 210 vertically separate gate 212 from second active layer 206. In certain embodiments, gate 212 may comprise a gate electrode and a gate field plate member. In the example of FIG. 2, the portion of gate 212 which is above the second passivation layer 218 and extends laterally towards drain ohmic contact 216 serves as a gate field plate member, which functions to alleviate the electric field intensity at an edge (closest to drain ohmic contact 216).

[0032] As shown, source and drain ohmic contacts 214 and 216 are respectively disposed on opposite lateral sides of gate 212. Ohmic contacts 214 and 216 extend vertically the second gate dielectric layer 210 and passivation / first gate dielectric layer 208 to contact second active layer 206. In one embodiment, ohmic contacts 214 and 216 may be formed by etching openings in the second gate dielectric layer 210 and passivation / first gate dielectric layer 208, followed by a metal deposition and annealing steps. In another example fabrication process,

ohmic contacts 214 and 216 may be formed before the deposition of second gate dielectric layer 210.

[0033] Further, passivation / first gate dielectric layer 208 may be utilized as one gate dielectric layer along with second gate dielectric layer 210. Practitioners in the art will appreciate that utilizing multiple gate dielectric layers in the manner described herein may advantageously produce higher critical voltage operation of the resulting HFET device. The critical voltage, V_{CRIT} , is defined as the gate-to-source voltage, V_{GS} , at which there is a relatively sharp rise in the gate leakage current. In addition, the use of multiple gate dielectric layers may improve the thermal stability of semiconductor device 200 as compared to a device utilizing only a single gate dielectric layer. Thermal stability relates to how much the gate leakage current of the device increases with temperature.

[0034] FIG. 3 illustrates a cross-sectional side view of an example semiconductor device (HFET device) 300 which includes a first active layer 302, a second active layer 306, and a 2DEG layer 304 formed therebetween. Also shown are a passivation / first gate dielectric layer 308, a second gate dielectric 310, an upper passivation layer 318, a gate 312, and respective source and drain ohmic contacts 314 and 316. Semiconductor device 300 shown in FIG. 3 is similar to the semiconductor device 100 of FIG. 1 and 200 of FIG. 2, except that HFET device 300 includes upper passivation layer 318. Upper passivation layer 318 is disposed on second gate dielectric 310 and laterally surround respective source and drain ohmic contacts 314 and 316, as well as gate 312. Further, passivation / first gate dielectric layer 308 is similar to passivation layer 108, however is referred to as "passivation / first gate dielectric layer" to emphasize that the passivation layer / first gate dielectric layer 308 may also be utilized as one layer of multiple gate dielectric layers.

[0035] In one embodiment, upper passivation layer 318 may comprise a dielectric material such as silicon nitride (SiN). In other embodiments, upper passivation layer 318 may comprise multiple layers of material. It is appreciated that upper passivation layer 318 provides stability of the electrical characteristics of HFET device 300 by isolating the surface of the device from electrical and chemical contaminants in the surrounding environment. Upper passivation layer 218 may be deposited through chemical vapor deposition such as low pressure chemical vapor deposition (LPCVD) or plasma-enhanced chemical vapor deposition (PECVD).

[0036] As shown, upper passivation layer 318, passivation / first gate dielectric layer 308 and second gate dielectric layer 310 vertically separate gate 312 from second active layer 306. In certain embodiments, gate 312 may comprise a gate electrode and a gate field plate member. As shown, gate 312 extends vertically through an opening formed in upper passivation layer 318 to contact second gate dielectric layer 210. In an example fabrication process, gate 312 may be formed by etching an opening in upper passivation layer 318, followed by a gate metal deposition. In the example of FIG. 3, the portion of gate 312 which is above the upper passivation layer 318 and extends laterally towards drain ohmic contact 316 serves as a gate field plate member, which functions to alleviate the electric field intensity at an edge (closest to drain ohmic contact 316).

[0037] As shown, source and drain ohmic contacts 314 and 316 are respectively disposed on opposite lateral sides of gate 312. Ohmic contacts 314 and 316 extend vertically through upper passivation layer 318, second gate dielectric layer 310, and passivation / first gate dielectric layer 308 to contact second active layer 306. In one embodiment, ohmic contacts 314 and 316 may be formed by etching openings in upper passivation layer 318, second gate dielectric layer 310, and passivation / first gate dielectric layer 308, followed by a metal deposition and

annealing steps. In another example fabrication process, ohmic contacts 314 and 316 may be formed before the deposition of second gate dielectric layer 310 and the upper passivation layer 318.

[0038] FIG. 4 illustrates an example process flow 400 for constructing a semiconductor device such as HFET devices 100, 200, or 300 respectively shown in FIGS. 1, 2, and 3. In the example shown, the process starts after the completion of the epitaxial growth or deposition of the first and second active layers on the substrate. Formation of the layer (also referred to as the passivation / first gate dielectric layer above) comprising AlSiN is carried out in-situ after growth of the GaN / AlGaN active layers (block 402). In one embodiment, the passivation layer is deposited using a MOCVD technique carried out at a temperature range between 800-900 °C with a reactor pressure of about 100 Torr. In one embodiment a passivation layer comprising AlSiN is grown with a MOCVD technique using silane (SiH_4), ammonia (NH_3) and trimethylaluminum (TMAI) as precursors for the AlSiN. Hydrogen (H_2) and nitrogen (N_2) may be used as carrier gases. A total flow of about 50 l/min. with NH_3 flow in a range of about 1-10 l/min., SiH_4 of about 1 l/min., and TMAI flow in a range of about 5-20 sccm. The NH_3 flow is maintained so that the integrated N composition is maintained at stoichiometry between Si_3N_4 and AlN as monitored by the overall refractive index and the density of the AlSiN film.

[0039] The passivation / layer is formed to a thickness in a range of approximately 1-10 nm, and is continuous over the surface of the wafer. In one embodiment, the thickness of the passivation layer is about 5 nm. In still another embodiment, the passivation layer is formed in-situ with the first and second active layers. For example, the same MOCVD machine that is used to form the first and second active layers may also be used to form the passivation / first gate dielectric layer. In one example, the passivation layer / first gate dielectric layer has purity,

density, and strength characteristic to a layer grown in-situ using MOCVD. For example, a layer grown in-situ generally has greater purity, higher strength, and higher density to a layer grown ex-situ.

[0040] After growth of the passivation layer, the surface of the passivation layer undergoes mesa isolation etching to define the active region of the ohmic contacts (block 404). The mesa isolation may be performed utilizing a reactive-ion etching (RIE) system. In other fabrication methods, the mesa isolation may be performed using inductively coupled plasma (ICP) RIE. At this point in the process flow, ohmic via openings may optionally be formed through the passivation layer, followed by ohmic metallization and annealing (block 306). An example ohmic contact metal is TiAlMoAu. The metal ohmic contacts may be annealed utilizing a RTA tool at a temperature range of approximately 600-900 °C for about one minute.

[0041] Next, the second gate dielectric layer which may be comprised of Al_2O_3 may be optionally deposited on the passivation layer (block 408). The second gate dielectric layer may also be deposited over the source and drain ohmic contacts. In one embodiment, the second gate dielectric layer is deposited on the wafer surface using ALD at 300 °C. The second gate dielectric layer may be grown to a thickness in a range of approximately 10-20 nm.

[0042] In one embodiment, the deposition of the formation of the second gate dielectric layer may be performed ex-situ from the first and second active layers and the passivation / first gate dielectric layer. For example, both the passivation / first and second gate dielectric layers may be deposited on the wafer surface using the same ALD chamber or other machine or system.

[0043] A high temperature anneal may be performed after the second gate dielectric layer has been deposited (block 410) to improve the film and interface quality of the second gate dielectric layer. By way of example, the annealing step

may be performed in a furnace at temperature range of 450-750 °C for approximately 5-10 minutes. Annealing may also be performed using a number of different tools, such as a rapid temperature annealing (RTA) tool. It should be appreciated that block 408 and block 410 are considered optional, as the blocks
5 apply to the HFET devices shown in FIGS. 2 and 3, which illustrate a second gate dielectric layer.

[0044] After annealing, an upper passivation layer may be optionally deposited over the second gate dielectric layer (block 412). In one embodiment, the upper passivation layer may be deposited using PECVD. The upper passivation
10 layer may also be deposited using LPCVD. The upper passivation layer is typically formed to a thickness in a range of approximately 100-150 nm. As discussed above, the upper passivation layer may comprise silicon nitride (SiN) or other materials having similar properties.

[0045] Gate via formation is shown in block 314. This step is optionally
15 performed when a upper passivation layer has been formed over the stack of multiple gate dielectric layers. Gate via formation comprises masking and etching the upper passivation layer such that an opening is formed through the upper passivation layer, thereby exposing the underlying second gate dielectric layer. In one embodiment, dry etching may be utilized with a gas such as CF₄ or SF₆ to etch
20 through the upper passivation layer. After the etching process exposes the second gate dielectric layer, a gate metal or metal alloy deposition (block 316) is performed to fill the etched opening. In one example, NiAu is used as the gate metal. As shown in FIGS. 1, 2, and 3, a field plate portion of the gate may be formed by masking or etching the gate metal such that a top portion laterally extends over the upper
25 passivation layer towards the farthest (drain) ohmic contact. It should be

appreciated that blocks 412 and 414 are considered optional, as the blocks apply to the HFET device 300 shown in FIG. 3, which illustrates an upper passivation layer.

[0046] Persons of ordinary skill in the semiconductor arts will understand that other standard post-fabrication or back-end processing steps may be performed, including forming metal (e.g., patterned lines or traces) on the surface of the wafer, wafer backgrinding (also called backlapping or wafer thinning), die separation, and packaging.

[0047] FIG. 5 is a diagram illustrating another example process flow 400 for constructing a HFET device such as semiconductor device 200 or 300 shown in FIGS. 2 and 3. The process shown in FIG. 5 is the same as that discussed in connection with FIG. 4, with like numbered steps being the same as described above, except that process flow 500 includes additional block 503 interposed between block 502 and block 504. After the in-situ grown of the AlSiN passivation / first gate dielectric layer, aluminum nitride (AlN) is grown on top of the AlSiN layer (block 503). In one embodiment, the AlN layer is grown in-situ with the AlSiN passivation / first gate dielectric layer and first and second active layers. The thickness of the AlN layer may be about 1 nm thick. After mesa isolation etching and ohmic metallization and annealing in blocks 504 and 506, the AlN layer is effectively utilized as a seed layer to form the Al₂O₃ second gate dielectric layer (block 508).

[0048] The above description of illustrated example embodiments, including what is described in the Abstract, are not intended to be exhaustive or to be limitation to the precise forms disclosed. While specific embodiments and examples of the subject matter described herein are for illustrative purposes, various equivalent modifications are possible without departing from the broader spirit and scope of the present invention. Indeed, it is appreciated that the specific example

thicknesses, material types, temperatures, voltages, times, etc., are provided for explanation purposes and that other values may also be employed in other embodiments and examples in accordance with the teachings of the present invention.