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(71) Applicant *(for all designated States except US)*: MICRON TECHNOLOGY, INC. [US/US]; 8000 South Federal Way, Boise, ID 83706 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: SANDHU, Gurtej, S. [GB/US]; 2964 East Parkriver Drive, Boise, ID 83706 (US). FAZAN, Pierre, C. [CH/US]; 2267 Illinois Avenue, Boise, ID 83706 (US).

(74) Agents: MATKIN, Mark, S. et al.; Suite 1300, 601 West First Avenue, Spokane, WA 99204 (US).

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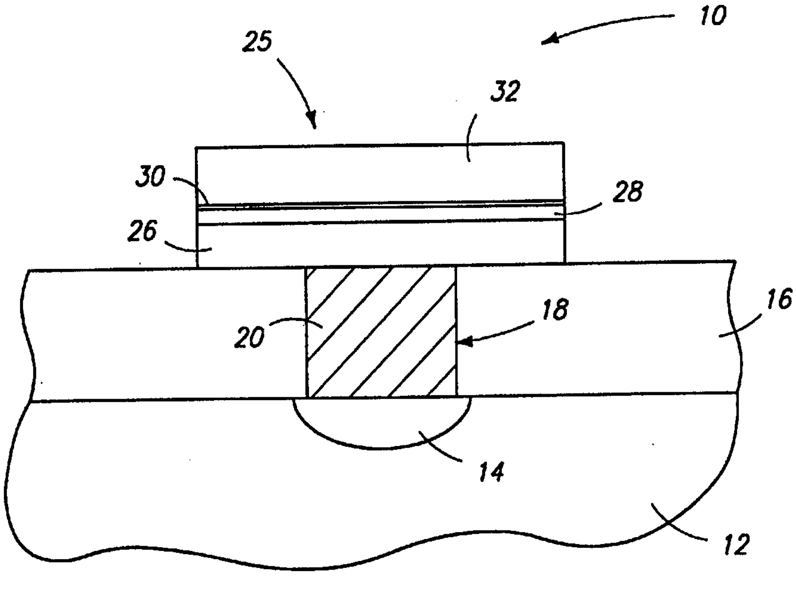
(54) Title: METHOD OF FORMING A Ta_2O_5 DIELECTRIC LAYER



(57) Abstract

A method of forming a capacitor includes: (a) providing a node to which electrical connection to a capacitor is to be made; (b) providing a first electrically conductive capacitor plate over the node; (c) chemical vapor depositing a capacitor dielectric layer of Ta_2O_5 over the first electrically conductive capacitor plate; and (d) providing a predominately amorphous diffusion barrier layer over the Ta_2O_5 dielectric layer. A capacitor construction is also disclosed. The preferred amorphous diffusion barrier layer is electrically conductive and constitutes a metal organic chemical vapor deposited $TiC_xN_yO_z$, where "x" is in the range of from 0.01 to 0.5, and "y" is in the range of from 0.99 to 0.5, and "z" is in the range of from 0 to 0.3, with the sum of "x", "y" and "z" equalling about 1.0.

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DESCRIPTION

METHOD OF FORMING A TA_2O_5 DIELECTRIC LAYER

Technical Field

This invention relates to methods of forming a capacitor having a Ta_2O_5 dielectric layer, to methods of forming a Ta_2O_5 dielectric layer, and to capacitor constructions.

Background Art

As DRAMs increase in memory cell density, there is a continuing challenge to maintain sufficiently high storage capacitance despite decreasing cell area. Additionally, there is a continuing goal to further decrease cell area. One principal way of increasing cell capacitance is through cell structure techniques. Such techniques include three-dimensional cell capacitors, such as trenched or stacked capacitors. Yet as feature size continues to become smaller and smaller, development of improved materials for cell dielectrics as well as the cell structure are important. The feature size of 256 Mb DRAMs will be on the order of 0.25 micron, and conventional dielectrics such as SiO_2 and Si_3N_4 might not be suitable because of small dielectric constants.

Chemical vapor deposited (CVD) Ta_2O_5 films are considered to be very promising cell dielectrics layers, as the dielectric constant of Ta_2O_5 is approximately three times that of Si_3N_4. Proposed prior art capacitor constructions include the use of Ta_2O_5 as a capacitor dielectric layer, in combination with an overlying predominately crystalline TiN electrode or other layer. However, diffusion relative to the tantalum layer is problematic in the resultant capacitor construction. For example, tantalum from the Ta_2O_5 tends to undesirably out-diffuse from the dielectric layer. Further, materials from the adjacent conductive capacitor plates can diffuse into the tantalum layer. In either event, the dielectric properties of the Ta_2O_5 layer are adversely affected in a less than predictable or an uncontrollable manner.

Brief Description of the Drawings

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment in accordance with the invention.

Fig. 2 is a diagrammatic sectional view of an alternate embodiment semiconductor wafer fragment in accordance with the invention.

Fig. 3 is a diagrammatic sectional view of yet another alternate embodiment semiconductor wafer fragment in accordance with the invention.

Best Modes for Carrying Out the Invention and Disclosure of Invention

In accordance with one aspect of the invention, a method of forming a capacitor includes the following steps:

providing a node to which electrical connection to a capacitor is to be made;

providing a first electrically conductive capacitor plate over the node;

chemical vapor depositing a capacitor dielectric layer of Ta_2O_5 over the first electrically conductive capacitor plate; and

providing a predominately amorphous diffusion barrier layer over the Ta_2O_5 dielectric layer.

In accordance with another aspect of the invention, a method of forming a dielectric layer comprises the following steps:

chemical vapor depositing a dielectric layer of Ta_2O_5 atop a substrate; and

providing a predominately amorphous diffusion barrier layer over the Ta_2O_5 dielectric layer.

In accordance with still a further aspect of the invention, a capacitor comprises:

a first electrically conductive capacitor plate;

a capacitor dielectric layer adjacent the first electrically conductive capacitor plate, the capacitor dielectric layer comprising Ta_2O_5;

a predominately amorphous diffusion barrier adjacent the Ta_2O_5 dielectric layer; and

a second electrically conductive capacitor plate, the Ta_2O_5 dielectric layer being positioned between the first and second electrically conductive plates.

More particularly and first with reference to Fig. 1, a semiconductor wafer fragment is indicated generally with reference numeral 10. Such comprises a bulk silicon substrate 12 having a conductive diffusion area 14 formed therein. An insulating layer 16, typically borophosphosilicate glass (BPSG), is provided over substrate 12, with a contact opening 18 having been previously provided therein to diffusion area 14. A conductive material 20 fills contact opening 18, with material 20 and oxide layer 16 having been planarized as shown. Material

20 might be any suitable conductive material, such as tungsten or conductively doped polysilicon. A capacitor construction 25 is provided atop layer 16 and plug 20, with conductive plug 20 constituting a node to which electrical connection to capacitor 25 is made.

Capacitor 25 comprises a first electrically conductive capacitor plate 26 which has been provided and patterned over node 20. An example and preferred material is conductively doped polysilicon, provided to a thickness of 1000 Angstroms for 256 Mb density. A capacitor dielectric layer 28 of Ta_2O_5 is provided over first electrically conductive capacitor plate 26. An example process for depositing layer 28 is by low pressure chemical vapor deposition at 450° C using $Ta(OC_2H_5)_5$ and oxygen as precursors. $Ta(OC_2H_5)_5$ can be vaporized at 170° C, and introduced into a reactor chamber using argon or another suitable carrier gas. Subsequently, densification by rapid thermal annealing in a dry oxygen atmosphere at a temperature ranging from 700° C to 900° C is utilized. Preferably, the polysilicon surface of lower capacitor plate 26 is cleaned by an *in situ* HF dip prior to provision of the Ta_2O_5. Rapid thermal nitrogen treatment can also be carried out immediately prior to Ta_2O_5 deposition, such as at 900° C for 60 seconds in NH_3. An example and preferred thickness for layer 28 in accordance with 256 Mb integration is 100 Angstroms.

A predominately amorphous diffusion barrier layer 30 is provided over Ta_2O_5 dielectric layer 28. Such layer is preferably electrically conductive, with an example and preferred thickness for 256 Mb integration being 200 Angstroms. A most preferred material for layer 30 is predominately amorphous $TiC_xN_yO_z$ deposited by metal organic chemical vapor deposition (MOCVD), where "x" is in the range of from 0.01 to 0.5, and "y" is in the range of from 0.99 to 0.5, and "z" is in the range of from 0 to 0.3, with the sum of "x", "y" and "z" equalling about 1.0. A preferred metal organic precursor for such deposition is $Ti(NR_2)_4$, where R is selected from the group consisting of H and a carbon containing radical. Deposition conditions for producing such a predominately amorphous layer include from 200° C to 600° C, and from 0.1 to 100 Torr. Most preferably, the amorphous diffusion barrier layer comprises a material which is a barrier to out-diffusion of tantalum from the Ta_2O_5 layer. The preferred $TiC_xN_yO_z$ material provides this function.

Also most preferably, "z" will be equal to zero. Unfortunately however, oxygen can undesirably become incorporated in the deposited film when it is exposed to oxygen, even ambient air. This incorporated oxygen undesirably affects conductivity. Accordingly, exposure to oxygen is preferably minimized until the subject film is covered by subsequent layers which can effectively act as a barrier to oxygen incorporation.

Subsequently, a second electrically conductive capacitor plate 32 is provided outwardly of diffusion barrier layer 30, such that Ta_2O_5 dielectric layer 28 is positioned between the first and second electrically conductive plates. Accordingly, second electrically conductive capacitor plate 32 constitutes a discrete, second electrically conductive capacitor plate provided over the amorphous diffusion barrier layer 30. An example and preferred material for second capacitor plate 32 is polysilicon, with 1000 Angstroms being an example preferred thickness for 256 Mb integration.

Prior art constructions and proposals for utilizing Ta_2O_5 as a capacitor dielectric layers suffer from the drawback of undesired out-diffusion of tantalum atoms from such layer, or diffusion of undesired components into such layer. Provision of a thin predominately amorphous diffusion barrier layer as described above in the preferred embodiment facilitates maintaining integrity of the Ta_2O_5 layer and, accordingly, its associated desired high dielectric constant in such a small application. It has been discovered in the context of the invention that amorphous materials are better diffusion barriers due to absence of crystal grain boundaries which can provide an easy path for diffusion in polycrystalline materials.

Fig. 2 illustrates an alternate embodiment capacitor construction and method in accordance with the invention. Like numerals from Fig. 1 have been utilized where appropriate, with differences being indicated by either different numerals, or like numerals with the suffix "a". Wafer fragment 10a comprises a capacitor construction 25a differing from the first described embodiment in provision of a predominately amorphous, electrically conductive second capacitor plate 32a which functions as an inherent amorphous diffusion barrier layer. The preferred material is the previously described metal organic chemical vapor deposited $TiC_xN_yO_z$ which is provided to a thickness which is effective to form the predominant portion (the entire portion, as shown) of second electrically conductive capacitor plate 32a. Alternately, both of plates 32 and 26 might be provided to constitute a conductive inherently amorphous diffusion barrier layer, such as the MOCVD $TiC_xN_yO_z$.

Fig. 3 illustrates yet another alternate embodiment capacitor construction and method. Again, like numerals from the first described embodiment are utilized where appropriate, with differences being indicated by different numerals or with the suffix "b". Wafer fragment 10b includes a capacitor construction 25b having the same first and second capacitor plates 26 and 32, respectively, of the first described embodiment. However, a pair of predominately amorphous diffusion barrier layers 30 and 40 are provided to encapsulate Ta_2O_5 dielectric layer 28 to prevent tantalum out-diffusion.

The invention was reduced to practice in a study of three types of rapid thermal nitrogen annealed polysilicon films having Ta_2O_5 films thereatop, with different overlying titanium nitride or titanium carbonitride layers being deposited. The inventive constructions were deposited by metal organic chemical vapor deposition of a $TiC_xN_yO_z$ film deposited from tetrakisdimethylamido titanium (TDMAT) at 450° C, and 0.5 Torr in a cold wall chemical vapor deposition reactor. These wafers were compared with two non-inventive deposited titanium nitride layers. These two non-invention layers were deposited by chemical vapor deposition and by sputtering, respectively. The CVD TiN films were formed by reacting $TiCl_4$ and NH_3 at 600° C (i.e., non-MOCVD) in a low pressure chemical vapor deposition reactor. The sputtered TiN films were formed by reactive sputtering of Ti in an Ar-N_2 ambient at 0.014 Torr. The substrates were heated to 400° C during deposition. On top of the CVD TiN film, and also on the inventive MOCVD films, an additional capping layer of sputtered TiN was deposited for protection against oxidation during plasma steps used to remove photoresist. The sputter deposited and CVD TiN films using $TiCl_4$ and NH_3 were crystalline, while the MOCVD films of the invention are substantially amorphous.

Four samples of each group were prepared, out of which three were annealed at 700° C, 800° C and 900° C for thirty minutes at 7×10^{-6} Torr. With respect to the control CVD TiN films, out-diffusion of Ta into this crystalline TiN layer was observed, and to increase with increasing annealing temperature. Also with the crystalline sputtered TiN films, significant out-diffusion of tantalum into the TiN layer was observed after the 900° C anneal.

With the amorphous MOCVD $TiC_xN_yO_z$ films, no out-diffusion of tantalum was observed. Twenty atomic percent of carbon and oxygen were however detected in the film. Yet, the absence of interaction of the MOCVD $TiC_xN_yO_z$

layers with the dielectric Ta_2O_5 up to 900° C makes such composite layers attractive candidates for capacitor and other dielectric layers.

CLAIMS

1. A method of forming a capacitor comprising the following steps:

forming a first electrically conductive capacitor plate over a substrate;

forming a capacitor dielectric layer of Ta_2O_5 over the first electrically conductive capacitor plate; and

forming a predominately amorphous diffusion barrier layer over the Ta_2O_5 dielectric layer.

2. The method of forming a capacitor of claim 1 wherein the amorphous diffusion barrier layer is provided to be a barrier to out diffusion of tantalum from the Ta_2O_5 layer.

3. The method of forming a capacitor of claim 1 wherein the amorphous diffusion barrier layer is provided to be electrically conductive.

4. The method of forming a capacitor of claim 1 wherein the amorphous diffusion barrier layer is provided to be electrically conductive and to a thickness which is effective to form the predominate portion of a second electrically conductive capacitor plate.

5. The method of forming a capacitor of claim 1 further comprising providing a discrete, second electrically conductive capacitor plate over the amorphous diffusion barrier layer.

6. The method of forming a capacitor of claim 1 wherein the step of forming the amorphous diffusion barrier layer comprises metal organic chemical vapor depositing a $TiC_xN_yO_z$ layer over the Ta_2O_5, where "x" is in the range of from 0.01 to 0.5, and "y" is in the range of from 0.99 to 0.5, and "z" is in the range of from 0 to 0.3, with the sum of "x", "y" and "z" equalling about 1.0.

7. The method of forming a capacitor of claim 1 wherein the step of forming the amorphous diffusion barrier layer comprises metal organic chemical vapor depositing a $TiC_xN_yO_z$ layer over the Ta_2O_5, where "x" is in the range of from 0.01 to 0.5, and "y" is in the range of from 0.99 to 0.5, and "z" is in the range of from 0 to 0.3, with the sum of "x", "y" and "z" equalling about 1.0; and the step of metal organic chemical vapor depositing $TiC_xN_yO_z$ comprises utilizing a gaseous titanium organometallic precursor of the formula $Ti(NR_2)_4$, where R is selected from the group consisting of H and a carbon containing radical, and utilizing deposition conditions of from 200° C to 600° C and from 0.1 to 100 Torr.

8. The method of forming a capacitor of claim 1 wherein the step of forming the amorphous diffusion barrier layer comprises metal organic chemical vapor depositing a $TiC_xN_yO_z$ layer over the Ta_2O_5, where "x" is in the range of from 0.01 to 0.5, and "y" is in the range of from 0.99 to 0.5, and "z" is in the range of from 0 to 0.3, with the sum of "x", "y" and "z" equalling about 1.0; and the step of metal organic chemical vapor depositing $TiC_xN_yO_z$ comprises utilizing a gaseous titanium organometallic precursor of the formula $Ti(NR_2)_4$, where R is selected from the group consisting of H and a carbon containing radical, and utilizing deposition conditions of from 200° C to 600° C and from 0.1 to 100 Torr; and

further comprising providing a discrete, second electrically conductive capacitor plate over the amorphous diffusion barrier layer.

9. The method of forming a capacitor of claim 1 wherein the step of forming the amorphous diffusion barrier layer comprises metal organic chemical vapor depositing a $TiC_xN_yO_z$ layer over the Ta_2O_5, where "x" is in the range of from 0.01 to 0.5, and "y" is in the range of from 0.99 to 0.5, and "z" is in the range of from 0 to 0.3, with the sum of "x", "y" and "z" equalling about 1.0; and

further comprising providing a discrete, second electrically conductive capacitor plate over the amorphous diffusion barrier layer.

10. A method of forming a dielectric layer comprising the following steps:

forming a dielectric layer of Ta_2O_5 atop a substrate; and

forming a predominately amorphous diffusion barrier layer over the Ta_2O_5 dielectric layer.

11. The method of forming a dielectric layer of claim 10 wherein the amorphous diffusion barrier layer is provided to be a barrier to out diffusion of tantalum from the Ta_2O_5 layer.

12. The method of forming a dielectric layer of claim 10 wherein the amorphous diffusion barrier layer is provided to be electrically conductive.

13. The method of forming a dielectric layer of claim 10 wherein the step of forming the amorphous diffusion barrier layer comprises metal organic chemical vapor depositing $TiC_xN_yO_z$ layer over the Ta_2O_5, where "x" is in the range of from 0.01 to 0.5, and "y" is in the range of from 0.99 to 0.5, and "z" is in the range of from 0 to 0.3, with the sum of "x", "y" and "z" equalling about 1.0.

14. The method of forming a dielectric layer of claim 10 wherein the step of forming the amorphous diffusion barrier layer comprises metal organic chemical vapor depositing a $TiC_xN_yO_z$ layer over the Ta_2O_5, where "x" is in the range of from 0.01 to 0.5, and "y" is in the range of from 0.99 to 0.5, and "z" is in the range of from 0 to 0.3, with the sum of "x", "y" and "z" equalling about 1.0; and the step of metal organic chemical vapor depositing $TiC_xN_yO_z$ comprises utilizing a gaseous titanium organometallic precursor of the formula $Ti(NR_2)_4$, where R is selected from the group consisting of H and a carbon containing radical, and utilizing deposition conditions of from 200° C to 600° C and from 0.1 to 100 Torr.

15. A capacitor comprising:

a first electrically conductive capacitor plate;

a capacitor dielectric layer adjacent the first electrically conductive capacitor plate, the capacitor dielectric layer comprising Ta_2O_5;

a second electrically conductive capacitor plate, the Ta_2O_5 dielectric layer being positioned between the first and second electrically conductive plates; and

a predominately amorphous diffusion barrier layer adjacent the Ta_2O_5 dielectric layer.

16. The capacitor of claim 15 wherein the amorphous diffusion barrier layer comprises a material which is a barrier to out diffusion of tantalum from the Ta_2O_5 dielectric layer.

17. The capacitor of claim 15 wherein the amorphous diffusion barrier layer is electrically conductive.

18. The capacitor of claim 15 wherein the amorphous diffusion barrier layer is electrically conductive and constitutes a thickness which is effective to form a predominate portion of the second electrically conductive capacitor plate.

19. The capacitor of claim 15 wherein the amorphous diffusion barrier layer is electrically conductive, and a predominate portion of the second capacitor plate is discrete from the amorphous diffusion barrier layer.

20. The capacitor of claim 15 wherein the amorphous diffusion barrier layer comprises $TiC_xN_yO_z$, where "x" is in the range of from 0.01 to 0.5, and "y" is in the range of from 0.99 to 0.5, and "z" is in the range of from 0 to 0.3, with the sum of "x", "y" and "z" equalling about 1.0.

21. The capacitor of claim 15 wherein the amorphous diffusion barrier layer comprises $TiC_xN_yO_z$, where "x" is in the range of from 0.01 to 0.5, and "y" is in the range of from 0.99 to 0.5, and "z" is in the range of from 0 to 0.3, with the sum of "x", "y" and "z" equalling about 1.0; and

the amorphous diffusion barrier layer is electrically conductive and constitutes a thickness which is effective to form a predominate portion of the second electrically conductive capacitor plate.

22. The capacitor of claim 15 wherein the amorphous diffusion barrier layer comprises $TiC_xN_yO_z$, where "x" is in the range of from 0.01 to 0.5, and "y" is in the range of from 0.99 to 0.5, and "z" is in the range of from 0 to 0.3, with the sum of "x", "y" and "z" equalling about 1.0; and

the amorphous diffusion barrier layer is electrically conductive, and a predominate portion of the second capacitor plate is discrete from the amorphous diffusion barrier layer.

23. A capacitor comprising:

a first electrically conductive capacitor plate;

a capacitor dielectric layer adjacent the first electrically conductive capacitor plate, the capacitor dielectric layer comprising Ta_2O_5;

a second electrically conductive capacitor plate, the Ta_2O_5 dielectric layer being positioned between the first and second electrically conductive plates; and

a pair of predominately amorphous diffusion barrier layers adjacent the Ta_2O_5 dielectric layer.

24. The capacitor of claim 23 wherein the amorphous diffusion barrier layers comprise a material which is a barrier to out diffusion of tantalum from the Ta_2O_5 dielectric layer.

25. The capacitor of claim 23 wherein the amorphous diffusion barrier layers are electrically conductive.

26. The capacitor of claim 23 wherein the amorphous diffusion barrier layers are electrically conductive and constitute respective thicknesses which are effective to form a predominate portion of the first and the second electrically conductive capacitor plates, respectively.

27. The capacitor of claim 23 wherein the amorphous diffusion barrier layers are electrically conductive, and predominate portions of each of the first and the second capacitor plate are discrete from the amorphous diffusion barrier layers.

28. The capacitor of claim 23 wherein the amorphous diffusion barrier layers comprise $TiC_xN_yO_z$, where "x" is in the range of from 0.01 to 0.5, and "y" is in the range of from 0.99 to 0.5, and "z" is in the range of from 0 to 0.3, with the sum of "x", "y" and "z" equalling about 1.0.

29. The capacitor of claim 23 wherein the amorphous diffusion barrier layers comprise $TiC_xN_yO_z$, where "x" is in the range of from 0.01 to 0.5, and "y" is in the range of from 0.99 to 0.5, and "z" is in the range of from 0 to 0.3, with the sum of "x", "y" and "z" equalling about 1.0; and

the amorphous diffusion barrier layers are electrically conductive and constitute respective thicknesses which are effective to form a predominate portion of the first and the second electrically conductive capacitor plates, respectively.

30. The capacitor of claim 23 wherein the amorphous diffusion barrier layers comprise $TiC_xN_yO_z$, where "x" is in the range of from 0.01 to 0.5, and "y" is in the range of from 0.99 to 0.5, and "z" is in the range of from 0 to 0.3, with the sum of "x", "y" and "z" equalling about 1.0; and

the amorphous diffusion barrier layers are electrically conductive, and predominate portions of each of the first and the second capacitor plate are discrete from the amorphous diffusion barrier layers.

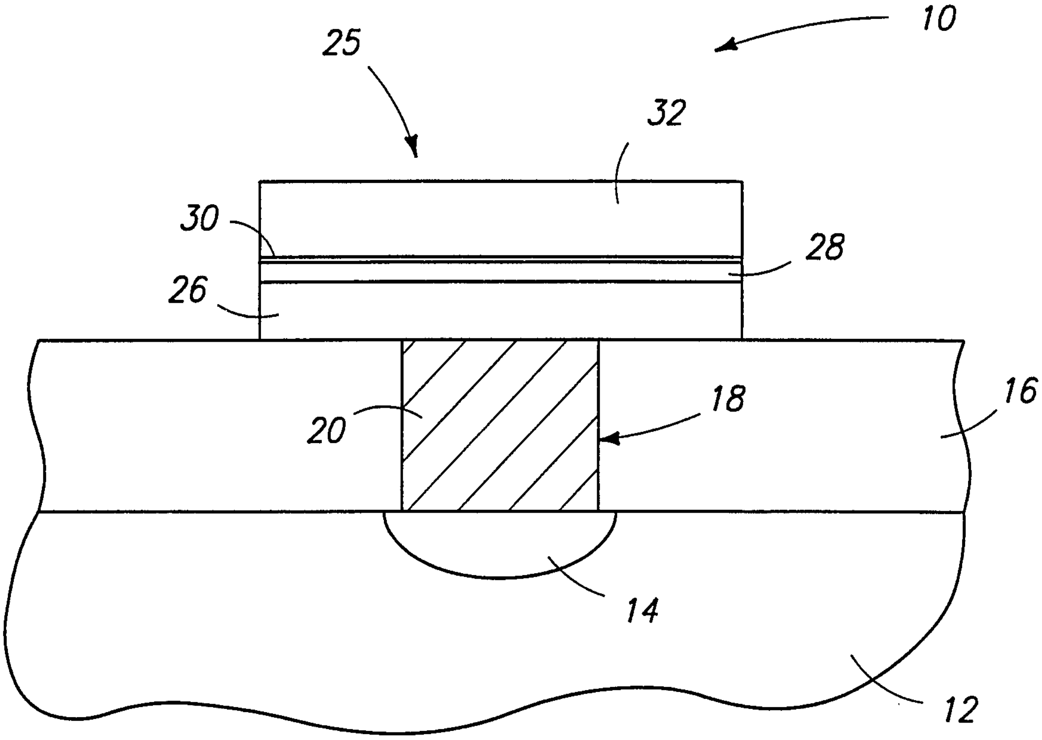

Fig 1

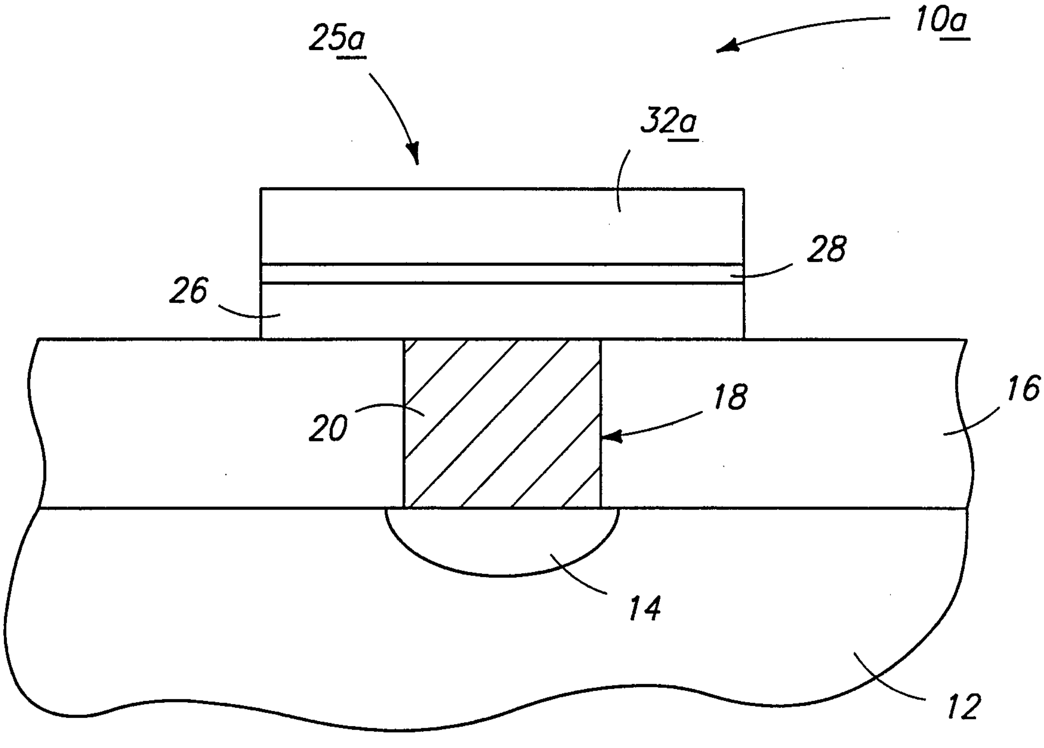

Fig 2

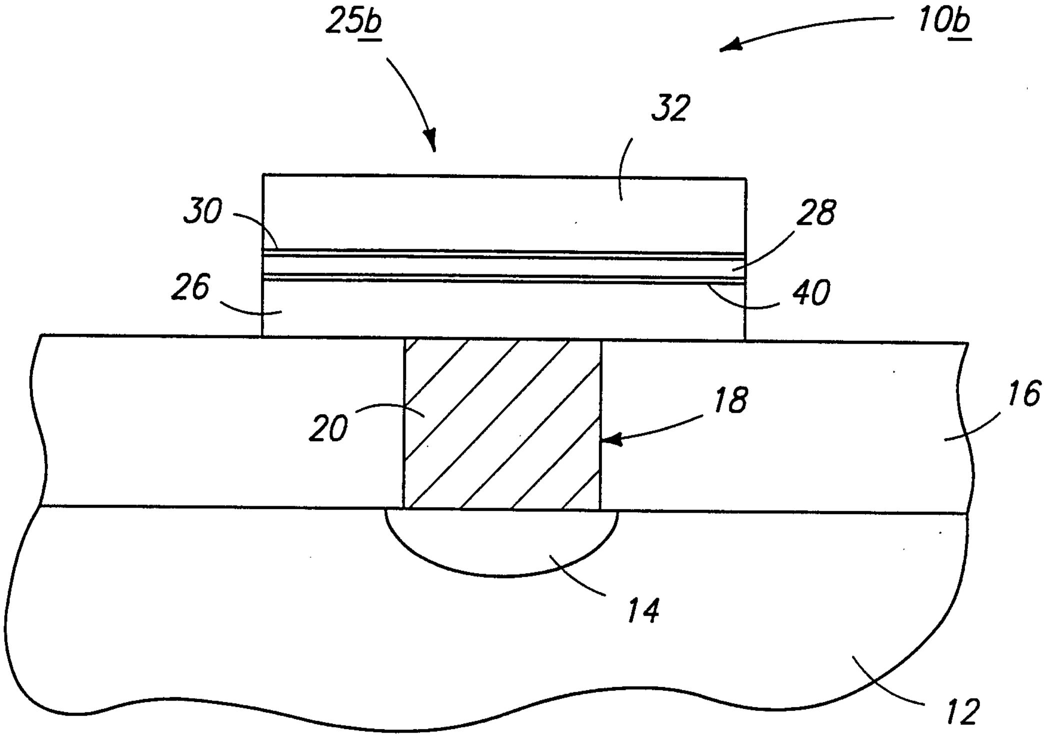

FIG 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/07212

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 21/70, 27/00
US CL :437/60
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 437/52; 437/60; 437/919; 257/295; 257/300; 257/303 257/306; 257/310

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P	US,A, 5,504,041 (Summerfelt) 02 April 1996	1-30
A	US,A, 5,057,447 (PATERSON) 15 October, 1991	1-30
A	US,A, 5,142,438 (Reinberg et al.) 25 August 1992	1-30
A	Zaima et al., "Conduction mechanisum of leakage current in Ta2O5 films on Si Prepared by LPCVD" J. Electrochemical Society, vol. 137, No. 9, September 1990, Pages 2876-2879	1-30
A	US,A, 5,471,364 (Summerfelt et al.) 28 November, 1995	1-30
A	US,A, 5,348,894 (Gnade et al.) 20 September 1994	1-30

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:
"A"	document defining the general state of the art which is not considered to be of particular relevance
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Date of the actual completion of the international search
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/07212

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Nicolet, M-A, "Thin Film diffusion Barriets fun metal-Semi conductor contact" 1997 Material Research pages 19-26.	1-30