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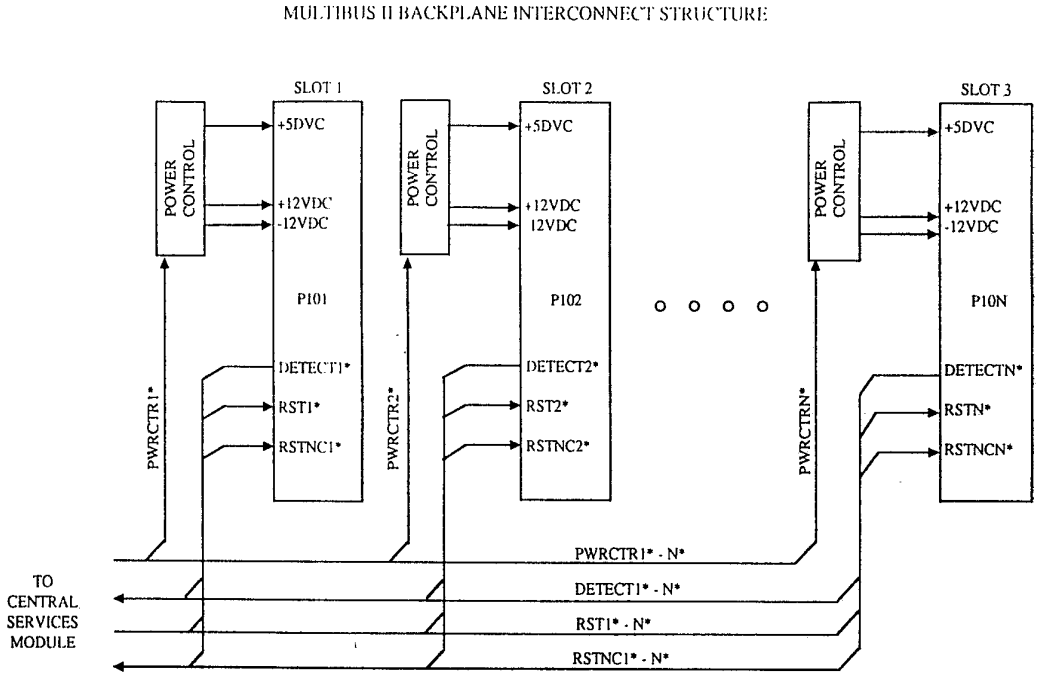

(57) Abstract

A method for the insertion or removal of a board (P101) without shutting down system power. A detect signal (DETECT 1*) indicates the insertion or removal of a board. Once a board has been detected, the slot controller will arbitrate for the bus, wait for existing bus traffic to subside, then power up (PWRCTR1*) and reset (RST1*) the new board.

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LIVE INSERTION OF COMPUTER MODULES

BACKGROUND AND SUMMARY OF THE INVENTION

The present invention relates generally to the insertion and the removal of a circuit device into a bus network, and more particularly, but not exclusively, to the insertion and removal of computer modules from a system which is under power.

Computers are becoming an ever increasing part of modern society. There have already been numerous examples where major disruption has occurred when a computer system has failed. Nonstop computer operation is already a requirement for many banks, hospitals, airlines, military applications, and communication systems. Up to now the solution to preventing disruption when a computer system fails is to provide a redundant system in conjunction with a primary system to go into operation when the primary system fails. This requires using two or more independent computer systems linked together. When one fails the other is ready to take its place.

Redundancy is one way of solving the failure problem and there are currently numerous commercial applications of this approach. However, there are drawbacks such as the expense (could be several hundred thousand dollars), the technical

complexity of setting up such a system, and adverse affects on the speed of operation when redundant systems are connected. Examples of reasons for some computer system failures are such things as earthquakes, fires, power disruptions, and communication network failures.

Sometimes only one board or module mounted on a computer backplane may fail while the others remain functional. A computer module may also be replaced simply to change the programming function of the computer system. Conventional computer systems provide power for the boards in the system through connectors in a backplane. The backplane not only provides power to each board but it also provides the signals used to communicate between boards. In the past, in order to insert or remove boards from a system, it was necessary to turn off the main power to the system. In large system configurations or critical real time applications, it is not always possible to shut down a system to add or replace boards. This has resulted in the development of complex redundant systems as described above which allow the user to switch from one system to another to facilitate the upgrade or repair of equipment. The need for equipment that can be easily serviced and maintained without shutting down the entire system is becoming critical.

The present invention facilitates board insertion and removal without shutting down system power. The present

invention is accomplished by: switching of power to the board when it is inserted or removed; and, controlling the communications between boards as the power to the board is turned on and off. To control the power to the board it is necessary to switch all power connections either on or off when there are no board-to-board communications occurring. To accomplish this a controller with a terminal interface will provide the user with the ability to notify the system that a board is to be either inserted or removed and to identify the location. The controller will use a bus master priority scheme to assume control of the board to board communication. Once the controller has secured communications control, it will provide a signal to either turn on or off the power to the appropriate board location and allow board-to-board communications to proceed.

Each family of computer systems typically have a unique definition of the connector associated with a board location in the system. To implement the live insertion feature, the computer system must support multimaster communications capability. Therefore, the present invention should be specifically designed for each family of computers. The specific computer communications system (bus) currently addressed by the present invention is Multibus II. Multibus II is a reliable backplane system which is well suited for multiprocessing. If one node on the backplane fails, it is usually possible for the remainder of the system to continue

functioning in a diminished capacity. Bus traffic can be rerouted to another available server, pending replacement of the faulty module. The present invention enables live insertion (i.e.- while the power remains on) of faulty boards to be replaced. Downtime will be minimal and users of the system which are currently logged on to the system will be allowed to continue their work without significant disruption. The live insertion feature is implemented through an intelligent slot controller module on the backplane. This circuitry is capable of detecting changes in configuration, safely controlling power, and independently resetting a newly-inserted board. The Multibus system architecture also includes firmware which allows the newly-inserted board to run its own diagnostics and locate a boot server so that the entire process can be fully automated. The present live insertion technique is compatible with the firmware which exists on most Multibus II boards. The interconnect subsystem remains unchanged, and boards which implement the Multibus system architecture will function correctly in a special live insertion backplane.

The foregoing and other objects and advantages will become more apparent when viewed in light of the accompanying drawings and following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic view of an FET used in the present invention;

FIG. 2 is a schematic representation of a slot controller which isolates RST on each board;

FIG. 3 is a schematic representation of a slot controller which isolates RNC on each board;

FIG. 4 is a backplane layout of the present invention;

FIG. 5 is a chart showing the interconnect record for slot control of the present invention;

FIG. 6 is a view of a front panel of an HBI system having LED's and switches;

FIG. 7 is a view of an FET mounting showing power plane connections;

FIG. 8 is a table showing a MULTIBUS II CENTRAL SERVICES MODULE;

FIG. 9 is a schematic representation of a Multibus II Backplane Interconnect Structure;

FIG. 10 is a table showing a Multibus II Central Services Module Connector Specification; and

FIGURE 11 is a table showing a Multibus II Connector Specification.

DESCRIPTION OF PREFERRED EMBODIMENT(S)

Referring now to the drawings, a preferred feature of the present invention is the ability of the backplane resident slot controller to automatically detect the presence of a new board in the system. This is accomplished by isolating one of the ground pins on the backplane and attaching a pull-up resistor to plus five volts. When a board is inserted, the pin will be grounded and this signal becomes the detect line for the slot controller. Redefinition of a ground pin will cause no incapability or reliability problems since there are fourteen other ground pins on the P1 connector alone. Multibus II uses nine pins for plus five volts and two pins each for plus and minus twelve volts, so there is still ample grounding relative to the number of supply pins. The detect signal allows the slot controller to know within a few microseconds that a board has been inserted or removed. Empty card slots are not supplied with power, so it is safe to insert a board in any open position. Once a board has been detected, the slot controller will arbitrate for the bus, wait for existing bus traffic to subside, then power up and reset the new board.

With most commercial backplanes, the insertion of a board into the system while under power can damage the board and disrupt the operation of the system. There are several possible mechanisms for how this can happen. Component

damage can occur if the ground pins and the signal pins are connected before the power pins, then a device will have voltage applied to its I/O pins before a supply voltage is present. Another possibility is that the plus twelve and plus five voltages make contact before the ground pins. This will lead to a shift in ground potential as the by-pass capacitors charge up. The actual voltage on the ground pins will fall somewhere between plus five and plus twelve volts, depending on the ratio of the capacitances. Damage to on board logic can occur quite rapidly since power to these devices will be reversed. This highlights the need for power sequencing, current limiting, and voltage clamping when boards are inserted into a backplane under power. One solution is to control power on a slot-by-slot basis at the backplane.

An ideal device for this application is a power field effect transistor (FET). One embodiment of an FET is shown in FIG. 1. Power FET's are capable of switching up to fifty amps at fifty volts, and are stable over a broad temperature range. One disadvantage of power FET's is that the internal resistance of the device will cause a slight drop in the supply voltage. This affect can be minimized since FET's with .01 ohm internal resistance are now available. FET's can also be connected in parallel to increase their current handling capacity while reducing the voltage drop due to internal resistance.

The Multibus II reset initialization sequence involves writing a card slot ID and an arbitration ID to each slot in the backplane while the RST (reset) signal is held active low preferably for a minimum of fifty msec. When the RST signal is removed, each board will be driving an open collector RSTNC (reset not complete) signal for a period of time preferably not to exceed thirty seconds. The RSTNC signal tells other bus agents that there are boards in the system which have not yet completed their power-on testing sequence. When a new board is inserted into a system which is already running, the problem becomes how to assign a valid card slot and arbitration ID to the newly inserted board without forcing other boards into a reset cycle. The solution is to connect independent RST and RSTNC lines to each slot in the backplane and gather them at the P2 connector of one of the boards in the system. This module would serve as a "slot controller" as shown in FIG. 4. The slot controller is also responsible for the FET power controls and the front panel LED's which help guide the operator through a live insertion or removal sequence.

Selective reset works because agents which actually receive the RST signal are receptive to receiving a new arbitration and slot ID. The RST line is isolated from other boards in the system, and they will ignore the reset event, provided there are no other transactions pending on the system bus. The RSTNC signal must also be isolated for each

board because other agents will not resume bus traffic until this line is cleared.

The RST signal is unidirectional (input only) so it may be controlled with a tristate gate or AND gate. RSTNC is bi-directional and therefore much more difficult to control. Various solutions such as relays and FET's have been suggested, but in the preferred embodiment of the present invention analog switches are used. These devices act as interruptable bi-directional lines, however the DC output current is only twenty five m-A much less than the IEEE 1296 specified 60 m-AP. Since the RSTNC signal is no longer bussed, much lighter termination can be used rather than 330 over 220 as is currently specified for RSTNC termination. To reduce pin out requirements of the slot controller, the RST and RNC signals can be combined on a per slot basis. Both pins will be isolated when a live insertion sequence takes place and this board is not selected. FIG's. 2 and 3 show the recommended circuitry for control of RST and RNC for each slot.

As the new board enters the backplane, there will be a small amount of stray capacitance on each of the signal lines (about 20 pf) whether the board is under power or not. If there is active bus traffic while the board is being inserted, there is a possibility of introducing bus errors due to capacitative effects. When a board is inserted or removed, it may glitch the signal lines when power is

disconnected by the FET device, because it is not possible to guarantee the state of the bus transceivers and control lines until operating voltages have stabilized. Ideally, there should be no bus traffic allowed until the new board has completed power on initialization.

The Multibus II arbitration scheme provides a mechanism of insuring the bus is inactive. Under normal operation, a board signals its desire to use the bus by activating an open collector bus request line (BREQ). If more than one request occurs in the same bus cycle, the agent with the higher arbitration ID number wins, and the other agents must wait their turn. Note that because of the principle of fairness, no new arbitration requests can be issued until the bus request line is clear. The slot controller takes advantage of this fact by holding down BREQ as if it were a low priority requesting agent. The slot controller monitors the system control lines until at least two cycles have passed with no bus traffic. This indicates that all existing arbitration requests have been honored, and that the bus will be quiet as long as the slot controller holds BREQ. This works unless the high priority mode of arbitration is used. High priority allows an agent to drive BREQ any time it wants -- potentially in the middle of a live insertion sequence. Fortunately, there is a hardware mechanism which can be used to eliminate (and cancel) all existing bus arbitration requests. The BUSERR line is an open collector bus error

signal which is normally driven by the parity checkers on each board. The effect of a BUSERR is that all boards must remove their arbitration requests from the bus and suspend all activity until the BUSERR is cleared. Once BUSERR is removed, agents can resume arbitration and continue with normal operations. It is preferred to request the bus first using BREQ then after getting the bus grant, drive BUSERR until the live insertion sequence is completed.

In an actual application, a service technician would identify which board has failed by running diagnostics. The service technician would press a momentary contact switch to warn the system that the bus must be cleared. The replacement board is inserted or a failed board is removed and the slot controller automatically restarts bus traffic. System downtime could be as short as five seconds or less from a user's perspective. In another embodiment of the present invention, individual on/off switches could be placed at each slot. Signal lines only glitch when they undergo a power transition. The slot controller arbitrates, and gains control of the bus, then power cycles the selected board. This technique is different from the above method in that a board can be placed into any empty slot and it won't turn on until the power switch for that slot is enabled. Likewise, a board can be powered off while the system is running and remain in the card cage until it is removed some time later.

System downtime using this technique could potentially be as little as fifty Msec which is the minimum reset duration.

In one embodiment of the present invention, a full sized Multibus II board was used along with forty six TTL packages. A large gate array or EPLD (erasable programmable logic device) was selected as a cost effective device to control a large number of lines with component count. With the present invention existing computer systems can be retrofit for live insertion by replacing the backplane(s) with a backplane modified as above.

The slot controller is programmed by writing control information to registers and interconnect address space. Only five bytes are needed for a slot address. A second register is used to indicate whether this is an insertion or removal and to indicate system status. This is shown in FIG. 5. For board insertions, it is not necessary to program the slot controller registers, all functions will be handled automatically. Likewise, removals can be done automatically, but the system needs some warning so that the bus can be cleared of traffic. This warning could come from a single systemwide momentary contact switch, or from an interconnect command to power cycle a board. Removal of boards without warning the system should be avoided, but at worst will only cause a BUSERR.

To initiate an HBI event, a system programmer first writes the slot address to interconnect, followed by a

controlled byte to differentiate between insertion or removal and to start the process. An HBI error is signalled if both the removal and insertion bits are set, or if you request removal from an empty slot or insertion in a slot which is currently occupied. An HBI error will also be signalled if an illegal slot number is entered or if you attempt to insert or remove a board in slot 0.

Suggested console commands for initiating a sequence of events which enable board removal and insertion are:

```
Insert (slot number)
     Board Found
     Passed Diagnostics
     Booting
     Complete

Remove (slot number)
     Check for Removal
     Complete.
```

Preferably, the front panel of an HBI system will have LED indicators positioned above each of the card slots so that it is very clear which board has been selected. If spacing is a problem, the LED indicators could be located on the slot controller board, but it is preferable that each slot be clearly numbered to prevent operator confusion. FIG. 6 shows an example of a typical front panel layout.

FIG. 7 shows an example of a backplane layout for placement of the FET device. The drain of the FET should be directly connected to the power supply, and the source to the plus five volt power layer of that slot. A zener diode is

shown as protection for the gate of the FET, however this diode is internal on some types of FET's.

The original specifications of Multibus II were designed to isolate the operation of the system bus from local processors at the board level. This is accomplished with the Message Passing Coprocessor (MPC), which manages system bus traffic rates up to 80 Mbytes per second without intervention from the local processor. The MPC also provides a communications path for a local configuration processor called the interconnect controller. The primary purpose of the interconnect controller is to manage the power-up and reset operation of the board, as well as provide configuration data about the board to the CSM. This makes it possible to implement both the hardware and software requirements of Live Insertion Technology, utilizing the capabilities of the interconnect controller.

The interconnect communication for each board are coordinated by the CSM. To support Live Insertion Technology, the CSM must be able to detect the presence of a board in the system, arbitrate for control of the system bus, switch power on or off to a specific slot and initialize new boards in the system. The Multibus II initialization sequence involves writing a card slot ID and an arbitration ID to each slot in the backplane while the RST* (RESET) signal is held active low. When the RST* signal is removed, each board in the system will drive the open collector RSTNC*

(Reset Not Complete) signal for a period of time up to about 30 seconds. All boards in the system release RSTNC* to complete the initialization process. By using individual RST* and RSTNC* signals for each slot, the CSM can control the initialization process of a board on a slot-by-slot basis. This allows a board inserted into a system to be assigned a slot and arbitration ID without disrupting the operation of other boards in the system. (Table 1)

To initiate the live board insertion process, it is necessary to detect a board when it is inserted into the system. (Figure 2) Board detection is accomplished by isolating one of the ground pins (A1) on the backplane and running individual detect lines to this pin for each slot. The CSM will use a pull-up resistor attached to this line to determine when a board ID is present in the system. Up to 20 boards can be configured in Multibus II system, so the CSM can support up to 20 detect lines.

Once a board is inserted into a Multibus II system and detected by the CSM (Figure 3), the CSM arbitrates for the system bus and suspends system bus communications during the period when power is supplied to the board. Each slot in the system must be powered separately to allow the CSM to manage the insertion and removal process. This requires the CSM to manage 20 signals for power control to each slot. (Table 2) The CSM then initiates the RST* sequence and monitors the RSTNC* signal when powered to determine when it is fully

functional. As soon as the RSTNC* signal is released by the new board, it can be integrated into systems operation.

The process of removing a board from the system relies on the CSM to coordinate activities between system operations and the board to be removed. Interconnect communications are used to identify the board to be powered down and to initiate the CSM board removal sequence. The CSM arbitrates for the system bus, turns off power to the board to be removed, and relinquishes control of the system bus once the board is no longer active. A powered down board can then be removed at any time without impacting system operations.

It is thought that the techniques of the present invention and many of its attendant advantages will be understood from the foregoing description. It will be apparent that various changes may be made in the form and construction of the components thereof without departing from the spirit and scope of the invention or sacrificing all of its material advantages. The form of the invention described herein is merely a preferred or exemplary embodiment.

What is Claimed is:

1. A method of inserting a circuit device into a bus network of a computer system having a plurality of powered circuit devices interconnected by a communication bus of said network, said method comprising the steps of: providing a controller having means to notify the system that a circuit device is to be inserted; identifying the location for said circuit device in said system; and inserting said circuit device into a slot in a backplane of said system while said system remains powered.
2. The method of Claim 1, wherein said means to notify is accomplished by isolating a ground pin on said backplane and attaching a pull-up resistor such that when a circuit device is inserted said pin will be grounded thereby providing a detect signal.
3. The method of Claim 1, wherein said circuit device is a printed circuit board.
4. The method of Claim 1, further comprising the step of:

   Controlling power to individual ones of said slots on said backplane.

5. The method of Claim 4, wherein a power field effect transistor (FET) is used to control power to said slots.

6. The method of Claim 1, wherein said bus is Multibus II.

7. The method of Claim 1, wherein said controller is a board of said system having RST and RSTNC lines to each slot in said backplane, gathered at the P2 connector of said board.

8. The method of Claim 7, further comprising the steps of:

Writing a board slot ID and writing an arbitration ID to each slot while an RST signal is held active low; and removing said RST signal.

9. The method of Claim 8, further comprising the steps of:

Requesting said bus through one of said boards activating an open collector bus request line; and driving an open collector bus error line until the live insertion sequence is completed.

10. The method of Claim 1, further comprising the step of:

Providing individual on/off switches at each of said slots.

11. A method of removing a circuit device from a bus network having a plurality of powered circuit devices and said circuit device interconnected by a communication bus of said network, said method comprising the steps of:

Activating a momentary contact switch to warn the system that the bus must be cleared; disconnecting said circuit device from said network; and automatically activating a slot controller to restart bus traffic.

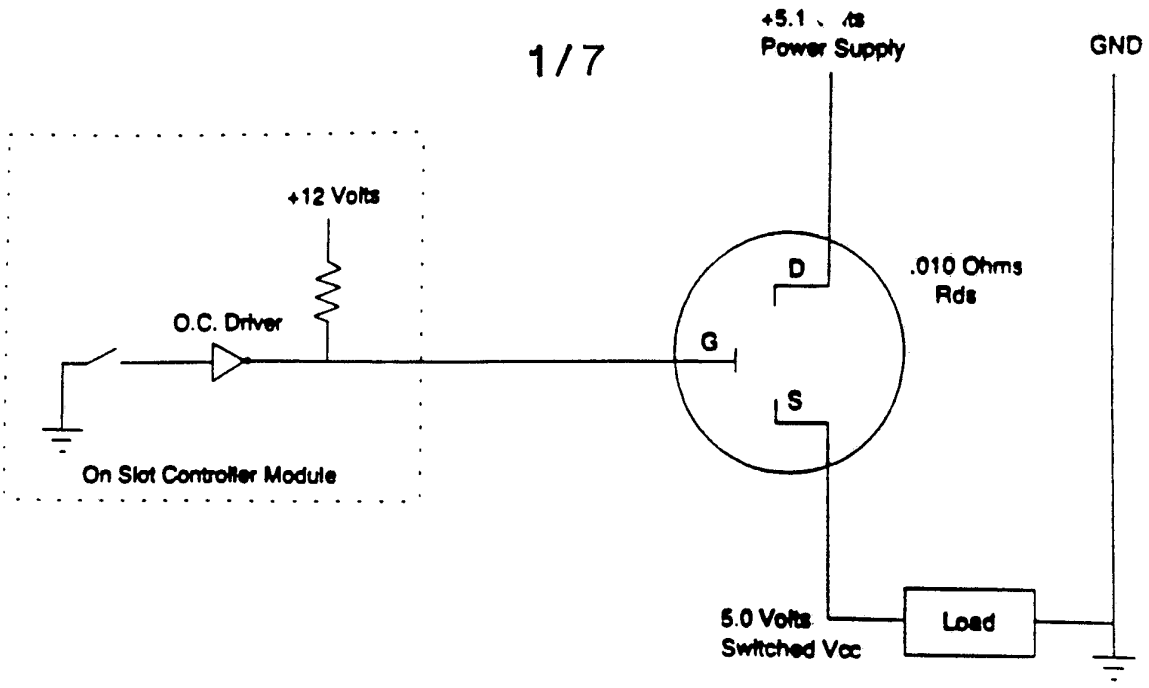
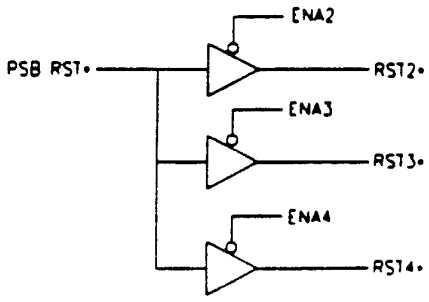
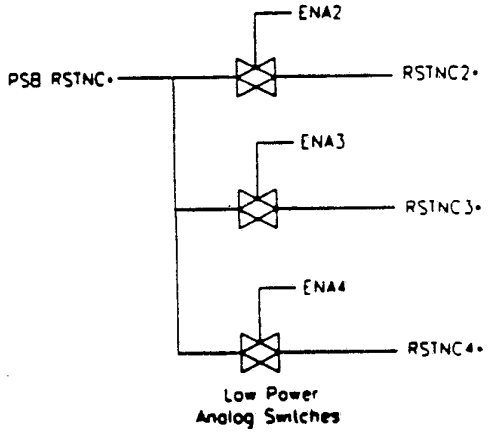


Figure 1



Reset Control Circuit

Figure 2.



RSTNC Control Circuit

Figure 3.

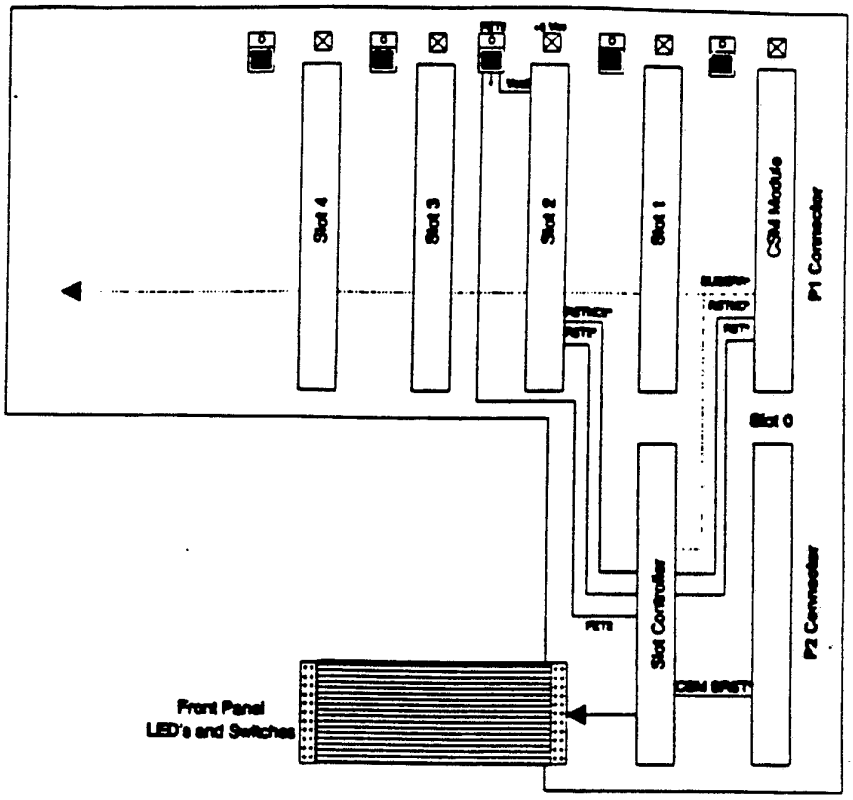


Figure 4.

```
LI Record Type          0 0 1 1 0 0 0 0    Record Type = 30h (48 decimal)
LI Record Length        0 0 0 0 0 1 0 0    Length = 4
LI Slot Address         0 0 0 x x x x x    5 bit slot address
LI Status/Control       0 0 0 1 1 1 1 0
                        | | | | | | | |_ Programming Error = 1 (read only)
                        | | | | | | |___ Board detected    = 1 (read only)
                        | | | | | |_____FET On             = 1
                        | | | | |_______RST Connected     = 1
                        | | | |_________RSTNC Connected   = 1
Default values assume   | | |___________RSTNC Active      = 1
board is installed in   | |_____________Remove this board = 1
this slot.              |_______________Insert this board = 1
```

Interconnect Record for Slot Control

Figure 5.

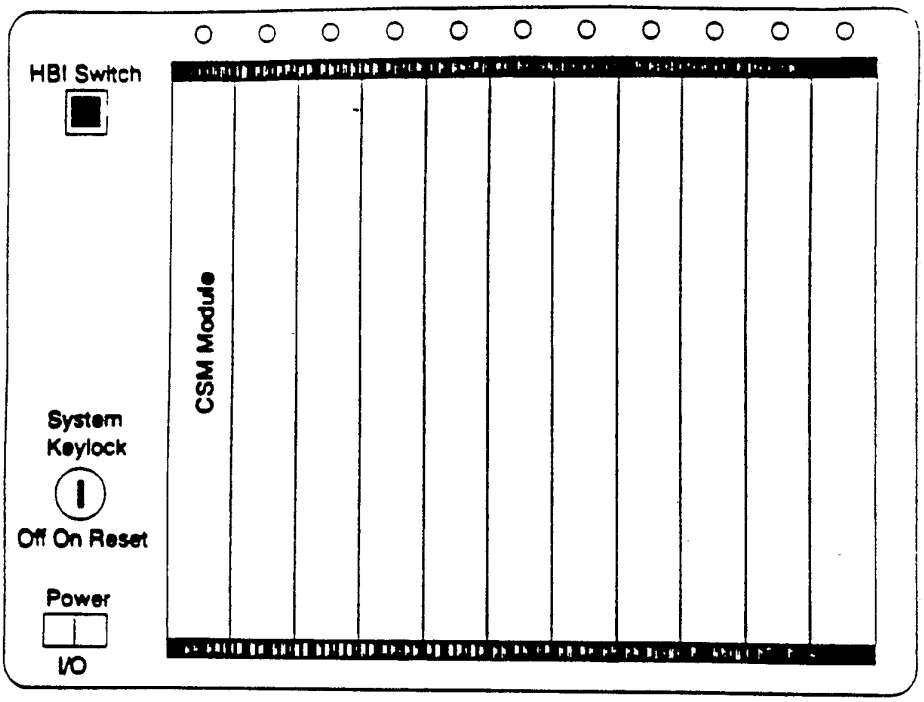


Figura 6.

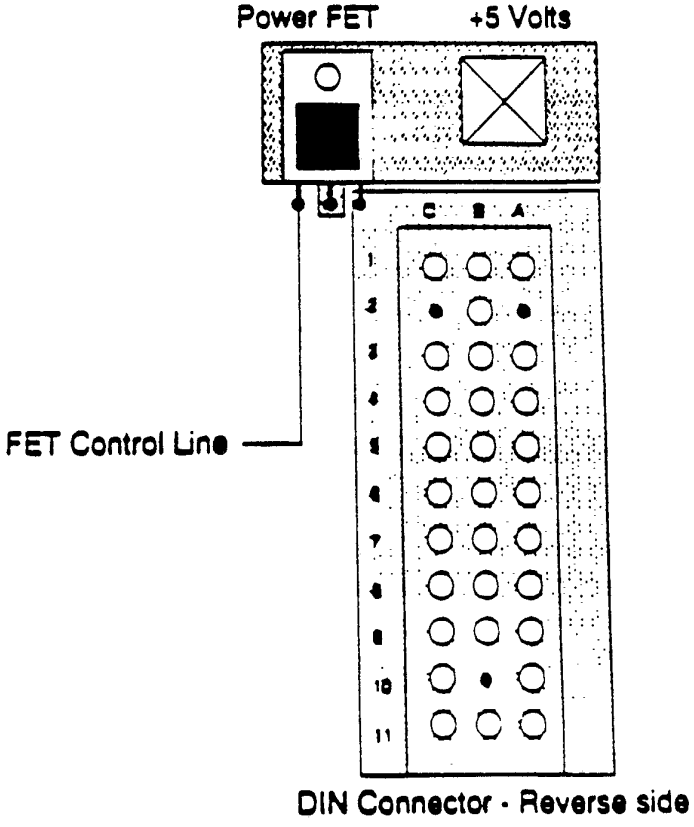


Figura 7

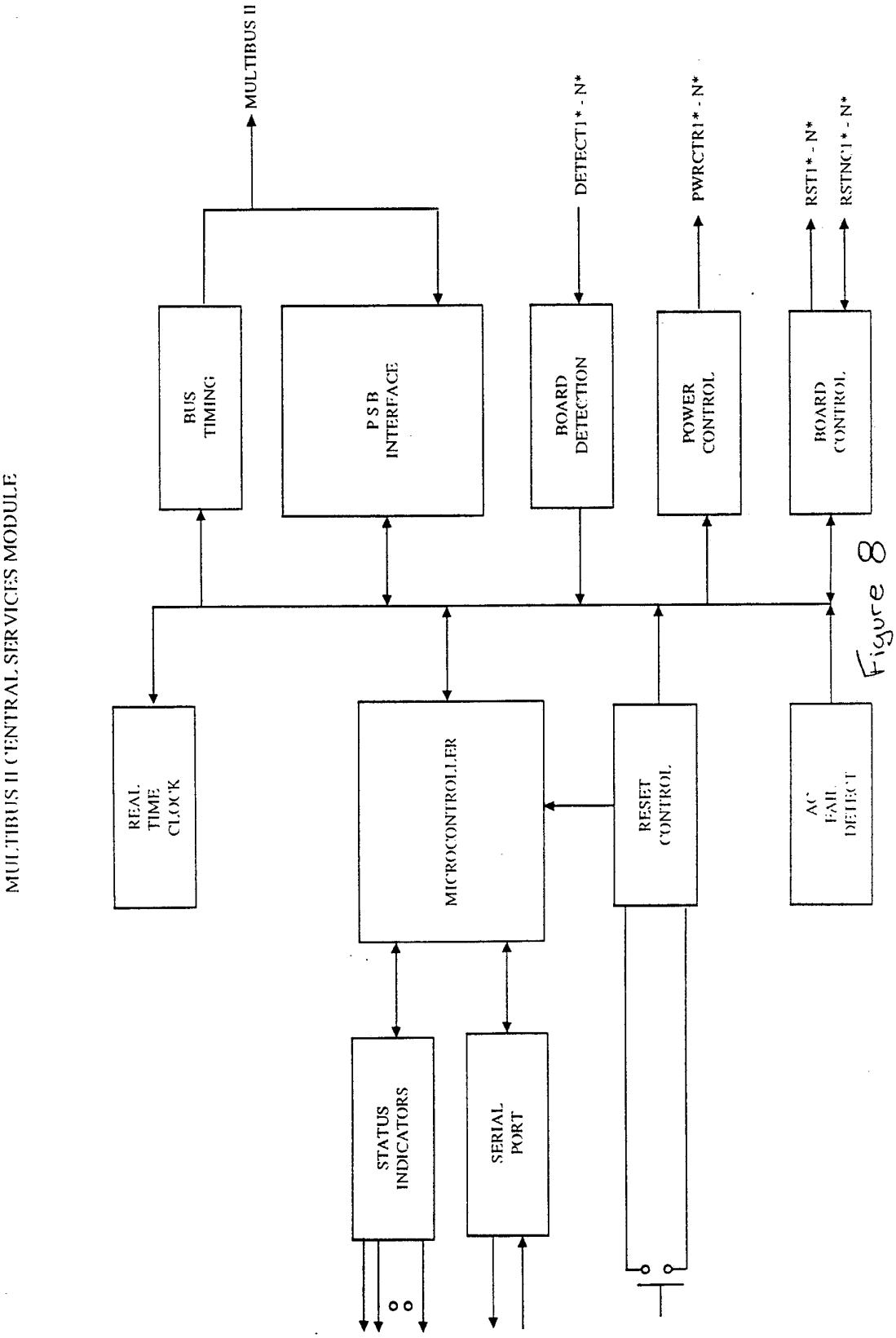

MULTIBUS II CENTRAL SERVICES MODULE
MULTIBUS II
DETECT1* - N*
PWRCTR1* - N*
RST1* - N*
RSTNC1* - N*
BUS TIMING
P S B INTERFACE
BOARD DETECTION
POWER CONTROL
BOARD CONTROL
REAL TIME CLOCK
MICROCONTROLLER
RESET CONTROL
AC FAIL DETECT
STATUS INDICATORS
SERIAL PORT

Figure 8

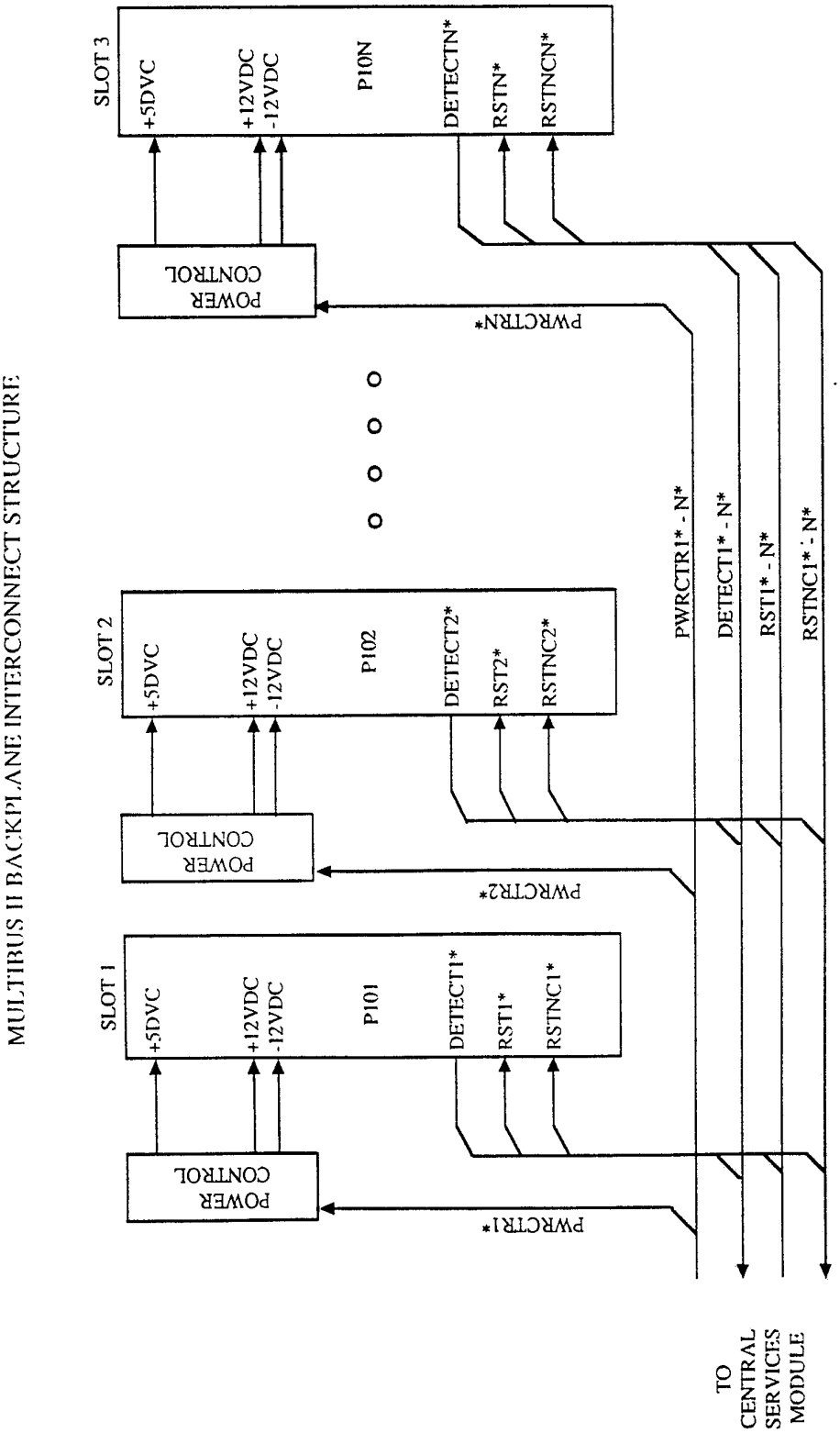

MULTIBUS II BACKPLANE INTERCONNECT STRUCTURE
SLOT 3
+5DVC
+12VDC
-12VDC
P10N
DETECTN*
RSTN*
RSTNCN*
POWER CONTROL
PWRCTRN*
SLOT 2
+5DVC
+12VDC
-12VDC
P102
DETECT2*
RST2*
RSTNC2*
POWER CONTROL
PWRCTR2*
SLOT 1
+5DVC
+12VDC
-12VDC
P101
DETECT1*
RST1*
RSTNC1*
POWER CONTROL
PWRCTR1*
PWRCTR1* - N*
DETECT1* - N*
RST1* - N*
RSTNC1* - N*
TO CENTRAL SERVICES MODULE

Figure 9

MULTIBUS II CENTRAL SERVICES MODULE CONNECTOR SPECIFICATION

P1 SPECIFICATIONS

Pin Number	Row A	Row B	Row C
1		PROT*	0 Volts
2		DCLOW*	
3		+5 Battery	
4		SDA	
5	TIMOUT*	SDB	0 Volts
6		0 Volts	
7	AD00*	AD01*	0 Volts
8	AD02*	0 Volts	AD03*
9	AD04*	AD05*	AD06*
10	AD07*		PAR0*
11	AD08*	AD09*	AD10*
12	AD11*		AD12*
13	AD13*	AD14*	AD15*
14	PAR1*	0 Volts	AD16*
15	AD17*	AD18*	AD19*
16	AD20*	0 Volts	AD21*
17	AD22*	AD23*	PAR2*
18	AD24*	0 Volts	AD25*
19	AD26*	AD27*	AD28*
20	AD29*	0 Volts	AD30*
21	AD31*	Reserved	PAR3*
22			Reserved
23	BREQ*		BUSERR*
24	ARB5*		ARB4*
25	ARB3*		ARB2*
26	ARB1*	0 Volts	ARB0*
27	SC9*	SC8*	SC7*
28	SC6*	0 Volts	SC5*
29	SC4*	SC3*	SC2*
30			
31		SC1*	
32	0 Volts	SC0*	0 Volts

P2 SPECIFICATIONS

Pin Number	Row A	Row B	Row C
1	DETECT1*	DETECT2*	DETECT3*
2	DETECT4*	DETECT5*	DETECT6*
3	DETECT7*	DETECT8*	DETECT9*
4	DETECT10*	DETECT11*	DETECT12*
5	DETECT13*	DETECT14*	DETECT15*
6	DETECT16*	DETECT17*	DETECT18*
7	DETECT19*	DETECT20*	+5 Volts
8	BCLK1*	BCLK2*	BCLK3*
9	RSTNC1*	RSTNC2*	RSTNC3*
10	RSTNC4*	RSTNC5*	RSTNC6*
11	RSTNC7*	RSTNC8*	RSTNC9*
12	RSTNC10*	RSTNC11*	RSTNC12*
13	RSTNC13*	RSTNC14*	RSTNC15*
14	RSTNC16*	RSTNC17*	RSTNC18*
15	RSTNC19*	RSTNC20*	+5 volts
16	BLCK4*	BCLK5*	BCLK6*
17	RST1*	RST2*	RST3*
18	RST4*	RST5*	RST6*
19	RST7*	RST8*	RST9*
20	RST10*	RST11*	RST12*
21	RST13*	RST14*	RST15*
22	RST16*	RST17*	RST18*
23	RST19*	RST20*	+12 volts
24	BCLK7*	BCLK8*	BCLK9*
25	PWRCTR1*	PWRCTR2*	PWRCTR3*
26	PWRCTR4*	PWRCTR5*	PWRCTR6*
27	PWRCTR7*	PWRCTR8*	PWRCTR9*
28	PWRCTR10*	PWRCTR11*	PWRCTR12*
29	PWRCTR13*	PWRCTR14*	PWRCTR15*
30	PWRCTR16*	PWRCTR17*	PWRCTR18*
31	PWRCTR19*	PWRCTR20*	-12 volts
32	BCLK10*	CCLK1*	CCLK2*

Figure 10

MULTIBUS II CONNECTOR SPECIFICATION

CURRENT P1 SPECIFICATIONS

Pin Number	Row A	Row B	Row C
1	0 Volts	PROT*	0 Volts
2	+5 Volts	DCLOW*	+5 Volts
3	+12 Volts	+5 Battery	+12 Volts
4	0 Volts	SDA	BCLK*
5	TIMOUT*	SDB	0 Volts
6	LACHn*	0 Volts	CCLK*
7	AD00*	AD01*	0 Volts
8	AD02*	0 Volts	AD03*
9	AD04*	AD05*	AD06*
10	AD07*	+5 Volts	PAR0*
11	AD08*	AD09*	AD10*
12	AD11*	+5 Volts	AD12*
13	AD13*	AD14*	AD15*
14	PAR1*	0 Volts	AD16*
15	AD17*	AD18*	AD19*
16	AD20*	0 Volts	AD21*
17	AD22*	AD23*	PAR2*
18	AD24*	0 Volts	AD25*
19	AD26*	AD27*	AD28*
20	AD29*	0 Volts	AD30*
21	AD31*	Reserved	PAR3*
22	+5 Volts	+5 Volts	Reserved
23	BREQ*	RST*	BUSERR*
24	ARB5*	+5 Volts	ARB4*
25	ARB3*	RSTNC*	ARB2*
26	ARB1*	0 Volts	ARB0*
27	SC9*	SC8*	SC7*
28	SC6*	0 Volts	SC5*
29	SC4*	SC3*	SC2*
30	-12 Volts	+5 Battery	-12 Volts
31	+5 Volts	SC1*	+5 Volts
32	0 Volts	SC0*	0 Volts

PROPOSED P1 SPECIFICATIONS

Pin Number	Row A	Row B	Row C
1	**DETECTN***	PR0T*	0 Volts
2	+5 Volts	DCL0W*	+5 Volts
3	+12 Volts	+5 Battery	+12 Volts
4	0 Volts	SDA	BCLK*
5	TIMOUT*	SDB	0 Volts
6	LACHn*	0 Volts	CCLK*
7	AD00*	AD01*	0 Volts
8	AD02*	0 Volts	AD03*
9	AD04*	AD05*	AD06*
10	AD07*	+5 Volts	PAR0*
11	AD08*	AD09*	AD10*
12	AD11*	+5 Volts	AD12*
13	AD13*	AD14*	AD15*
14	PAR1*	0 Volts	AD16*
15	AD17*	AD18*	AD19*
16	AD20*	0 Volts	AD21*
17	AD22*	AD23*	PAR2*
18	AD24*	0 Volts	AD25*
19	AD26*	AD27*	AD28*
20	AD29*	0 Volts	AD30*
21	AD31*	Reserved	PAR3*
22	+5 Volts	+5 Volts	Reserved
23	BREQ*	**RSTN***	BUSERR*
24	ARB5*	+5 Volts	ARB4*
25	ARB3*	**RSTNCN***	ARB2*
26	ARB1*	0 Volts	ARB0*
27	SC9*	SC8*	SC7*
28	SC6*	0 Volts	SC5*
29	SC4*	SC3*	SC2*
30	-12 Volts	+5 Battery	-12 Volts
31	+5 Volts	SC1*	+5 Volts
32	0 Volts	SC0*	0 Volts

Figure 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/01051

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :G06F 11/00
US CL :395/575
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/575 395/575,750; 364/231.31,935.4

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Please See Extra Sheet.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	"An Introduction To Operating Systems" Second Edition by Harvey M. Deitel 1990 by Addison-Wesley Publishing Company, Inc. pp. 536.	1-11
Y	"Computer Architecture And Organization" Second Edition by John P. Hayes 1988 by McGraw-Hill Inc. pp. 484-491.	1-11
A	US,A, 4,750,136 (Arpin et al.) 07 June 1988 See Col. 8, lines 17-62.	1-11
A	US,A, 4,835,737 (Herrig et al.) 30 May 1989 See Col. 3, lines 23-50.	1-11

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 11 MARCH 1993	Date of mailing of the international search report 19 APR 1993
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. NOT APPLICABLE	Authorized officer Debbie Wilder VINCENT CANNEY Telephone No. (703) 305-9682

Form PCT/ISA/210 (second sheet)(July 1992)★

B. FIELDS SEARCHED
Electronic data bases consulted (Name of data base and where practicable terms used):

APS L1 S(BOZRO? (5A) REMOVE?)
L2 S(POWER AND RESET)
L3 S L1 & L2
L4 S(INSERT? OR INSTALL?) AND SLOT
L5 S L3 & L4