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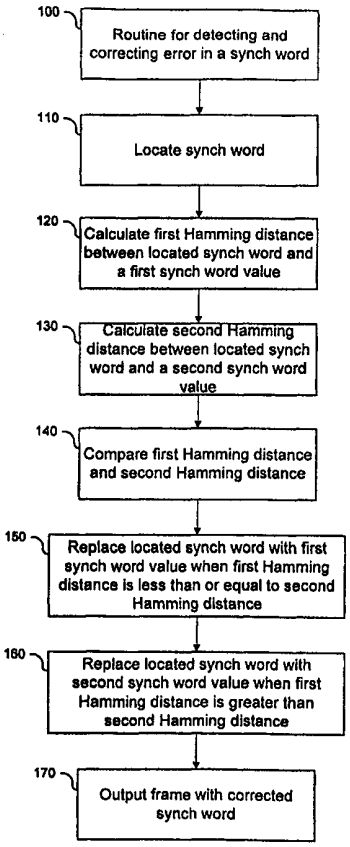
(54) Title: METHOD, SYSTEM, AND COMPUTER PROGRAM PRODUCT FOR ERROR DETECTION AND CORRECTION IN A SYNCHRONIZATION WORD

(57) Abstract

A method, system, and computer program product detects and corrects error in a synchronization (synch) word. At least one bit error in a synch word is detected and corrected prior to correcting bit errors in a frame. In one embodiment, bit errors in a synch word are detected by locating a synch word in data. A first Hamming distance between the located synch word and a first synch word value is calculated. A second Hamming distance between the located synch word and a second synch word value is also calculated. Next, the calculated first and second Hamming distances are compared to detect which of the first and second synch word values are the correct synch word value. In one example, the first and second Hamming distances represent counts of the number of bit errors between the located synch word and the first and second synch word values, respectively. The first and second synch word values are binary complements to maximize accuracy. Detected synch word error is corrected by replacing the located synch word with the first synch word value in the received frame when the first Hamming Distance is less than or equal to the second Hamming distance. Otherwise, the located synch word is replaced with the second synch word value when the first Hamming Distance is greater than the second Hamming distance. In one example implementation, the present invention is included in a receiver including, but not limited to, a Digital Video Broadcast (DVB) receiver that receives data from a satellite or cable.



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Method, System, and Computer Program Product for Error Detection and Correction in a Synchronization Word

Background of the Invention

Field of the Invention

The present invention pertains to the field of data reception. In particular, the present invention relates to error correction of synchronization words.

Related Art

Data communication is used in a wide variety of applications. Data is transferred between locations in a stream of frames, also called packets. The format and content of a frame can vary depending upon a particular application. Frames can have a fixed or variable length. Each frame often has a synchronization (synch) field and/or a payload field. Synch fields include recognizable words or bit patterns that enable a receiver to detect and synch up with data sent in a stream of frames. The payload field carries the data being communicated. Synch words and payload data are encoded in a secure transmission.

In a wireless or cable broadcast, data is sent from a transmitter in frames. A receiver receives the frames. Satellites or other intermediate network stations relay frames between the transmitter and receiver. A synch word is sent in a predetermined synch pattern over one or more frames. A receiver decodes the frames and extracts the synch words. Communication and data transfer is initiated once a synch pattern has been detected.

For example, the Digital Video Broadcast - Satellite (DVB-S) standard uses eight frames (synch frames) to synchronize a receiver. The value of the

synch word is predetermined and in the current DVB-S standard is equal to 47 in hexadecimal notation, that is, 10000111 in binary form. A synch word is sent in seven consecutive frames. The complement of the synch word (B8 in hexadecimal) is sent in an eighth frame. A receiver detects and verifies the synch pattern of frames (seven synch frames with a 47hex synch word value followed by an eighth synch frame with a B8hex synch word value).

Error correction is often provided in receivers to ensure high data integrity and reliable communication. Errors can be corrected anywhere in a frame including the synch word. However, the maximum number of bytes which can be corrected in a frame is limited in certain applications. For example, the DVB-S standard limits the required error correction of a Reed-Solomon decoder to only eight bytes of errors per frame. If an error occurs in one byte of the sync word, the Reed-Solomon decoder can only correct a maximum of seven bytes in the rest of a frame.

As recognized by the inventor, error in a synch word needs to be detected and corrected separate from error detection and correction in the rest of a frame. In this way, a maximum number of bytes can be corrected for the remaining data in a frame other than the synch word.

Summary of the Invention

The present invention provides a method, system, and computer program product for detecting and correcting error in a synch word. At least one bit error in a synch word is detected and corrected prior to correcting bit errors in a frame.

In one embodiment, bit errors in a synch word are detected by locating a synch word in digital data. A first Hamming distance between the located synch word and a first synch word value is calculated. A second Hamming distance between the located synch word and a second synch word value is also calculated.

Next, the calculated first and second Hamming distances are compared to detect which of the first and second synch word values are the correct synch word value. In one example, the first and second Hamming distances represent counts of the number of bit errors between the located synch word and the first and second synch word values, respectively. The first and second synch word values are binary complements to maximize accuracy.

Detected synch word error is corrected by replacing the located synch word with the first synch word value in the received frame when the first Hamming Distance is less than or equal to the second Hamming distance. Otherwise, the located synch word is replaced with the second synch word value when the first Hamming Distance is greater than the second Hamming distance.

In one example implementation, the present invention is included in a receiver including, but not limited to, a Digital Video Broadcast (DVB) receiver that receives data from a satellite and/or cable transmission. The receiver includes a deinterleaver, a synch word detection and correction module, and a decoder. The synch word detection and correction module is coupled between the deinterleaver and the decoder such that bit errors in a synch word in a frame output from the deinterleaver are corrected prior to decoding of data in the frame by the decoder. In one application, the decoder is a Reed-Solomon decoder.

Further embodiments, features, and advantages of the present inventions, as well as the structure and operation of the various embodiments of the present invention, are described in detail below with reference to the accompanying drawings.

Brief Description of the Figures

The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate the present invention and, together with the description, further serve to explain the principles of the invention and to enable a person skilled in the pertinent art to make and use the invention.

In the drawings:

FIG. 1 is a flowchart of a routine for detecting and correcting error according to an embodiment of the present invention.

FIG. 2 is a block diagram of an example of the present invention implemented primarily in hardware in a DVB-S compliant receiver.

FIG. 3 is an example computer system and computer program product in which the present invention is implemented primarily in software.

FIGs. 4A, 4B, and 4C are block diagrams of an example DVB-compliant receiver that incorporates synch word error detection and correction according to the present invention.

FIG. 5 is an example timing diagram of a received serial frame data stream.

The present invention will now be described with reference to the accompanying drawings. In the drawings, like reference numbers indicate identical or functionally similar elements. Additionally, the left-most digit(s) of a reference number identifies the drawing in which the reference number first appears.

Detailed Description of the Preferred Embodiments

I. Overview and Discussion

The present invention provides a method, system, and computer program product for detecting and correcting bit error in a synch word. Error correction and detection in a synch word is performed prior to error detection and correction in the rest of a frame. In this way, a decoder need not correct bit errors in a synch word. A decoder can correct a maximum number of bit errors in remaining frame data, such as, payload data. In general, the present invention can be applied to any type of data having at least one known synch word value.

The present invention is described in terms of a receiver environment where a low bit error rate is desired. In one embodiment, error correction and detection in the synch word is performed in a satellite and/or cable receiver after received frames or packets have passed through a demodulator, Viterbi decoder, and deinterleaver, and prior to being sent to a Reed-Solomon decoder. In one example, the present invention is used as an addition to a Direct Video Broadcast (DVB) receiver that complies with the Digital Video Broadcast - Satellite (DVB-S) standard for satellite data transmission and/or the Digital Video Broadcast - Cable (DVB-C) standard for cable data transmission. An example implementation of a DVB receiver that includes synch word error detection and correction is described further below with respect to FIGs. 4A to 4C and 5.

The present invention is described in terms of this example receiver environment. However, the present invention can be used in any data receiver or processor where the value of one or more synch words is known, as would be apparent to a person skilled in the art given this description. For example, the present invention can be used in a receiver in a Very Small Aperture Terminal (VSAT), a satellite or cable receiver compliant with standards other than DVB,

a broadcast receiver, or any data receiver that receives voice, video, multimedia, digital information, or other data.

Description in these terms is provided for convenience only. It is not intended that the invention be limited to application in these example environments. In fact, after reading the following description, it will become apparent to a person skilled in the relevant art how to implement the invention in alternative environments known now or developed in the future.

II. Terminology

To more clearly delineate the present invention, an effort is made throughout the specification to adhere to the following term definitions as consistently as possible.

The terms "synchronization word," "synch word," and "synch" are used interchangeably to refer to any number of bits that are used by a receiver to synchronize communication or read out of data from a frame.

"Frame" refers to any fixed or variable length block of data. A frame can include, but is not limited to, carrying a synch word field and/or a payload field. A frame is also referred to as a packet.

"Data" carried in a frame refers to any type of digital or analog data, and can include, but is not limited to, binary data or bits. "Data" can be voice, video, multimedia, digital information, or other data.

III. Error Detection and Correction in a Synch Word

FIG. 1 shows a routine 100 for detecting and correcting error in a synch word according to an embodiment of the present invention. First, a synch word is located (step 110). For example, data from a deinterleaver can be monitored to locate a synch word.

Next, a first Hamming distance between the located synch word and a first synch word value is calculated (step 120). A second Hamming distance between the located synch word and a second synch word value is also calculated (step 130). In steps 120 and 130, the Hamming distance calculated is simply a count of the number of bits which are different between the located synch word and the first and second synch word values respectively. To further ensure accuracy, the second synch word value is the bit-complement of the first synch word value. The first and second synch word values are predetermined. In one example, these first and second synch word values are pre-stored in a register or other storage device. The present invention is not so limited and bit or byte error detection techniques other than calculating Hamming distance can be used.

The calculated first Hamming distance and second Hamming distance are compared (step 140). The located synch word is replaced with a first synch word value when the first Hamming Distance is less than or equal to the second Hamming distance (step 150). The located synch word is replaced with a second synch word value when the first Hamming Distance is greater than the second Hamming distance (step 160). Steps 150 and 160 then ensure that a corrected synch word is substituted in a frame for the located synch word value when the located synch word value has a bit error. The corrected synch word has either the first synch word value or the second synch word value.

A frame of data including the corrected synch word is then output for further processing in a receiver (step 170). For example, the frame of data can be sent to a Reed-Solomon decoder. Because the synch word has already been corrected, the maximum number of bytes which can be corrected by the Reed-Solomon decoder can be corrected in the remaining frame apart from the synch word.

Routine 100 and each of its constituent steps 110-160 can be implemented in hardware, firmware, software, and any combination thereof. FIG. 2 is a block diagram of an example of the present invention implemented primarily in

hardware in a DVB-S compliant receiver. FIG. 3 is an example computer system in which the present invention is implemented primarily in software.

FIG. 2 shows an error detection and correction system 200 according to an example hardware implementation of the present invention. System 200 is coupled between a deinterleaver (not shown) and a decoder (not shown). Any type of conventional deinterleaver and decoder can be used. In one example where Reed-Solomon encoding and decoding is used in a satellite receiver, system 200 is coupled between a periodic (also called convolutional) deinterleaver and a Reed-Solomon decoder. See, e.g., the convolution deinterleaver described by Forney, Jr., "Burst-Correcting Codes for the Classic Bursty Channel," *I.E.E.E. Trans. on Comm. Tech.*, vol. com-19, no. 5, October 1971 (incorporated in its entirety herein by reference). A modified Ramsey type II deinterleaver can also be used. A Reed-Solomon decoder such as the AWT1001 Reed-Solomon Codec Core sold by Advanced Wireless Technologies, Inc., can be used.

System 200 includes a synch word locator 210, first Hamming distance calculator 220, second Hamming distance calculator 230, comparator 240, selector 250, sync word corrector 260, delay element 270, and a second selector 280. Synch word locator 210 monitors data from a de-interleaver to locate a synch word.

First Hamming distance calculator unit 220 calculates a first Hamming distance between the located synch word and a first synch word value (47hex). Second Hamming distance calculator 230 calculates a second Hamming distance between the located synch word and a second synch word value (B8hex). The Hamming distance calculated is simply a count of the number of bits which are different between the located synch word and the first or second synch word values. To further ensure accuracy, the second synch word value is the bit-complement of the first synch word value. The present invention is not so limited

and bit or byte error detection techniques other than calculating Hamming distance can be used.

Comparator 240 compares the first Hamming distance and second Hamming distance calculated by the first and second Hamming calculator units 220 and 230. The output of comparator 240 controls the setting of first selector 250. When the first Hamming Distance is less than or equal to the second Hamming distance, output from comparator 240 switches first selector 250 to select the first synch word value (47hex). When the first Hamming Distance is greater than the second Hamming distance, output from comparator 240 switches first selector 250 to select the second synch word value (B8hex). First selector 250 then outputs a corrected synch value (47hex or B8hex) to synch word corrector 260.

Synch word corrector 260 replaces the located synch word output from synch word locator 210 with the corrected synch value output from first selector 250. Delay element 270 delays received frames until processing by system 200 is complete. Once a synch word has been replaced in a delayed frame, synch word corrector 260 switches selector 280 to output the delayed frame with a corrected synch word to a decoder. For example, the delayed frame of data can be sent to a Reed-Solomon decoder. Because the synch word has already been corrected, the maximum number of bytes which can be corrected by the Reed-Solomon decoder can be corrected in the remaining frame apart from the synch word.

An example of a computer system 300 is shown in FIG. 3. The computer system 300 represents any single or multi-processor computer. Single-threaded and multi-threaded computers can be used. Unified or distributed memory systems can be used.

The computer system 300 includes one or more processors, such as processor 304. One or more processors 304 can execute software implementing routine 100 as described above. Each processor 304 is connected to a

communication infrastructure 302 (e.g., a communications bus, cross-bar, or network). Various software embodiments are described in terms of this exemplary computer system. After reading this description, it will become apparent to a person skilled in the relevant art how to implement the invention using other computer systems and/or computer architectures.

Computer system 300 also includes a main memory 308, preferably random access memory (RAM), and can also include a secondary memory 310. The secondary memory 310 can include, for example, a hard disk drive 312 and/or a removable storage drive 314, representing a floppy disk drive, a magnetic tape drive, an optical disk drive, etc. The removable storage drive 314 reads from and/or writes to a removable storage unit 318 in a well known manner. Removable storage unit 318 represents a floppy disk, magnetic tape, optical disk, etc., which is read by and written to by removable storage drive 314. As will be appreciated, the removable storage unit 318 includes a computer usable storage medium having stored therein computer software and/or data.

In alternative embodiments, secondary memory 310 may include other similar means for allowing computer programs or other instructions to be loaded into computer system 300. Such means can include, for example, a removable storage unit 322 and an interface 320. Examples can include a program cartridge and cartridge interface (such as that found in video game devices), a removable memory chip (such as an EPROM, or PROM) and associated socket, and other removable storage units 322 and interfaces 320 which allow software and data to be transferred from the removable storage unit 322 to computer system 300.

Computer system 300 can also include a communications interface 324. Communications interface 324 allows software and data to be transferred between computer system 300 and external devices via communications path 326. Examples of communications interface 324 can include a modem, a network interface (such as Ethernet card), a communications port, etc. Software and data transferred via communications interface 324 are in the form of signals which can

be electronic, electromagnetic, optical or other signals capable of being received by communications interface 324, via communications path 326. Note that communications interface 324 provides a means by which computer system 300 can interface to a network such as the Internet.

The present invention can be implemented using software running (that is, executing) in an environment similar to that described above with respect to FIG. 3. In this document, the term "computer program product" is used to generally refer to removable storage unit 318, a hard disk installed in hard disk drive 312, or a carrier wave carrying software over a communication path 326 (wireless link or cable) to communication interface 324. A computer useable medium can include magnetic media, optical media, or other recordable media, or media that transmits a carrier wave. These computer program products are means for providing software to computer system 300.

Computer programs (also called computer control logic) are stored in main memory 308 and/or secondary memory 310. Computer programs can also be received via communications interface 324. Such computer programs, when executed, enable the computer system 300 to perform the features of the present invention as discussed herein. In particular, the computer programs, when executed, enable the processor 304 to perform the features of the present invention. Accordingly, such computer programs represent controllers of the computer system 300.

In an embodiment where the invention is implemented using software, the software may be stored in a computer program product and loaded into computer system 300 using removable storage drive 314, hard drive 312, or communications interface 324. Alternatively, the computer program product may be downloaded to computer system 300 over communications path 326. The control logic (software), when executed by the one or more processors 304, causes the processor(s) 304 to perform the functions of the invention as described herein.

In another embodiment, the invention is implemented primarily in firmware and/or hardware using, for example, hardware components such as application specific integrated circuits (ASICs). Implementation of a hardware state machine so as to perform the functions described herein will be apparent to persons skilled in the relevant art(s).

IV. Error Detection and Correction of Multiple Synch Word Values

Multiple, different synch word values can also be evaluated. As would be apparent to a person skilled in the art given this description, errors in one or more synch word values can be detected and corrected by using multiple stages of Hamming distance calculators and comparators or other multi-threshold evaluation devices. In particular, a pair of Hamming distance calculators and a comparator is used for each synch word value (and its complement) to be corrected. Thus, single or multiple synch word values in frames of fixed or variable length can be detected and corrected, according to the present invention, as described herein.

V. Example DVB Receiver Implementation

FIGs. 4A to 4C show an example DVB receiver 400 according to a further feature of the present invention. DVB receiver 400 receives data from an antenna 402 and/or a cable 404. The data can be compliant with either the DVB-S or DVB-C standard. FIG. 5 shows an example timing diagram 500 of a received serial frame data stream 510. Data stream 510 includes a frame 505 which is DVB compliant. Frame 505 includes a synch field 506, payload field 507, and Reed-Solomon RS encoding/decoding field 508. In one case, frame 505 has 204 total bytes at eight bits per byte (a one byte synch field 506, a 187 byte payload field 507, and a one byte RS field 508). Frame 505 then has 188 bytes of valid

data indicated by the positive data valid signal 520 and one byte for use in RS decoding indicated by the negative data valid signal 530.

DVB receiver 400 includes a downconverter and analog/digital converter stage 405 and processing block 470. Processing block 470 includes demodulator 410, Viterbi decoder and autosynch unit 420, deinterleaver 430, synch word error detection and correction unit 440, RS decoder 450, and demultiplexer (or descrambler) 460. Data output from DVB receiver 400 can be sent to any number of end user applications and systems 490 including a personal computer, modem, television, video cassette recorder (VCR), audio system, telephone, and/or personal digital assistant. DVB receiver 400 can be a separate unit, such as, as a set-top box, or it can be integrated into any other end user device. Synch word error detection and correction unit 440 detects and corrects bit errors in a synch word (e.g., in synch word 506), according to the present invention, as described above with respect to FIGs. 1 to 3.

In general, downconverter and analog/digital converter stage 405, demodulator 410, Viterbi decoder and autosynch unit 420, deinterleaver 430, RS decoder 450, and demultiplexer (or descrambler) 460 can be assembled or fabricated from any known or conventional components as would be apparent to a person skilled in the art given this description. For example, demodulator 410 can be a binary phase shift keying and/or quadrature phase shift keying (BPSK/QPSK) demodulator that supports baud rates from 2 to 20 Mbps (megabits/sec). An example output data rate can range from 1 to 35 Mbps depending upon the code rate and modulation method used.

FIG. 4B shows an example downconverter and A/D stage 405 that includes an L-band down converter and synthesizer 406. An RF signal in an L-band between 950-2150 Megahertz (MHz) is down converted to baseband in-phase and/or quadrature phase signals. The down converted signal(s) pass through an amplifier 407 and bandpass filter (BPF) 408. BPF 408 has a frequency center (Fc) equal to approximately 480 MHz with a bandwidth B_{IF} at

approximately 32 MHz. A second down converter 409 includes two analog-to-digital converters which provide a lower frequency digital data stream sampled at 50 MHz to the receiver processing block 470. Receiver output from block 470 passes to an optional interface (I/F) unit 482 and BERG connector 484. Optional I/F unit 482 allows byte wide data transfer.

Feedback for automatic gain control passes from block 470 to a low pass filter 411 to second down converter 409 and L-band converter and synthesizer 406. Microcontroller 480 is coupled to control L-band converter and synthesizer 406, block 470, and the optional I/F 482. Microcontroller 480 allows parameters to be set through an interface (such as, a software interface). These parameters include RF center frequency, frequency range to search during acquisition, baud rate, tracking loop bandwidths, code rates, data interface mode, etc.

FIG. 4C shows one example where receiver 400 is implemented on a circuit board coupled to a power supply 498. Block 470 is implemented as an ASIC. End user device 490 includes a user data processing application 492, processor 494, and a power supply 496. Demultiplexer or descrambler 460 passes valid data (synch field 506 and payload field 507) to end user data processing application 492. Other data and clock signals can also be passed.

Microcontroller 480 and processor 494 also communicate. Microcontroller 480 forwards monitor data to processor 494. Processor 494 sends control data to microcontroller 480. Automatic gain control and lock signals also pass from receiver 400 to processor 494. Power supplies 496 and 498 can supply a desired power, such as, a 5V, 12V, 28V, or LNB voltage.

VI. Conclusion

While specific embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. It will be understood by those skilled in the art that

various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined in the appended claims. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

What Is Claimed Is:

1. A method for detecting and correcting bit errors in digital data, comprising the steps of:

(a) locating a synch word in digital data;

(b) calculating a first Hamming distance between the located synch word and a first synch word value;

(c) calculating a second Hamming distance between the located synch word and a second synch word value;

(d) comparing the calculated first and second Hamming distances;

(e) replacing the located synch word with the first synch word value in the received packet when the first Hamming Distance is less than or equal to the second Hamming distance; and

(f) replacing the located synch word with the second synch word value when the first Hamming Distance is greater than the second Hamming distance.

2. The method of claim 1, wherein said steps (a) to (f) are performed prior to Reed-Solomon decoding of the digital data.

3. The method of claim 2, wherein said steps (a) to (f) are performed after the digital data has been deinterleaved into a frame.

4. The method of claim 3, further comprising the step of delaying the deinterleaved frame; and wherein said replacing step (e) replaces the located synch word in the delayed deinterleaved frame with the first synch word value when the first Hamming Distance is less than or equal to the second Hamming distance; and said replacing step (f) replaces the located synch word in the

delayed deinterleaved frame with the second synch word value when the first Hamming Distance is greater than the second Hamming distance.

5. The method of claim 1, wherein said first synch word value and said second word value are binary complements each having the same number of bits, and wherein said step (b) calculates a first Hamming distance equal to a count of the number of bit errors between the located synch word and a first synch word value; and said step (c) calculates a second Hamming distance equal to a count of the number of bit errors between the located synch word and a second synch word value.

6. An error detection and correction system, comprising:

a synch word locator that locates a synch word in digital data;

first and second Hamming distance calculators coupled to said synch word locator; wherein said first Hamming distance calculator calculates and outputs a first output representative of a first Hamming distance between the located synch word and a first synch word value and said second Hamming distance calculator calculates and outputs a second output representative of a second Hamming distance between the located synch word and a second synch word value;

a first comparator coupled to said first and second Hamming distance calculators, said first comparator compares said first and second outputs from said first and second Hamming distance calculators, respectively, and generates a first comparator output; and

a synch word corrector coupled to said first comparator; wherein said synch word corrector replaces the located synch word with the first synch word value in the digital data when the first comparator output indicates the first Hamming Distance is less than or equal to the second Hamming distance and replaces the located synch word with the second synch word value when the first

comparator output indicates the first Hamming Distance is greater than the second Hamming distance.

7. The system of claim 6, further comprising:

a first selector coupled between said first comparator and said synch word corrector, said first selector generates a signal indicating a selection of either said first synch word value or said second synch word value depending upon the value of said first comparator output.

8. The system of claim 6, wherein the digital data comprises a stream of digital data deinterleaved into a frame, and further comprising:

a second selector coupled to said synch word corrector; and

a delay element coupled to said second selector, the delay element stores the deinterleaved frame, and said synch word corrector replaces the located synch word in the delayed deinterleaved frame with the first synch word value when the first Hamming Distance is less than or equal to the second Hamming distance; and replaces the located synch word in the delayed deinterleaved frame with the second synch word value when the first Hamming Distance is greater than the second Hamming distance; whereby the delayed, deinterleaved frame with a corrected synch word value can be output to a Reed-Solomon decoder.

9. The system of claim 6, wherein said first synch word value and said second word value are binary complements each having the same number of bits, and wherein said first Hamming distance calculator calculates a first Hamming distance equal to a count of the number of bit errors between the located synch word and a first synch word value; and said second Hamming distance calculator calculates a second Hamming distance equal to a count of the number of bit errors between the located synch word and a second synch word value.

10. The system of claim 6, wherein said digital data comprises a DVB-S or DVB-C compliant stream of digital data.

11. An error detection and correction system, comprising:

(a) means for locating a synch word in digital data;

(b) means for calculating a first Hamming distance between the located synch word and a first synch word value;

(c) means for calculating a second Hamming distance between the located synch word and a second synch word value;

(d) means for comparing the calculated first and second Hamming distances;

(e) means for replacing the located synch word with the first synch word value in the received packet when the first Hamming Distance is less than or equal to the second Hamming distance; and

(f) means for replacing the located synch word with the second synch word value when the first Hamming Distance is greater than the second Hamming distance.

12. A computer program product comprising a computer useable medium having computer program logic for enabling at least one processor in a computer system to provide error detection and correction, said computer program logic comprising:

means for enabling the at least one processor to locate a synch word in digital data;

means for enabling the at least one processor to calculate a first Hamming distance between the located synch word and a first synch word value;

means for enabling the at least one processor to calculate a second Hamming distance between the located synch word and a second synch word value;

means for enabling the at least one processor to compare the calculated first and second Hamming distances;

means for enabling the at least one processor to replace the located synch word with the first synch word value in the received packet when the first Hamming Distance is less than or equal to the second Hamming distance; and

means for enabling the at least one processor to replace the located synch word with the second synch word value when the first Hamming Distance is greater than the second Hamming distance.

13. A method for detecting and correcting bit errors in digital data, the digital data including a frame with a synch word, the method comprising the steps of:

detecting at least one bit error in a synch word in the digital data; and

correcting the at least one bit error in the synch word prior to correcting bit errors in the frame.

14. The method of claim 13, wherein said detecting step comprises the steps of:

(a) locating a synch word in digital data;

(b) calculating a first Hamming distance between the located synch word and a first synch word value;

(c) calculating a second Hamming distance between the located synch word and a second synch word value; and

(d) comparing the calculated first and second Hamming distances.

15. The method of claim 14, wherein said correcting step comprises the steps of:

(e) replacing the located synch word with the first synch word value in the received packet when the first Hamming Distance is less than or equal to the second Hamming distance; and

(f) replacing the located synch word with the second synch word value when the first Hamming Distance is greater than the second Hamming distance.

16. A receiver comprising:

means for detecting at least one bit error in a synch word in digital data; and

means for correcting the at least one bit error in the synch word prior to correcting bit errors in the frame.

17. A receiver comprising:

a deinterleaver;

a synch word detection and correction module; and

a decoder; wherein, said synch word detection and correction module is coupled between said deinterleaver and said decoder such that bit errors in a synch word in a frame output from the deinterleaver are corrected prior to decoding of data in said frame by said decoder.

18. The receiver of claim 17, wherein said decoder is a Reed-Solomon decoder.

19. The receiver of claim 17, wherein the frame complies with a DVB–S or DVB-C specification.

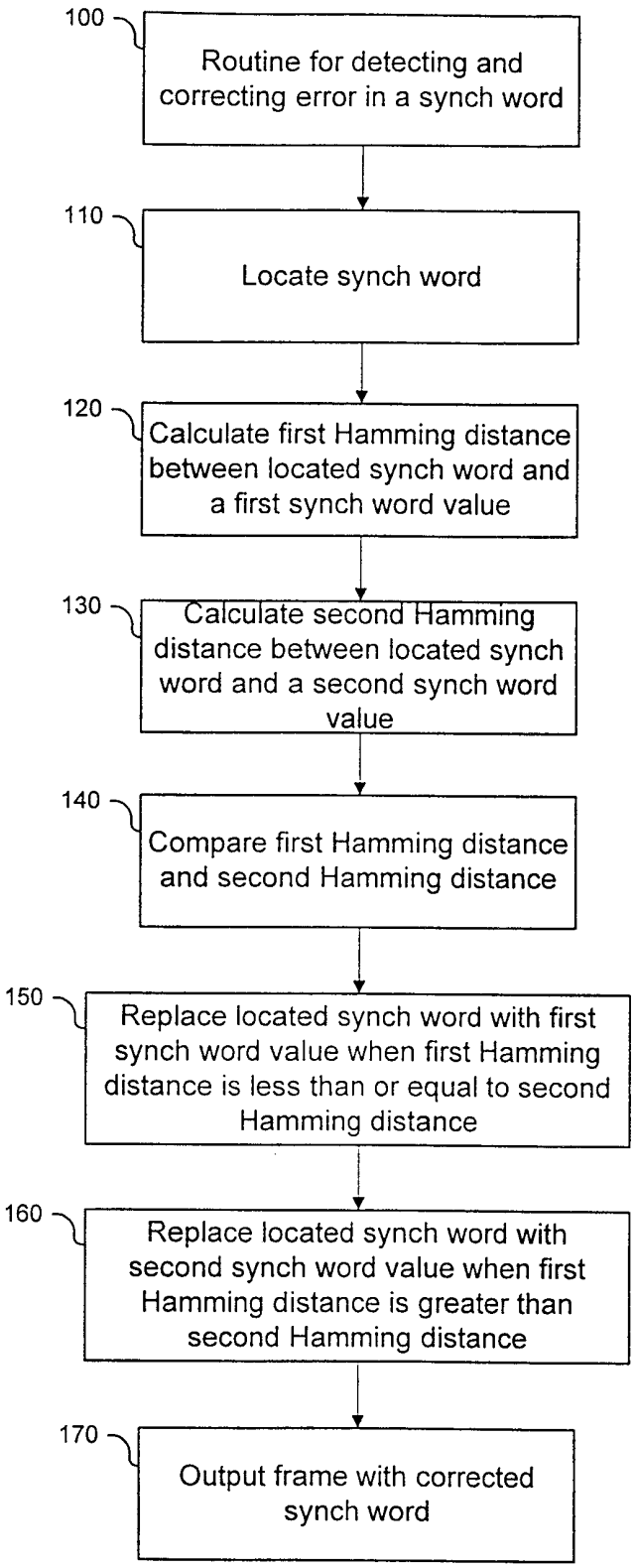
100
Routine for detecting and correcting error in a synch word
110
Locate synch word
120
Calculate first Hamming distance between located synch word and a first synch word value
130
Calculate second Hamming distance between located synch word and a second synch word value
140
Compare first Hamming distance and second Hamming distance
150
Replace located synch word with first synch word value when first Hamming distance is less than or equal to second Hamming distance
160
Replace located synch word with second synch word value when first Hamming distance is greater than second Hamming distance
170
Output frame with corrected synch word

FIG. 1

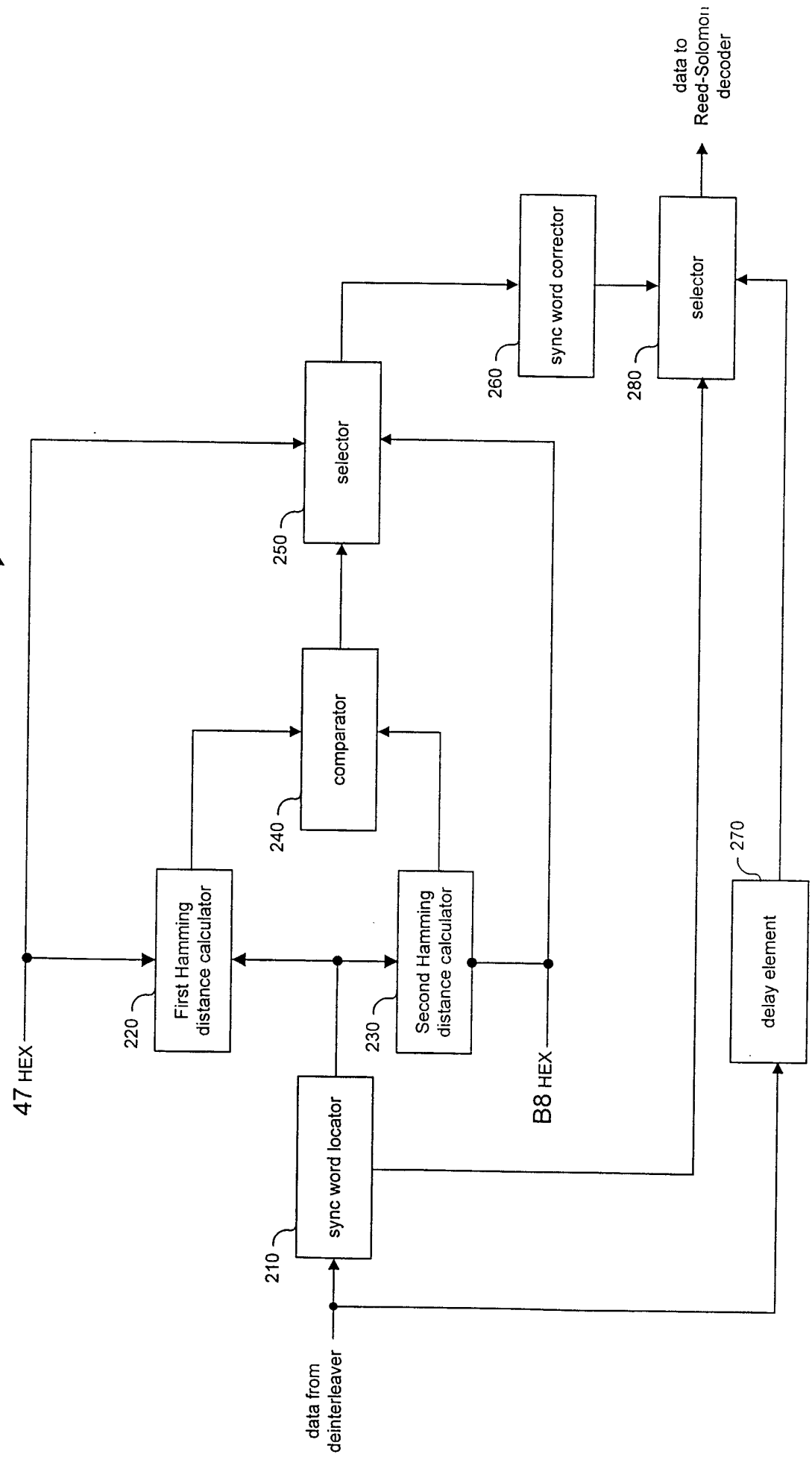
200
data from deinterleaver
sync word locator
210
47 HEX
First Hamming distance calculator
220
B8 HEX
Second Hamming distance calculator
230
comparator
240
selector
250
sync word corrector
260
selector
280
delay element
270
data to Reed-Solomon decoder

FIG. 2

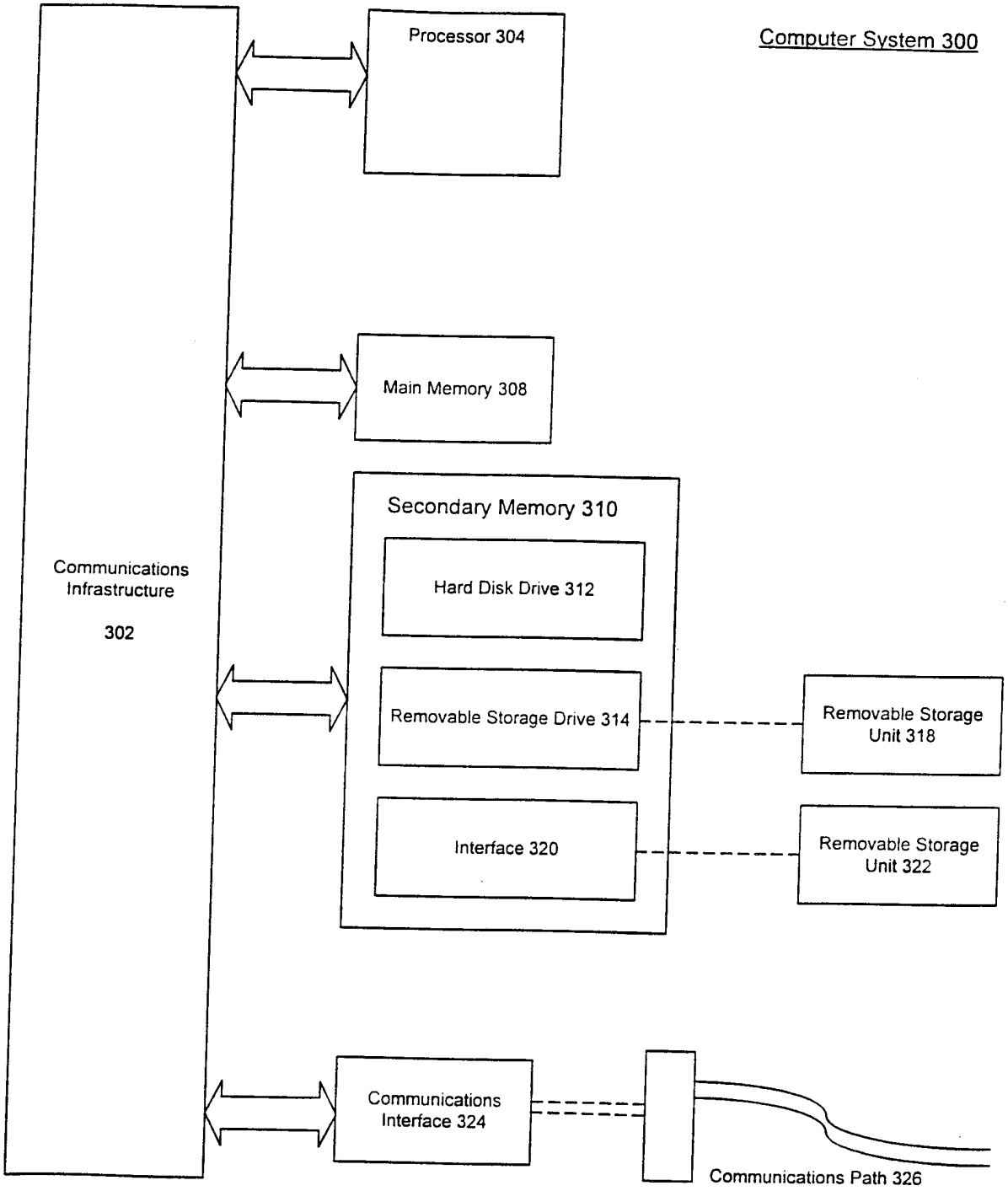
Computer System 300
Processor 304
Main Memory 308
Secondary Memory 310
Hard Disk Drive 312
Removable Storage Drive 314
Removable Storage Unit 318
Interface 320
Removable Storage Unit 322
Communications Infrastructure 302
Communications Interface 324
Communications Path 326

FIG. 3

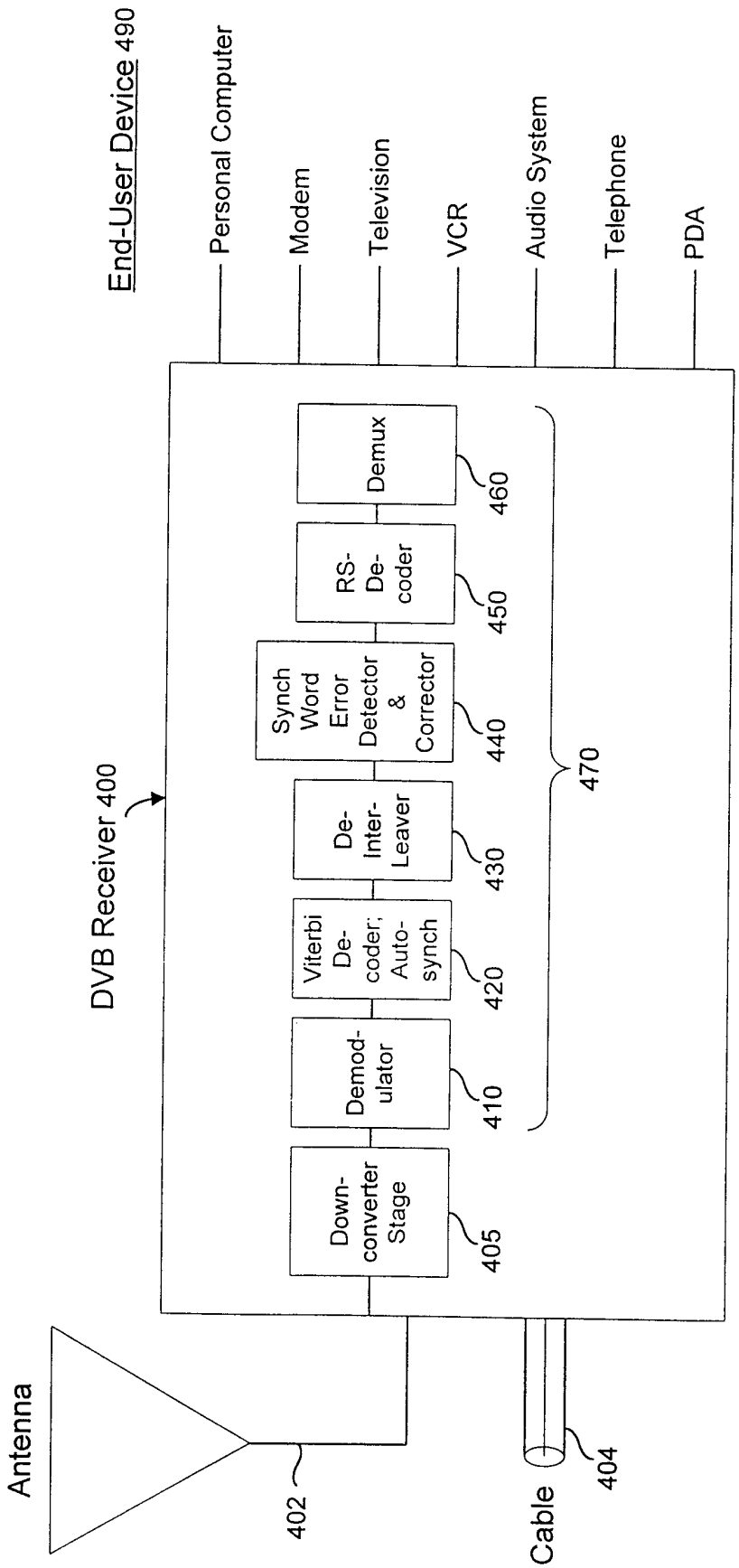
End-User Device 490
Personal Computer
Modem
Television
VCR
Audio System
Telephone
PDA
DVB Receiver 400
Demux
460
RS-De-coder
450
Synch Word Error Detector & Corrector
440
De-Inter-Leaver
430
Viterbi De-coder; Auto-synch
420
Demod-ulator
410
Down-converter Stage
405
470
Antenna
402
Cable
404

FIG. 4A

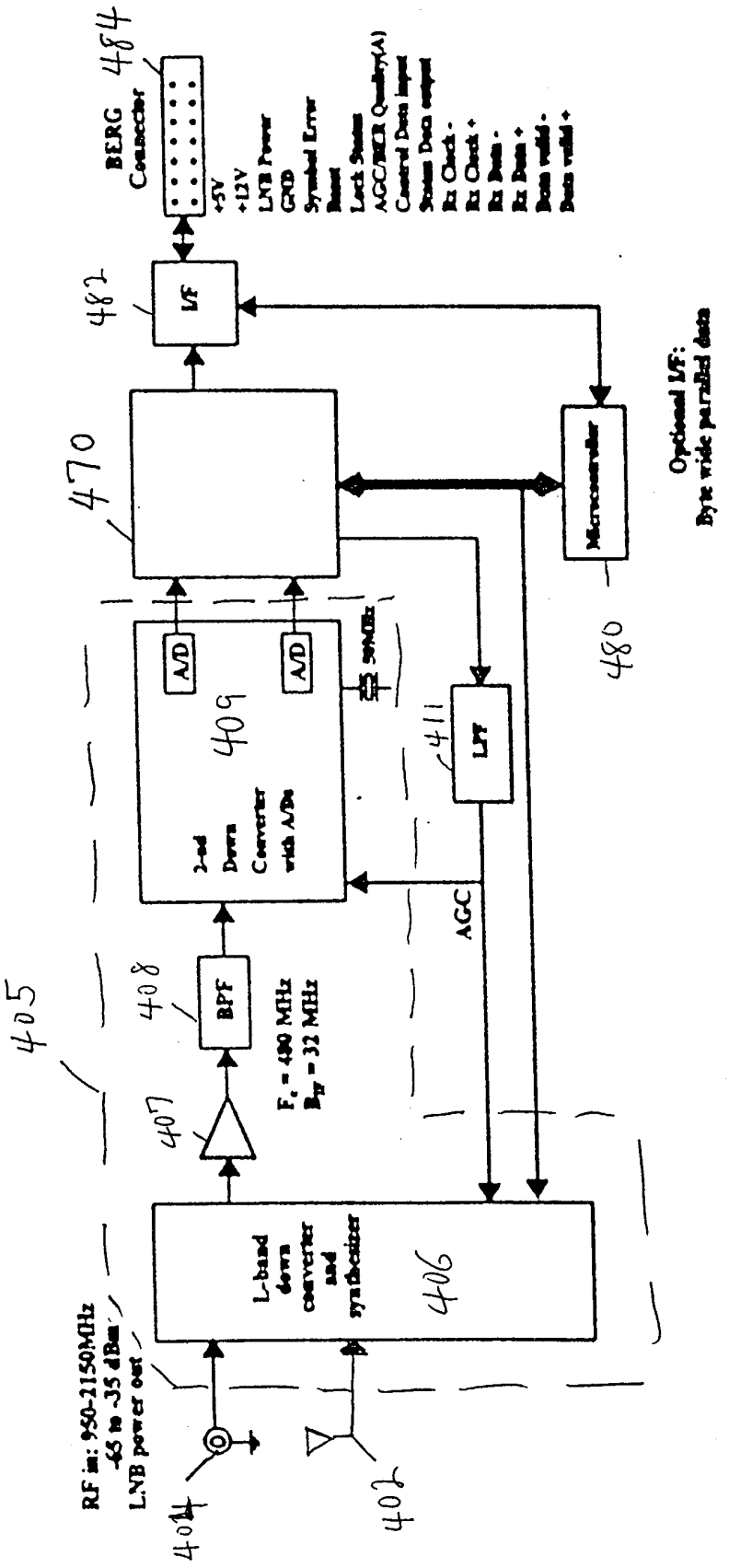
BERG Connector
484
+5V
+12V
LNB Power
GND
Symbol Error
Burst
Lock Status
AGC/SIGN Quality(AI)
Control Data input
Status Data output
Rx Clock -
Rx Clock +
Rx Data -
Rx Data +
Data valid -
Data valid +
I/F
482
470
Microcontroller
Optional I/F:
Byte wide parallel data
480
A/D
A/D
Sample
2nd Down Converter with A/Ds
409
LPF
411
AGC
BPF
408
F_c = 480 MHz
B_W = 32 MHz
405
407
L-band down converter and synthesizer
406
RF in: 950-2150MHz
-65 to -35 dBm
LNB power out
404
402

FIG. 4B

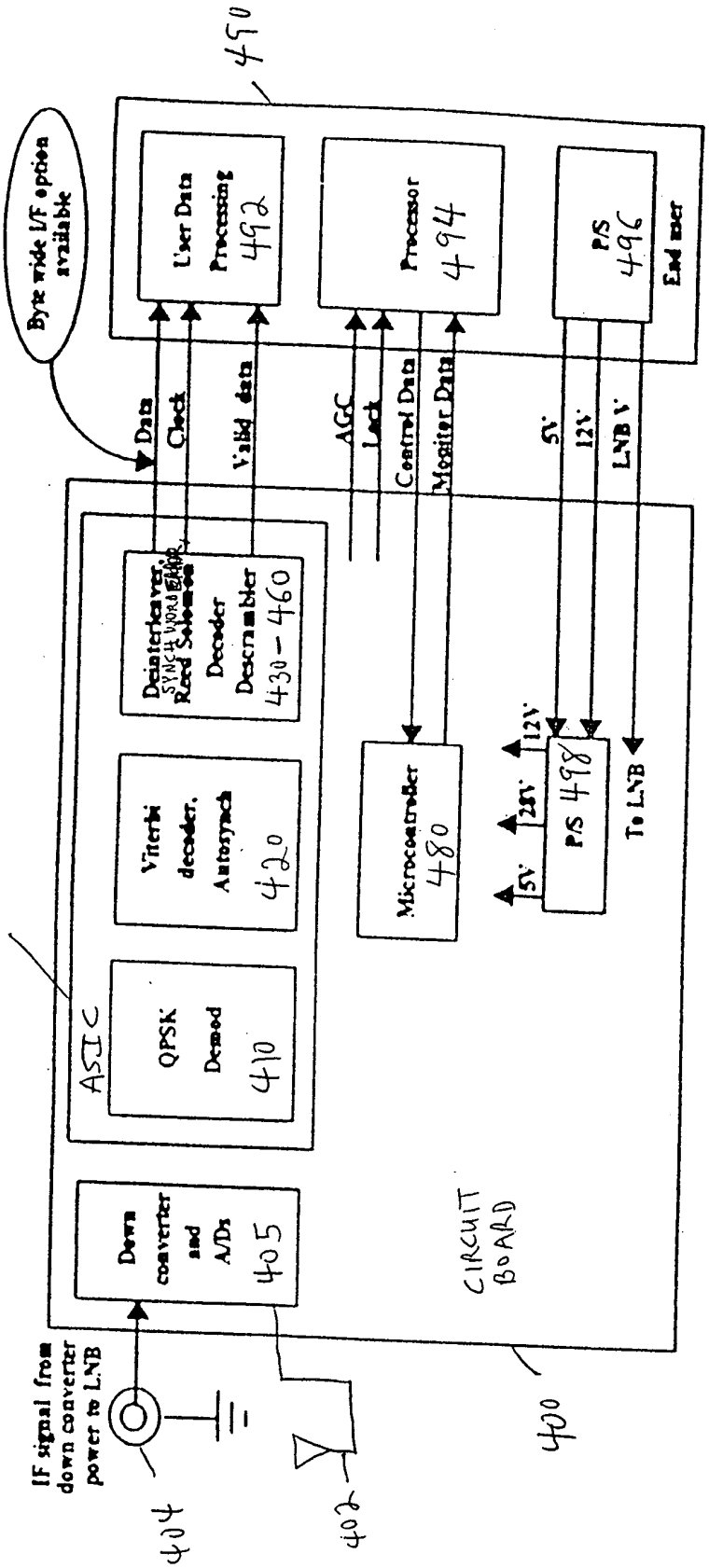
450
User Data Processing 492
Processor 494
P/S 496
End user
Byte wide I/F option available
Data
Clock
Valid data
AGC
Lock
Control Data
Monitor Data
5V
12V
LNB V
470
ASIC
QPSK Demod 410
Viterbi decoder, Autosynch 420
Deinterleaver, Reed Solomon Decoder Descrambler 430 - 460
Microcontroller 480
5V
12V
12V
P/S 498
To LNB
Down converter and A/Ds 405
CIRCUIT BOARD
400
IF signal from down converter power to LNB
404
402

FIG. 4C

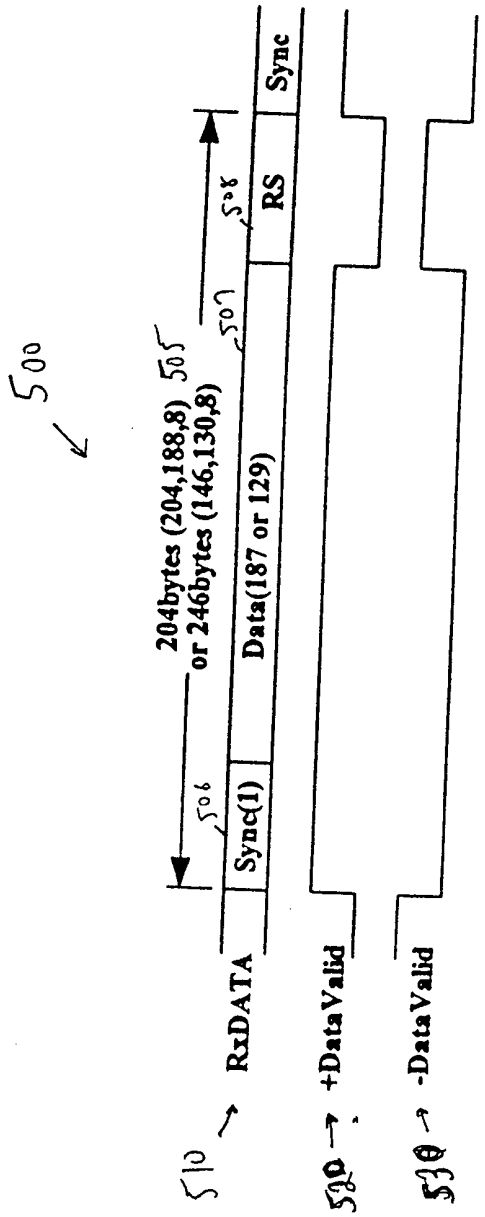
500
204bytes (204,188,8)
or 246bytes (146,130,8)
505
506
507
508
Sync(1)
Data(187 or 129)
RS
Sync
510
RxDATA
520
+DataValid
530
-DataValid

FIG. 5