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(71) Applicant (for all designated States except US): MIMOS

BERHAD [MY/MY]; Technology Park Malaysia, 57000 Kuala Lumpur (MY).

(72) Inventors; and

(75) Inventors/Applicants (for US only): WITJAKSONO,

Gunawan [ID/MY]; Mimos Berhad, Technology Park

Malaysia, 57000 Kuala Lumpur (MY). BIEN CHIA

SHENG, Daniel [MY/MY]; Mimos Berhad, Technology

Park Malaysia, 57000 Kuala Lumpur (MY). NABIPOOR,

Mohsen [IR/MY]; Mimos Berhad, Technology Park

Malaysia, 57000 Kuala Lumpur (MY).

(74) Agent: YAP, Kah Hong; Pyprus Sdn Bhd, Suite 8.02, 8th

Floor, Plaza First Nationwide, 161, Jalan Tun H.S. Lee, 50000 Kuala Lumpur (MY).

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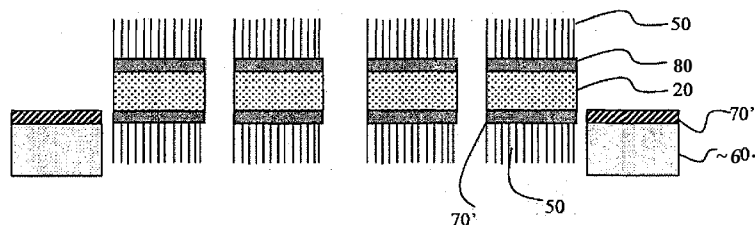


FIG 3

(57) **Abstract:** The present invention provides a nanostructured double-sided super capacitor device dial comprises a substrate, a first metal catalyst layer disposed on top of the substrate, an electric conductive layer disposed and etched on top of the first metal catalyst layer to form a plurality of finger electrodes and contact pads, wherein the plurality of the finger electrodes are configured to be interdigitated, a second metal catalyst layer disposed on the top of the finger electrodes; wherein, when the second metal catalyst layer is disposed, the substrate is etched to expose the first metal catalyst layer underneath of the finger electrodes, so that the top and bottom surfaces of the finger electrodes are exposed, carbon nanotubes (CNTs) extending from the exposed first and second metal catalyst layers of the finger electrodes, electrolyte filled into the finger electrodes and CNTs, and an encapsulating bottom and top encapsulating the interdigitated finger electrodes, CNTs and electrolyte to produce the nanostructured double-sided super capacitor device. The present invention also provides a process of fabricating the nano structured double sided super capacitor.



DOUBLE-SIDED SUPER CAPACITOR AND METHOD FOR MAKING THE
SAME

Field of the Invention

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[0001] The present invention relates generally to super capacitors, and more particularly to a nanostructured double-sided super capacitor device and a method for making the nanostructured double-sided super capacitor device.

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Background of the Invention

[0002] A conventional capacitor is formed by two parallel electrical conductive plates and a dielectric layer is disposed between the plates. The capacity of a capacitor for storing electric charge is called the capacitance that is measured in Farads (F). The higher
15 the capacitance, the greater the capacitor is able to store electric potential/electric charge. Capacitance is proportional to the area of the two plates in a capacitor; thus augment of the area of the plates increases the capacitance of the capacitor. However, the area of the plates is limited for practical uses.

[0003] Supercapacitors are becoming attractive power sources in memory backup
20 devices, electric vehicles, military weapons, space equipment and in a number of day-to-day electronic equipment. Super capacitor is intended to solve the issue of limited plate areas in a conventional capacitor and assumed to theoretically work the same way as does a conventional capacitor. A super capacitor has high surface area electrodes and ion-mobile electrolyte to produce high energy density. One widely-used construction platform
25 employs interdigitated electrodes. Typically, the top surface of the electrodes is completely filled with liquid electrolyte. However, by having electrolyte and nanostructures only on the top surface of the interdigitated electrode, the surface between electrodes being utilized is 50%.

Summary of the Invention

[0004] One aspect of the present invention provides a nanostructured double-sided super capacitor device. In one embodiment, the nanostructured double-sided super capacitor device comprises a substrate, a first metal catalyst layer disposed on top of the substrate, an electric conductive layer disposed and etched on top of the first metal catalyst layer to form a plurality of finger electrodes and contact pads, wherein the plurality of the finger electrodes are configured to be interdigitated, a second metal catalyst layer disposed on the top of the finger electrodes; wherein, when the second metal catalyst layer is disposed, the substrate is etched to expose the first metal catalyst layer underneath of the finger electrodes, so that the top and bottom surfaces of the finger electrodes are exposed, carbon nanotubes (CNTs) extending from the exposed first and second metal catalyst layers of the finger electrodes, electrolyte filled into the finger electrodes and CNTs, and an encapsulating bottom and top encapsulating the interdigitated finger electrodes, CNTs and electrolyte to produce the nanostructured double-sided super capacitor device.

[0005] Another aspect of the present invention provides a process for fabricating a nanostructured double-sided super capacitor device, in one embodiment, the process comprises providing a substrate; depositing an insulating layer onto both bottom and top surfaces of the substrate, wherein the bottom insulating layer is etched to expose the substrate; depositing and etching an electric conductive layer to form a plurality of finger electrodes and contact pads, wherein the plurality of the finger electrodes are configured to be interdigitated; depositing a second metal catalyst layer on the top surfaces of the interdigitated electrodes; etching the silicon substrate and the insulating layer from the bottom side to form a through substrate opening beneath the finger electrodes so that the first metal catalyst layer underneath the finger electrodes is exposed; growing of carbon nanotubes (CNTs) at the exposed metal catalyst areas on the top and bottom surfaces of the finger electrodes; encapsulating with an encapsulating bottom the bottom part of the device; introducing electrolyte to the interdigitated electrodes and carbon nanotubes; and encapsulating with an encapsulating top the top part of the device enclosing the interdigitated electrodes, carbon nanotubes and ionic electrolytes, producing a double-sided super capacitor device.

[0006] The objectives and advantages of the invention will become apparent from the following detailed description of preferred embodiments (hereof in connection with the accompanying drawings).

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Brief Description of the Drawings

[0007] Preferred embodiments according to the present invention will now be described with reference to the Figures, in which like reference numerals denote like elements.

10 [0008] FIG 1 shows a schematic plan view of the planar double-sided super capacitor.

[0009] FIG 2 shows a cross-section view of the super capacitor with one side (top) carbon nanotubes (CNT)-based electrodes.

15 [0010] FIG 3 shows a schematic cross-section view of the double-sided super capacitor in accordance with one embodiment of the present invention.

[0011] FIGS 4-5 illustrate a process for fabricating the double-sided super capacitor in accordance with one embodiment of the present invention.

Detailed Description of the Invention

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[0012] The present invention may be understood more readily by reference to the following detailed description of certain embodiments of the invention.

[0013] Throughout this application, where publications are referenced, the disclosures of these publications are hereby incorporated by reference, in their entireties,
25 into this application in order to more fully describe the state of art to which this invention pertains.

[0014] The present invention provides a double-sided super capacitor with metal electrodes on a silicon substrate. In one embodiment, the double-sided super capacitor has the configuration of a planar electrochemical super capacitor. FIG 1 shows a schematic
30 plan view of the planar double-sided super capacitor. As shown in FIG 1, the planar double-sided super capacitor comprises two electric conductive sheets serving as positive or negative connectors with external components. Each electric conductive sheet contains

a contact pad 10, 40 and a plurality of finger electrodes 20, where the plurality of finger electrodes from body electric conductive sheets are arranged in an alternative manner to form a configuration of interdigitated finger electrodes. When the electrolyte 30 is filled on the surfaces of the interdigitated finger electrodes, a double-sided planar electrochemical super capacitor is formed.

[0015] It is to be noted that prior arts have mainly focused on increasing the surface area of electro-active materials and paid much less attention to increasing the geometry capacitance of super capacitor. For both double layer super capacitor and electrochemical super capacitor, the most important parameter to enhance the capacitance is optimizing the geometry capacitance by structuring the super capacitor with utilizing more effective surface area per unit volume of the structure.

[0016] If the planar double layer super capacitor as shown in FIG 1 is only filled with an electrolyte on the top surface of the interdigitated finger electrodes, only 50% of the surface areas are utilized. FIG 2 shows a cross-section view of the super capacitor with one side (top) carbon nanotubes (CNT)-based electrodes. The super capacitor as shown in FIG 2 comprises a substrate 60, a first metal catalyst layer 70 disposed on top of the substrate, an electrical conductive layer disposed and etched on top of the first metal catalyst layer to form a plurality of finger electrodes 20, a second metal catalyst layer 80 disposed on top of the finger electrodes, and carbon nanotubes (CNTs) 50 extending from the top electric conductive layer. The electrolyte 30 (not shown) is filled into the CNTs; then all are encapsulated. While the contact surface area of electrolyte and electrodes is increased with a bigger capacitance with the use of CNTs, the geometry capacitance is not optimized. It is to be noted that the supercapacitor shown in FIG 2 is so simplified as to illustrate the principle of its configuration. In practice, the CNTs formed are not so uniformed and can take different orientations. In addition, CNTs can also be formed between the electrodes, resulting in fringing electric fields. Thus, the accumulated charges from the supercapacitor comprise both the ones formed between the conductive carbon nanotubes and the ones from the fringing electric fields between the interdigitated electrodes. Nonetheless, the charges between the conductive CNTs are significantly dominant.

[0017] Referring now to FIG 3, there is provided a schematic cross-section view of the double-sided super capacitor in accordance with one embodiment of the present

invention. The double-sided super capacitor has a through substrate opening so as to allow the utilization of both surfaces of the interdigitated finger electrodes, increasing the geometry capacitance. The super capacitor as shown in FIG 3 comprises a substrate 60' that is similar to the substrate 60 shown in FIG 2 except for having a through opening underneath of the electrodes, a first metal catalyst layer 70' disposed on top of the substrate where the first metal catalyst layer 70' is similar to the first metal catalyst layer 70 shown in FIG 2 except for being exposed underneath of the finger electrodes, an electric conductive layer disposed and etched on top of the first metal catalyst layer 70' to form a plurality of finger electrodes 20 and contact pads (not shown), a second metal catalyst layer 80 disposed on the top of the finger electrodes, and carbon nanotubes (CNTs) 50 extending from the first and second metal catalyst layers 70', 80 of the finger electrodes. The electrolyte 30 (not shown) is filled into the finger electrodes and CNTs; then all are encapsulated (the encapsulating bottom and top are not shown; more details of the encapsulation are provided in reference to FIG 5 below). Similar to FIG 2, it is to be noted that the supercapacitor shown in FIG 3 is so simplified as to illustrate the principle of its configuration. In practice, the CNTs formed are not so uniformed and can take different orientations, in addition, CNTs can also be formed between the electrodes, resulting in fringing electric fields. Thus, the accumulated charges from the supercapacitor comprise both the ones formed between the conductive carbon nanotubes and the ones from the fringing electric fields between the interdigitated electrodes. Nonetheless, the charges between the conductive CNTs are significantly dominant.

[0018] In some embodiments, the double-sided super capacitor further comprises an insulating layer disposed onto both silicon substrate surfaces. In some embodiments, the insulating layer is composed of silicon oxide or nitride.

[0019] The suitable materials for the substrate include high temperature materials that are able to withstand the growth temperature of CNTs at at least 650°C; examples are silicon and quartz. The suitable materials for the first and second metal catalyst layers include material(s) selected from a group consisting of, but not limited to, iron (Fe), nickel (Ni), cobalt (Co) or a combination thereof. The suitable materials for the electric conductive layer to form the electrodes and contact pads include any suitable electrical conductive materials that can withstand the growth temperature of carbon nanotubes of above 600 °C; in some embodiments, the material for the conductive layer is preferably

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tungsten, gold (Au) or platinum (Pt); the electrode materials can be deposited by sputtering, evaporation or chemical vapour deposition and the electrodes can be patterned by plasma etching or chemical etching). The CNTs can be grown by a method selected from the group consisting of chemical vapour deposition (CVD), metalorganic chemical vapour deposition (MOCVD), plasma enhanced chemical vapour deposition (PECVD), hot wire chemical vapour deposition (HWCVD), atomic layer deposition (ALD), electrochemical deposition, solution chemical deposition and combinations thereof. The suitable electrolyte includes ionic liquids such as potassium hydroxide and 3-methylimidazolium hexafluorophosphate ([BMIM][PF₆]). The encapsulating material for the encapsulating bottom and top includes, but not limited to, flexible polymers such as polydimethylsiloxane (PDMS), polyimide, silicon or glass type substrates.

[0020] Carbon nanotubes (CNTs), with their unique architecture, excellent conductivity, and high surface area, have drawn significant attraction as nanosized supercapacitor electrodes. Extremely high rate capability—the rate at which the supercapacitor can be charged and discharged—can be achieved by using CNT electrodes in supercapacitors as compared to conventional carbonaceous materials.

[0021] In some embodiments, the carbon nanotubes are further functionalized with at least nickel (Ni), gold (Au) or platinum (Pt) to further enhance the energy density of the super capacitor.

[0022] The capacitance of standard capacitor is determined by the area of the plates, dielectric permittivity and the spacing, where:

$$C = \epsilon_0 \cdot \epsilon_r \cdot A/d \quad (\text{equation I})$$

[0024] where ϵ_0 is the dielectric constant, and ϵ_r the relative dielectric permittivity, A is the total area and d is the gap between fingers.

[0025] There are two main differences between a super capacitor and a regular capacitor. First, a super capacitor device comprises electrodes with ion conducting electrolyte between them as compared with standard capacitors where the electrodes are separated with dielectric materials. When the super capacitor is biased the positive and negative ions in the electrolyte will separate, migrate and accumulate around the electrode surface, forming a thin layer called electro-chemical double layer. Second, porous electrode materials are utilised in super capacitors to enhance the interfacial capacitance

where it maximises the electro-chemical double layer phenomenon giving the device a very high value of capacitance per unit area.

[0026] Another aspect of the present invention provides a process for fabricating the double-sided super capacitors. Referring now to FIGS 4-5, there is provided a process for fabricating the double-sided super capacitor in accordance with one embodiment of the present invention. FIG 4 illustrates the formation of the double-sided interdigitated electrodes with carbon nanolubes on both surfaces, and FIG 5 illustrates the introduction of ion conductive electrolytes to the carbon nanotube structures and the encapsulation of the device from both sides.

10 [0027] Referring now to FIG 4, the process of fabricating the double-sided interdigitated electrodes with CNTs on both surfaces comprises:

[0028] (a) providing a substrate (e.g., silicon) 60 and depositing an insulating layer 61 onto both bottom and top silicon substrate surfaces, where the bottom insulating layer is etched to expose the substrate; in some embodiments, the insulating layer 61 is composed of silicon oxide or nitride;

15 [0029] (b) depositing a first metal catalyst layer 70 on the top insulating layer 61 as a seed layer for growing carbon nanolubes beneath the interdigitated electrodes. The catalyst is deposited by physical or chemical vapour deposition methods with materials selected from a group consisting of, but not limited to, iron (Fe), nickel (Ni), cobalt (Co) or a combination thereof;

20 [0030] (c) depositing and etching a conductive layer to form the interdigitated electrodes 20 and contact pads 10, 40; where the conductive layer is made of any suitable electrical conductive materials that can withstand the growth temperature of carbon nanotubes of above 600 °C; in some embodiments, the material for the conductive layer is preferably gold (Au) or platinum (Pt); the electrode materials can be deposited by sputtering, evaporation or chemical vapor deposition and the electrodes can be patterned by plasma etching or chemical etching);

25 [0031] (d) depositing a second metal catalyst layer 80 on the top surfaces of the interdigitated electrodes 20 to act as a seed layer for growing carbon nanotubes on the top surface of the second metal catalyst layer. The second metal catalyst layer 80 is etched to expose the contact pad regions to ensure that nanotubes are not formed on the pad regions

for the nanotubes formed on the pad regions will hinder electrical connections during testing and packaging;

[0032] (e) etching the silicon substrate 60 and the insulating layer 61 from the back to form a through substrate opening beneath the electrode fingers 20 so that the first metal catalyst layer 70 under the electrode fingers is exposed;

[0033] (f) growing of carbon nanotubes 50 at the exposed metal catalyst areas on the top and bottom surfaces of the finger electrodes. The CNTs can be grown by a method selected from the group consisting of chemical vapour deposition (CVD), metalorganic chemical vapour deposition (MOCVD), plasma enhanced chemical vapour deposition (PECVD), hot wire chemical vapour deposition (HWCVD), atomic layer deposition (ALD), electrochemical deposition, solution chemical deposition and combinations thereof.

[0034] Referring now to FIG 5, the encapsulating process comprises:

[0035] (a) encapsulating with an encapsulating bottom 100 the bottom part of the device fabricated by the process shown in FIG 4 prior to the introduction of ion conductive electrolyte, preventing the electrolyte from leaking. The encapsulating material includes, but not limited to, flexible polymers such as polydimethylsiloxane (PDMS), polyimide, silicon or glass type substrates;

[0038] (b) introducing the electrolyte 30 to the interdigitated electrodes and carbon nanotubes. The electrolyte is an ionic liquid including, but not limited to, potassium hydroxide and 3-methylimidazolium tetrafluoroborate ([BM1M][B1'4]);

[0037] (c) encapsulating with an encapsulating top 110 the top part of the device enclosing the interdigitated electrodes, carbon nanotubes and ionic electrolytes, producing a double-sided super capacitor.

[0038] The double-sided super capacitor can be fabricated by for example MEMS technology, MEMS technology is preferred because it is compatible with integrated circuits and energy harvesting devices such as solar cell, allowing formation or integration of all components onto the same platform or on-chip.

[0039] While the present invention has been described with reference to particular embodiments, it will be understood that the embodiments are illustrative and that the invention scope is not so limited. Alternative embodiments of the present invention will become apparent to those having ordinary skill in the art to which the present invention pertains. Such alternate embodiments are considered to be encompassed within the scope

of the present invention. Accordingly, the scope of the present invention is defined by the appended claims and is supported by the foregoing description.

CLAIMS

What is claimed is:

- 5 1. A nanostructured double-sided super capacitor device, comprising:
a substrate;
a first metal catalyst layer disposed on top of the substrate;
an electric conductive layer disposed and etched on top of the first metal catalyst
layer to form a plurality of finger electrodes and contact pads, wherein the plurality of the
10 finger electrodes are configured to be interdigitated;
a second metal catalyst layer disposed on the top of the finger electrodes; wherein,
when the second metal catalyst layer is disposed, the substrate is etched to expose the first
metal catalyst layer underneath of the finger electrodes, so that the top and bottom surfaces
of the finger electrodes are exposed;
15 carbon nanotubes (CNT's) extending from the exposed first and second metal
catalyst layers of the finger electrodes;
electrolyte filled into the finger electrodes and CNT's; and
an encapsulating bottom and top encapsulating the interdigitated finger electrodes,
CNTs and electrolyte to produce the nanostructured double-sided super capacitor device.
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2. The nanostructured double-sided super capacitor device of claim 1, further
comprising an insulating layer disposed onto both surfaces of the substrate, wherein the
substrate is made of silicon, and the insulating layer is composed of silicon oxide or nitride,
and the substrate is made of silicon or quartz.
- 25 3. The nanostructured double-sided super capacitor device of claim 1, wherein the
first and second metal catalyst layers is made of the material(s) selected from a group
consisting of iron (Fe), nickel (Ni), cobalt (Co) and a combination thereof.
- 30 4. The nanostructured double-sided super capacitor device of claim 1, wherein the
electric conductive layer is made of tungsten, gold (Au) or platinum (Pt).

5. The nanostructured double-sided super capacitor device of claim 1, wherein the electrolyte is potassium hydroxide or 3-methylimidazolium tetrafluoro-borate ([BMIM][BF₄]).

5 6. The nanostructured double-sided super capacitor device of claim 1, wherein the encapsulating bottom and top is made of materials selected from the group of polydimethylsiloxane (PDMS), polyimide, silicon and glass type substrates.

7. The nanostructured double-sided super capacitor device of claim 1, wherein the
10 carbon nanotubes are further functionalized with nickel (Ni), gold (Au) or platinum (Pt).

8. A process for fabricating a nanostructured double-sided super capacitor device, comprising:

providing a substrate;

15 depositing an insulating layer onto both bottom and top surfaces of the substrate, wherein the bottom insulating layer is etched to expose the substrate;

depositing and etching an electric conductive layer to form a plurality of finger electrodes and contact pads, wherein the plurality of the finger electrodes are configured to be interdigitated;

20 depositing a second metal catalyst layer on the top surfaces of the interdigitated electrodes;

etching the silicon substrate and the insulating layer from the bottom side to form a through substrate opening beneath the finger electrodes so that the first metal catalyst layer underneath the finger electrodes is exposed;

25 growing of carbon nanotubes (CNTs) at the exposed metal catalyst areas on the top and bottom surfaces of the finger electrodes;

encapsulating with an encapsulating bottom the bottom part of the device;

introducing electrolyte to the interdigitated electrodes and carbon nanotubes; and

30 encapsulating with an encapsulating top the top part of the device enclosing the interdigitated electrodes, carbon nanotubes and ionic electrolytes, producing a double-sided super capacitor device.

9. The process of claim 8, wherein the substrate is made of silicon, and the insulating layer is composed of silicon oxide or nitride.
10. The process of claim 8, wherein the first and second metal catalyst layers are deposited by physical or chemical vapor deposition methods with material(s) selected from a group consisting of iron (Fe), nickel (Ni), cobalt (Co) and a combination thereof;
11. The process of claim 8, wherein the electric conductive layer is made of tungsten, gold (Au) or platinum (Pt), wherein the electric conductive layer is formed by sputtering, evaporation or chemical vapor deposition, and wherein the tmgr electrodes are patterned by plasma etching or chemical etching.
12. The process of claim 8, wherein the CNTs are grown by a method selected from the group consisting of chemical vapour deposition (CVD), metalorganic chemical vapour deposition (MOCVD), plasma enhanced chemical vapour deposition (PECVD), hot wire chemical vapour deposition (HWCVD), atomic layer deposition (ALD), electrochemical deposition, solution chemical deposition and combinations thereof.
13. The process of claim 8, wherein the electrolyte is potassium hydroxide or 3-methylimidazolium tetrafluoro-borate ([BML][BF₄]).
14. The process of claim 8, wherein the encapsulating bottom and top are made of materials selected from the group consisting of polydimethylsiloxane (PDMS), polyimide, silicon and glass type substrates.
15. The process of claim 10, further comprising functionalizing the carbon nanotubes with nickel (Ni), gold (Au) or platinum (Pt).

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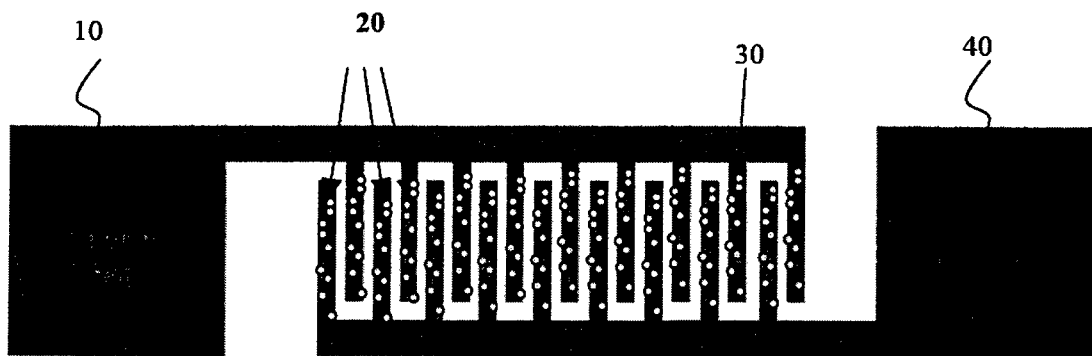


FIG 1

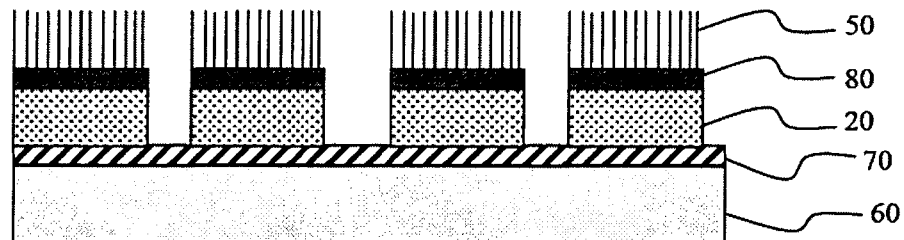


FIG 2

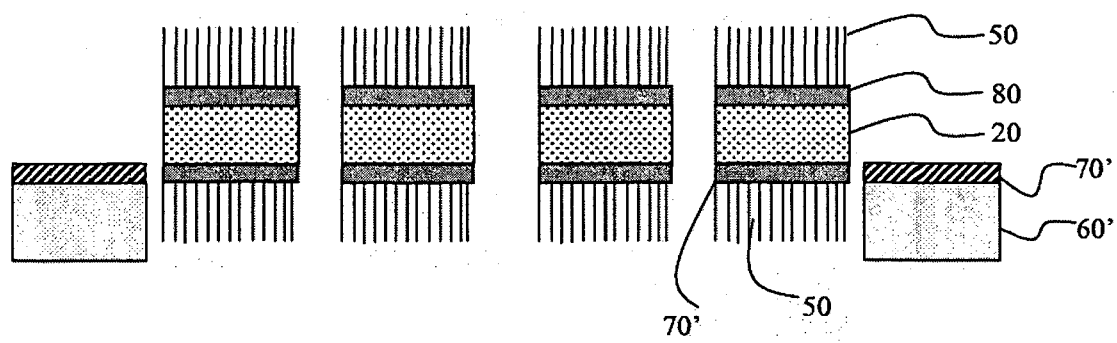


FIG 3

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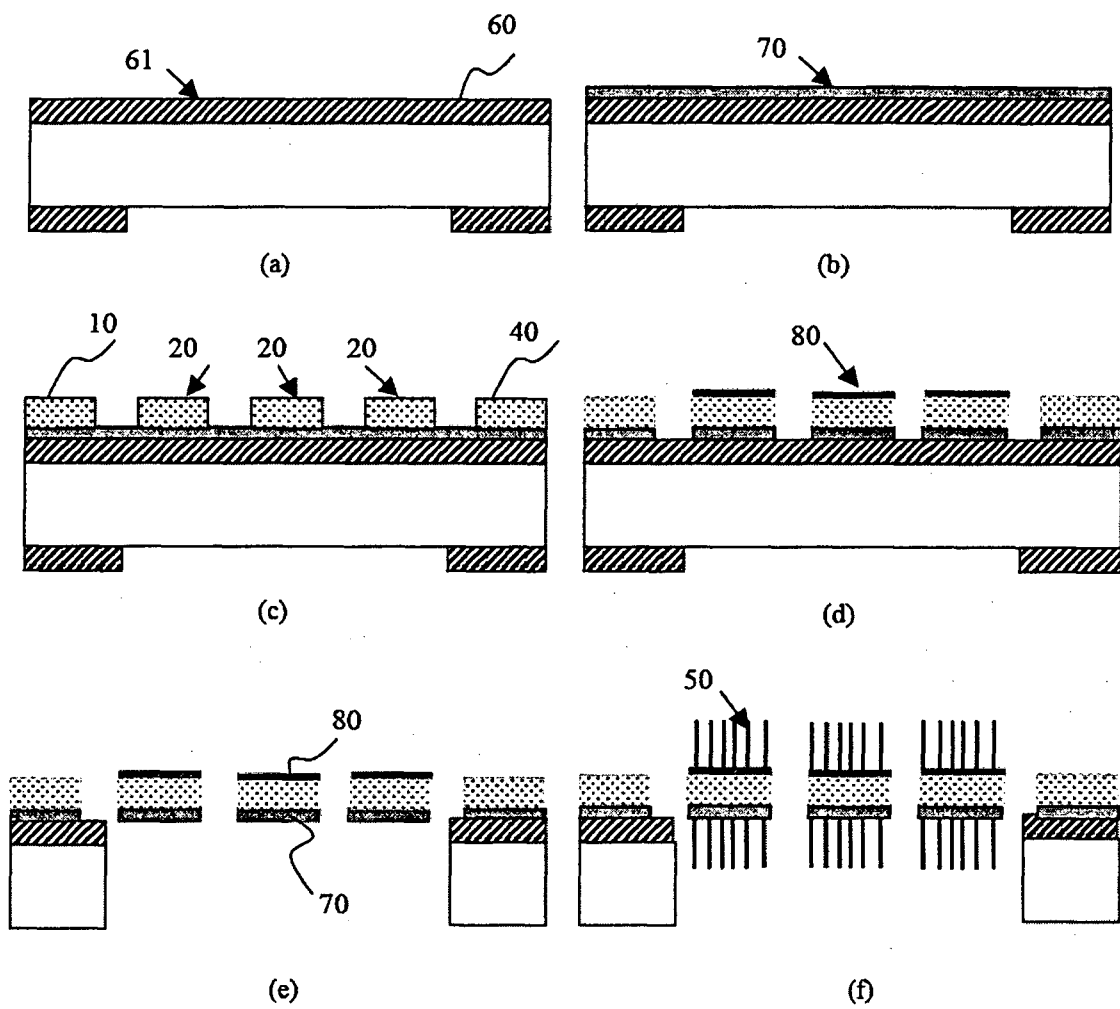
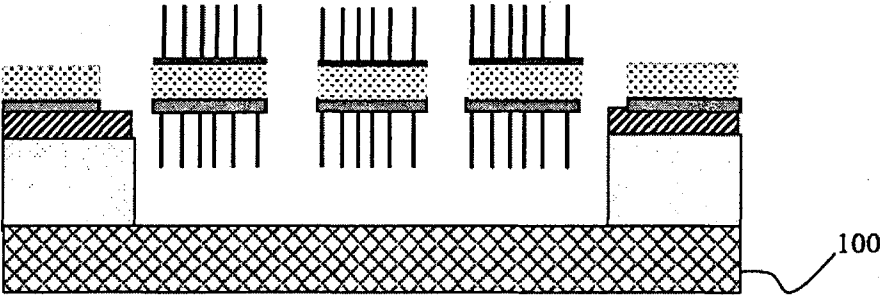
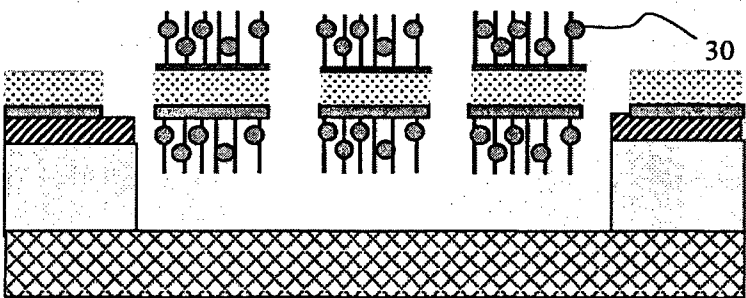


FIG 4

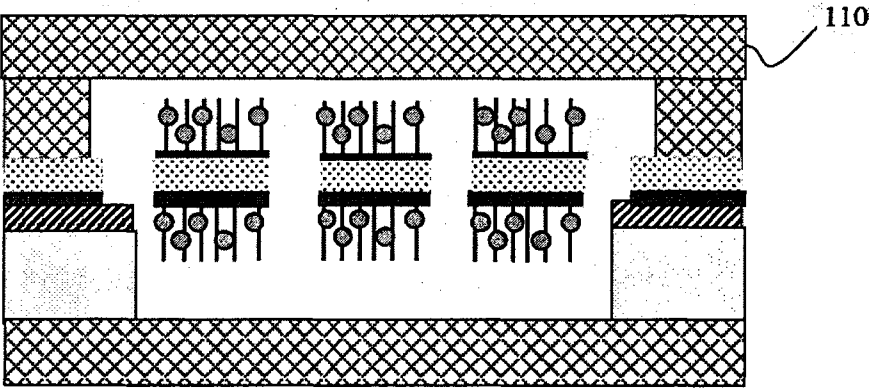
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(a)



(b)



(c)

FIG 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/MY2012/000163

A. CLASSIFICATION OF SUBJECT MATTER INV. H01G9/04 H01G9/042 H01G9/048 H01G9/058 H01G11/24 H01G11/26 H01G11/36		
ADD. According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H01G		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal , WPI Data		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 7 988 746 B2 (CHIANG YET-MING [US] ET AL) 2 August 2011 (2011-08-02) col umn 11 - col umn 16 -----	1-15
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A	US 2011/304964 A1 (FLEISCHER COREY ADAM [US] ET AL) 15 December 2011 (2011-12-15) paragraph [0061] -----	1-15
<input style="width: 20px; height: 20px; margin-right: 5px;" type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" style="width: 20px; height: 20px; margin-right: 5px;" type="checkbox"/> See patent family annex.		
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Date of the actual completion of the international search 9 January 2013	Date of mailing of the international search report 22/01/2013	
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Lescop, Emmanuel l e	

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Information on patent family members

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