

[54] ELECTRONIC TIMEPIECE HAVING A CHRONOGRAPH MECHANISM

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[51] Int. Cl. G04b 19/00

[58] Field of Search 58/50 R, 153, 23 R, 23 AC, 58/23 D, 39.5, 74-79, 23 A; 307/293

[56] References Cited

UNITED STATES PATENTS

2,970,226	1/1961	Skelton et al.....	58/39.5 X
3,646,751	3/1972	Purland et al.....	58/50 R

3,662,535	5/1972	Hedrick et al.....	58/39.5
3,672,155	6/1972	Bergey et al.....	58/85.5 X

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Assistant Examiner—U. Weldon
Attorney, Agent, or Firm—Blum, Moscovitz, Friedman & Kaplan

[57] ABSTRACT

An electronic timepiece having a pulse generator for generating a high frequency time standard signal and a first divider for dividing the time standard signal into low frequency timing signals. A second chronograph divider divides the time standard signal of said pulse generator starting at a first time and ending at a second time independent of the operation of said first divider to produce chronograph timing signals. A digital display means is provided for selectively digitally displaying the present time represented by said first divider timing signals or elapsed time represented by said second divider chronograph timing signals.

15 Claims, 3 Drawing Figures

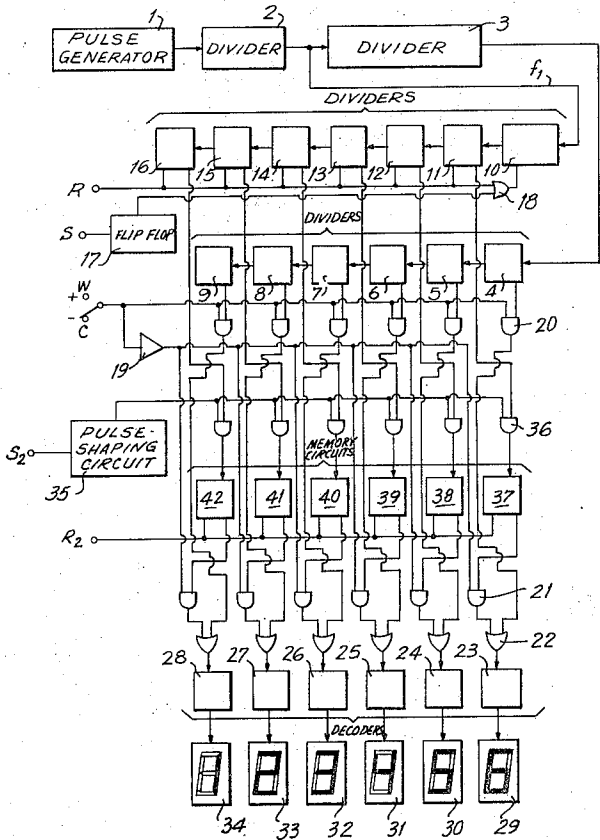
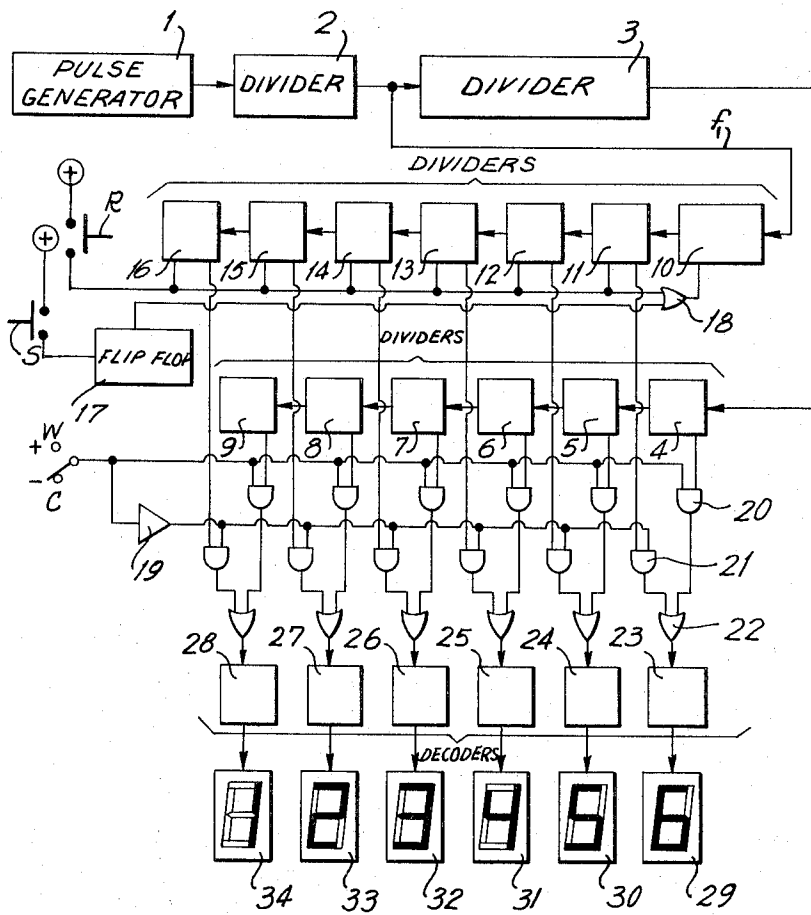
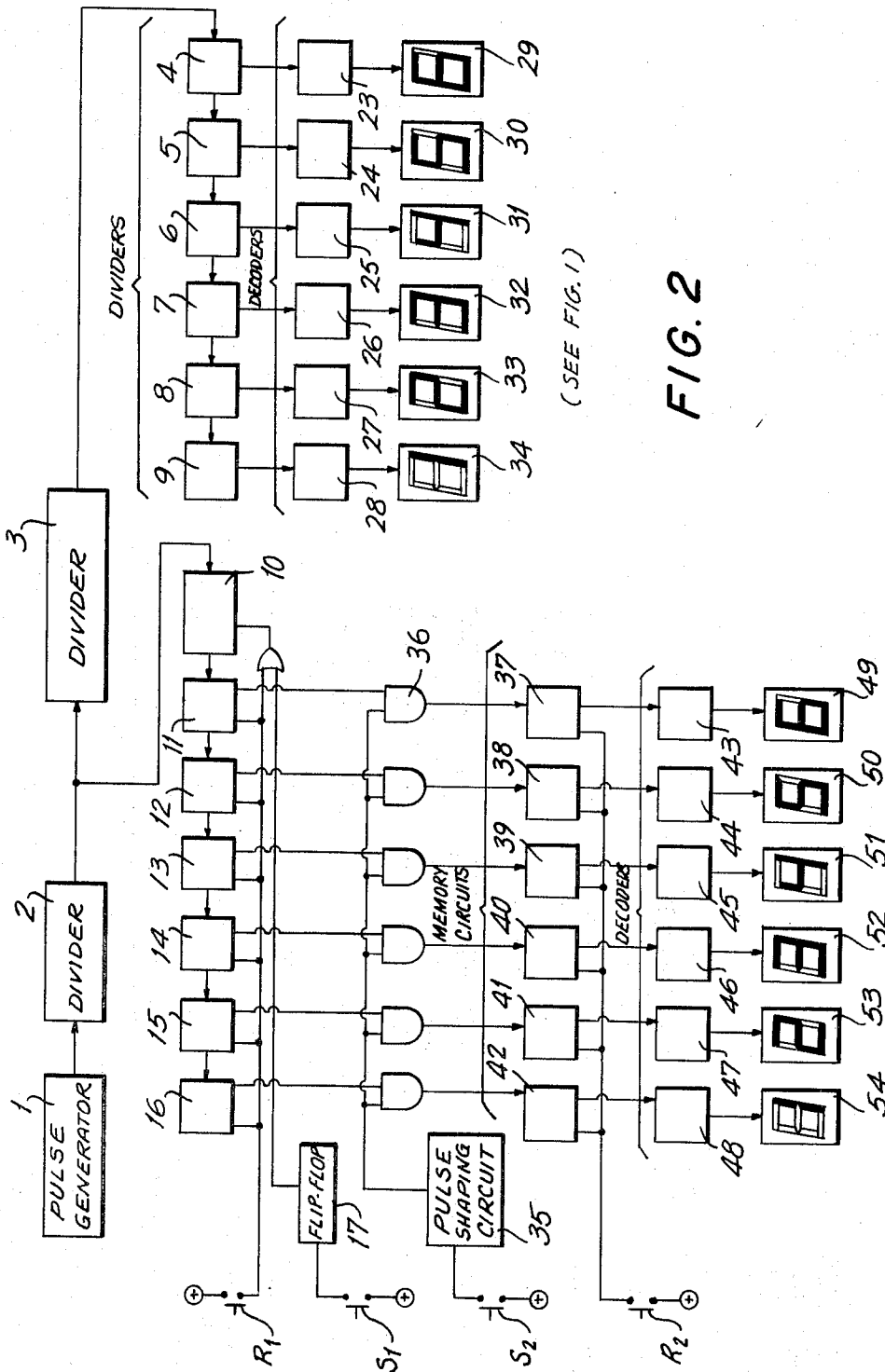


FIG. 1





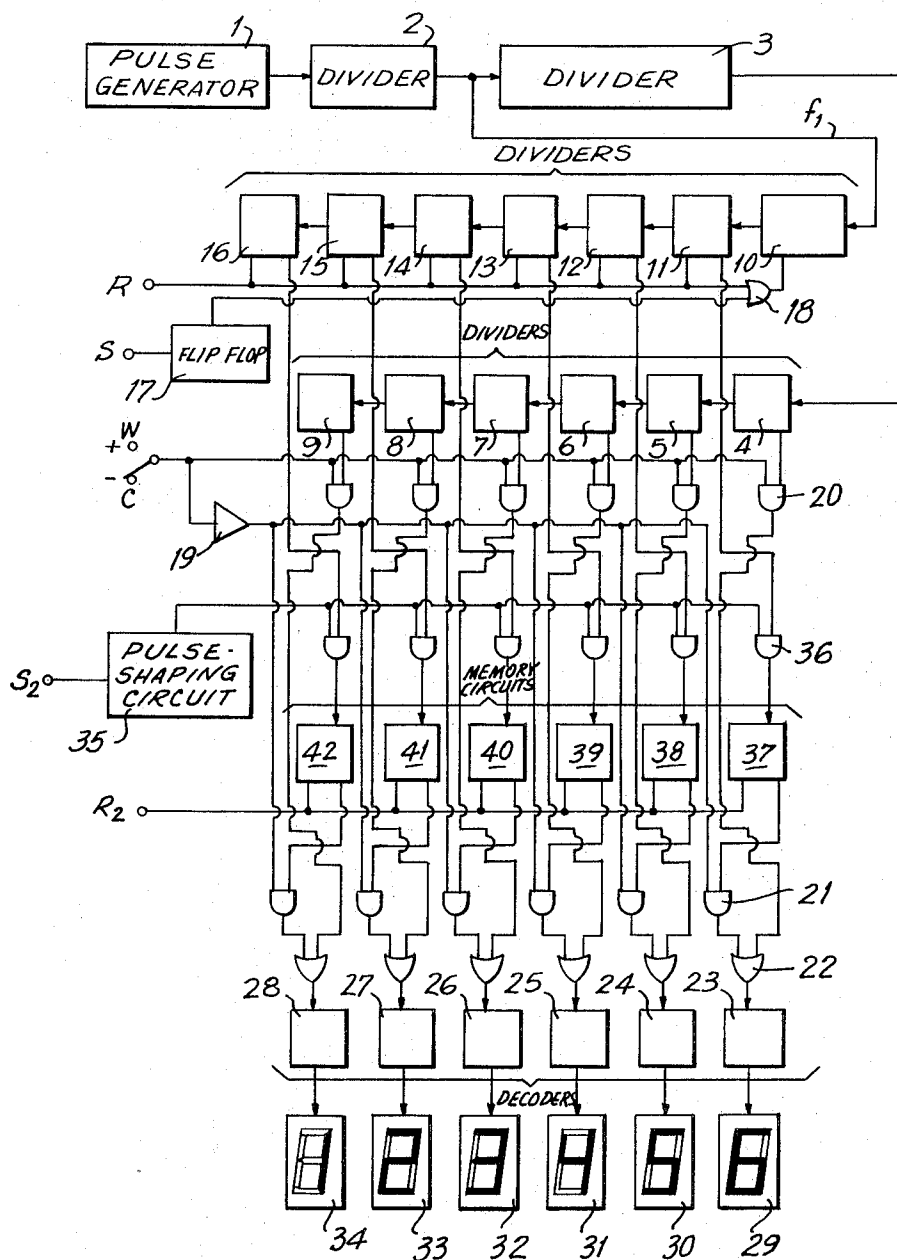


FIG. 3

ELECTRONIC TIMEPIECE HAVING A CHRONOGRAPH MECHANISM

BACKGROUND OF THE INVENTION

This invention relates to electronic timepieces having digital displays, and in particular, to the provision of chronograph mechanisms for such electronic timepieces. In the art, much effort has been devoted to the development of electronic timepieces incorporating digital displays, but these developments have principally concentrated on the time keeping mechanism itself. While electronic stop watches have been provided, such electronic stop watches cannot simultaneously function as both stop watches and conventional watches, and further, have been found to consume too much energy for practical application with the small-sized batteries customarily incorporated in electronic watches. Whenever such prior art arrangements are utilized as stop watches, normal watch operation is discontinued, so that the time must be re-set after each such use. Further, the size of the electronic circuits incorporated in such devices, as well as the power consumption thereof has made it difficult to obtain a small-sized embodiment suitable for a commercial wrist-watch.

SUMMARY OF THE INVENTION

Generally speaking, in accordance with the invention, an electronic timepiece is provided including pulse generator means for producing a high frequency time standard signal; first divider means for producing low frequency time signals from said pulse generator means; second divider means for dividing said high frequency time standard signal commencing at selected time t_1 and ending at a selected time t_2 independent of the operation of said first divider means to produce low frequency chronograph timing signals, and digital display means for selectively providing a digital representation of present time in response to said timing signals of said first divider and elapsed time between times t_1 and t_2 from said chronograph timing signals of said second divider means.

Memory means may be provided intermediate said second divider means and said digital display means for selectively recording the instantaneous chronograph timing signals of said second divider means at a selected time t_3 , where $t_1 \leq t_3 \leq t_2$. Logic gate means may be provided intermediate said second divider means and said memory means for the selective application of said chronograph timing signals to said memory means at time t_3 . Selective gate means may be provided intermediate said digital display means and said first divider means and said second divider means and memory means for selecting which of said timing signals and chronograph timing signals are applied to said digital display means.

First and second digital display means may be provided, said first display means being connected to said first divider for displaying present time, said second display means being connected to said second divider or said memory means for displaying elapsed time in response to the chronograph timing signals.

Accordingly, it is an object of the invention to provide an electronic timepiece having a digital display provided with a chronograph mechanism adapted to display elapsed time without stopping the functioning of the time keeping mechanism of said timepiece.

Still other objects and advantages of the invention will in part be obvious and will in part be apparent from the specification.

The invention accordingly comprises the features of construction, combinations of elements, and arrangement of parts which will be exemplified in the constructions hereinafter set forth, and the scope of the invention will be indicated in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a fuller understanding of the invention, reference is had to the following description taken in connection with the accompanying drawings, in which:

FIG. 1 is a logic block diagram of a first embodiment of an electronic timepiece having a chronograph mechanism in accordance with the invention;

FIG. 2 is a portion of a logic block diagram of a second embodiment of an electronic timepiece having a chronograph mechanism in accordance with the invention; and

FIG. 3 is a logic block diagram of a third embodiment of an electronic timepiece having a chronograph mechanism in accordance with the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1, the basic logic diagram of the digital electronic timepiece in accordance with the invention is depicted. Certain features of the timepiece not directly related to the present invention have been omitted to simplify the drawing. Accordingly, a timepiece would normally be provided with operation switches, a source circuit, a calendar mechanism, a time-adjusting mechanism, etc., all of which features are omitted from the block diagram of FIG. 1. In the electronic timepiece in accordance with the invention, pulse generator 1 is provided for generating a relatively high frequency time standard signal. This pulse generator may take the form of an atomic standard, a quartz crystal standard, or a mechanical tuning fork. A quartz crystal oscillator having a frequency of from several kHz to several MHz is preferred as the time standard pulse generator. Said time standard signal is applied to a divider circuit 2 formed from a binary divider chain for producing an intermediate signal of a frequency f_1 . It is desirable that said intermediate frequency be of a value of at least several kHz, if the lowest order of chronograph display is 1/1000 second, as will be more particularly explained below. The intermediate signal of frequency f_1 is applied to a further divider circuit 3 and a first chronograph divider circuit 10. Divider circuit 3 is formed from a binary divider chain and divides the intermediate signal into a timing signal at the lowest level required for display in the watch in question. Thus, if the watch in question is to digitally display seconds, the signal output of divider 3 would be a signal having a period of 1-second referred to herein as the second signal. If the digital display is to display minutes but not seconds, the lowest signal would have a period of 1-minute, and would be referred to as a minute signal. In the embodiment of FIG. 1, the digital display device displays time down to the second so that the output of divider circuit 3 is a second signal. Said second signal is applied to a series of dividers 4-9 which divides the second signal into the other timing signals required for time indication. Specifically, divider circuit 4 is a 1/10 divider circuit for producing an output signal

having a 10-second period for application to divider circuit 5. Divider circuit 5 is a 1/6 divider circuit for producing an output signal having a period of 1-minute for application to divider circuit 6. Divider circuits 6-9 are respectively 1/10, 1/6, 1/10 and 1/10 divider circuits for producing output signals having respective periods of 10-minutes, 1-hour, 10-hours and 100-hours. If the digital time display employs a 24-hour display, divider circuit 9 would be a 1/3 divider for indicating 0, 1 and 3.

When the embodiment of FIG. 1 is to be utilized as a conventional electronic watch, selection switch WC is connected to the W contact so that a positive voltage is applied to one input of each of the AND gates 20 to open said AND gates. When said AND gates are open, the contents (information) in divider circuits 4-9 is passed through the respective AND gates to one input of the respective OR gates, which passes said information to the respective decoder circuits 23-28. Each of said decoder circuits is connected to one digit 29-34 of the digital display device. In the embodiment depicted in FIG. 1, each of said digits consists of a seven bar display, the corresponding decoder circuit being adapted to produce the appropriate driving signals required to energize the bars of each digit required to digitally display the value of the respective instantaneous timing signals from divider circuits 4-9. Thus, if divider circuit 4 has counted 6 second signals, this information is transmitted through the associated AND gate 20 and OR gate 22 to decoder 23 which excites all of the segments of digit 29 of the digital display except the upper right segment as shown in FIG. 1. Similarly, digit 30 is excited by the 10-second signal from divider circuit 5, digit 31 is controlled by the 1-hour signal from divider circuit 6, digit 32 is controlled by the 10-minute signal from divider circuit 7, digit 33 is controlled by the 1-hour signal from divider circuit 8 and digit 34 is controlled by the 10-hour signal from divider circuit 9.

The chronograph mechanism of the watch according to the invention includes the divider chain 10-16 to which the intermediate signal of frequency f_1 is applied. Divider circuit 10 divides said intermediate signal into a signal of a period of 1/100 second identified as a 1/100 second signal or into a signal of a period of 1/1000 second referred to as a 1/1000 second signal, depending on the number of digits to be displayed by the chronograph mechanism. The actual number of digits displayed in a commercial electronic watch in accordance with the invention depends on the use thereof. For general use, a display down to 1/10 second may be sufficient.

The operation of divider circuit 10 is stopped when flip-flop circuit 17 connected thereto is in a re-set state, as for example, when controlling switch S connected to said flip-flop is in the "stop" position. This control of divider circuit 10 by flip-flop circuit 17 may be achieved through OR gate 18. In one embodiment, the output of OR gate 18 controls whether or not operating voltage is supplied to one or more stages of chronograph divider circuit 10.

When selector switch WC is positioned with the moving contact thereof in engagement with fixed contact C, a negative voltage is applied to one input of each AND gates 20 to close said AND gates. On the other hand, a positive voltage is applied to one input of each of AND gate 21 through inverter 19 to open said AND gates. Thus, when switch WC is positioned as depicted

in FIG. 1, the information of chronograph divider circuits 11-16 are applied respectively to decoders 23-28 through AND gates 21 and OR gates 22, said information being indicated by the digits 29-34 of the digital display means. Since control switch S is in the "stop" position so that divider circuit 10 is in a rest state, this indication has no meaning. A re-set switch R is provided coupled to each of the chronograph divider circuits 10-16 for applying a re-set signal to each of said chronograph divider circuits to set each of said divider circuits at zero. When this is done, digital display means 29-34 indicates all zero, the preparative state for operation of the chronograph. If control switch S is then operated to place said switch in the "start" position, flip-flop circuit 17 is set and divider circuit 10 starts dividing the intermediate signal of a frequency f_1 applied thereto. If the frequency dividing ratio of divider circuit 10 is large, the measuring error becomes extremely small, so that it is almost $1/f_1$ seconds. The 1/100 second signal or the 1/1000 second signal obtained from chronograph divider circuit 10 is transmitted to the next chronograph divider circuit 11. If the output signal of chronograph divider circuit 10 is a 1/100 second signal, then chronograph divider circuits 11-16 are respectively 1/10, 1/10, 1/10, 1/6, 1/10 and 1/6 divider circuits and provide indication of 1/100 second, 1/10 second, 1-second, 10-seconds, 1-minute and 10-minutes, respectively. If it is desired to provide chronograph indications from 1/100 second to 1-hour, additional divider circuits and digital display means may be provided. Thus, it is possible to provide a timepiece having more digits of digital display then are needed for operation of a normal watch, all of said digits being operated only when the chronograph mechanism is used.

When selector switch WC is engaged with the C contact, the instantaneous information in divider circuits 11-16 is displayed. When control switch S is pushed again, flip-flop circuit 17 is re-set and the operation of chronograph divider circuit 10, and therefore of chronograph divider circuits 11-16 is stopped. The information stored in the chronograph divider circuits at the instant that switch S is placed in the "stop" position would then be displayed on the digital display means. Thus, if the time at which control switch S was first pushed to start chronograph divider circuit 10 is t_1 and the time at which control switch S was again pushed to stop chronograph divider circuit 10 was t_2 , the elapsed time difference $t_2 - t_1$ is displayed on the digital display means 29-34.

Since divider circuits 3-9 are continuously operating irrespective of the setting of selector switch WC, the correct present time can be displayed on the digital display means by merely placing selector switch WC in the W position. The embodiment of FIG. 1 is provided with two series of divider circuits, namely, divider circuits 2-9 and divider circuits 10-16. However, in the embodiment of FIG. 1, the chronograph mechanism can only be stopped once in each series of readings so that more than one lap time cannot be measured by the timepiece of FIG. 1.

Referring now to FIG. 2, the electronic watch depicted overcomes the latter difficulty. Like elements in the circuit of FIG. 2 are assigned the same reference numerals as were assigned in the circuit of FIG. 1. The electronic watch of FIG. 2 is provided with two control switches S_1 and S_2 . Control switch S_1 corresponds to

control switch S of FIG. 1 and controls flip-flop 17 to start and stop chronograph divider 10. An AND gate 36 is provided associated with each of chronograph divider circuits 11-16, one input to said AND gates being the chronograph timing signal from the corresponding chronograph divider circuits. At the moment that control switch S_2 is operated, a sharp pulse is transmitted by pulse shaping circuit 35 to the other input of each of AND gate 36 to momentarily open said AND gates. Said pulse shaping circuit may be formed of a monostable multivibrator. At the instant that AND gate 36 is open, the information of each in chronograph divider circuits 11-16 is applied to respective memory circuits 37-42. Said memory circuits comprised, by way of example, of set-reset flip-flop circuits of the type described in Circuit Design of Digital Computers, by Joseph K. Hawkins, p. 276 (1968), FIG. 6.4, may take many forms. In the embodiment of FIG. 2, said memory circuits are provided with a re-set switch R_2 and the storage of information in the memory circuits would be accomplished after resetting by means of said switch S_2 . Storage in said memory circuits may also be achieved by breaking the old memory and immediately applying the new information thereto. The information stored in memory circuits 37-42 is applied to respective decoders 43-48 to drive the corresponding digits 49-54 of a chronograph digital display means separate and apart from the normal time keeping display means 29-34.

Since chronograph divider circuits 10-16 continue to operate until control switch S_1 is again operated, intermediate levels of elapsed time may be indicated by operation of control switch S_2 without interfering with the continued accumulation of elapsed time in chronograph divider circuits 10-16. This permits the measuring of an individual lap time. Where separate normal time displays 29-34 are provided, logic gates 20, 21 and 22 may be dispensed with along with selector switch WC and inverter 19. The outputs of divider circuits 4-9 would be applied directly to decoders 23-28 to provide a time indication. This arrangement requires a great amount of space and power, and is extremely expensive. Thus, the output of memory circuits 37-42 of FIG. 2 may be supplied to AND gate 21 in place of the output of chronograph divider circuits 11-16 as shown in FIG. 1 so that a chronograph adapted to measure lap times may be formed with only a single series of digital display means 29-34. Further, control switch S of FIG. 1, and control switch S_2 of FIG. 2 may be connected with a photoelectric switch or the like disposed outside the watch, so that elapsed time can be measured electronically and automatically.

The electronic timepiece according to the invention can be utilized as a stop watch without interfering with the normal time keeping operation of the watch and is particularly adapted for application to electronic timepieces utilizing digital displays. If the divider circuits, memory circuits, logic gates and decoders are formed from complementary MOS (metal oxide semiconductor transistor) integrated circuits, a timepiece operated by small amounts of energy can be readily obtained. Further, if liquid crystal displays or light emitting elements are utilized as the digital display elements, a full electronic timepiece can be readily constructed.

It will thus be seen that the objects set forth above, among those made apparent from the preceding description, are efficiently attained and, since certain changes may be made in the above constructions with-

out departing from the spirit and scope of the invention, it is intended that all matter contained in the above description or shown in the accompanying drawings shall be interpreted as illustrative and not in a limiting sense.

It is also to be understood that the following claims are intended to cover all of the generic and specific features of the invention herein described, and all statements of the scope of the invention which, as a matter of language, might be said to fall therebetween.

What is claimed is:

1. An electronic timepiece comprising pulse generator means for generating a relatively high frequency time standard signal; time keeping divider means for producing time keeping timing signals in response to said time standard signal; chronograph divider means for producing low frequency chronograph timing signals in response to said time standard signal, said chronograph divider means including a plurality of series-connected divider stages, a group of which produces said chronograph timing signals; means for selectively starting a first stage of said chronograph divider means producing a signal of a frequency greater than that of said chronograph timing signals at a time t_1 and stopping said chronograph divider means first stage at a time t_2 , independent of the operation of said time keeping divider means, resetting means coupled to said chronograph divider means for selectively and simultaneously resetting all of said chronograph divider means stages to a zero state; digital display means; and controlled gate means for the selective connection of one of said time keeping divider means and said group of chronograph divider means stages to said digital display means for the selective digital display of present time or elapsed time ($t_2 - t_1$) in response to said time keeping timing signals or said chronograph timing signals respectively.

2. An electronic timepiece as recited in claim 1, including memory means disposed intermediate said chronograph divider means and digital display means adapted for selective momentary connection to said chronograph divider means for detecting and storing the instantaneous state of said chronograph timing signals at a selected time t_3 , where $t_1 \leq t_3 \leq t_2$, without interrupting said chronograph divider means; said controlled gate means permitting the selective connection of said digital display means to one of said time keeping divider means and said memory means to provide a digital representation of present time or elapsed time up to said selected time ($t_3 - t_1$) in response to said time keeping timing signals or the instantaneous chronograph timing signals stored in said memory means.

3. An electronic timepiece as recited in claim 2, wherein said controlled gate means further selectively permits the display of elapsed time ($t_2 - t_1$) on said digital display means in response to said chronograph timing signals from said chronograph divider means.

4. An electronic timepiece as recited in claim 1, wherein said pulse generator means includes a quartz crystal oscillator; said time keeping divider means, chronograph divider means, controlled gate means, and means for selectively starting and stopping said chronograph divider means being formed from MOS integrated circuits.

5. An electronic timepiece as recited in claim 4, wherein said display means is formed from liquid crystal display means.

6. An electronic timepiece as recited in claim 4, wherein said display means is formed from light emitting elements.

7. An electronic timepiece as recited in claim 1, including a first divider circuit means for producing an intermediate signal of intermediate frequency from said time standard signal; said time keeping divider means including second divider circuit means including 1/10, 1/6, 1/10, 1/6, and 1/10 binary divider stages for producing said time keeping timing signals from said intermediate frequency signal; said chronograph divider means including third divider circuit means for producing a further intermediate signal of a frequency less than said first-mentioned intermediate signal from said first-mentioned intermediate signal and a fourth divider circuit means including 1/10, 1/10, 1/10, 1/6, 1/10 and 1/6 divider stages for producing said chronograph timing signals in response to said further intermediate signal; said means for stopping and starting said chronograph divider means being operatively connected to said third divider circuit means for the stopping and starting of said chronograph divider means.

8. An electronic timepiece as recited in claim 1, including decoder means positioned intermediate said controlled gate means and said digital display means for converting said time keeping timing signals and said chronograph timing signals into a form suitable for driving said digital display means.

9. An electronic timepiece as recited in claim 1, wherein the signal produced by said chronograph divider means first stage has a period of 1/100 second or less.

10. An electronic timepiece as recited in claim 1, wherein the signal produced by said chronograph divider means first stage has a period of 1/1000 second or less.

11. An electronic timepiece comprising pulse generator means for producing a high frequency time standard signal; time keeping divider means for producing low frequency time keeping timing signals in response to said time standard signal; chronograph divider means for producing low frequency chronograph timing signals in response to said time standard signal; means for selectively stopping and starting said chronograph divider means without affecting the operation of said time keeping divider means; memory means coupled to said chronograph divider means; switch means for selective momentary actuation of said memory means to detect and store the instantaneous chronograph timing signals at the moment of selective actuation without interrupting said chronograph divider means; digital display means; and controlled gate means for the selective coupling of said digital display means to one of said time keeping divider means and said memory means for the selective digital display of present time or elapsed time up to said time of actua-

tion of said memory means, respectively, in response to said time keeping time signals or said instantaneous chronograph timing signals, respectively.

12. An electronic timepiece as recited in claim 12, wherein said chronograph divider means includes a plurality of series-connected divider stages, said control gate means selectively connecting the group of said divider stages of said chronograph divider means producing said chronograph timing signals to said digital display means, said starting and stopping means being coupled to the first stage of said chronograph divider means, said first stage producing a signal of a frequency greater than that of said chronograph timing signals.

13. An electronic timepiece as recited in claim 11, including resetting means coupled to said chronograph divider means for selectively resetting said chronograph divider means to a zero state.

14. An electronic timepiece comprising pulse generator means for generating a high frequency time standard signal; time keeping divider means for producing low frequency time keeping timing signals in response to said time standard signal; chronograph divider means for producing low frequency chronograph timing signals in response to said time standard signal, said chronograph divider means including a plurality of series-connected divider stages; means for selectively starting and stopping a first stage of said chronograph divider means producing a signal of a frequency greater than that of said chronograph timing signals independent of said time keeping divider means, resetting means coupled to said chronograph divider means for selectively and simultaneously resetting all of said chronograph divider means stages to a zero state; first digital display means; means coupling said first digital display means to said time keeping divider means for the digital display of time in response to said time keeping timing signals; second digital display means; and means coupling said second digital display means to said chronograph divider means for the digital display of elapsed time between the starting and stopping of said chronograph divider means in response to said chronograph timing signals.

15. An electronic timepiece as recited in claim 15, wherein said means coupling said chronograph divider means and said second digital display means includes memory means adapted to selectively instantaneously detect and store the instantaneous chronograph timing signals from said chronograph divider means at the instant of actuation thereof without interrupting said chronograph divider means; and means for selectively actuating said memory means, said second digital display means displaying elapsed time between the start of said chronograph divider means and said instant of actuation in response to said stored instantaneous chronograph timing signals from said memory means.

* * * * *

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 3,795,099
DATED : March 5, 1974
INVENTOR(S) : Yuki Tsuruishi

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

On the title page, after the name of the Inventor,
insert --[73] Assignee: Kabushiki Kaisha Suwa Seikosha--.

Signed and Sealed this

twenty-sixth **Day of** *July* 1977

[SEAL]

Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents and Trademarks

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,795,099 Dated March 5, 1974

Inventor(s) Yuki Tsuruishi

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 8, line 4, the claim reference numeral "12" should read --11--.

Column 8, line 43, the claim reference numeral "15" should read --14--.

Signed and sealed this 3rd day of June 1975.

(SEAL)
Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
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and Trademarks