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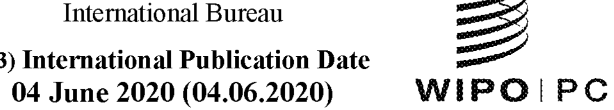

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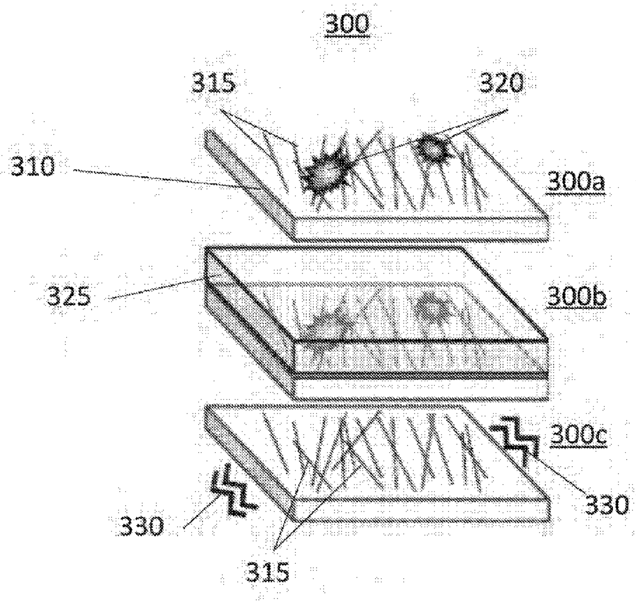

FIG. 3

(57) **Abstract:** A technology called RINSE (Removal of Incubated Nanotubes through Selective Exfoliation) is demonstrated. RINSE removes carbon nanotube (CNT) aggregates in CNFETs without compromising CNFET performance. In RINSE, CNTs are deposited on a substrate, coated with a thin adhesive layer, and sonicated. The adhesive layer is strong enough to keep the individual CNTs on the substrate, but not the larger CNT aggregates. When combined with a CNFET CMOS process as disclosed here, record CNFET CMOS yield and uniformity can be realized.

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[Continued on next page]

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RINSE - REMOVAL OF INCUBATED NANOTUBES THROUGH SELECTIVE EXFOLIATION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Provisional Application No. 62/773,419 filed November 30, 2018, titled “REMOVAL OF INCUBATED NANOTUBES THROUGH SELECTIVE EXFOLIATION”, the entire disclosure of which is incorporated herein by reference.

BACKGROUND

[0002] Carbon nanotube field effect transistors (CNFETs, shown in FIG. 1) are leading candidates for supplementing silicon complementary metal-oxide semiconductor (CMOS) transistors to realize next-generation energy-efficient digital systems. CNFETs are projected to improve the energy-delay product (EDP, a measure of energy efficiency) of digital very large scale integrated (VLSI) circuits by an order of magnitude vs. silicon CMOS. Moreover, CNFETs provide an exciting opportunity to naturally enable monolithic three-dimensional (3D) integrated circuits (ICs), whereby CNFETs are fabricated at low temperature on upper circuit layers (in the back-end-of-line (BEOL), potentially directly over starting silicon CMOS), leading to additional EDP benefits.

[0003] While academic and research labs have made important progress with carbon nanotubes (CNTs), there remain at least three major obstacles that have prohibited realizing an HVM-compatible CNT technology. The first obstacle is limited yield: carbon nanotube (CNT) deposition results in CNT aggregates as shown in FIG. 2. These CNT aggregates act as particle contamination, reducing die yield by inhibiting successful deposition of subsequent layers, contaminating CMOS fabrication facilities, and possibly breaking apart to scatter metallic CNTs on the substrate. While several techniques are used to remove these aggregates prior to CNT deposition (e.g., centrifugation or filtering), these techniques are complex, difficult to scale, and

could alter the CNTs themselves. And it is impossible to perfectly disperse and subsequently remove all aggregates prior to CNT deposition.

[0004] The second obstacle is production of robust, high-yield CNFET CMOS logic. Large-scale CNFET circuits have used positive metal-oxide semiconductor (PMOS)-only logic relying on circuits that are robust to errors, whereas CNFET CMOS demonstrations have been smaller scale (<150 CNFETs) and suffer from variability and lack wafer-scale characterization.

[0005] The third obstacle is compatibility with silicon CMOS: contaminants (both from the metal catalyst used during CNT synthesis as well as ions introduced during the semiconducting CNT sorting process) usually far exceed the allowable limits for use in commercial silicon facilities (contaminants introduce additional sources of device variability and failure), and techniques for realizing CNFET CMOS in research facilities are often not compatible with high-volume manufacturing (HVM) due to material or processing constraints. For instance, CNFET CMOS has been primarily realized by using reactive low work-function metals that are considered contaminants in silicon manufacturing facilities. Other methods for CMOS that do not meet HVM requirements include evaporating nanometer-thin layers of reactive metals, followed by allowing it to oxidize in ambient.

SUMMARY

[0006] A method of forming a layer of carbon nanotubes on a substrate includes depositing individual carbon nanotubes and at least one carbon nanotube aggregate on the substrate. The method further includes forming an adhesive layer on the individual carbon nanotubes and at least one carbon nanotube aggregate on the substrate. The adhesive layer adheres the individual carbon nanotubes to the substrate. The method further includes mechanically exfoliating the at least one carbon nanotube aggregate from the substrate.

[0007] A method of making a carbon nanotube logic device includes depositing individual carbon nanotubes and carbon nanotube aggregates on a substrate, and forming a polydimethyldiglutarimide (PMGI) layer on the substrate, the PMGI layer having a thickness of

about 100 nm to about 150 nm. The method also includes submerging the substrate in a solvent for a duration sufficient to remove a portion of the PMGI layer, and to retain a remaining portion of the PMGI layer. The method further includes sonicating the substrate in the solvent to remove the carbon nanotube aggregates from the substrate to yield a substrate surface coated with individual carbon nanotubes and fewer than 10 carbon nanotube aggregates per square millimeter, such that the remaining portion of the adhesive layer aids in maintaining adherence of the individual carbon nanotubes to the substrate during said sonicating.

[0008] A method of making a carbon nanotube field effect transistor (CNFET) complementary metal-oxide semiconductor (CMOS) device includes depositing a first channel of individual carbon nanotubes (CNTs) and a second channel of individual CNTs on the substrate, such that at least one carbon nanotube aggregate is also deposited on the substrate. The method further includes forming an adhesive layer on the substrate, the adhesive layer adhering the first channel and the second channel to the substrate. The method also includes mechanically exfoliating the at least one carbon nanotube aggregate from the substrate. The method further includes forming, in electrical contact with the first channel, a first source electrode and a first drain electrode to generate a p-type metal-oxide semiconductor (PMOS) CNFET. The method also includes forming, in electrical contact with the second channel, a second source electrode and a second drain electrode to generate an n-type metal-oxide semiconductor (NMOS) CNFET.

[0009] A carbon nanotube logic device includes a substrate, and a first adhesive layer formed on the substrate. The device also includes a channel of individual CNTs deposited on the first adhesive layer. The first adhesive layer promotes adhesion of the channel of individual CNTs to the substrate. The device further includes a second adhesive layer deposited on the substrate and on the channel of individual CNTs to maintain adhesion of the channel of individual CNTs to the substrate.

[0010] It should be appreciated that all combinations of the foregoing concepts and additional concepts discussed in greater detail below (provided such concepts are not mutually inconsistent) are contemplated as being part of the inventive subject matter disclosed herein. In particular, all combinations of claimed subject matter appearing at the end of this disclosure are contemplated as

being part of the inventive subject matter disclosed herein. It should also be appreciated that terminology explicitly employed herein that also may appear in any disclosure incorporated by reference should be accorded a meaning most consistent with the particular concepts disclosed herein.

BRIEF DESCRIPTIONS OF THE DRAWINGS

[0011] The skilled artisan will understand that the drawings primarily are for illustrative purposes and are not intended to limit the scope of the inventive subject matter described herein. The drawings are not necessarily to scale; in some instances, various aspects of the inventive subject matter disclosed herein may be shown exaggerated or enlarged in the drawings to facilitate an understanding of different features. In the drawings, like reference characters generally refer to like features (e.g., functionally similar and/or structurally similar elements).

[0012] FIG. 1 shows schematic (top) and scanning electron microscope (SEM) (bottom) images of a typical back-gate CNFET.

[0013] FIG. 2 illustrates CNFETs whose yield is limited by CNT aggregates (“bundles”) that deposit on wafers (the bottom SEM image shows a CNT aggregate over a CNT monolayer).

[0014] FIG. 3 illustrates an example of the RINSE process: step (1) deposit CNTs; step (2) deposit polydimethyldiglutarimide (PMGI) photoresist and cure; and step (3) sonicate in solvent.

[0015] FIG. 4A shows CNFETs made without the adhesion coating in RINSE. Without the adhesion coating, sonicating the wafer removes CNTs.

[0016] FIG. 4B shows CNFETs made without the adhesion coating in RINSE. The adhesion coating leaves an atomic layer of carbon that remains after sonication, adhering CNTs to the wafer after removing aggregates.

[0017] FIG. 5A shows that RINSE does not impact CNTs/ CNFETs, and is a plot of CNT density versus sonication time and shows that the CNT density is the same pre- vs. post-RINSE.

[0018] FIG. 5B also shows that RINSE does not impact CNTs/ CNFETs, and is a plot of CNFET I_D-V_{GS} characteristics showing that RINSE causes minimal change

[0019] FIG. 5C also shows that RINSE does not impact CNTs/ CNFETs, and is a plot CNFET I_D-V_{GS} characteristics showing that CNFETs can still be doped NMOS after RINSE.

[0020] FIG. 6A is an image illustrating CNT aggregates on a substrate, pre-RINSE.

[0021] FIG. 6B shows the substrate of FIG. 6A, after RINSE, and illustrates a reduction in CNT aggregates.

[0022] FIG. 6C is a plot illustrating that RINSE reduces CNT aggregate density by >250× and can be optimized by modifying sonication power and time.

[0023] FIG. 7 is an example CNFET CMOS process flow diagram. Both the PMOS and NMOS CNFETs use a back-gate geometry, and the doping to realize the NMOS can be accomplished by (1) metal contact work function engineering (e.g., platinum is used for PMOS source/drain, while titanium is used for NMOS source/drain) or (2) electrostatic doping. In step 1, platinum back-gates are deposited on a SiO_2 substrate. In step 2, HfO_2 is deposited via atomic layer deposition (ALD). In step 3, CNTs are deposited and patterned, consistent with RINSE. In step 4, platinum source and drain electrodes are deposited for the PMOS. In step 5, a passivation layer of SiO_2 is deposited on the PMOS. In step 6, titanium source and drain electrodes are deposited for the NMOS. In step 7, a nonstoichiometric oxide is deposited on the NMOS via ALD. Notably, in step 7, the ALD-deposited oxide electrostatically dopes CNTs in NMOS CNFETs, while CNTs in PMOS are protected by the passivation layer deposited in step 5.

[0024] FIG. 8 is a plot of CNFET CMOS I_D-V_{DS} characteristics for PMOS and NMOS CNFETs (for varying V_{GS}), fabricated following the processing flow in FIGS. 6A-6B, where the length L is about 2 μm and width W is about 2 μm.

[0025] FIG. 9A illustrates wafer-scale CNFET CMOS fabrication and characterization, and illustrates a 150 mm wafer, die area: 2 cm × 2 cm. Each die contains 10,400 CNFET CMOS NOR2 gates (and therefore 41,600 CNFETs)

[0026] FIG. 9B illustrates experimental measurements of the wafer of FIG. 9A, showing the voltage transfer curves (VTCs) of all 10,400 CNFET CMOS NOR2 gates, without any outliers removed. The functional yield is 10,400/10,400. The first VTC plot (leftmost plot) shows the output voltage (V_{OUT}) when input voltage "A" ($V_{IN,A}$) is swept from 0 to 1.2V while input voltage "B" ($V_{IN,B}$) is held constant at 0 V. The second VTC plot shows V_{OUT} when $V_{IN,A}$= 0 and $V_{IN,B}$ is swept form 0 to 1.2V. The third VTC plot shows V_{OUT} when $V_{IN,A}$ is swept from 0 to 1.2V while $V_{IN,B}$=1.2V. The fourth VTC plot (rightmost plot), shows V_{OUT} when $V_{IN,B}$ is swept from 0 to 1.2V while $V_{IN,A}$= 1.2V.

[0027] FIG. 10 is a plot illustrating definitions of key metrics extracted from VTC. SNM: static noise margin; H = high, L = low.

[0028] FIG. 11A is a distribution of "output low" voltage (V_{OL}), "output high" voltage (V_{OH}), "input low" voltage (V_{IL}), and "input high" voltage (V_{IH}) for the 10,400 CMOS NOR2 logic gates when $V_{IN,B}$ = 0V and $V_{IN,A}$ is swept from 0 to V_{DD} .

[0029] FIG. 11B is a distribution of output swing as a percent of V_{DD} when for the 10,400 CMOS NOR2 logic gates when $V_{IN,B}$ = 0V and $V_{IN,A}$ is swept from 0 to V_{DD} .

[0030] FIG. 11C is a distribution of gain when for the 10,400 CMOS NOR2 logic gates when $V_{IN,B}$ = 0V and $V_{IN,A}$ is swept from 0 to V_{DD}.

[0031] FIG. 11D is a plot of distribution of "output low" voltage (V_{OL}), "output high" voltage (V_{OH}), "input low" voltage (V_{IL}), and "input high" voltage (V_{IH}) for the 10,400 CMOS NOR2 logic gates when $V_{IN,A}$ = 0V and $V_{IN,B}$ is swept from 0 to V_{DD} .

[0032] FIG. 11E is a distribution of output swing as a percent of V_{DD} when for the 10,400 CMOS NOR2 logic gates when $V_{IN,A}$ = 0V and $V_{IN,B}$ is swept from 0 to V_{DD}.

[0033] FIG. 11F is a distribution of gain when for the 10,400 CMOS NOR2 logic gates when $V_{IN,A}$ = 0V and $V_{IN,B}$ is swept from 0 to V_{DD}. FIGS. 11A-11F generally show the metrics defined in FIG. 10 for the 10,400 CNFET CMOS NOR2 logic gates measured in FIG. 9. V_{DD} is 1.2 V.

[0034] FIG. 12A is a distribution of the static noise margin high values (SNMH) for input A.

[0035] FIG. 12B is a distribution of the static noise margin low values (SNML) for input A.

[0036] FIG. 12C is a distribution of the static noise margin high values (SNMH) for input B .

[0037] FIG. 12D is a distribution of the static noise margin low values (SNML) for input B. Generally, FIGS. 12A-12D show histograms of SNM extracted by analyzing >100 million logic gate pairs (cascading every pair of NOR2 gates above, using the equations from FIG. 10). The percentages of cascaded gate pairs that have positive SNM are: 99.90% (SNMH,A) 99.94% (SNML,A) 99.98% (SNMH,B) 99.92% (SNML,B). V_{DD} is 1.2 V.

[0038] FIG. 13 illustrates spatial dependence of V_{IH} (as an example parameter to compute SNM). Each pixel represents the V_{IH} of the NOR2 at that location in the die. V_{IH} increases across the die (increasing from top to bottom). The change in V_{IH} corresponds with slight changes in CNFET threshold voltage. The fact that the threshold voltage variations are not uniformly distributed, but rather have spatial dependence, illustrates that a portion of the threshold voltage variations (and therefore variation in SNM) is due to wafer-level processing-related variations (CNT deposition is more uniform across the 150 mm wafer). Optimizing uniformity of the ALD oxide deposition used for electrostatic doping could further improve SNM for realizing VLSI circuits.

[0039] FIG. 14A illustrates four dies across a 150 mm wafer, each die includes 10,400 CNFETs.

[0040] FIG. 14B shows wafer-scale CNFET CMOS characterization of the dies of FIG. 14A. 1000 CNFET CMOS NOR2 logic gates are sampled randomly from the ensemble of 10,400 CNFETs in each die. No outliers are removed. The top four distributions in FIG. 14B correspond to the four sampling locations and show distributions of output voltage swings for the 1000 CNFET CMOS NOR2 gates when $V_{IN,A}$ is swept from 0 to V_{DD} and $V_{IN,B}$=0. The bottom four distributions in FIG. 14B also correspond to the four sampling locations and show distributions of output voltage swings for the 1000 CNFET CMOS NOR2 gates when $V_{IN,B}$ is swept from 0 to V_{DD} and $V_{IN,A}$=0. Yield and performance variations are negligible across wafer as illustrated by the distribution of the output voltage swing.

[0041] FIG. 15 illustrates a pilot implementation of CNFETs within a commercial silicon manufacturing facility. CNFETs were fabricated on upper circuit layers (conventional planarized

Tungsten plugs were used as embedded back-gates and all CNFET-related fabrication is low temperature: < 400 °C). The SEM image shows an embedded metal gate covered with gate dielectric and CNTs.

[0042] FIG. 16 illustrates plots of experimental I_D-V_{GS} of 100 PMOS (left plot) and 100 NMOS (right plot) CNFETs fabricated in a commercial facility.

[0043] FIG. 17 shows that customized CNT solution preparations successfully remove chemical contaminants from the solution, confirmed with laser-ablation ICP-MS. The 70 elements listed in FIG. 17 had contamination below the detectable limits and within the requirements for introducing CNTs within commercial silicon fabrication facilities.

[0044] FIG. 18A is an image of a fabricated RV16X-NANO chip. The die area is 6.912 mm × 6.912 mm, with input/output pads placed around the periphery. Scanning electron microscopy images with increasing magnification are shown inset. RV16X-NANO is fabricated entirely from CNFET CMOS, in a wafer-scalable, VLSI-compatible, and silicon-CMOS compatible fashion.

[0045] FIG. 18B is a three-dimensional to-scale rendered schematic of the RV16X-NANO physical layout (all dimensions are to scale except for the z axis, which is magnified to clarify each individual vertical layer). RV16X-NANO leverages a new three-dimensional (3D) physical architecture in which the CNFETs are physically located in the middle of the stack, with metal routing both above and below.

[0046] FIG. 19A is a block diagram of the architecture and design of RV16X-NANO, showing the organization of RV16X-NANO, including the instruction fetch, instruction decode, register read, execute + memory access, and write-back stages.

[0047] FIG. 19B is a schematic describing the high-level register transfer level (RTL) description of each stage of the design of FIG. 19A, including inputs, outputs and signal connections.

[0048] FIG. 20A shows an experimentally measured waveform from RV16X-NANO, executing the ‘Hello, World’ program. The waveform shows the 32-bit instruction fetched from memory, the program counter stored in RV16X-NANO, as well as the character output from RV16X-NANO.

Below the waveform, the binary output (shown in hexadecimal code) is converted to their ASCII characters to their ASCII characters, showing RV16X-NANO printing out "Hello, world! I am RV16XNano, made from CNTs." In addition to this program, functionality was tested by executing all of the 31 instructions within RV32E (see Example 3).

[0049] FIG. 20B shows RV16X-NANO as designed using conventional electronic design automation (EDA) tools, leveraging a CNT process design kit as disclosed here, and a CNT CMOS standard cell library. An example combinational cell (full-adder) and example sequential cell (D-flip-flop) are shown alongside an optical microscopy image of the fabricated cells, their schematics, as well as their experimentally measured waveforms. For the full-adder, shown here are the outputs (sum and carry-out outputs) for all possible biasing conditions in which sweeping the voltage of input (from 0 to V_{DD}) causes a change in the logical state of the output (that is, for the full adder, with $C_{OUT} = A*B + B*C_{IN} + A*C_{IN}$, with A = logical '0' and B = logical '1', then sweeping C_{IN} from '0' to '1' causes C_{OUT} to change from logical '0' to logical '1'). (C_I indicates C_{IN} and C_O indicates C_{OUT}.) For the sum output S(V_{OUT}), there are 12 such conditions: six where V_{OUT} has the same polarity as the swept input (positive unate) and six where V_{OUT} has the opposite polarity to the swept input (negative unate). For the carry-out output C(V_{OUT}) there are six such conditions (all positive unate); the measurements are overlaid over one another. Gain for all transitions is >15, with output voltage swing >99%. The D-flip-flop waveform (voltage versus time) illustrates correct functionality of the positive edge-triggered D-flip-flop (output state Q shows correct functionality based on data input D and clock input CLK). CK and $\bar{C}\bar{K}$ are the clock input and the inverse of the clock input, respectively.

[0050] FIG. 21A illustrates design and manufacturing flow for RV16X-NANO, illustrating how the manufacturing methodology described herein seamlessly integrates within conventional silicon-based EDA tools. Black boxes show conventional steps in silicon-CMOS design flows. The "fabricate CNFET..", "Bottom metal layers", "Deposit CNTs…" and "Top metal layers…" steps are adjusted for CNTs instead of silicon. The "DREAM-enforcing…", "MIXED…" and "RINSE" steps represent the additions to implement the manufacturing methodology. RV16X-NANO is the first hardware demonstration of a beyond-silicon emerging nanotechnology

leveraging a complete RTL-to-GDS physical design flow. Software packages are from Synopsys, Cadence, and Mentor Graphics.

[0051] FIG. 21B illustrates scanning electron microscopy images showing that CNTs inherently bundle together, forming thick CNT aggregates. These aggregates result in CNFET failure (reduced CNFET yield) as well as prohibitive particle contamination for VLSI manufacturing.

[0052] FIG. 21C illustrates the Removal of Incubated Nanotubes through Selective Exfoliation (RINSE) process steps: (1) CNT incubation, (2) adhesion coating, (3) mechanical exfoliation (see text for details).

[0053] FIG. 21D shows how, after performing RINSE, CNT aggregates are removed from the wafer.

[0054] FIG. 21E shows that after performing RINSE, the individual CNTs not in aggregates are not removed from the wafer, while without RINSE, sonication inadvertently removes large areas of all CNTs from the wafer. Top panel shows CNT incubation pre-RINSE, middle panel shows CNTs left on the wafer post-RINSE, and the bottom panel shows CNTs inadvertently removed from the wafer after sonicating a wafer to remove CNT aggregates without performing the adhesion-coating step in RINSE.

[0055] FIG. 21F illustrates particle contamination reduction due to RINSE. RINSE decreases particle density by >250×.

[0056] FIG. 21G shows how increasing the time of step 3 of FIG. 21C (sonication time) to over 7 hours results in no change in CNT density across the wafer.

[0057] FIG. 22A is a schematic of CNFET CMOS fabricated using Metal Interface engineering Crossed with Electrostatic Doping (MIXED). MIXED is a combined doping process that leverages both metal contact work-function engineering as well as electrostatic doping to realize a robust wafer-scale CNFET CMOS process. Employed here are platinum contacts and SiOx passivation for p-CNFETs, and titanium contacts and HfOx passivation for n-CNFETs.

[0058] FIG. 22B shows dies fabricated with 10,400 CNFET CMOS digital logic gates across 150-mm wafers to characterize MIXED.

[0059] FIG. 22C illustrates I_D versus V_{DS} characteristics showing p-CNFETs and n-CNFETs that exhibit similar I_D–V_{DS} characteristics (for opposite polarity of input bias conditions, for example, $V_{DS,P} = -V_{DS,N}$), achieved with MIXED. The gate-to-source voltage V_{GS} is swept from $-V_{DD}$ to V_{DD} in increments of 0.1 V. See Example 2 for I_D–V_{GS} and additional CNFET characteristics.

[0060] FIG. 22D illustrates output voltage transfer curves (VTCs, V_{OUT} versus V_{IN}) for all 10,400 CNT CMOS logic gates (nor2) within a single die of FIG. 22B. Each VTC illustrates V_{OUT} as a function of the input voltage of one input (V_{IN}), while the other input is held constant. For each nor2 logic gate (with logical function OUT = !(IN_A|IN_B), the VTC is measured for each of two cases: V_{OUT} versus $V_{IN,A}$ with $V_{IN,B}$ = 0 V and V_{OUT} versus $V_{IN,B}$ with $V_{IN,A}$ = 0 V). All 10,400/10,400 exhibit correct functionality (defined as having output voltage swing >70%). The middle dotted line represents the average VTC (average V_{IN} across all measured VTC for each value of V_{OUT}), while the outer dotted lines represent the boundary of ±3 standard deviations (again, across all V_{IN} values for each value of V_{OUT}). See Example 4 for extracted distributions of key metrics from these experimental measurements (gain, output voltage swing and SNM analyzing >100 million possible cascaded logic gates pairs formed from these 10,400 samples), as well as uniformity characterization across the 150-mm wafer. Despite the high yield and robust CNFET CMOS enabled by MIXED and RINSE, there are outlier gates with degraded output swing (the outermost lines). These outliers are caused by CNT CMOS logic gates that contain metallic CNTs; the third component of the manufacturing methodology (DREAM), is a design technique for overcoming the presence of these metallic CNTs.

[0061] FIG. 23A illustrates, for DREAM, VTCs for driving logic stages and mirrored VTCs for loading logic stages, showing SNM simulated for 4 different logic stage pairs, with up to two metallic CNTs in all CNFETs. The logic stage pairs: (nand2, nand2) and (nor2, nor2) have lower SNMs than do (nand2, nor2) and (nor2, nand2) despite all logic stages having exactly the same VTCs. Logic stages (for example, an inverter) are distinguishable from logic gates (for example, a buffer, by cascading two inverters), where a logic gate can include multiple logic stages.

Generally, DREAM overcomes the presence of metallic CNTs through circuit design, and is one component of the manufacturing methodology. DREAM relaxes the requirement on metallic CNT purity by about 10,000×, without imposing any additional processing steps or redundancy. DREAM is implemented using standard EDA tools, has minimal cost (≤10% energy, ≤ 10% delay and ≤ 20% area), and enables digital VLSI systems with CNT purities that are available commercially today (e.g., 99.99% semiconducting CNT purity).

[0062] FIG. 23B is an example DREAM SNM table (analyzed for a projected 7-nm node with a scaled VDD of 500 mV), which shows the minimum SNM for each pair of connected logic stages. As an example, values less than 83 mV are highlighted and indicate that these combinations would not be permitted during design, to reduce overall susceptibility to noise at the VLSI circuit level.

[0063] FIG. 23C illustrates yield (p_{NMS}) versus semiconducting CNT purity for a required SNM level (SNM_R) of $SNM_R = V_{DD}/5$, shown for the OpenSparc 'dec' module designed using the 7-nm node CNFET standard library cells derived from the ASAP7 process design kit with a scaled VDD of 500 mV.

[0064] FIG. 23D shows a fabricated CNT CMOS die including 1,000 NMOS CNFETs and 1,000 PMOS CNFETs. Semiconducting CNT purity is $p_S \approx 99.99\%$, with around 15–25 CNTs per CNFET.

[0065] FIG. 23E illustrates VTCs for nand2 and nor2 generated by randomly selecting two NMOS and two PMOS CNFETs from FIG. 23D (some of which contain metallic CNTs). This is repeated to form 1,000 unique nor2 (left panel) and nand2 (right panel) VTCs. The (nor2, nor2) logic stage pairs maintain minimum SNM > 0, while the (nand2, nor2) logic stage pairs suffer from minimum SNM < 0 in the presence of metallic CNTs; >99.99% of the (nor2, nor2) and (nand2, nand2) logic stage pairs achieve SNM > 0 V, while about 97% of the (nand2, nor2) logic stage pairs achieve SNM > 0 V.

[0066] FIG. 23F illustrates cumulative distributions of SNM over one million logic stage pairs. The SNMs for over one million logic stage pairs are analyzed and correspond to all combinations

of 1,000 VTCs for the driving logic stage and 1,000 VTCs for the loading logic stage shown in FIG. 23E.

[0067] FIGS. 24A–24N illustrate the fabrication process flow for RV16X-NANO.The fabrication process is a 5-metal-layer (M1 to M5) process and involves >100 individual process steps. s-CNT, semiconducting CNT; S/D, source/drain. FIG. 24A illustrates patterning of the first metal layer.

[0068] FIG 24B illustrates deposition of an interlayer dielectric.

[0069] FIG. 24C illustrates patterning and etching of vias.

[0070] FIG. 24D illustrates bottom gate formation.

[0071] FIG. 24E illustrates atomic layer deposition of the gate dielectric.

[0072] FIG. 24F illustrates additional etching of vias.

[0073] FIG. 24G illustrates CNT deposition.

[0074] FIG. 24H illustrates etching to remove CNTs outside the CNFET.

[0075] FIG. 24I illustrates PMOS source and drain formation via metal layer deposition.

[0076] FIG. 24J illustrates passivation via SiO_2 deposition.

[0077] FIG. 24K illustrates NMOS source and drain formation via metal layer deposition.

[0078] FIG. 24L illustrates deposition of a nonstoichiometric doping oxide (NDO).

[0079] FIG. 24M illustrates additional etching of vias and removal of the NDO over the PMOS CNFET.

[0080] FIG. 24N illustrates formation of terminals for power distribution.

[0081] FIG. 25 is a microscopy image of a full fabricated RV16X-NANO die. The processor core is in the middle of the die, with test circuitry surrounding the perimeter (when the RV16X-NANO is diced for packaging, these test structures are removed). The test structures include test structures for monitoring fabrication, as well as for measuring and characterizing all of the 63 standard cells in the standard cell library of FIG. 26.

[0082] FIG. 26 illustrates a CNFET standard cell library. This is a list of all of the standard cells in a standard cell library as disclosed herein, along with a microscopy image of each fabricated standard cell, the schematic of each cell, and a typical measured waveform from each fabricated cell. As expected for static CMOS logic stages, the CNFET logic stages exhibit output voltage swing exceeding 99% of V_{DD}, and achieve gain of >15. Experimental waveforms are not shown for cells whose functionality is not demonstrated by output voltage as a function of either input voltage or time; for example, for cells without outputs (for example, fill cells: cell names that start with 'fill_' or decap cells: cell names that start with 'decap_'), for cells whose output is constant (tied high/low: cell names that start with 'tie_'), or for transmission gates (cell names that start with 'tg_').

[0083] FIG. 27 is an image of a completed RV16X-NANO 150-mm wafer. Each wafer includes 32 dies.

[0084] FIG. 28A illustrates the negligible effect of RINSE on CNTs and CNFETs, and that CNT density is the same pre- versus post-RINSE.

[0085] FIG. 28B illustrates how the CNFET I_D–V_{GS} curve exhibit minimal change for sets of CNFETs fabricated with and without RINSE (V_{DS} = −1.8 V for all measurements shown). Both samples came from the same wafer, which was diced after the CNT deposition but before the RINSE process. One sample underwent RINSE while the other sample did not.

[0086] FIG. 28C is a plot illustrating that CNFETs can still be doped NMOS after the RINSE process, leveraging the MIXED process (VDS = −1.2 V for all measurements shown).

[0087] FIG. 29A shows definitions of metrics for characterizing logic gates, including SNM, gain and swing. V_{OH}, V_{IH}, V_{IL} and V_{IL} (labelled on the VTCs, where (V_{IL}, V_{OH}) and (V_{IH}, V_{OL}) are the points on the VTC where $\Delta V_{OUT}/\Delta V_{IN} = -1$) are used to extract the noise margin: SNM = min(SNM_H, SNM_L).

[0088] FIG. 29B illustrates metrics (defined in FIG. 29A) extracted for the 10,400 CNFET CMOS nor2 logic gates. V_{DD} is 1.2 V.

[0089] FIG. 29C illustrated SNM extraction based on the distributions from FIG. 29B. >100 million logic gate pairs are analyzed based on these experimental results.

[0090] FIG. 29D shows spatial dependence of V_{IH} (as an example parameter to compute SNM). Each pixel represents the VIH of the nor2 at that location in the die. VIH increases across the die (from top to bottom). The change in VIH corresponds with slight changes in CNFET threshold voltage. The fact that the threshold voltage variations are not independently and identically distributed (i.i.d.), but rather have spatial dependence, illustrates that a portion of the threshold voltage variations (and therefore variation in SNM) is due to wafer-level processing-related variations (CNT deposition is more uniform across the 150-mm wafer).

[0091] FIG. 29E illustrates wafer-scale CNFET CMOS characterization. Measurements from 4 dies across 150-mm wafer (1,000 CNFET CMOS nor2 logic gates are sampled randomly from the 10,400 such logic gates in each die). No outliers are excluded. Yield and performance variations are negligible across the wafer, as illustrated by the distribution of the output voltage swing.

[0092] FIG. 30A generally illustrates the effect of metallic CNTs on digital VLSI circuits, and specifically shows reduction in CNFET EDP benefits versus p_S (metallic CNTs increase I_{OFF}, degrading EDP). $p_S \approx 99.999\%$, sufficient to minimize EDP cost due to metallic CNTs to $\leq 5\%$. Results are simulated for VLSI circuit modules from a 7-nm node processor core.

[0093] FIG. 30B illustrates, p_{NMS} versus p_S (metallic CNTs degrade SNM), (shown for $SNM_R = V_{DD}/5$, and for a circuit of one million logic gates). Although 99.999% p_S is sufficient to limit EDP degradation to $\leq 5\%$, this plot shows that SNM imposes stricter requirements on purity: $p_S \approx 99.999999\%$ to achieve pNMS $\geq 99\%$. Results are simulated for VLSI circuit modules from a 7-nm node processor core.

[0094] FIG. 31A generally shows a methodology to solve VTCs using CNFET I–V measurements, and specifically illustrates experimentally measured I_D versus VGS for all 1,000 NMOS (V_{DS} = 1.8 V) and 1,000 PMOS CNFETs (V_{DS} = −1.8 V), with no CNFETs omitted. Metallic CNTs (m-CNTs) present in some CNFETs result in high off-state leakage current ($I_{OFF} = I_D$ at V_{GS} = 0 V). CNFETs are fabricated at a ~1 μm technology node, and the CNFET width is 19 μm.

[0095] FIG. 31B shows VTC and SNM parameter definitions, for example, for (nand2, nor2). DR is the driving logic stage; LD is the loading logic stage. SNM = min(SNM_H, SNM_L), where SNM_H = V_{OH}(DR) – V_{IH}(LD) and SNM_L = V_{IL}(LD) – V_{OL}(DR).

[0096] FIG. 31C illustrates example I_D versus V_{DS} for NMOS and PMOS CNFETs (V_{GS} is swept from −1.8 V to 1.8 V in 0.1-V increments).

[0097] FIG. 31D is a circuit schematic to solve a VTC (for example, V_{OUT} versus V_A with V_B = V_{DD}): for each V_A, find V_1 and V_{OUT} such that i_{PA} + i_{PB} = i_{NA} = i_{NB} (DC, direct current, convergence).

[0098] FIG. 31E illustrates current in the pull-up network (i_{PU}, where i_{PU} = i_{PA} + i_{PB}, and i_{PA} and i_{PB} are the labelled drain currents of the PMOS FETs gated by A and B, respectively) and current in the pull-down network (i_{PD}, where i_{PD} = i_{NA} = i_{NB}, and i_{NA} and i_{NB} are the labelled drain currents of the NMOS FETs gated by A and B, respectively) versus V_{OUT} and V_A. The VTC is seen where these currents intersect.

[0099] FIG. 32A generally illustrates DREAM implementation and methodology, and specifically shows standard cell layouts (derived using the ‘asap7sc7p5t’ standard cell library), illustrating the importance of CNT correlation: because the length of CNTs (which can be of the order of hundreds of micrometers) is typically much longer compared with the CNFET contacted gate pitch (CGP, for example about 42–54 nm for a 7-nm node), the number of s-CNTs and m-CNTs in CNFETs can be uncorrelated or highly correlated depending on the relative physical placement of CNFET active regions. For many CMOS standard cell libraries at sub-10-nm nodes, the active regions of FETs are highly aligned, resulting in highly correlated number of m-CNTs among CNFETs in library cells, further degrading VTCs (because one m-CNT can affect multiple CNFETs simultaneously).

[00100] FIG. 32B generally illustrates how to generate a variation-aware CNFET SNM model, shown for a D-flip-flop (dff) derived from the asap7sc7p5t standard cell library. Specifically, shown is a layout used to extract netlists for each logic stage.

[00101] FIG. 32C is a schematic illustrating how CNFETs are grouped by logic stage (with nodes arbitrarily labelled 'D', 'MH', 'MS', 'SH', 'SS', 'CLK', 'clkn', 'clkb' and 'QN' for ease of reference).

[00102] FIG. 32D shows that for each extracted netlist, there can be multiple VTCs: for each logic stage output, a logic stage input is sensitized if the output state (0 or 1) depends on the state of that input (given the states of all the other inputs). For example, for a logic stage with Boolean function: Y = !(A*B+C), C is sensitized when (A, B) = (0, 0), (0, 1) or (1, 0). All possible VTCs are simulated (over all logic stage outputs and sensitized inputs), and also in the presence of m-CNTs. For example, FIG. 32D shows a subset of the VTCs for the logic stage in FIG. 32B with output node 'MH' (labelled in FIG. 32C), and sensitized input 'D' (with labelled nodes ('clkb', 'clkn', 'MS') = (0, 1, 0)). The dashed line indicates VTC with no m-CNTs, and the solid lines are example VTCs in the presence of m-CNTs (including the effect of CNT correlation). In each case, VOH, VIH, VIL and VOL are modeled as affine functions of the number of m-CNTs (M_i) in each of r regions (M_1, ..., M_r), with calibration parameters in the static noise margin (SNM) model matrix T (shown in FIG. 32F).

[00103] FIG. 32E illustrates an example calibration of the SNM model matrix T for the VTC parameters extracted in FIG. 32D. The symbols are VTC parameters extracted from circuit simulations (using Cadence Spectre), and solid lines are the calibrated model.

[00104] FIG 32F illustrates the Affine model form used to compute SNM in the presence of metallic carbon nanotubes (m-CNTs).

[00105] FIG. 32G illustrates design flow to optimize energy and delay of CNFET digital VLSI circuits, including: (1) library power/timing characterization (using Cadence Liberate) across multiple VDD and using parasitics extracted from standard cell layouts (derived from the asap7sc7p5t standard cell library), in conjunction with a CNFET compact model; (2) Synthesis (using Cadence Genus), place-and-route (using Cadence Innovus) with back-end-of-line (BEOL) wire parasitics from the ASAP7 process design kit (PDK); (3) Circuit EDP optimization: both VDD and target clock frequency are swept (during synthesis/place-and-route) to create multiple

physical designs. The one with best EDP is used to compare design options (for example, DREAM versus baseline).

[00106] FIG. 32H illustrates a subset of logic gates in an example circuit module, showing the effect of CNT correlation at the circuit level (for example, the m-CNT counts of CNFETs $P_{3,1}$ and $P_{5,1}$ are both equal to $M_1 + M_2 + M_3$).

[00107] FIG. 32I illustrates distribution of SNM over all connected logic stage pairs, for a single sample of the circuit m-CNT counts. The minimum SNM for each trial limits the probability that all noise margin constraints in the circuit are satisfied (p_{NMS}).

[00108] FIG. 32J illustrates cumulative distribution of minimum SNM over 10,000 Monte Carlo trials, shown for multiple target p_S values, where p_S is the probability that a given CNT is a semiconducting CNT. These results are used to find p_{NMS} versus p_S for a target SNM requirement (SNM_R), where p_{NMS} is the fraction of trials that meet the SNM requirement for all logic stage pairs. Note that p_{NMS} can then be exponentiated to adjust for various circuit sizes based on the number of logic gates.

[00109] FIG. 32K illustrates CNFET compact model parameters (for example, for a 7-nm node).

[00110] FIG. 33 illustrates details of implementing RISC-V instruction set architecture. The top panel shows all supported instructions implemented in RV16X-NANO, adhering to RISC-V format specifications for RV32E, with high-level description summary for each. Each instruction is categorized into one of six formats, including instruction type (R-type, I-type, S-type, U-type) and immediate variant (I-immediate, U-immediate, B-immediate, J-immediate, S-immediate), forming one of six formats (type immediate): R, I-I, I-U, S-B, S-S, U-J (shown in the bottom panel). For the assembly code, ‘rd’ is the destination register, ‘rs1’ is the source register 1, ‘rs2’ is the source register 2, ‘imm’ is immediate. The bottom panel shows the bit-level description of each instruction format. The bottom 7 bits (inst[6:0]) are always the OPCODE, and then the remaining bits are decoded depending on the instruction format (determined by the OPCODE). Values that are crossed out indicate bits that are not used for the 16-bit data path implementation (RV16E)

with four registers, instead of 32-bit data path implementation (RV32E) with 16 registers. For example, for instruction 'auipc', only 2 of the 5 reserved bits for 'rd' are required to address the register file for register 'rd' (because there are only 22 = 4 registers instead of 25 = 32), and also the upper 16 bits of the 32-bit immediate (that is, imm[31:16]) are not used because the data path is truncated to 16 bits.

DETAILED DESCRIPTION

[00111] Conventional CNT deposition processes result in CNT bundles (bundles of CNTs are sometimes referred to as "CNT aggregates"), resulting in prohibitive particle contamination and reduced CNFET yield. Disclosed and demonstrated herein is a new technique, called RINSE (Removal of Incubated Nanotubes through Selective Exfoliation), that reduces CNT aggregate density by >250× without affecting CNT deposition or CNFET performance. In RINSE, CNTs are deposited on a substrate, coated with a thin adhesive layer, and sonicated. The adhesive layer is strong enough to keep the individual CNTs on the substrate, but not the larger CNT aggregates. While the sonication removes a significant portion of the adhesive layer, although a residual adhesive layer can remain. This residual layer can aid in maintaining adherence of the deposited CNTs on the substrate. RINSE can be used to deposit other "solution-processed" nanomaterials, i.e., materials that are spin-coated, ink-jet printed, or dropped onto wafer surface, including 2D materials (e.g., graphene), and/or to remove dust or other aggregates in silicon processing.

[00112] By combining RINSE with a CNT doping process as described herein, high yield and robust wafer scale CNFET CMOS can be achieved. For example, entire dies with 10,400 CNFET CMOS digital logic gates (functional yield 10,400/10,400 CMOS gates, 41,600 CNFETs) are achievable, and presented herein is the first wafer-level CNFET CMOS uniformity characterization across 150 mm wafers, such as extracting static noise margin by analyzing >100 million possible cascaded logic gate pairs. These methods meet the stringent contamination levels required inside silicon HVM facilities, leverages conventional materials and processing techniques available within silicon HVM facilities, and can realize high yields for thousands of CNFET CMOS digital logic gates.

RINSE: Removal of Incubated Nanotubes through Selective Exfoliation

[00113] FIG. 2 shows a wafer for forming CNFETs, on which CNTs have been deposited from solution. As a result, CNT aggregates 210 are inadvertently deposit on the wafer as well, as illustrated. The CNFET yield, or the die yield of such a substrate, is limited by such CNT aggregates 210 ("bundles") that deposit on wafers.

[00114] Current techniques for removing these particle contaminants include high-power sonication, centrifugation, and filtering. Unfortunately, these techniques are insufficient for at least four reasons. First, excessive high-power sonication for dispersing aggregates in solution damage CNTs degrades CNFET performance and does not disperse all CNTs. Second, centrifugation does not remove all smaller aggregates, and aggregates can re-form post centrifugation. Third, excessive filtering can remove both aggregates and the CNTs themselves from the solution. Fourth, etching the aggregates is infeasible due to a lack of selectivity relative to the underlying individual CNTs themselves.

[00115] FIG. 3 illustrates a RINSE process/method 300 that can remove CNT aggregates. A first step 300a in the process 300 includes CNT incubation, where individual CNTs (e.g., in solution) are deposited on a substrate/wafer 310 that can be pre-treated with a CNT adhesion promoter (e.g., HMDS, Bis(trimethylsilyl)amine). For example, the pre-treatment can involve exposing the substrate/wafer 310 to HMDS vapor at a reduced pressure, at about 150 °C. This results in formation of a monolayer of HMDS on the surface that can aid promote CNT adhesion. This can result in the deposition of desirable, individual CNTs 315, and undesirable CNT aggregates 320 on the substrate 310.

[00116] The CNT solution concentration can range from 1 mg/100mL to 0.01 mg/100 mL (including all values and sub-ranges in between) with a semiconducting CNT purity ranging from 99.9% to 99.99% (including all values and sub-ranges in between). Said another way, when the purity is 99.99%, then 99.99% of CNTs in solution are semiconducting and 0.01% of CNTs in solution are metallic. A higher concentration of CNTs can generally yield faster CNT deposition, and can result in more and/or larger CNT aggregates 320. The CNT solution includes individual

CNTs dispersed in an organic solvent such as, for example, xylene or toluene. The CNTs may or may not be wrapped in a selective polymer, i.e., be polymer-wrapped CNTs.

[00117] The CNTs can be deposited by submerging/incubating the wafer in the CNT solution for >10 minutes, during which time the CNTs form a uniform film on the wafer. For example, the time duration of immersion of the wafer in the CNT solution can be based on the concentration of the CNT solution (i.e., grams of CNTs per unit volume of solution). More concentrated CNT solutions will require less time to deposit, whereas less concentrated CNT solutions can require more time, e.g., over 48 hours of wafer immersion in the CNT solution, to achieve a desired deposition density. The deposition can be carried out at room temperature, though the use of higher and/or lower temperatures is also possible. Once a desired CNT film/network of deposited CNTs of uniformity and thickness is achieved, the wafer is removed from the CNT solution, rinsed in a solvent such as acetone or IPA (iso-propyl alcohol) to remove any CNT solution that remains on the wafer after the wafer is removed from the CNT solution, and then dried with nitrogen gas. Similar results can be attained through techniques other than incubation such as, for example, spin-coating, dip-coating, and/or the like. For example, CNTs can be deposited onto a wafer by spin coating the CNT solution onto the wafer and allowing the CNT solution to uniformly spread over the wafer during the spinning process. CNTs can also be deposited onto a wafer by dip-coating for example, where the wafer is dipped into bath of CNT solution and removed at a controlled rate while CNTs deposit at the interface where the wafer meets the surface of the CNT solution bath.

[00118] The next step 300b in the process 300 can include adhesion coating, where an adhesive layer 325, such as a photoresist material, is spin-coated on the wafer 310 (including on the individual CNTs 315 as well as the CNT aggregates 320) and then cured to evaporate any remaining solvent. The photoresist can include, for example, polymethylglutarimide (PMGI), hexamethyldisilazane (HMDS), SPR, and/or the like. Generally, any suitable positive resist, the exposure of which to UV light will change the chemical properties of the resist so that the resist can be developed, can be used. The curing can be carried out at, for example, about 235 °C for PMGI or about 90 °C for SPR, and can generally be any suitable temperature less than about 400

°C. Curing aids in developing the photoresist so that it acts as an adhesion layer. The adhesive layer 325 may have a thickness of about less than 1 nm to about 1.5 μm (e.g., less than about 1 nm for HMDS, about 100–150 nm for PMGI, or about 1–1.5 μm for SPR), including all values and sub-ranges in between.

[00119] In this manner, when an adhesion promoter is used as described in relation to step 300a, the layer of adhesion promoter can be considered a first adhesive layer than is useful for promoting CNT adhesion, and the adhesive layer 325 can be considered a second adhesive layer than is useful for maintaining adhesion of the desirable CNTs during exfoliation as described below for step 300c. The first adhesive layer, the second adhesive layer, or both, can be optional in some cases.

[00120] The next step 300c in the process 300 can include exfoliation, such as mechanical exfoliation to remove the CNT aggregates 320. While described here with respect to removing the aggregates 320, the exfoliation at step 300c can also remove other undesirable particles, such as nanoparticles, dust, polymer residue, undesirable particle contaminants, and/or the like, that may be present on and/or deposited on the wafer 310, such as during deposition of the CNTs at step 300a.

[00121] The wafer 310 is placed in a solvent (e.g., N-Methyl-2-Pyrrolidone (NMP) for PMGI photoresist) and sonicated, as indicated by the sonication waves 330 in FIG. 3, for long enough to remove a portion of the adhesive layer 325. For instance, a wafer 310 with a PMGI adhesive layer 325 may be submerged in an NMP bath (not shown) for one hour at room temperature to remove some portion of the PMGI. Another portion of the adhesive layer 325, e.g., about 1 to 2 nm of PMGI, may be left behind to form a remaining portion (e.g., about 1-2 nm thick, including all values and sub-ranges in between), as indicated by an increase in surface roughness of the CNTs. This remaining portion can act as an adhesive to maintain the desirable, individual CNTs on the water. The wafer with the remaining portion is then sonicated for about 40 minutes to remove the aggregates 320. Generally, the duration of sonication can be about 5 minutes, 10 minutes, 30 minutes, 40 minutes, one hour, or more (including all values and sub-ranges in between), and the degree of removal of the aggregates is relatively greater for a longer duration of

sonication. The solvent in the sonicator (not shown) may be filtered and/or circulated to prevent the build-up and dispersion of the aggregates 320 shaken off the wafer 310. Accordingly, the step 300c can sometimes encompass two separate steps or sub-steps, where the first step includes placing the water 310 in the solvent to be submerged for some suitable duration. The second step can then include sonication. In this way, there is a time gap between the first step and the second step during which the water 310 is submerged in the solvent but not sonicated.

[00122] The adhesion coating/layer 325 deposited in step 300b can prevent the sonication from inadvertently removing desirable sections of individual CNTs 315 in addition to the aggregates 320 (see FIG. 4). Without being bound by any particular theory, the adhesion coating can leave an atomic layer of carbon that remains after step 300c, which exerts sufficient force to adhere the CNTs to the wafer surface while still allowing for the removal of the aggregates.

[00123] Experimental results of RINSE are shown in FIGS. 4–6. By optimizing the adhesion coating cure temperature and time as well as the sonication power and time, RINSE can reduce CNT aggregate density by >250× (when quantified by the number of CNT aggregates per unit area) without damaging the desirable CNTs or impacting CNFET performance, as best illustrated in FIG. 5. The reduction in CNT aggregate density can be to fewer than ten CNT aggregates per square millimeter, or to fewer than one CNT aggregate per square millimeter, including all values and sub-ranges in between.

[00124] Step 300b can be optional. Specifically, depending on the sonication parameters, the adhesion coating/layer 325 formed in step 300b may not be required. Instead, the substrate 310 can be submerged in a CNT solution for CNT deposition as in step 300a above. Then the substrate would be sonicated as in step 300c, skipping the adhesion coating as in step 300b, with a sonication pulse sequence, sonication frequency, sonication amplitude, and/or sonication medium selected to remove the CNT aggregates without exfoliating the individual CNTs from the substrate. For example, the sonication parameters for step 300c when the adhesion coating is formed at step 300b can include a sonication frequency at 35 kHz at 180W RF power. If step 300b is not employed, a reduced sonication frequency and/or RF power setting can be used, such as, for example, a sonication frequency below 35kHz and/or a RF power setting below 180W.

[00125] Further, as described below for FIG. 7 and in even further detail in Example 2, the individual CNTs 315 retained on the wafer 310 can be electrostatically doped to be n-channel CNTs.

Wafer-Scale CNFET CMOS

[00126] Leveraging RINSE, FIG. 7 illustrates an example process flow/method 700 for fabricating a wafer-scale CNFET CMOS, and/or any CNT-based logic device generally. At step (1) of the method 700, back-gates 705a, 705b are deposited on a wafer/substrate 710, where both back-gates 705a, 705b can be composed of platinum. At step (2) of the method 700, a dielectric layer 715 is deposited on the substrate 710. The layer 715 can be composed of a nonstoichiometric oxide, such as HFO_2. The layer 715 can be deposited via atomic layer deposition (ALD).

[00127] At step (3) of the method 700, CNT channels 720a, 720b can be selectively deposited and patterned. Deposition of the CNT channels can be carried out using the RINSE approach as detailed above for FIG. 3. In some cases, steps 300a, 300b, and 300c can be executed for creating the CNT channels 720a, 702b, while in other cases, as noted for FIG. 3, step 300b (depositing an adhesion layer) may be omitted. For example, step (3) of the method 700 can encompass deposition of individual CNTs and (as a result) of CNT aggregates on the substrate 710. It can also encompass forming a photoresist layer, such as a layer of PMGI, on the CNT channels 720a, 720b. The photoresist layer can have a thickness of about 100 nm to about 150 nm. Then, the substrate 710 can be immersed, submerged, and/or otherwise incubated in a solvent for a time period as necessary or desirable to remove a portion of the photoresist layer and to retain some remaining portion of it. The substrate 710 can be sonicated in the solvent to mechanically remove any CNT aggregates without removing individual CNTs. In some cases, fewer than 1-10 CNT aggregates per square millimeter remain on the substrate 710, and the remaining portion of the adhesive layer aids in maintaining adherence of the individual CNTs to the substrate 710. As noted above for FIG. 3, in some cases, a CNT adhesion promoter is deposited on the substrate 710 prior to deposition of the CNTs to form the CNT channels 720a, 720b.

[00128] At step (4) of the method 700, a source terminal/electrode 725a and drain terminal/electrode 730a are formed for the PMOS CNFET in electrical contact with the CNT channel 720a. These electrodes can be formed of platinum as illustrated in FIG. 7. At step (5) of the method 700, a passivation layer 735 (e.g., composed of or including SiO_2 as illustrated in FIG. 7) is deposited on the PMOS CNFET to protect the PMOS CNFET from oxide deposition at step (7) (explained below for method 700, and in greater detail in Example 2).

[00129] At step (6) of the method 700, source terminal/electrode 725b and drain terminal/electrode 730b is formed for the NMOS CNFET in electrical contact with the CNT channel 720b, and can be formed of titanium as illustrated. The use of a lower work function metal (titanium) as contacts for NMOS CNFETs and a higher work function metal (platinum) as contacts for PMOS CNFETs improve the on-state drive current of both (for a given off-state leakage current).

[00130] Returning to FIG. 7, at step (7) of the method 700, nonstoichiometric HfO_X is deposited over the CNTs 720b via atomic layer deposition (ALD). The oxide electrostatically dopes the CNTs 720b, while the CNTs 720a in the PMOS CNFET are protected by the passivation layer 735 deposited in step (5).

[00131] In summary, both the PMOS and NMOS CNFETs in FIG. 7 use a back-gate geometry, and the doping to realize the NMOS CNFET is accomplished through (1) engineering of metal contact work function (platinum is used for the PMOS source/drain, while titanium is used for NMOS source/drain), and (2) electrostatic doping. This process leverages silicon CMOS compatible materials, allows for precise threshold voltage tuning through controlling the stoichiometry of the ALD doping oxide, and is robust due to tight process control afforded by ALD.

[00132] FIG. 9A shows a 150 mm wafer with test patterns that are duplicated on each die and include the NOR2 gates to be measured. Each die of the wafer has 10,400 CNFET CMOS two-input “not-or” (NOR2) logic gates. Separate NOR2 logic gates are fabricated and measured as this can enable characterization of several gate-level metrics, including the voltage transfer

curves (VTCs, which are used to compute the static noise margin of cascaded logic gates) V, gain, and output voltage swing (see FIG. 10 for definitions of relevant metrics). The experimentally measured VTCs for all 10,400 CNFET CMOS NOR2 logic gates are shown in FIG. 9B, and no logic gates have been excluded. The functional yield, which is defined as having an output voltage swing >70% V_{DD}, for all logic gates within the die is 10,400/10,400.

[00133] To illustrate the uniformity of the CNFET CMOS, FIGS. 11A-11F show distributions and extraction of the key metrics for all of the 10,400 logic gates in FIG. 9A (for instance, the average output voltage swing is >98% V_{DD} with <1% standard deviation). By extracting V_{OH}, V_{OL}, V_{IH}, and V_{IL} from the VTCs associated with each of the 10,400 logic gates, one can calculate the static noise margin (SNM) of all combinations of two cascaded NOR2 gates (i.e., with driving logic gate and loading logic gate). FIGS. 12A-12D show the distributions of the SNM for the >100 million possible combinations of cascaded logic gate pairs (i.e., with a driving logic gate and a loading logic gate): 99.93% of logic gate pairs have positive noise. FIGS. 12A-12D show the VTC (for example, V_{IH}) has spatial dependency. The CNT deposition is highly uniform across the substrate and exhibits substantially no spatial dependencies, which is indicative that sources of threshold variations are likely processing induced.

[00134] FIG. 13 shows that the noise margin violations (SNM < 0) can partially be attributed to the wafer processing (i.e., not the CNTs), and therefore can be improved by optimizing processing (e.g., by increasing ALD doping oxide uniformity over the 150 mm wafer). Additionally, FIGS. 14A-14B show wafer-scale CNFET CMOS characterization: measurements across four additional dies distributed across the 150 mm wafer (1000 CNFET CMOS NOR2 logic gates are sampled randomly from the 10,000 ensemble in each die; as before no logic gates are removed) illustrating yield across the 150 mm wafer (total yield across wafer: 14,400/14,400 logic gates, 57,600 CNFETs). This is the first demonstration of large-area, uniform, and high-yield CNFET CMOS logic, enabled by combining RINSE with the CNFET CMOS fabrication process.

Example 1 - Fabrication in an HVM Facility

[00135] To demonstrate that the entire CNFET process is HVM-compatible, shown here is an implementation of CNFETs within a commercial silicon manufacturing facility. The CNFETs are fabricated on upper circuit layers in the BEOL. Planarized tungsten plugs are used as the embedded back-gates and all CNFET-related fabrication was at low temperature (e.g., < 400 °C) to avoid damaging BEOL metal layers or devices fabricated beneath the CNFETs. (FIG. 15, I_D-V_{GS} curves in FIG. 16). Customized CNT solution preparations successfully removed chemical contaminants from the CNT solution as confirmed through inductively coupled plasma mass spectrometry (ICP-MS) analysis of the wafers post-CNT deposition (FIG. 17). The CNFET process was the same as detailed for FIG. 7, showing that the same high-yield process is HVM-compatible as well as scalable to more scaled nodes. The CNFETs are manufactured at a range of nodes in the commercial silicon facility, down to sub-250 nm nodes (sub-10 nm CNFETs have been experimentally demonstrated previously).

Example 2 - Microprocessor Built from Carbon Nanotube Transistors

[00136] Electronics is approaching a major paradigm shift as silicon transistor scaling no longer yields historical energy efficiency benefits, spurring research on beyond-silicon nanotechnologies. In particular, carbon nanotube (CNT) field-effect transistor (CNFET)-based digital circuits promise significant energy efficiency benefits, but the inability to perfectly control intrinsic nanoscale defects and variability in CNTs have made realizing very-large-scale systems infeasible. Here, these challenges are overcome to experimentally show a beyond-silicon microprocessor built entirely from CNFETs. This 16-bit microprocessor is based on the RISC-V instruction set, runs standard 32-bit instructions on 16-bit data and addresses, comprises >14,000 complementary metal-oxide-semiconductor (CMOS) CNFETs, and is designed and fabricated using industry-standard design flows and processes. This demonstration uses a set of combined processing and design techniques for overcoming nanoscale imperfections at macroscopic scales.

[00137] With diminishing returns of silicon field-effect transistor (FET) scaling, the need for FETs leveraging nanotechnologies has been steadily increasing. Carbon nanotubes (or CNTs,

nano-scale cylinders made of a single sheet of carbon atoms with diameters of ~10-20 Å) are prominent among a variety of nanotechnologies that are being considered for next generation energy-efficient electronic systems . Due to the nano-scale dimensions and simultaneously high carrier transport of CNTs , digital systems built from FETs fabricated with CNTs as the transistor channel (i.e., CNFETs) are projected to improve energy efficiency of today’s silicon-based technologies by an order of magnitude.

[00138] Over the past decade, CNT technology has progressed in maturity: from single CNFETs to individual digital logic gates to small-scale digital circuits and systems. In 2013, this progress led to the demonstration of a complete digital system: a miniature computer comprising 178 CNFETs that implemented only a single instruction operating on only a single bit of data (see Example 3 for a full discussion of prior work). However, as with all emerging nanotechnologies, there remained a significant disconnect between these small-scale demonstrations and modern systems comprising tens of thousands of FETs (e.g., microprocessors) to billions of FETs (e.g., high performance computing servers). Perpetuating this divide is the inability to achieve perfect atomic-level control of nanomaterials across macroscopic scales (e.g., yielding consistent 10 Å diameter CNTs uniformly across industry-standard 150-300 mm diameter wafer substrates). Resulting intrinsic defects and variations have made realizing such modern systems infeasible. For CNTs, these major intrinsic challenges are:

[00139] *Material defects*: while semiconducting CNTs (s-CNTs) form energy-efficient FET channels, the inability to precisely control CNT diameter and chirality results in every CNT synthesis containing some percentage of metallic CNTs (m-CNTs). m-CNTs have little to no bandgap and therefore their conductance cannot be sufficiently modulated by the CNFET gate, resulting in high leakage current and potentially incorrect logic functionality.

[00140] *Manufacturing defects*: during wafer fabrication, CNTs “bundle” together forming thick CNT aggregates. These aggregates can result in CNFET failure (reducing CNFET circuit yield), as well as prohibitively high particle contamination rates for very-large-scale integration (VLSI) manufacturing.

[00141] *Variability*: energy-efficient complementary metal-oxide-semiconductor (CMOS) digital logic requires the ability to fabricate CNFETs of complementary polarities (*p*-CNFETs and *n*-CNFETs) with well-controlled characteristics (e.g., tunable and uniform threshold voltages, and *p*- and *n*-CNFETs with matching on- and off-state current). Prior techniques for realizing CNFET CMOS have relied on either extremely reactive, not air-stable, non-silicon CMOS compatible materials or have lacked tunability, robustness, and reproducibility. This severely limited the complexity of CNT CMOS demonstrations, and no complete CNT CMOS digital system has ever been fabricated till date.

[00142] While substantial prior work has focused on overcoming these challenges, none meets all of the strict requirements for realizing VLSI systems. In this work, the intrinsic CNT defects and variations are overcome to enable the first demonstration of a beyond-silicon modern microprocessor: RV16X-NANO, designed and fabricated entirely using CNFETs. RV16X-NANO is a 16-bit microprocessor based on the open-source and commercially available RISC-V instruction set processor, running standard RISC-V 32-bit instructions on 16-bit data and addresses. It integrates >14,000 CMOS CNFETs, and operates as modern microprocessors today (e.g., it can run compiled programs; in addition, its functionality is demonstrated by executing all types and formats of instructions in the RISC-V instruction-set architecture (ISA)). This is made possible by a set of original processing and circuit design techniques that are combined to overcome the intrinsic CNT challenges. The elements of this manufacturing methodology for CNTs are:

[00143] RINSE (Removal of Incubated Nanotubes through Selective Exfoliation): removes CNT aggregate defects through a new selective mechanical exfoliation process. RINSE can reduce CNT aggregate defect density by >250× without affecting non-aggregated CNTs or degrading CNFET performance.

[00144] MIXED (Metal Interface engineering Crossed with Electrostatic Doping): this combined CNT doping process leverages both metal contact work function engineering as well as electrostatic doping to realize the first robust wafer-scale CNFET CMOS process. Entire dies with >10,000 CNFET CMOS digital logic gates (2-input “not-or” gates with functional yield

14,400/14,400, comprising 57,600 total CNFETs) are made, and presented here is the first wafer-scale CNFET CMOS uniformity characterization across 150 mm wafers (such as analyzing yield for >100 million combinations pairs of cascaded experimental logic gates).

[00145] DREAM (Designing Resiliency Against Metallic CNTs): overcomes the presence of m-CNTs entirely through circuit design. DREAM relaxes the requirement on m-CNT purity by ~10,000× (from 99.999,999% m-CNT purity requirement relaxed to 99.99%), without imposing any additional processing steps or redundancy. DREAM is implemented using standard electronic design automation (EDA) tools, has minimal cost, and enables digital VLSI systems with CNT purities that are available commercially today.

[00146] The entire Manufacturing Methodology for CNTs is wafer-scale, VLSI-compatible, and is seamlessly integrated within existing infrastructures for silicon CMOS – both in terms of design and processing. RV16X-NANO is designed with standard EDA tools, and leverages materials and processes that are compatible with and exist within commercial silicon CMOS manufacturing facilities.

[00147] RV16X-NANO – FIG. 18A shows an optical microscopy image of a fabricated RV16X-NANO die alongside three-dimensional to-scale rendered schematics of the physical layout. It is the largest CMOS electronic system ever realized using beyond-silicon nanotechnologies: comprising 3,762 CMOS digital logic stages, totaling 14,702 CNFETs containing >10 million CNTs, and includes logic paths comprising up to 86 stages of cascaded logic between flip-flops (i.e., that evaluate sequentially in a single clock cycle). It operates with 1.8 supply voltage (V_{DD}), receives an external referenced clock (generating local clock signals internally), receives inputs (instructions and data) from and writes directly to an off-chip main memory (dynamic random-access memory: DRAM), and stores data on-chip in a register file – no other external biasing or control signals are supplied. Furthermore, RV16X-NANO demonstrates a new three-dimensional (3D) physical architecture, as the metal interconnect layers are fabricated both above and below the layer of CNFETs (see FIG. 18B). This is in stark contrast to silicon-based systems where all metal routing can only be fabricated above the bottom layer of silicon FETs. In RV16X-NANO, the metal layers below the CNFETs are primarily used for signal

routing, while the metal layers above the CNFET are primarily used for power distribution (FIG. 18B). The fabrication process implements 5 metal layers and includes >100 individual processing steps. Such new 3D layout promises improved routing congestion (a major challenge for today's systems), and is uniquely enabled by CNTs (due to their low-temperature fabrication)

[00148] Physical Design - The design flow of RV16X-NANO can leverage industry-standard tools and techniques: here, a standard process design kit (PDK) for CNFETs as well as a library of standard cells for CNFETs was created that is compatible with existing EDA tools and infrastructure without modification. This CNFET PDK includes a compact model for circuit simulations that is experimentally calibrated to the fabricated CNFETs. The standard cell library comprises 63 unique cells, and includes both combinational and sequential circuit elements implemented with both static CMOS and complementary transmission-gate digital logic circuit topologies (see Example 4 for a full list of standard library cells, including circuit schematic and physical layouts). The CNFET PDK is used to characterize the timing and power for all of the library cells, which are experimentally validated by fabricating and measuring all cells individually (see Example 4 for full description and experimental characterization of the standard cell library). A full description of the VLSI design methodology, including how DREAM is implemented during logic synthesis and place-and-route, is provided below.

[00149] Computer Architecture – FIGS. 19A-19B illustrate the architecture of RV16X-NANO, which can follow conventional microprocessor design (implementing instruction fetch, instruction decode, register read, execute/ memory access, and write-back stages). It is designed from RISC-V, a standard open instruction set architecture used in commercial products today and gaining wide-spread popularity in both academia and industry . RV16X-NANO is derived from a full 32-bit RISC-V microprocessor supporting the RV32E instruction set (31 different 32-bit instructions, see Supplemental Information), while truncating the data path width from 32-bits to 16-bits, and reducing the number of registers from 16 to 4. It is designed using publicly available Bluespec, and is verified using SMT-based bounded model checking against a formal specification of the RISC-V ISA (see Supplemental Information). Correct functionality of the microprocessor is demonstrated by experimentally running and validating correct functionality of all types and

formats of instructions on the fabricated RV16X-NANO. FIGS. 20A-20B show the first program executed on RV16X-NANO: the famous “Hello, world”, as described further below

[00150] Manufacturing Methodology for CNTs - Described here is a manufacturing methodology for CNTs – a set of combined processing and design techniques for making the RV16X-NANO (FIG. 21A). All design and fabrication processes are wafer-scale and VLSI compatible, not requiring any per-unit customization or redundancy.

[00151] RINSE - The CNFET fabrication process begins by depositing CNTs uniformly over the wafer. 150 mm wafers (with the bottom metal signal routing layers and gate stack of the CNFET already fabricated for the 3D design) are submerged in solutions containing dispersed CNTs (Methods). While CNTs uniformly deposit over the wafer, the CNT deposition also inherently results in manufacturing defects, where CNT aggregates deposited randomly across the wafer (FIG. 21B). These CNT aggregates act as particle contamination, reducing die yield. While several existing techniques have attempted to remove these aggregates prior to CNT deposition, none is sufficient to meet wafer-level yield requirements for VLSI systems: (a) excessive high-power sonication for dispersing aggregates in solution damages CNTs, resulting in degraded CNFET performance, and does not disperse all CNTs; (b) centrifugation does not remove all smaller aggregates (and aggregates can re-form post centrifugation), (c) excessive filtering removes both aggregates and the CNTs themselves from the solution, and (d) etching the aggregates is infeasible due to lack of selectivity versus the underlying CNTs themselves. To remove these aggregates, a new process technique, RINSE, is developed that consists of three steps (FIG. 21C):

[00152] 1) CNT incubation: solution-based CNTs are deposited on wafers pre-treated with a CNT adhesion promoter (HMDS, Bis(trimethylsilyl)amine).

[00153] 2) Adhesion coating: a standard photoresist (Polymethylglutarimide, PMGI) is spin-coated on the wafer and cured at ~200 °C.

[00154] 3) Mechanical exfoliation: the wafer is placed in solvent (NMP) and sonicated.

[00155] Without adhesion coating (step 2), sonicating the wafer may inadvertently remove section of CNTs in addition to the aggregates (FIG. 21D). The adhesion coating leaves an atomic layer of carbon that remains after step 3, which can exert sufficient force to adhere the CNTs to the wafer surface while still allowing for the removal of the aggregates. Experimental results for RINSE are shown in FIGS. 21D-21G. By optimizing the adhesion-coating cure temperature and time as well as the sonication power and time, RINSE reduces CNT aggregate density by >250× (quantified by the number of CNT aggregates per unit area) without damaging the CNTs or impacting CNFET performance (see Example 4).

[00156] MIXED - After using RINSE to overcome intrinsic CNT manufacturing defects, CNFET circuit fabrication continues. While energy-efficient CMOS logic requires both *p*-CNFETs and *n*-CNFETs with controlled and tunable properties (such as threshold voltage), techniques for realizing CNT CMOS today result in significant FET-to-FET variability that has made realizing large-scale CNFET CMOS systems infeasible. Moreover, the vast majority of existing techniques are not air-stable (e.g., they use materials that are extremely reactive in air), are not uniform or robust (e.g., they do not always successfully realize CMOS), or rely on materials not compatible with conventional silicon CMOS processing (e.g., molecular dopants that contain ionic salts prohibited in commercial fabrication facilities).

[00157] These challenges are overcome by the processing technique MIXED, described in FIGS. 22A-22D. MIXED is based on a combined doping approach that engineers both the oxide deposited over the CNTs to encapsulate the CNFET as well as the metal contact to the CNTs. First, the CNFETs are encapsulated in oxide (deposited by atomic-layer deposition, ALD) to isolate them from their surroundings. By leveraging the atomic-layer control of ALD, the precise stoichiometry of this oxide encapsulating the CNTs is engineered, which enables simultaneous electrostatic doping of the CNTs (the stoichiometry dictates both the amount of redox reaction at the oxide-CNT interface as well as the fixed charge in the oxide). In addition, the metal source/drain contacts to the CNTs are engineered to further optimize the *p*- and *n*-CNFETs. A lower work function metal (Titanium) is employed as contacts to *n*-CNFETs and a higher work function metal is employed as contacts to *p*-CNFETs (Platinum), improving the on-state drive

current of both (for a given off-state leakage current). In contrast to previous approaches, MIXED leverages silicon CMOS-compatible materials, allows for precise threshold voltage tuning through controlling the stoichiometry of the ALD doping oxide, and is robust due to tight process control by using ALD and air-stable materials.

[00158] FIG. 22C shows the current-voltage (*I-V*) characteristics of *p*-CNFETs and *n*-CNFETs, demonstrating well-matched characteristics (such as on- and off-state currents). To demonstrate the reproducibility of MIXED at a wafer scale, FIG. 22D shows measurements from 10,400/10,400 correctly functioning 2-input "not-or" (NOR2) CNFET logic gates within a single die, and 1,000/1,000 correctly functioning NOR2 gates randomly selected from across a 150 mm wafer. Additional characterization results (including output voltage swing, gain, and static noise margin for >100 million possible combinations of cascaded logic gate pairs), are in Example 4. This is the first wafer-scale demonstration of solid-state, air-stable, VLSI- and silicon-CMOS compatible CNFET CMOS.

[00159] DREAM - Despite the robust CNFET CMOS enabled by RINSE and MIXED, a small percentage (~0.01%) of CNTs are m-CNTs, which stems from a major fundamental CNT material defect: the random presence of m-CNTs. Unfortunately, 0.01% m-CNT fraction can be prohibitively large for VLSI-scale systems, due to two major challenges: (1) increased leakage power, degrading EDP benefits, and (2) degraded noise immunity, potentially resulting in incorrect logic functionality. To quantify noise immunity of digital logic, the static noise margin (*SNM*) is extracted for each pair of connected logic stages, using the voltage transfer curves (*VTCs*) of each stages (details in FIGS. 32A-32K). The probability that all connected logic stages meet a minimum SNM requirement (SNM_R, typically chosen by the designer as a fraction of V_{DD}, e.g., $SNM_R = V_{DD}/4$) is p_{NMS}: the probability that all noise margin constraints are satisfied. While previous works have set requirements on s-CNT purity (p_S) based on limiting m-CNT-induced leakage power, no existing works have provided VLSI circuit-level guidelines for p_S based on both increased leakage and the resulting degraded SNM. While 99.999% p_S is sufficient to limit EDP degradation to ≤5%, SNM imposes far stricter requirements on purity: p_S ~99.999,999% to achieve $p_{NMS} \geq 99\%$ (analyzed for 1 million gate circuits, Example 4).

[00160] Unfortunately, typical CNT synthesis today achieves p_S ~66%. While many different techniques have been proposed to overcome the presence of m-CNTs (Supplemental Information), the highest reported purity is ~99.99% p_S: 10,000× below the requirement for VLSI circuits[34,35,36]. Moreover, these techniques have significant cost, requiring either: (a) additional processing steps (e.g., applying high voltages for electrical "breakdown" of m-CNTs during fabrication[10]) or (b) redundancy incurring significant energy efficiency penalties. Presented and experimentally validated here is a new technique, DREAM, that overcomes, for the first time, the presence of m-CNTs entirely through circuit design. DREAM reduces the required p_S by ~10,000×, allowing 99% p_{NMS} with p_S = 99.99% (for 1 million logic gate circuits). This enables digital VLSI circuits using CNT processing available today: p_S = 99.99% is already commercially available (and can be achieved through several means, including solution-based sorting which is used in the process for fabricating RV16X-NANO).

[00161] The key insight for DREAM is that m-CNTs affect different pairs of logic stages uniquely depending on how the logic stages are implemented (considering both the schematic and physical layout). As a result, the SNM of specific combinations of logic stages is more susceptible to m-CNTs. To improve overall p_{NMS} for a digital VLSI circuit, DREAM applies a logic transformation during logic synthesis to achieve the same circuit functionality, while prohibiting the use of specific logic stage pairs whose SNM is most susceptible to m-CNTs. As an example, let (G_D, G_L) be a logic stage pair with driving logic stage G_D and loading logic stage G_L. FIGS. 23A-23F show that some logic stage pairs have better SNM in the presence of m-CNTs versus others, despite using the exact same VTCs for the logic stages comprising the circuit (in this instance, logic stage pairs (nand2, nand2) and (nor2, nor2) have better SNM than (nand2, nor2) or (nor2, nand2)). Thus, a designer can improve p_{NMS} by prohibiting the use of logic stage pairs that are more susceptible to m-CNTs, while permitting logic stage pairs that maintain better SNM despite the presence of m-CNTs. Beyond this example to illustrate DREAM, the benefit of DREAM is quantified using both simulation and experimental analysis for VLSI-scale circuits; in simulation, a compact model for CNFETs is leveraged, which accounts for both s-CNTs and m-CNTs, to analyze the impact of m-CNTs on the leakage power, energy consumption, speed, and

noise susceptibility of physical designs of VLSI-scale circuits at a 7 nm technology node designed using standard EDA tools, with and without DREAM (results in FIGS. 23A-23F, additional discussion in Example 4). 2,000 CMOS CNFETs are fabricated with MIXED (1,000 PMOS and 1,000 NMOS CNFETs: FIGS. 23A-23F) and characterized. Using I-V measurements from these 2,000 CNFETs, 1 million combinations of CNFET digital logic gates are analyzed (whose electrical characteristics are solved using the I-V characteristics of the measured CNFETs, FIGS. 32A-32K) to show the benefits of DREAM to improve circuit susceptibility to noise. Further details of these analysis and implementation of DREAM for arbitrary digital VLSI circuits are provided below, including how to implement DREAM using standard industry-practice physical design flows, how to implement DREAM for RV16X-NANO, and an efficient algorithm to satisfy target p_{NMS} constraints (e.g., $p_{NMS} \geq 99\%$), while minimizing energy, delay, and area costs.

[00162] These combined processing and design techniques overcome the major intrinsic CNT challenges. This complete Manufacturing Methodology for CNTs enables the most advanced demonstration of a beyond-silicon modern microprocessor fabricated from CNTs, RV16X-NANO. In addition to demonstrating the RV16X-NANO microprocessor, all facets of this manufacturing methodology for CNTs is characterized and analyzed, illustrating the feasibility of this approach and more broadly of a future CNT technology.

[00163] Fabrication Process - The fabrication process is shown in FIG. 24. It uses 5 metal layers and over 100 individual processing steps.

[00164] Bottom metal routing layers - The starting substrate is a 150 mm silicon wafer with 800 nm thermal oxide for isolation. The bottom metal wire layers are defined using conventional processing (e.g., lithographic patterning, metal deposition, etching, *etc.*). After the first metal layer is patterned (FIG. 24, step (a)), an oxide spacer (300 °C) is deposited to separate this first metal layer from the subsequent second metal layer (FIG. 24, step (b)). To define inter-layer vias between the first and second metal layer (hereby referred to simply as vias), vias are lithographically patterned and etched through this spacer dielectric using dry reactive ion etching (RIE) that stops on the bottom metal layer (FIG. 24, step (c)). The second metal layer is then defined lithographically and deposited. The vias are formed simultaneously with the second metal wire

layer, as the vias are filled during the metal deposition (FIG. 24, step (d)). RV16X-NANO has two bottom metal layers which are used for signal routing. The second metal layer also acts as the bottom gates for the CNFETs

[00165] Bottom gate CNFETs - The second metal layer (FIG. 24, step (d)) acts as both signal routing (local interconnect) as well as the bottom gate for the CNFETs. To fabricate the remaining bottom gate CNFET structure, a high-*k* gate dielectric (dual-stack of AlO_2 and HfO_2) is deposited through atomic layer deposition (ALD, at 300 °C) over the bottom metal gates (FIG. 24, step (e)). The HfO_2 is used as the majority of the dielectric stack due to its high-*k* dielectric constant, while the AlO_2 is used for its improved seeding and increased dielectric breakdown voltage.

[00166] Following gate dielectric deposition, contact vias through the gate dielectric are patterned, and again RIE is used to etch the contact vias, stopping on the local bottom gates (FIG. 24, step (f)). These contact vias are used by the top metal wiring to contact and route to the bottom gates and bottom metal routing layers. Post-etch, the surface is cleaned with both a solvent rinse as well as oxygen plasma, in preparation for the CNT deposition. Prior to CNT deposition, the surface is treated with hexamethyldisilazane (HMDS), a common photoresist adhesion promoter, which improves the CNT deposition (both density and uniformity) over the high-*k* gate dielectric. The 150 mm wafer is then submerged in a toluene-based solution of ~99.99% s-CNT purified CNTs (similar to the commercial Isosol-100 available from NanoIntegris). The amount of time the wafer incubates in the solution, as well as the concentration of the CNT solution, both affect the final CNT density; this process is optimized to achieve ~40-60 CNTs/μm of CNTs (FIG 24, step (g)). Immediately prior to CNT incubation, the CNT solution is diluted to the target concentration and is horn-sonicated briefly to maximize CNT suspension (some CNT aggregates will always remain). Post-CNT deposition, the RINSE method is performed to remove CNT aggregates that deposit on the wafer, leaving CNTs uniformly deposited across the 150 mm wafer. RINSE does not degrade the remaining CNTs or remove the non-aggregated CNTs on the wafer (FIGS. 29A-29E). After CNT incubation, the CNT active etch is performed in order to remove CNTs outside of the active region of the CNFETs (i.e., channel region of the CNFETs). To do so, the active

region of the CNFETs is lithographically patterned (protecting CNTs in these regions with photoresist), and all CNTs are etched outside of these regions in oxygen plasma. The photoresist is then stripped in a solvent rinse, leaving CNTs patterned in the intended locations (i.e., in the channel region of the CNFETs) on the wafer (FIG 24, step (h)). While solution-based CNTs are used, alternative methods for depositing CNTs on the substrate include aligned growth of CNTs on a crystalline substrate followed by transfer of the CNTs onto the wafer used for circuit fabrication. Both methods have shown the ability to achieve high drive current CNFETs.

[00167] MIXED method for CNT CMOS - Following active etch of the CNTs (described above), the p-CNFET source and drain metal contacts and lithographically patterned and defined. The p-CNFET contacts are deposited (0.6 nm Titanium for adhesion followed by 85 nm Platinum) through electron-beam evaporation, and the contacts are patterned through a dual-layer lift-off process (FIG. 24, step (i)). This third metal layer acts as both the p-CNFET source and drain contacts, as well as local interconnect. Following the p-CNFET source and drain contacts, the p-CNFETs are passivated by depositing 100 nm SiO_2 over the p-CNFETs (FIG. 24, step (j)). Following p-CNFET passivation, the wafer undergoes an oxide densification anneal in forming gas (dilute H_2 in N_2) at 250 °C for 5 minutes. This concludes the p-CNFET fabrication. To fabricate the n-CNFETs, the fourth metal layer (100 nm Titanium, n-CNFET source and drain contacts) is defined (FIG. 24, step (k), similar to p-CNFET source and drain contact definition). For the electrostatic doping, nonstoichiometric HfO_X is deposited through ALD at 200 °C uniformly over the wafer. Finally, contact vias are lithographically patterned and etched (FIG. 24, step (m)) through the HfO_X for metal contacts to the bottom metal layers, as well as etch the HfO_X covering the p-CNFETs (the p-CNFETs are protected during this etch by the SiO_2 passivation oxide deposited previously).

[00168] Back-end-of-line (BEOL) metal routing - Following the CNT CMOS fabrication, back-end-of-line metallization is used to define additional metal layers over the CNFETs, e.g., for power distribution and signal routing. As the metal layers below the CNFETs are primarily used for signal routing, the top (5th) metal layer in the process is used for power distribution (FIG. 24, step (n)). Additional metal can be deposited over the input/output (I/O) pads for wire bonding and

packaging. At the end of the process, the wafer undergoes a final anneal in forming gas at 325 °C. The finished wafer is diced into chips, and each chip can be packaged for testing or probed for standard cell library characterization.

[00169] This 3D physical architecture (with metal routing below and above the CNFETs) in uniquely enabled by the low-temperature processing of the CNFETs. The solution-based deposition of the CNTs decouples the high-temperature CNT synthesis from the wafer, enabling the entire CNFET to be fabricated with a maximum processing temperature <325 °C. This enables metal layers and the gate stack to be fabricated prior to the CNFET fabrication. This is in stark contrast to silicon CMOS, which requires high temperature processing (e.g., >1,000 °C) for steps such as doping activation annealing. This prohibits fabricating silicon CMOS over pre-fabricated metal wires, as the high-temperature silicon CMOS processing would damage or destroy these bottom metal layers.

[00170] Experimental measurements - Supply voltage (V_{DD}) of 1.8 V is chosen to maximize noise resilience of the CNT CMOS digital logic, given the experimentally-measured transfer characteristics of the fabricated CNFETs (noise resilience is quantified by the static noise margin metric: see DREAM in the manuscript). To interface with each RV16X-NANO chip, a high channel count data acquisition system (120 channels) is used that offers a maximum clock frequency of 10 kHz while simultaneously sampling all channels. This limits the frequency of running RV16X-NANO to 10 kHz, at which the power consumption is 969 μW (dominated by leakage current). However, this is not the maximum clock speed of RV16X-NANO; during physical design, using an experimentally-calibrated CNFET compact model and process design kit (PDK) in an industry-practice VLSI design flow, the maximum reported clock frequency is 1.19 MHz, reported by Cadence Innovus® following placement-and-routing of all logic gates.

[00171] VLSI design methodology - The design flow of RV16X-NANO leverages industry-standard tools and techniques: a standard process design kit (PDK) for CNFETs as well as a library of standard cells for CNFETs is created that is compatible with existing EDA tools and infrastructure without modification. This enables leveraging of decades of existing EDA tools and

infrastructure to design, implement, analyze, and test arbitrary circuits using CNFETs, which can be significant for CNFET circuits to be widely adopted in the mainstream.

[00172] A high-level description of RISC-V implementation is written in Bluespec and then compiled into a standard register transfer level (RTL) hardware description language (HDL): Verilog. Bluespec enables testing of all instructions (listed in FIGS. 28A-28C) written in assembly code (e.g., using the assembly language commands) to verify proper functionality of the RV16X-NANO. The functional tests for each instruction are also compiled into waveforms and tested on the RTL generated by Bluespec, they are verified using Verilator® to verify proper functionality of the RTL (inputs and outputs are recorded and analyzed as Verilog change dump (.vcd) files). RTL descriptions of each module are shown in FIGS. 19A-19B.

[00173] Next is the physical design of RV16X-NANO, including logic synthesis with a DREAM-enforcing standard cell library (see Methods: DREAM implementation), placement and routing, parasitic extraction, and design sign-off (i.e., design rule check (DRC), layout versus schematic (LVS), verification of the final GDSII), as shown in FIGS. 21A-21G. The RTL is synthesized into digital logic gates using Cadence Genus®, using the following components of the CNFET PDK and standard cell library: LIBERTY file (.lib) containing power/timing information for all standard library cells, cell macro layout exchange format (LEF) file (.macro.lef) containing abstract views of all standard library cells (e.g., signal/power pin locations and routing blockage information), technology LEF file (.tech.lef) containing metal routing layer information (e.g., metal/via width/spacing), and back-end-of-line (BEOL) parasitic information (.qrcTech file). To enforce DREAM, a subset of library cells in the standard cell library is used, including cells with inverter- and nor2-based logic stages (for combinational logic), and logic stages using tri-state inverters (for sequential logic), as well as fill cells (to connect power rails) and decap cells (to increase capacitance between power rails V_{DD} and V_{SS}); specifically, these 23 cells comprise (see FIG. 26): and2_x1, buf_x1, buf_x2, buf_x4, buf_x8, decap_x3, decap_x4, decap_x5, decap_x6, decap_x8, dff2xdlh_x1, fand2stk_x1, inv_x1, inv_x2, inv_x4, inv_x8, inv_x16, mux2nd2_x1, nand2_x1, nor2nd2_x1, or2nd2_x1, xnor2nd2_x1, and xor2nd2_x1. During synthesis, all output pads are buffered with library cell buf_x8 to drive the output pad so that no signal simultaneously

drives an output pad as well as another logic stage to prevent excessive capacitive loading in the core. Also, to minimize routing congestion in preparation for place-and-route, the register file (containing 4 registers as described in FIGS. 19A-19B) is directly synthesized from the Verilog HDL (instead of being designed "by hand" or using a memory compiler) so that the D-flip-flops (dff2xdlh_x1: FIG. 26) including the state elements (registers) can be dispersed throughout the chip to lower overall total wire length. The final netlist is flattened so there is no hierarchy, and so logic can be optimized across module boundaries, and is then exported for place and route.

[00174] Placement-and-routing is performed using Cadence Innovus®, loading the synthesized netlist output from Cadence Genus®. The core floorplan for standard library cells is defined as 6.912 mm × 6.912 mm. Given the standard cell library and logic gate counts from synthesis (and2_x1: 188, buf_x1: 3, buf_x8: 82, buf_x16: 25, dff2xdlh_x1: 68, fand2stk_x1: 15, inv_x1: 75, inv_x2: 15, inv_x4: 10, inv_x8: 27, mux2nd2_x1: 189, nand2_x1: 625, nor2nd2_x1: 27, or2nd2_x1: 211, xnor2nd2_x1: 14, xor2nd2_x1: 8), the resulting standard cell placement utilization is 40%. The pad ring for I/O is defined as another cell with 160 pads: 40 on each side, with 170 μm minimum width and 80 μm minimum spacing totaling 250 μm pitch. Inputs are primarily toward the top of the chip, outputs are primarily on the bottom, and power/ground (V_{DD}/V_{SS}) pads are on the sides (FIGS. 18A-18B). In addition to the core area, an additional boundary of 640 μm is permitted for signal routing around the core area (containing all standard library cells), e.g., for relatively long global routing signals. Placement is performed while optimizing for uniform cell density and low routing congestion. The power grid is defined on top of the core area using the 5th metal layer (as shown in FIGS. 18A-18B), while not consuming any additional routing resources within the metal layers for signal routing. The clock tree is implemented as a single high-fanout net loaded by all 68 D-flip-flops (for each of CLK and the inverted clock: CLKN), which is directly connect to an input pad, to minimize clock skew variations between registers.

[00175] All routing signals and vias are defined on a grid, with routing jogs enabled on each metal layer to enable optimization targeting maximum spacing between adjacent metal traces. After this stage of routing, incremental placement is performed to further optimize congestion, and

then filler cells and decap cells are inserted to connect the power rails between adjacent library cells and to increase capacitance between V_{DD} and V_{SS} to improve signal integrity. After this incremental placement, the final routing takes place, reconnecting all the signals and routing to the pads, including detailed routing to fix all DRC violations (e.g., metal shorts and spacing violations). Finally, parasitic resistance and capacitances are extracted to finalize power/timing analysis, and the final netlist is output to quantify static noise margin for all pairs of connected logic stages. The GDSII is streamed out from Cadence Innovus® and is imported into Cadence Virtuoso® for final DRC and LVS, using the standard verification rule format (SVRF) rule files with Mentor Graphics Calibre®. The synthesized netlist is again used in the RTL functional simulation environment to verify proper functionality of all instructions, using Synopsys VCS®, with waveforms for each test stored in a Verilog change dump (.vcd) file. Note that these waveforms constitute the input waveforms to test the final fabricated CNFET RV16X-NANO, as well as the expected waveforms output from the core, as shown in FIGS. 20A-20C.

[00176] Once the GDSII for the core is complete, it is instantiated in a full die, which contains the core in the middle, alignment marks, and test structures (including all standard library cells, CNFETs, and test structures to extract wire/via parasitic resistance and capacitance) around the outside of the core as shown in FIG. 25. This die (2 cm × 2 cm) is then tiled onto a 150 mm wafer, each of which comprises 32 dies (6 × 6 array of dies minus 4 dies in the corners). Each layer in the GDS is flattened for the entire wafer and then released for fabrication.

[00177] To implement DREAM:

[00178] Generate "DREAM SNM table" – for each pair of logic stages in the standard cell library, quantify its susceptibility to m-CNTs as follows: use the variation-aware CNFET SNM model to compute SNM for all possible combinations of whether or not each CNFET comprises an m-CNT (e.g., in a (nand2, nor2) logic stage pair, there are 2^8 such combinations since there are 8 total CNFETs). Record the minimum computed SNM in a table: the DREAM SNM table (FIG. 23B).

[00179] Determine prohibited logic stage pairs – choose an SNM cut-off value (SNM_C), such that all logic stage pairs whose SNM in the DREAM SNM table is less than SNM_C are prohibited during physical design (example in FIG. 23B, entries with values greater than 82 satisfy SNM_C and are allowable while entries with values 82 and below are prohibited cascaded logic gate pairs).

[00180] Physical design – use industry-practice design flows and electronic design automation (EDA) tools to implement VLSI circuits without using the prohibited logic stage pairs. Ideally, EDA tools will enable designers to set which logic stage pairs to prohibit during power/timing/area optimization, but this is currently not a supported feature. To demonstrate DREAM, a DREAM-enforcing library is created that comprises a subset of library cells such that no possible combination of cells can be connected to form a prohibited logic stage pair

[00181] One parameter for DREAM is SNM_C (described above): larger SNM_C prohibits more logic stage pairs, resulting in better p_{NMS} with higher energy/delay/area cost (and vice versa). To satisfy target p_{NMS} constraints (e.g., $p_{NMS} \geq 99\%$), while minimizing cost, SNM_C can be optimized via bisection search:

[00182] 1) Initialize a lower bound (L) and upper bound (U) for SNM_C. $L = 0$, and U is the maximum value of SNM_C that enables EDA tools to synthesize arbitrary logic functions (e.g., prohibiting all logic stage pairs except (inv, inv) would be insufficient);

[00183] 2) Find p_{NMS} using $SNM_C = (L + U)/2$. Record the set of prohibited logic stage pairs, as well as the circuit physical design, p_{NMS}, energy, delay, and area;

[00184] 3) If p_{NMS} satisfies the target constraint (e.g., $p_{NMS} \geq 99\%$), set $U = SNM_C$. Otherwise set $L = SNM_C$;

[00185] 4) Set $SNM_C = (L + U)/2$. If p_{NMS} has already been analyzed for the resulting set of prohibited logic stage pairs, terminate. Otherwise, return to #2.

[00186] For all physical designs recorded in #2, choose the one that satisfies the target p_{NMS} constraint with minimum energy/delay/area cost. The cost of implementing DREAM is 10%

energy, <10% delay, and <20% area; integrating DREAM within EDA tools – enabling p_{NMS} optimization simultaneously with power/timing/area optimization is future work for improving p_S versus power/timing/area trade-offs.

Example 3

[00187] Standard Cell Library - As part of the CNFET PDK, parameterized cells (Pcells) are created using Cadence Virtuoso® for both n-CNEETs and p-CNFETs, with the following open access (OA) layers: CNFET gate, goxcut (via between CNFET gate and source/drain), active, sdp (p-CNFET source/drain), pp (passivation over p-CNFETs to shield from doping oxide for n-CNFETs), sdn (n-CNFET source/drain), dopecut (etch doping oxide over p-CNFETs), and m5 (top-layer metal). CNFET Pcells offer the following user-controlled component description format (CDF) parameters, which are both provided as inputs by the designer, and extracted using design rule check (DRC) and layout versus schematic (LVS) rules: CNFET width, physical gate length, channel length, gate underlap, source/drain/gate extension width over the horizontal edge of the CNT active region, and source/drain extension length over the vertical edge of the CNT active region. These CDF parameters are also automatically checked using DRC, along with other design rules such as minimum spacing between CNT active region and goxcut via (connecting layers: gate and sdp). CNFET devices extracted using LVS (using Standard Rule Verification Format (SVRF) compatible with Mentor Graphics Calibre® integrated within Cadence Virtuoso®) instantiate CNFETs using the widely-used virtual source FET model calibrated to experimentally measured data from CNFETs (compact model written in Verilog-A).

[0001] The CNFET Pcell is used in conjunction with other OA layers in the PDK (e.g., m1 = metal routing layer, v1g = via between m1 and CNFET gate, v_sd_m5 = via between NMOS source/drain and metal 5 power distribution) to create 63 cells in the standard library cell; images, layouts, schematics, and experimentally measured waveforms for each standard cell are shown in FIG. 26. To facilitate automated and compact placement and routing, standard cells are designed with the convention of having standard cell height equal to 16 metal tracks, including one shared power rail (V_{DD}) and one shared ground (V_{SS}) rail (shared between vertically adjacent rows of standard cells), and some cells are “double height cells” comprising 32 metal tracks and conforming to the same

conventional site-based placement method used by placement-and-routing tools (e.g., Synopsys IC Compiler® and Cadence Innovus®). Standard library cells also conform to conventional CMOS-based layout styles with PMOS FETs aligned horizontally (e.g., on the top half of the layout towards the V_{DD} rail) and NMOS FETs aligned horizontally (e.g., on the bottom half of the layout toward the V_{SS} rail). Of the 16 metal tracks for standard cells, 3 are used for power rails, 3 are used for each of n-CNFET and p-CNFET width, and 7 are used for signal routing (2 tracks between p-CNFET and V_{DD}, 2 tracks between n-CNFET and V_{SS}, and 3 tracks between n-CNFET and p-CNFET), creating routing resources for local interconnects (e.g., within standard cells and between standard cells), and for global signal routing (for place-and-route tools).

[0002] Layouts for each cell are shown in FIG. 26, as well as schematics for each standard cell that are automatically extracted using LVS (and verified against drawn schematics in Cadence Virtuoso®). These netlists are then used in conjunction with Cadence Liberate® for library power/timing characterization, e.g., to compute rise/fall delay/output slew rate/energy consumption as functions of output load capacitance and input slew rate. Additional metrics quantified by Cadence Liberate® include cell leakage power and timing constraint tables for sequential logic (e.g., setup time, hold time, minimum clock pulse width). The results are written to standard file formats (LIBERTY file: .lib) for synthesis & place-and-route. In addition to .lib files, layout exchange format (.lef) files (defining abstracted standard cell views for place and route, including pin locations, power rail locations, and blockage information) are created using Cadence Abstract®. These .lib and .lef files for standard library cells are then used for synthesis & place and route, in conjunction with other technology files in the PDK (.lef for technology layers, e.g., defining layers and rules for metal routing, and .ict/.qrcTech files defining parasitic information between technology layers).

[0003] To experimentally characterize and calibrate the standard cell library, each of the standard cells is fabricated alongside the RV16X-NANO. As shown in FIG. 25, each die contains the RV16X-NANO processor core in its center, surrounded by test circuitry on the perimeter. For packaging, these test structures are removed during dicing to isolate the RV16X-NANO processor core. The test circuitry contains both test structures for process monitoring throughout the >100

fabrication process steps utilized for RV16X-NANO, but also contains all of the standard cells. FIG. 26 shows images, schematics, and measurements for each of the standard cells in the library, illustrating correct functionality, high output voltage swing (>99% V_{DD} swing), and high gain (>15). Output voltage swing is defined as the difference between the maximum output voltage and the minimum output voltage as the input voltage is swept from 0 to V_{DD}. Gain is defined as the maximum value of $|dV_{OUT}/dV_{IN}|$ as V_{IN} is swept from 0 to V_{DD}.

[0004] RISC-V: Operational Details - The RV16X-NANO processor is implemented as a finite state machine (FSM) with 3 different states: INST_FETCH (when it is requesting an instruction from memory), EXECUTE (when it is executing an instruction), and LOAD_FINISH (when it is loading data from memory). It comes out of reset initialized in INST_FETCH, with the program counter set to 0, and so it fetches the instruction from address 0 in the memory and advances to the EXECUTE state. Adhering to RISC-V specification, the 32-bit instruction is one of 4 base instruction types (R-type, I-type, S-type, or U-type) with 5 immediate variations within the instruction (I-immediate, U-immediate, S-immediate, B-immediate, J-immediate), forming 6 possible instruction formats (type-immediate): R, I-I, I-U, S-B, S-S, U-J: see FIGS. 28A-28C for bit-level descriptions of these instructions. The instruction is decoded as one of these formats in the "decode" block (FIGS. 19A-19B), which then access to the register file (e.g., which registers to read) and provides inputs the execute block. These inputs include: 16-bit values read from the register file, immediate values decoded from the instruction, the current value of the program counter, and control signals to select instructions from the sub-blocks including: add, shift, bitwise-and, bitwise-or, bitwise-xor, less than comparison, equal comparison (FIGS. 19A-19B). The outputs of these control blocks determine which values to write back into registers (e.g., for arithmetic operation such as add/subtract), and values to write back into memory. The execute block also computes the next value of the program counter, e.g., based on either incrementing (next pc = pc + 4) or otherwise for conditional branch or unconditional jump. For loads and stores, the specified memory access is performed in the EXECUTE state. For loads, the processor continues to the LOAD_FINISH state to write the load response to the register file and then request the next instruction. For stores, the processor continues to the INST_FETCH state to fetch the next

instruction. All other instructions fetch the next instruction as part of the EXECUTE state. This mode of operation continues during full execution of programs and adheres to the specification in riscv.org according to RV32E specification, but a reduced number of registers (4 instead of 16) and with 16-bit data words instead of 32-bit data words (all registers in the register file are 16-bit instead of 32-bit), though instructions remain 32-bits. A full list of all instructions is in FIG. 33, which is the full list for the RV32E in the RISC-V specification. To adjust RV32E to 16-bit, the instruction length remains 32 bits, and all data operations are performed on 16-bit values instead of 32-bit values, by truncating the upper-32 bits.

[0005] The full 32-bit RISC-V processor from which the 16-bit processor was derived was formally verified using the riscv-formal suite of RISC-V specifications and tools for SMT-based hardware model checking. The riscv-formal suite contains a set of specifications that describe correct behavior of RISC-V processors. These specifications are in the form of checks performed on packets emitted from a trace-emitting interface added to processors under test called the RISC-V Formal Interface (RVFI). There are specifications for each RISC-V instruction that check individual RVFI packets to make sure each instruction is implemented correctly, e.g., the add instruction correctly implements addition. There are also specifications to make sure the microarchitecture is implemented correctly that check bounded sequences of RVFI packets for necessary properties, e.g., reading a register returns the last value written to it. Both groups of specifications are implemented in Verilog with simple synthesizable code and immediate assertion statements. The specifications in the riscv-formal suite have been verified against the reference RISC-V software simulator Spike and another formal specification written in Haskell.

[0006] The riscv-formal suite also contains tools to perform SMT-based hardware model checking on each of these specifications using the SymbiYosys framework. A script within the riscv-formal suite produces a SymbiYosys configuration file for each piece of the specification. These configuration files can be used with SymbiYosys to perform bounded model checking for each piece of the specification separately.

[0007] To verify the 32-bit RISC-V processor against riscv-formal, an RVFI port was added to emit information about each instruction executed and implemented a wrapper for the processor to

match the rest of the interface expected by riscv-formal. The SymbiYosys framework is used to run bounded model checking with a depth of 30 clock cycles using the Boolector SMT solver resulting in all 42 tests passing. The free variables used by the SMT solver were the memory responses and the register file reset values. This allowed the SMT solver to explore arbitrary sequences of instructions from arbitrary initial states of the register file up to 30 clock cycles. Using a depth of 30 clock cycles is more than sufficient to cover all reachable microarchitectural states of the processor.

[0008] RINSE Method Characterization - In addition to demonstrating the ability for RINSE to reduce CNT aggregate defect density by >250×, RINSE is further characterized to show that the RINSE process does not negatively impact CNFET performance. As shown in FIGS. 29A-29E, scanning electron microscopy (SEM) images of CNT deposition pre- and post-RINSE show negligible change in the CNT density. Therefore, RINSE does not remove CNTs from the wafer surface, even after >60 minutes of performing RINSE sonication. Moreover, CNFETs fabricated on samples that have and have not undergone RINSE exhibit minimal change in electrical characteristics (FIG. 29B, note negligible change in the I_D-V_{GS} for a set of CNFETs). Not only does RINSE not impact the p-CNFETs, the CNFETs can still undergo the MIXED doping process (including the electrostatic doping oxide) to realize n-CNFETs (FIG. 29C).

[0009] MIXED Method Characterization – FIGS. 30A-30B provide additional characterization of the MIXED CNFET CMOS process, realizing the first demonstration of large-area (150 mm substrates), uniform, and high-yield CNFET CMOS logic.

[0010] FIG. 29B shows the 150 mm wafer with the test patterns (each die has 10,400 CNFET CMOS two-input “not-or” (NOR2) logic gates). Separate NOR2 logic gates are fabricated and measured as it enables characterization of key gate-level metrics, *e.g.* the voltage transfer curves (VTCs, which are used to compute the static noise margin of cascaded logic gates), gain, and output voltage swing. Explanations of these metrics are shown in FIG. 30A. FIG. 30B shows the extracted distributions of these key metrics for all of the experimentally measured VTCs from the 10,400 logic gates shown in FIG. 22D (these are the VTCs for all 10,400 CNFET CMOS NOR2 logic gates within a die, no logic gates have been excluded). To illustrate uniformity, the functional

yield (output voltage swing >70%) for all logic gates within the die is 10,400/10,400, and the average output voltage swing is >98% with a standard deviation of <2%. By extracting V_{OH}, V_{OL}, V_{IH}, V_{IL} from the VTCs associated with each of the 10,400 logic gates, one is able to calculate the static noise margin (SNM) of all combinations of two cascaded NOR2 gates (i.e., with *driving* logic gate and *loading* logic gate). FIG. 29C shows the distributions of the SNM for the >100 million combinations of cascaded logic gate pairs (i.e., with a driving logic gate and a loading logic gate): 99.93% of logic gate pairs have positive noise margin (i.e., $V_{OH}^{(DR)} > V_{IH}^{(LD)}$ and $V_{OL}^{(DR)} < V_{IL}^{(LD)}$, where (DR) is for the driving logic gate and (LD) is for the loading logic gate), indicating correct cascaded logic gate functionality. All of this characterization is performed at the scaled supply voltage of 1.2 V_{DD}.

[0011] Moreover, FIG 29D shows the noise margin violations (SNM < 0) can partially be attributed to the wafer processing (*i.e.*, not the CNTs), and therefore can be improved by optimizing processing (e.g., ALD doping oxide uniformity over the 150 mm wafer). As can be seen in FIG 29D, there is a spatial dependence of V_{IH} (as an example parameter to compute SNM; the other parameters exhibit similar spatial dependence): V_{IH} increases across the die (increasing from top to bottom). The change in V_{IH} corresponds with slight changes in CNFET threshold voltage. The fact that the threshold voltage variations are not uniformly distributed, but rather have spatial dependence, illustrates that a portion of the threshold voltage variations (and therefore variation in SNM) is due to wafer-level processing-related variations (CNT deposition is more uniform across the 150 mm wafer).

[0012] Additionally, to demonstrate that MIXED is wafer-scalable across 150 mm substrates, FIG 29E shows the first 150 mm wafer-scale CNT CMOS characterization: measurements across 4 additional dies distributed across the 150 mm wafer (1,000 CNT CMOS NOR2 logic gates are sampled randomly from the 10,000 ensemble in each die, with no logic gates omitted from the analysis) illustrating yield across the 150 mm wafer (total yield across wafer: 14,400 logic gates, 57,600 CNFETs). This is the first demonstration of large-area, uniform, and high-yield CNT CMOS logic, enabled by combining RINSE with the robust MIXED CNT CMOS process.

[0013] Prior work for overcoming metallic CNTs - The presence of m-CNTs has been a major obstacle in the field of CNTs since the first CNFET demonstrations over a decade ago. While a wide range of techniques have been developed in response to m-CNTs, no technique achieves the required s-CNT purity for realizing CNFET digital VLSI systems. While previous works have set p_S requirements based on limiting m-CNT-induced leakage power, no existing works have provided guidelines for p_S based on both increased leakage and degraded SNM due to m-CNTs for physical designs of VLSI circuits; while 99.999% ps is sufficient to limit EDP degradation to <5%, FIGS. 31A-31E show that SNM imposes far stricter requirements on purity: p_S ~99.999,999% to achieve $p_{NMS} \geq 99\%$ (for 1 million gate circuits).

[0014] To quantify the impact of m-CNTs on VLSI circuits, circuit modules are analyzed that are synthesized from the processor core of OpenSparc T2, a large multi-core chip that closely resembles the commercial Oracle/SUN Niagara 2 system ; thus, these results account for effects present in realistic VLSI circuits – such as wire parasitics, buffer insertion to meet timing constraints, and SNM for cross-coupled logic stages in sequential logic elements – that are not present in small circuit benchmarks. Standard cell libraries derived from the reference library “asap7sc7p5t” included with the ASAP7 process design kit (*PDK*) are leveraged to create physical designs of the OpenSparc modules at an example 7 nm technology node, to compare optimized energy, delay, area, and p_S required to achieve $p_{NMS} = 99\%$ for VLSI circuits. The baseline case, which permits all pairs of logic stages, requires $p_S \geq$ 99.999,996,3% to achieve $p_{NMS} \geq 99\%$ (for $SNM_R = V_{DD}/5$).

[0015] Performance Cost of Manufacturing Methodology for CNTs - the manufacturing methodology for CNTs (RINSE, MIXED, and DREAM) overcomes the major obstacles facing a future CNT technology with minor cost in performance or energy efficiency. First, RINSE does not degrade CNFET performance: this is validated experimentally in FIGS. 29A-29E. Second, MIXED enables CMOS CNFETs without significant (or costly) changes to transistor structure (*e.g.*, additional FET gates or 3D FET geometries that would increase parasitics), and without imposing additional design rules that would impact circuit layouts (in fact, although it is not discussed in this manuscript, CNFET CMOS can potentially enable more compact circuit layouts

versus silicon, due to the lack of design constraints enforced by n/p-wells, well taps, or doping implants in many silicon-based technologies). Finally, DREAM also enables CNFET EDP benefits to be maintained in the presence of m-CNTs using s-CNT purity that is available today. While a perfect, variation-free CNFET technology can offer 9.0× EDP benefit versus silicon at a 7 nm node (Hills 18), DREAM would still enable – in the worst case – a 7.4× EDP benefit despite 99.99% s-CNT purity (*i.e.*, while an ideal CNT technology promises a 9× EDP benefit, a worst-case 10% energy and 10% delay cost reduces this 9× EDP benefit to 9×/(1.1*1.1) = 7.4×, since energy and delay are both increased by 1.1×). Although the cost of DREAM in this particular case is quantified, DREAM is a general technique to trade-off circuit noise immunity with energy, delay, and area in the presence of variations (such as m-CNTs). Thus, DREAM offers circuit designers multiple solutions with varying costs and noise immunity improvements to meet design goals. There are consequently multiple paths to further reduce the cost of DREAM: (1) as s-CNT purity continues to improve, the cost of DREAM will naturally improve as well (<10% energy, <10% delay, <20% area, is for 99.99% s-CNT purity that is already commercially available today, improving s-CNT purity will decrease the cost imposed by DREAM); and (2) the analysis considers DREAM implemented using a DREAM-enforcing standard cell library (as described in Methods), so that standard EDA tools today (even though they are currently unaware of DREAM) can still implement DREAM by avoiding the use of prohibited logic stage during logic synthesis and place-and-route. However, integrating DREAM directly into synthesis and place-and-route algorithms can further optimize power/timing/area while simultaneously meeting noise margin constraints, further reducing any cost associated with DREAM.

[0016] DREAM is a major step towards realizing the benefits of CNFETs, overcoming the major obstacle of m-CNTs. Contrary to previous works, DREAM requires no additional CNT-specific processing for removing m-CNTs, enabling CNFET circuits to be fabricated with commercially-available CNT purities today (relaxing the required CNT purity by ~10,000×). As a general technique for improving noise margin resilience, DREAM can be applied both to arbitrary digital logic VLSI circuits as well as a broad range of technologies.

[00188] Integrated circuits designed specifically for improved SNM as described herein can be useful for (for example) space applications, by making such circuits more robust to several different types of radiation effects such as total-ionizing-dose and soft-errors. They can also be useful for ultra-low-power applications and sub-threshold circuits to enable lower supply voltages to be used. While described herein with respect to circuits including CNTs, such design approaches can be generally applicable to any transistor based circuits/technology.

[00189] Conclusion

[00190] While various inventive embodiments have been described and illustrated herein, those of ordinary skill in the art will readily envision a variety of other means and/or structures for performing the function and/or obtaining the results and/or one or more of the advantages described herein, and each of such variations and/or modifications is deemed to be within the scope of the inventive embodiments described herein. More generally, those skilled in the art will readily appreciate that all parameters, dimensions, materials, and configurations described herein are meant to be exemplary and that the actual parameters, dimensions, materials, and/or configurations will depend upon the specific application or applications for which the inventive teachings is/are used. Those skilled in the art will recognize or be able to ascertain, using no more than routine experimentation, many equivalents to the specific inventive embodiments described herein. It is, therefore, to be understood that the foregoing embodiments are presented by way of example only and that, within the scope of the appended claims and equivalents thereto, inventive embodiments may be practiced otherwise than as specifically described and claimed. Inventive embodiments of the present disclosure are directed to each individual feature, system, article, material, kit, and/or method described herein. In addition, any combination of two or more such features, systems, articles, materials, kits, and/or methods, if such features, systems, articles, materials, kits, and/or methods are not mutually inconsistent, is included within the inventive scope of the present disclosure.

[00191] Also, various inventive concepts may be embodied as one or more methods, of which an example has been provided. The acts performed as part of the method may be ordered in any suitable way. Accordingly, embodiments may be constructed in which acts are performed

in an order different than illustrated, which may include performing some acts simultaneously, even though shown as sequential acts in illustrative embodiments.

[00192] All definitions, as defined and used herein, should be understood to control over dictionary definitions, definitions in documents incorporated by reference, and/or ordinary meanings of the defined terms.

[00193] The indefinite articles “a” and “an,” as used herein in the specification and in the claims, unless clearly indicated to the contrary, should be understood to mean “at least one.”

[00194] The phrase “and/or,” as used herein in the specification and in the claims, should be understood to mean “either or both” of the elements so conjoined, i.e., elements that are conjunctively present in some cases and disjunctively present in other cases. Multiple elements listed with “and/or” should be construed in the same fashion, i.e., “one or more” of the elements so conjoined. Other elements may optionally be present other than the elements specifically identified by the “and/or” clause, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, a reference to “A and/or B”, when used in conjunction with open-ended language such as “comprising” can refer, in one embodiment, to A only (optionally including elements other than B); in another embodiment, to B only (optionally including elements other than A); in yet another embodiment, to both A and B (optionally including other elements); etc.

[00195] As used herein in the specification and in the claims, “or” should be understood to have the same meaning as “and/or” as defined above. For example, when separating items in a list, “or” or “and/or” shall be interpreted as being inclusive, i.e., the inclusion of at least one, but also including more than one, of a number or list of elements, and, optionally, additional unlisted items. Only terms clearly indicated to the contrary, such as “only one of” or “exactly one of,” or, when used in the claims, “consisting of,” will refer to the inclusion of exactly one element of a number or list of elements. In general, the term “or” as used herein shall only be interpreted as indicating exclusive alternatives (i.e. “one or the other but not both”) when preceded by terms of

exclusivity, such as "either," "one of," "only one of," or "exactly one of." "Consisting essentially of," when used in the claims, shall have its ordinary meaning as used in the field of patent law.

[00196] As used herein in the specification and in the claims, the phrase "at least one," in reference to a list of one or more elements, should be understood to mean at least one element selected from any one or more of the elements in the list of elements, but not necessarily including at least one of each and every element specifically listed within the list of elements and not excluding any combinations of elements in the list of elements. This definition also allows that elements may optionally be present other than the elements specifically identified within the list of elements to which the phrase "at least one" refers, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, "at least one of A and B" (or, equivalently, "at least one of A or B," or, equivalently "at least one of A and/or B") can refer, in one embodiment, to at least one, optionally including more than one, A, with no B present (and optionally including elements other than B); in another embodiment, to at least one, optionally including more than one, B, with no A present (and optionally including elements other than A); in yet another embodiment, to at least one, optionally including more than one, A, and at least one, optionally including more than one, B (and optionally including other elements); etc.

[00197] In the claims, as well as in the specification above, all transitional phrases such as "comprising," "including," "carrying," "having," "containing," "involving," "holding," "composed of," and the like are to be understood to be open-ended, i.e., to mean including but not limited to. Only the transitional phrases "consisting of" and "consisting essentially of" shall be closed or semi-closed transitional phrases, respectively, as set forth in the United States Patent Office Manual of Patent Examining Procedures, Section 2111.03.

CLAIMS

1. A method of forming a layer of carbon nanotubes on a substrate, the method comprising:

depositing individual carbon nanotubes and at least one carbon nanotube aggregate on the substrate;

forming an adhesive layer on the individual carbon nanotubes and the at least one carbon nanotube aggregate on the substrate, the adhesive layer adhering the individual carbon nanotubes to the substrate; and

mechanically exfoliating the at least one carbon nanotube aggregate from the substrate.

2. The method of claim 1, further comprising, before depositing the individual carbon nanotubes and the at least one carbon nanotube aggregate on the substrate:

coating the substrate with a carbon nanotube adhesion promoter.

3. The method of claim 1, wherein depositing the individual carbon nanotubes and the at least one carbon nanotube aggregate includes depositing via incubation, spin-coating, or dip coating.

4. The method of claim 1, wherein depositing the individual carbon nanotubes and the at least one carbon nanotube aggregate includes incubating the substrate with a solution containing carbon nanotubes having a semiconducting carbon nanotube purity from about 99.9% to about 99.99%.

5. The method of claim 1, wherein forming the adhesive layer includes forming a layer of a photoresist material on the individual carbon nanotubes.

6. The method of claim 5, wherein the photoresist material is selected from the group consisting of polydimethyldiglutarimide (PMGI), hexamethyldisilazane (HMDS), and SPR.

7. The method of claim 1, wherein forming the adhesive layer comprises:

depositing a layer of polydimethyldiglutarimide (PMGI) on the individual carbon nanotubes and the at least one carbon nanotube aggregate on the substrate; and

curing the layer of PMGI at a temperature of about 235 °C.

8. The method of claim 7, wherein the layer of PMGI has a thickness of from about 100 nm to about 150 nm.

9. The method of claim 1, wherein mechanically exfoliating the at least one carbon nanotube aggregate from the substrate comprises:

submerging the substrate in a solvent for a duration sufficient to remove a first portion of the adhesive layer and to retain a remaining portion of the adhesive layer; and

sonicating the substrate in the solvent to remove the at least one carbon nanotube aggregate from the substrate, the remaining portion of the adhesive layer adhering the individual carbon nanotubes to the substrate during the sonicating.

10. The method of claim 9, further comprising, while sonicating the substrate:

filtering and/or circulating the solvent to remove carbon nanotube aggregates released from the substrate into the solvent.

11. The method of claim 9, wherein the remaining portion of the adhesive layer is from about less than about 1 nm to about 2 nm in thickness.

12. The method of claim 1, wherein mechanically exfoliating the at least one carbon nanotube aggregate from the substrate yields a substrate surface having fewer than ten carbon nanotube aggregates per square millimeter.

13. The method of claim 1, wherein mechanically exfoliating the at least one carbon nanotube aggregate from the substrate yields a substrate surface having fewer than one carbon nanotube aggregate per square millimeter.

14. The method of claim 1, wherein mechanically exfoliating the at least one carbon nanotube aggregate comprises mechanically exfoliating the at least one carbon nanotube aggregate without exfoliating the individual carbon nanotubes.

15. The method of claim 1, further comprising:

doping at least some of the individual carbon nanotubes to be n-channel carbon nanotubes.

16. The method of claim 1, further comprising, prior to the depositing, coating the substrate with a carbon nanotube adhesion promoter to promote adhesion of the individual carbon nanotubes and the at least one carbon nanotube aggregate to the substrate.

17. A method of making a carbon nanotube logic device, the method comprising:

depositing individual carbon nanotubes and carbon nanotube aggregates on a substrate;

forming a polydimethyldiglutarimide (PMGI) layer on the substrate, the PMGI layer having a thickness of about 100 nm to about 150 nm;

submerging the substrate in a solvent for a duration sufficient to remove a portion of the PMGI layer and to retain a remaining portion of the PMGI layer; and

sonicating the substrate in the solvent to remove the carbon nanotube aggregates from the substrate to yield a substrate surface coated with individual carbon nanotubes and fewer than 10 carbon nanotube aggregates per square millimeter, the remaining portion of the adhesive layer adhering the individual carbon nanotubes to the substrate during the sonicating.

18. A method of making a carbon nanotube field effect transistor (CNFET) complementary metal-oxide semiconductor (CMOS) device, the method comprising:

depositing a first channel of individual carbon nanotubes (CNTs) and a second channel of individual CNTs on the substrate, such that at least one carbon nanotube aggregate is also deposited on the substrate;

forming an adhesive layer on the substrate, the adhesive layer adhering the first channel and the second channel to the substrate;

mechanically exfoliating the at least one carbon nanotube aggregate from the substrate;

forming, in electrical contact with the first channel, a first source electrode and a first drain electrode to generate a p-type metal-oxide semiconductor (PMOS) CNFET; and

forming, in electrical contact with the second channel, a second source electrode and a second drain electrode to generate an n-type metal-oxide semiconductor (NMOS) CNFET.

19. The method of claim 18, wherein the first source electrode and the first drain electrode are composed of platinum and the second source electrode and the second drain electrode are composed of titanium.

20. The method of claim 18, further comprising:

forming a layer of a nonstoichiometric oxide on the second channel via atomic layer deposition (ALD).

21. The method of claim 18, further comprising, before depositing the first channel, the second channel, and the at least one carbon nanotube aggregate on the substrate:

coating the substrate with a carbon nanotube adhesion promoter.

22. The method of claim 18, wherein forming the adhesive layer includes forming a layer of a photoresist material on the first channel and the second channel.

23. The method of claim 18, wherein mechanically exfoliating the at least one carbon nanotube aggregate from the substrate comprises:

submerging the substrate in a solvent for a duration sufficient to remove a first portion of the adhesive layer and to retain a remaining portion of the adhesive layer; and

sonicating the substrate in the solvent to remove the at least one carbon nanotube aggregate from the substrate, the remaining portion of the adhesive layer adhering the first channel and the second channel to the substrate during the sonicating.

24. A carbon nanotube (CNT) logic device comprising:

a substrate;

a first adhesive layer formed on the substrate;

a channel of individual CNTs deposited on the first adhesive layer, wherein the first adhesive layer promotes adhesion of the channel of individual CNTs to the substrate; and

a second adhesive layer deposited on the substrate and on the channel of individual CNTs to maintain adhesion of the channel of individual CNTs to the substrate.

FIG. 1

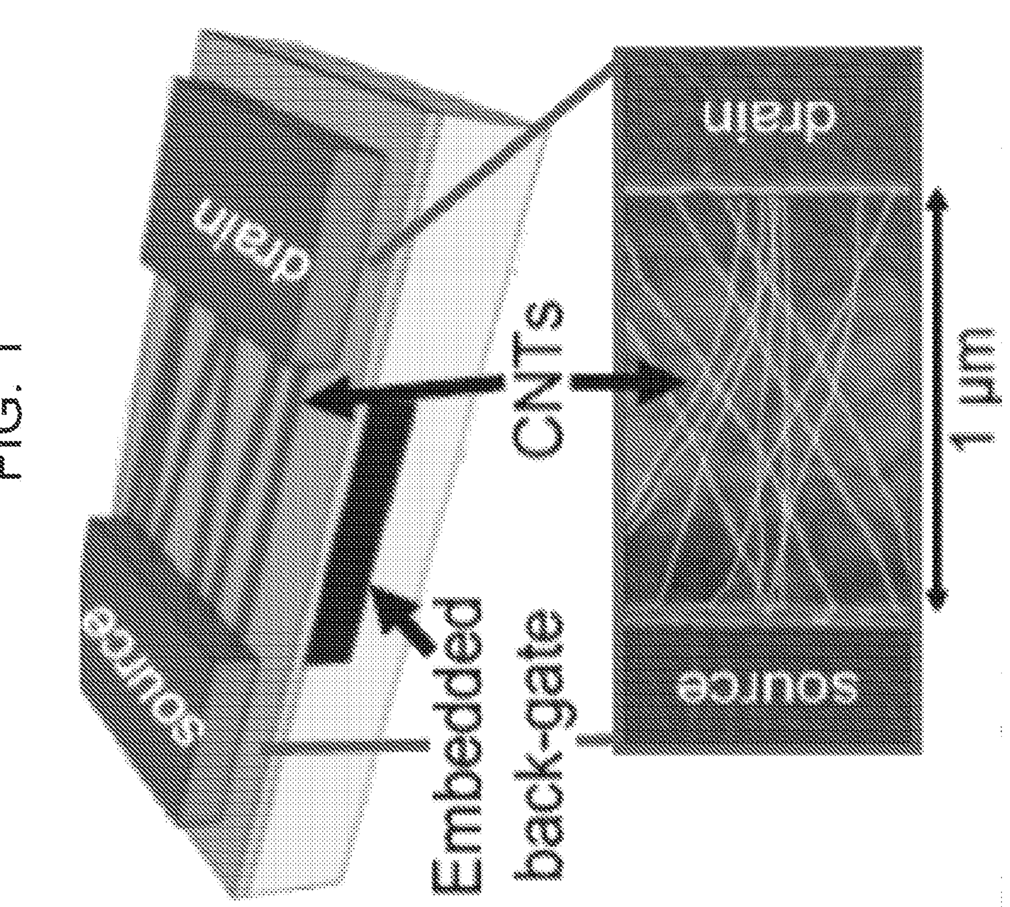


FIG. 2

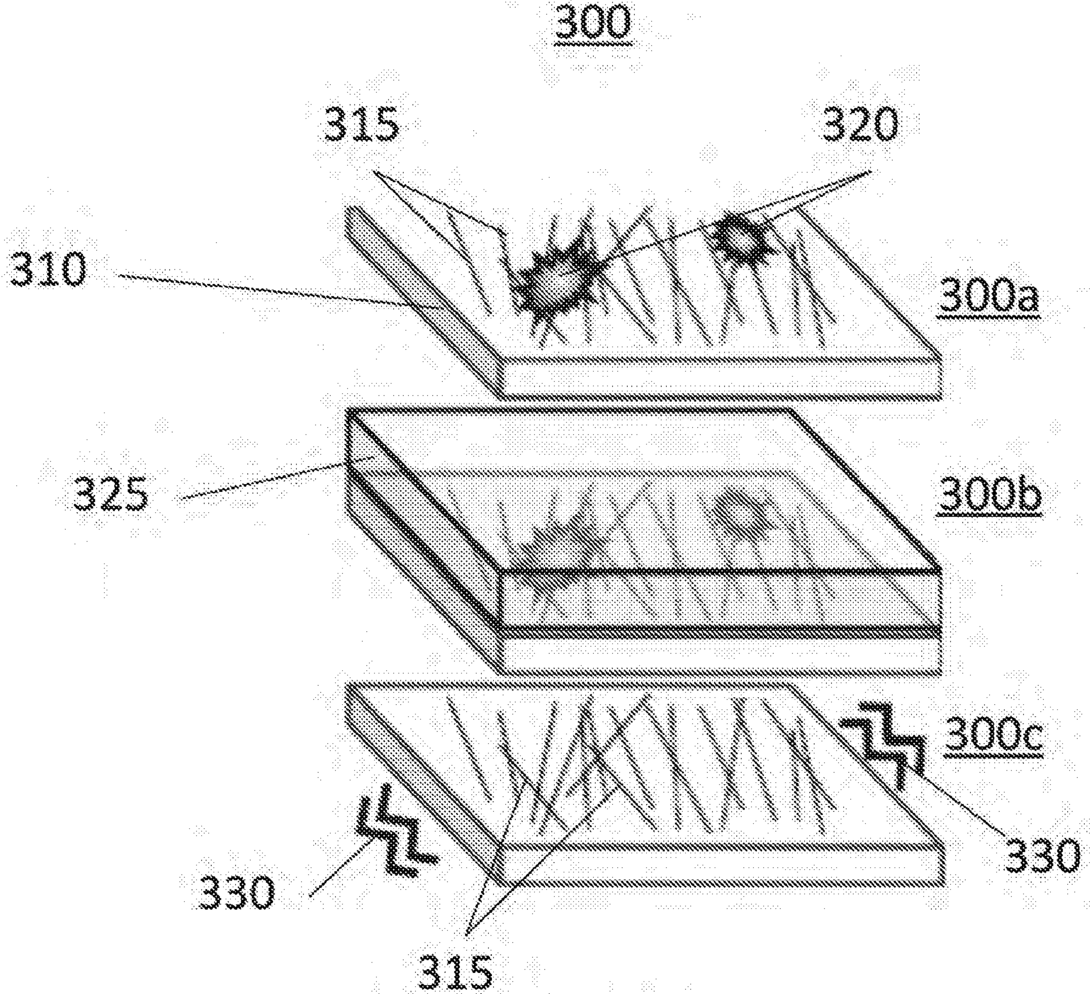


FIG. 3

FIG. 4A

FIG. 4B

FIG. 5A

FIG. 5B

FIG. 5C

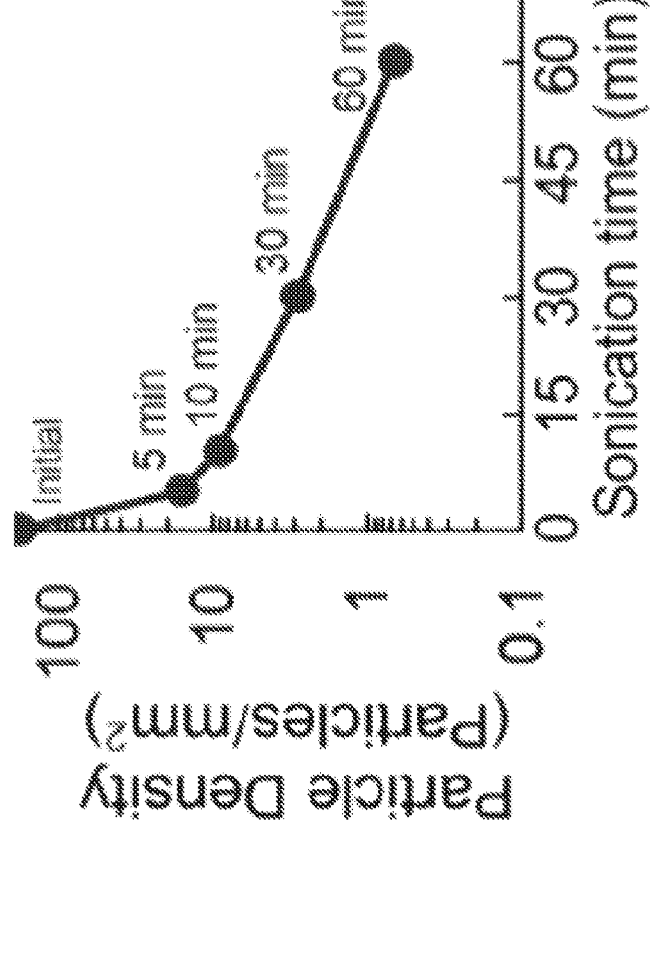


FIG. 6C

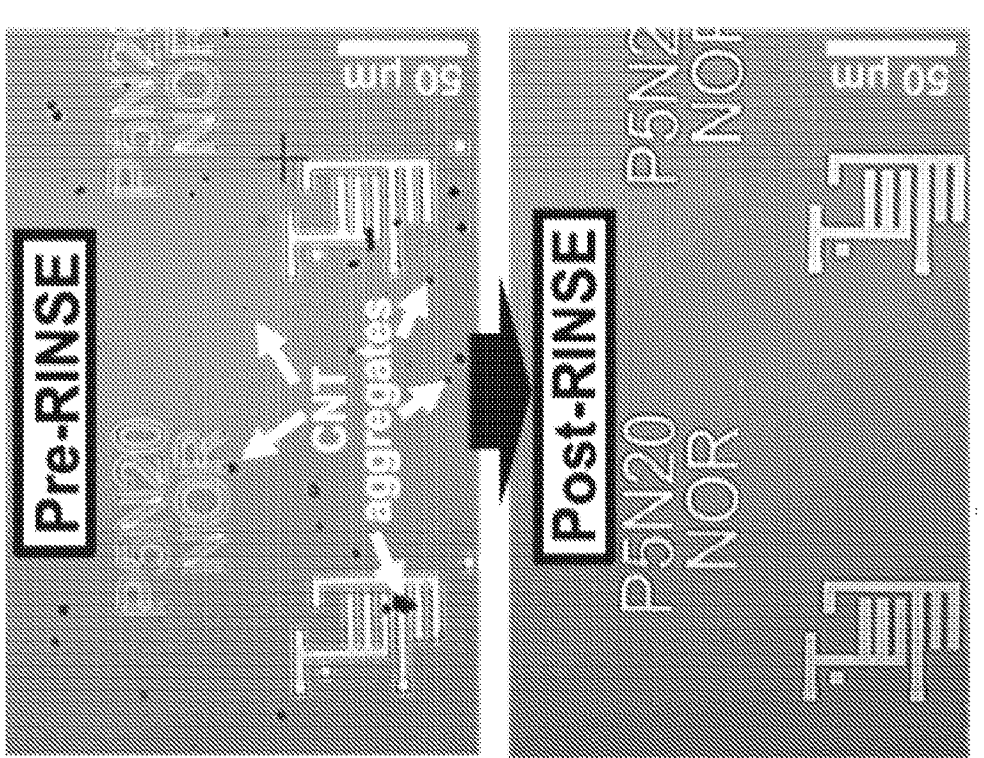


FIG. 6A

FIG. 6B

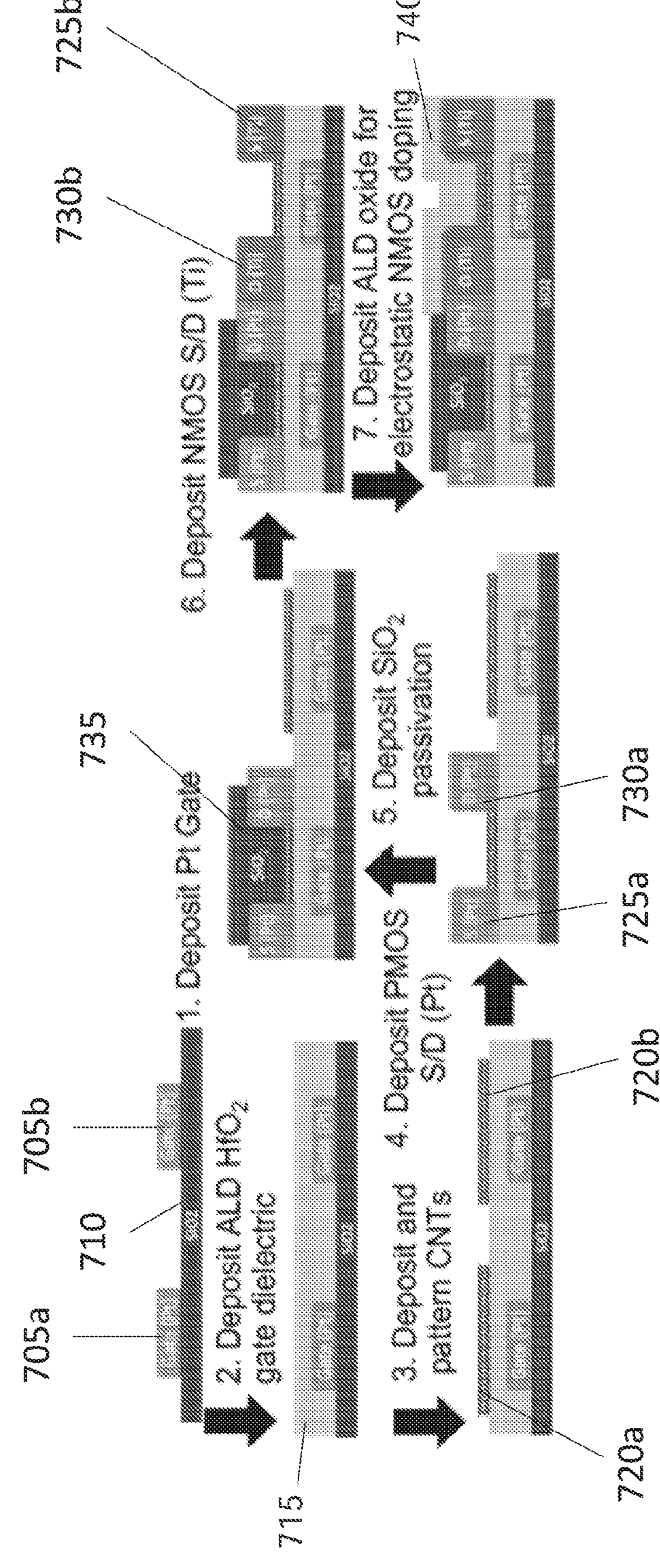


FIG. 7
705a
710
705b
1. Deposit Pt Gate
2. Deposit ALD HfO$_2$ gate dielectric
715
3. Deposit and pattern CNTs
720a
720b
4. Deposit PMOS S/D (Pt)
725a
730a
5. Deposit SiO$_2$ passivation
735
6. Deposit NMOS S/D (Ti)
730b
725b
7. Deposit ALD oxide for electrostatic NMOS doping
740

FIG. 8

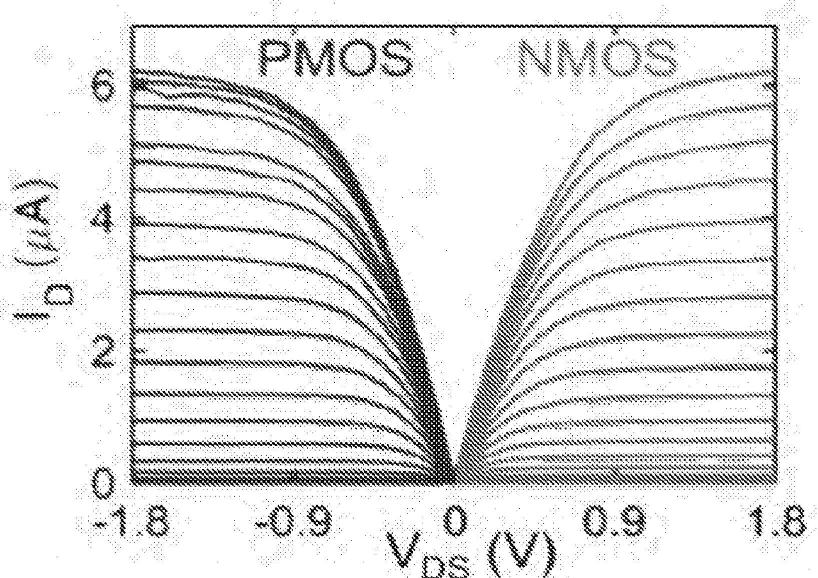


FIG. 9A

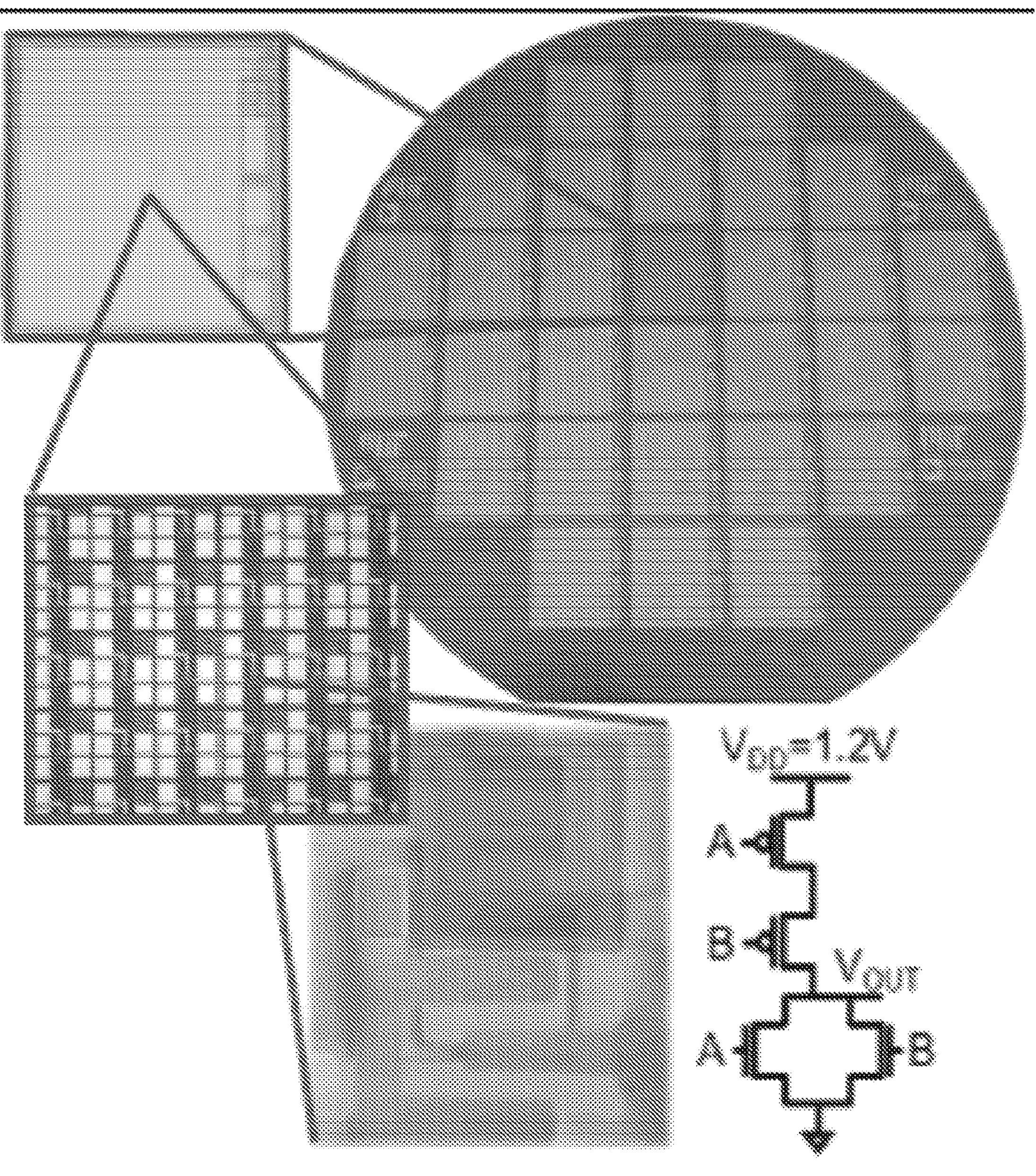


FIG. 9B

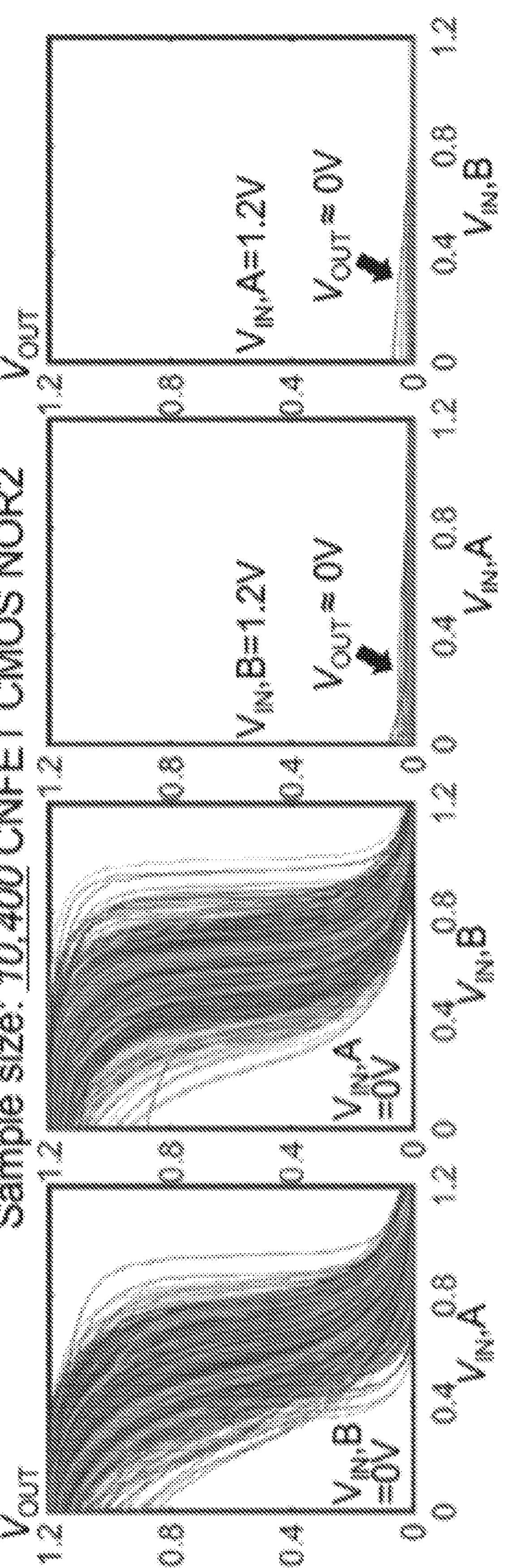
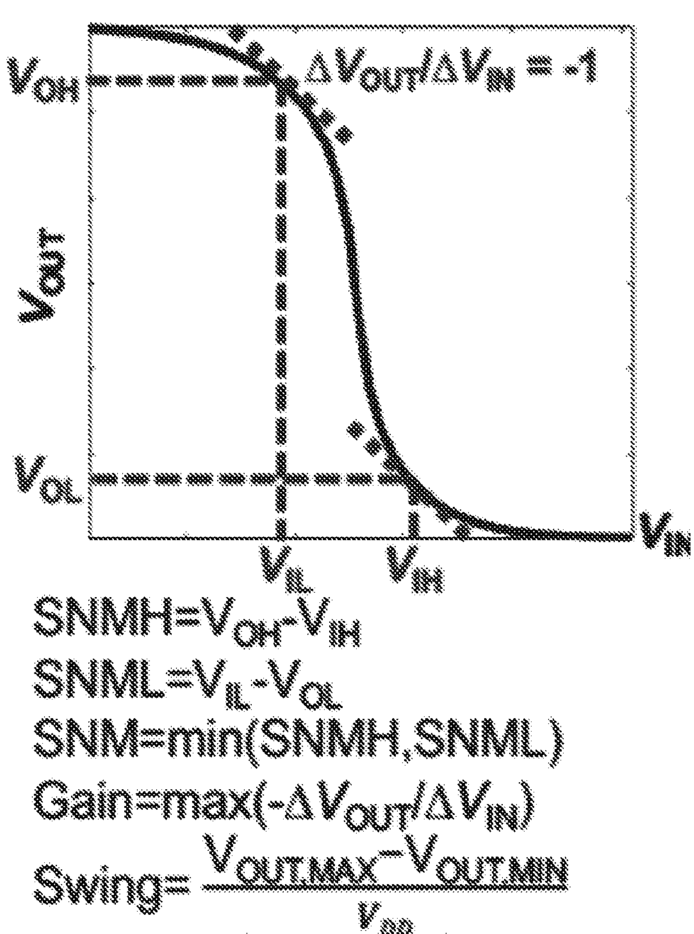


FIG. 10



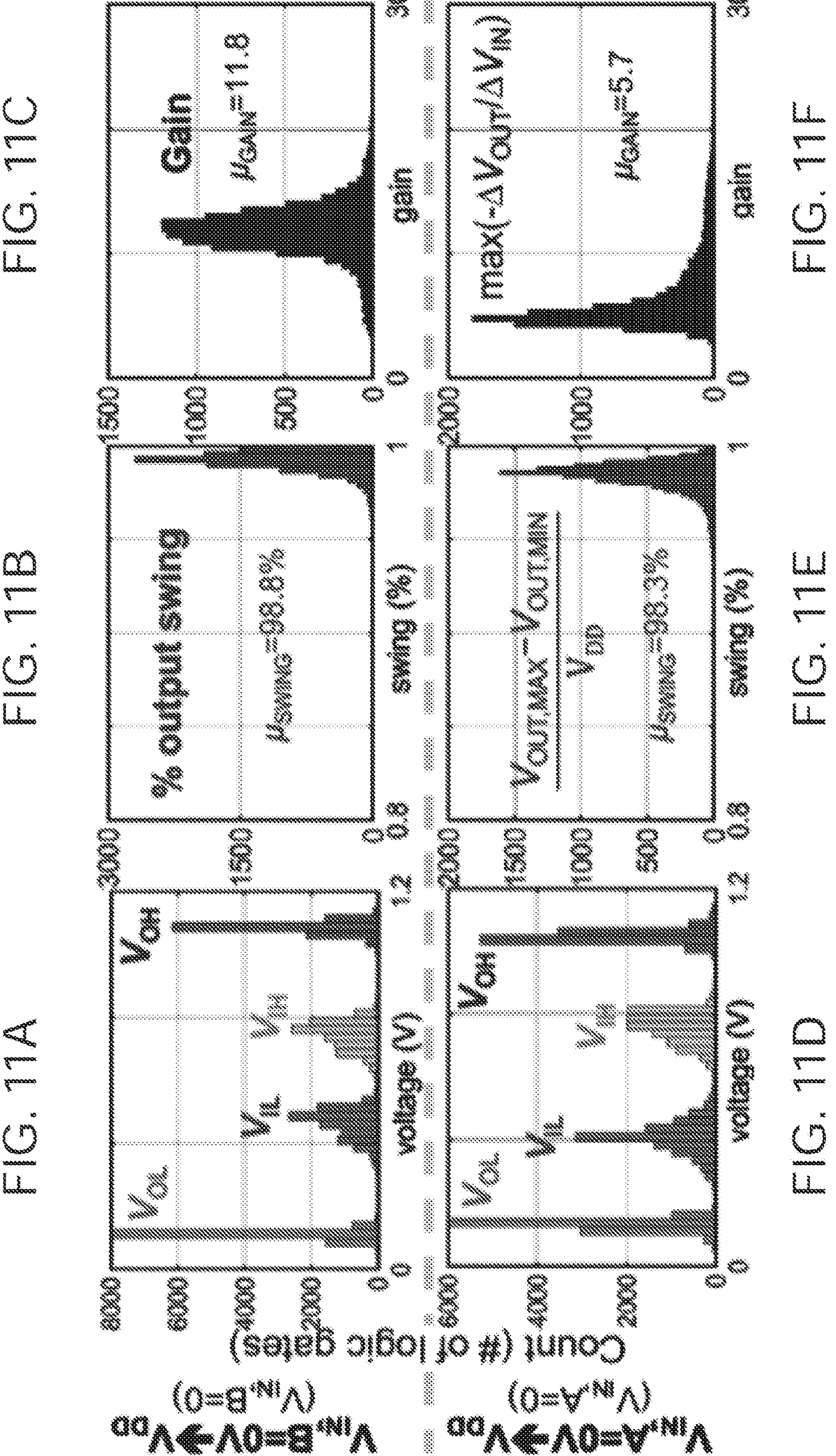


FIG. 11A
FIG. 11B
FIG. 11C
V_{OL}
V_{IL}
V_{IH}
V_{OH}
voltage (V)
% output swing
μ_{SWING}=98.8%
swing (%)
Gain
μ_{GAIN}=11.8
gain
FIG. 11D
FIG. 11E
FIG. 11F
$\frac{V_{OUT,MAX}-V_{OUT,MIN}}{V_{DD}}$
μ_{SWING}=98.3%
max$(-\Delta V_{OUT}/\Delta V_{IN})$
μ_{GAIN}=5.7
Count (# of logic gates)
$V_{IN,B}$=0V→V_{DD}
($V_{IN,B}$=0)
$V_{IN,A}$=0V→V_{DD}
($V_{IN,A}$=0)

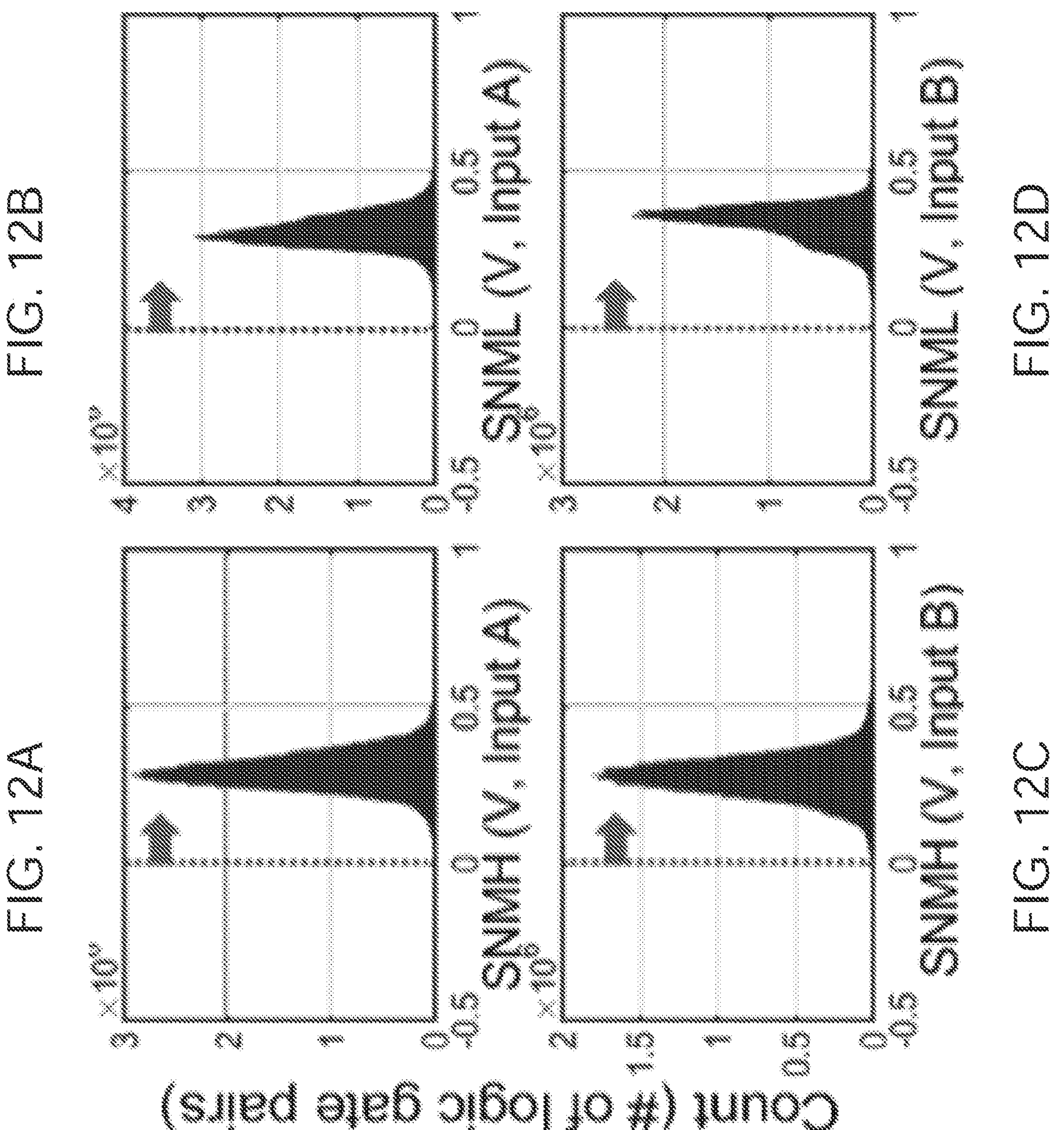


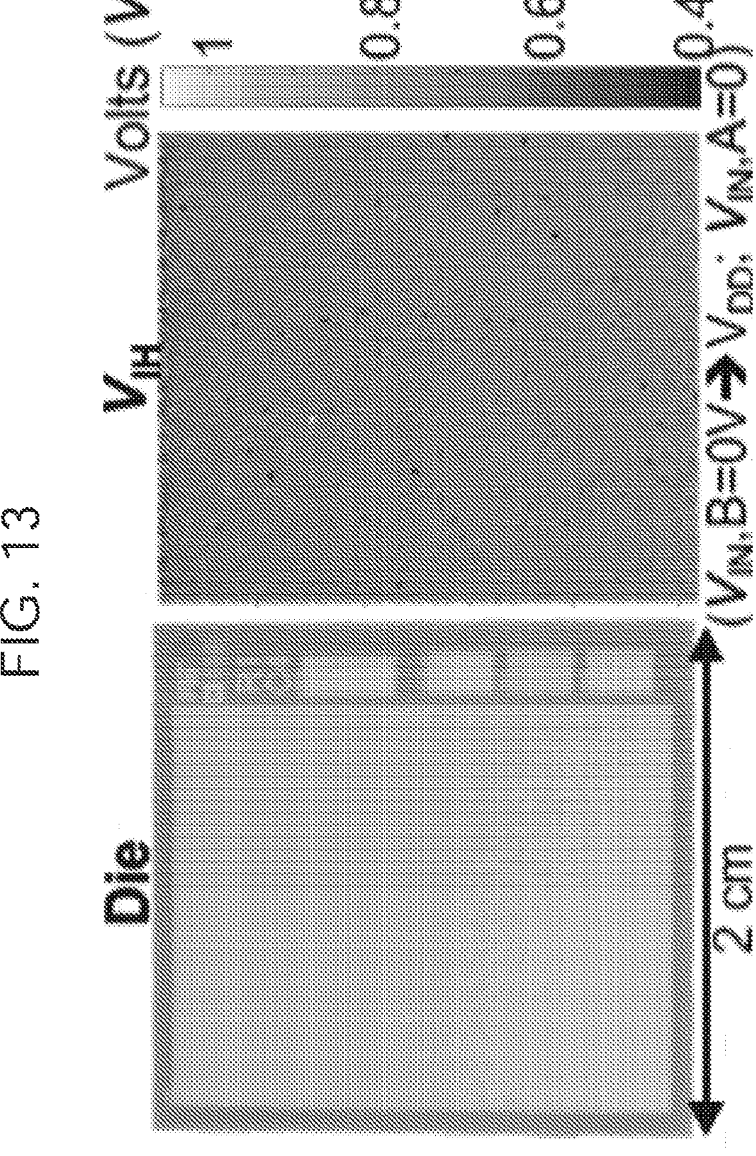
FIG. 12A

FIG. 12B

FIG. 12C

FIG. 12D

FIG. 13



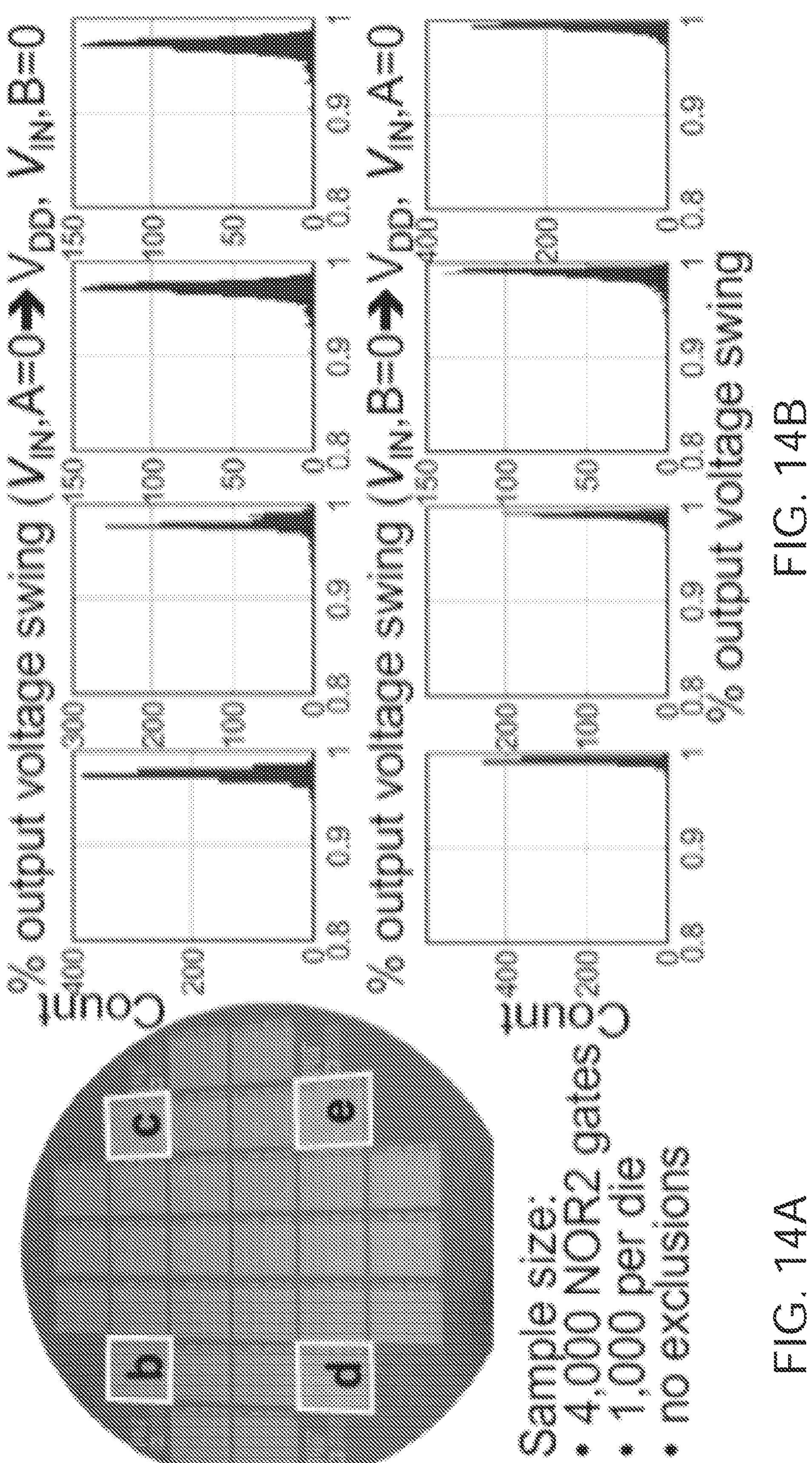


FIG. 14A

FIG. 14B

FIG. 15

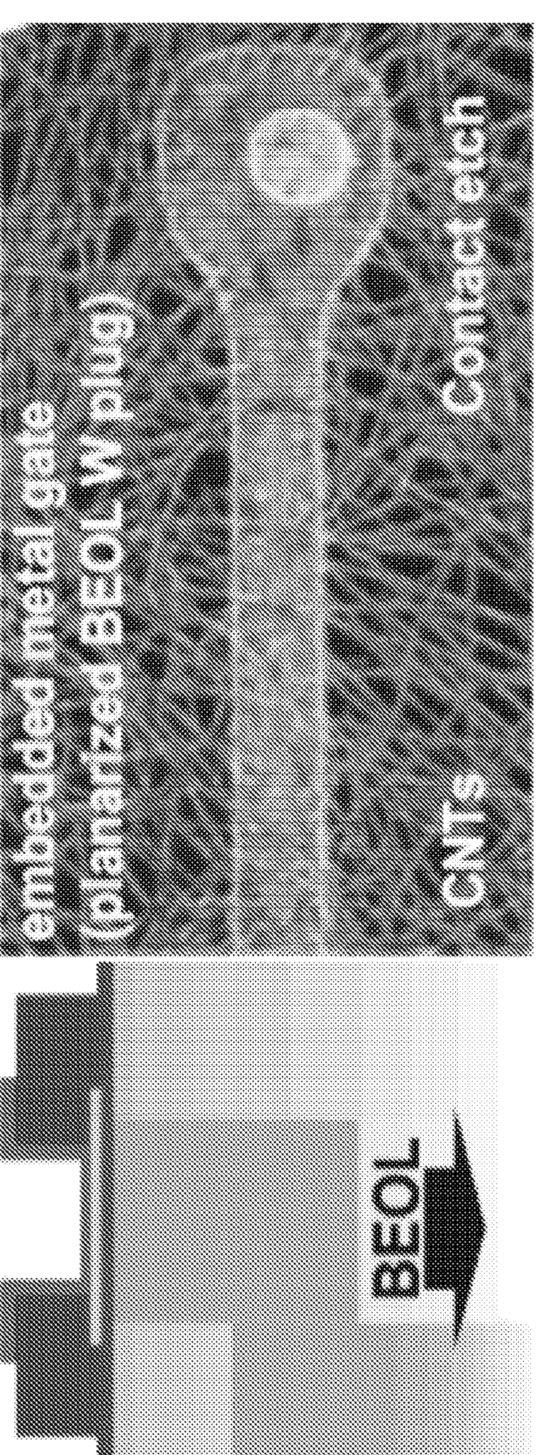


FIG. 16

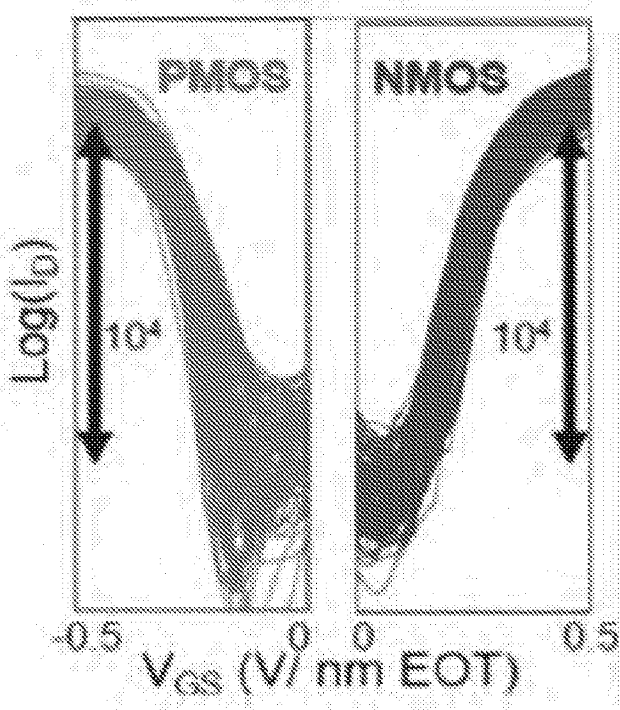


FIG. 17

Al	Sb	As	Ba	Be	Bi	B	Br	Cd	Ca
Ce	Cs	Cr	Co	Cu	Dy	Er	Eu	Gd	Ga
Ge	Au	Hf	Ho	In	I	Ir	Fe	La	Pb
Li	Lu	Mg	Mn	Hg	Mo	Nd	Ni	Nb	Os
Pb	P	Pt	K	Pr	Re	Rh	Rb	Ru	Sm
Sc	Se	Ag	Na	Sr	Ta	Te	Tb	Tl	Th
Tm	Sn	Ti	W	U	V	Yb	Y	Zn	Zr

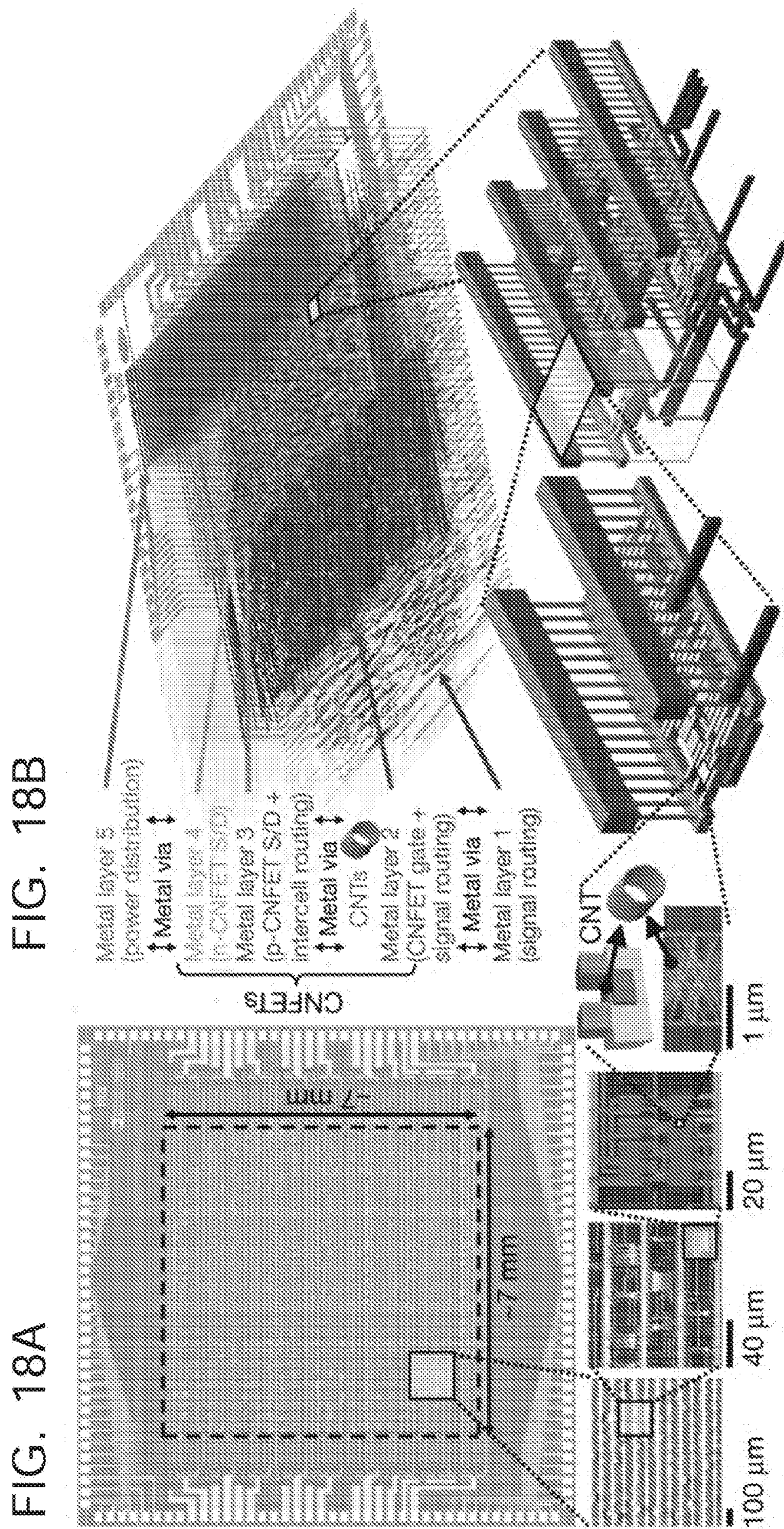


FIG. 18A
~7 mm
~7 mm
100 µm
40 µm
20 µm
1 µm
CNT
FIG. 18B
Metal layer 5
(power distribution)
Metal via
CNFETs
Metal layer 4
(n-CNFET S/D)
Metal layer 3
(p-CNFET S/D +
intercell routing)
Metal via
CNTs
Metal layer 2
(CNFET gate +
signal routing)
Metal via
Metal layer 1
(signal routing)

FIG. 19A

Instruction fetch
Instruction decode
Register read
Execute + memory access
Write-back
PC
State
next pc
Decode
instr
Register file
MUX
MUX
ALU
op
Rotate load
ADDR
RD

FIG. 19B

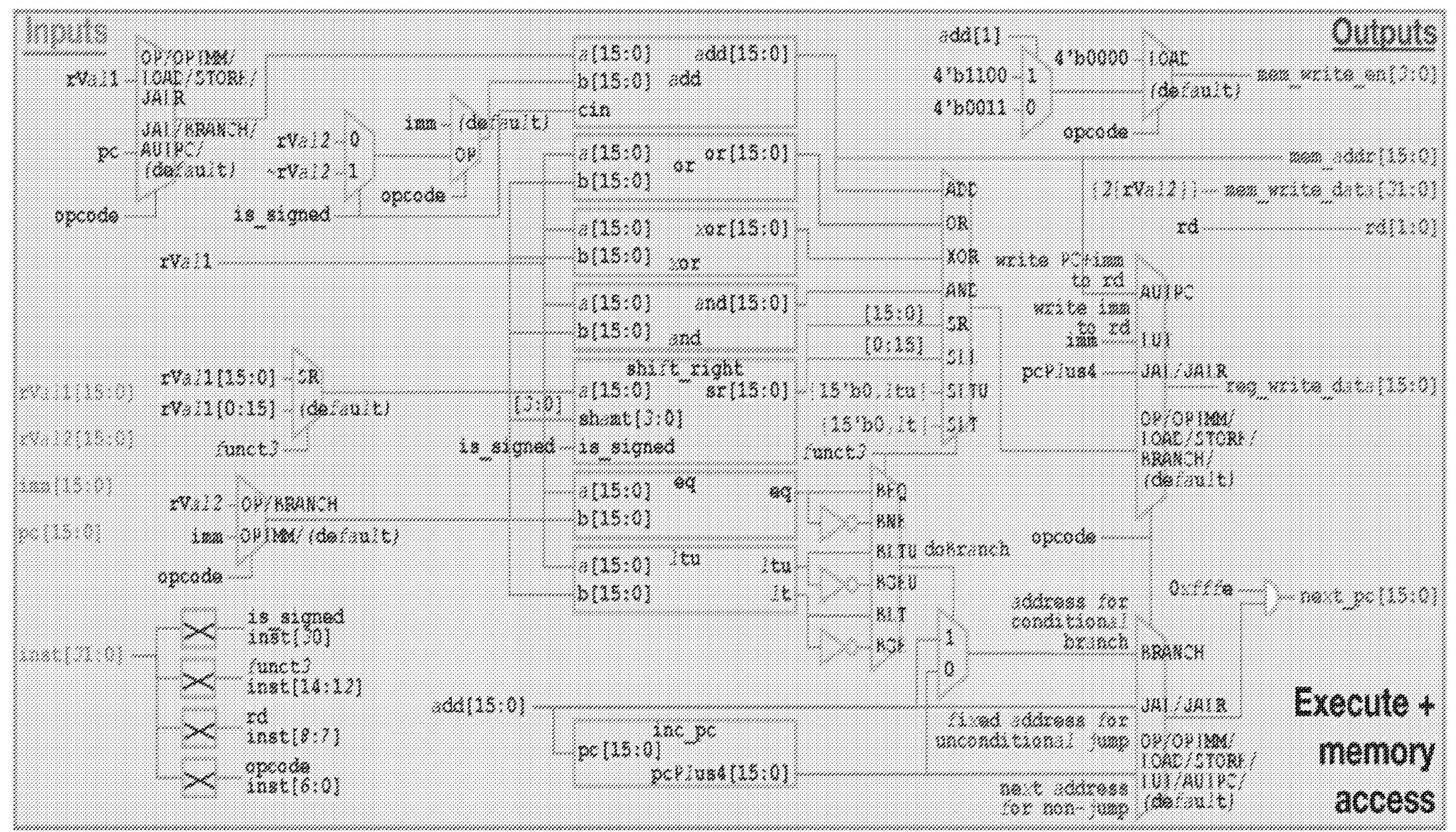


FIG. 19B-contd.

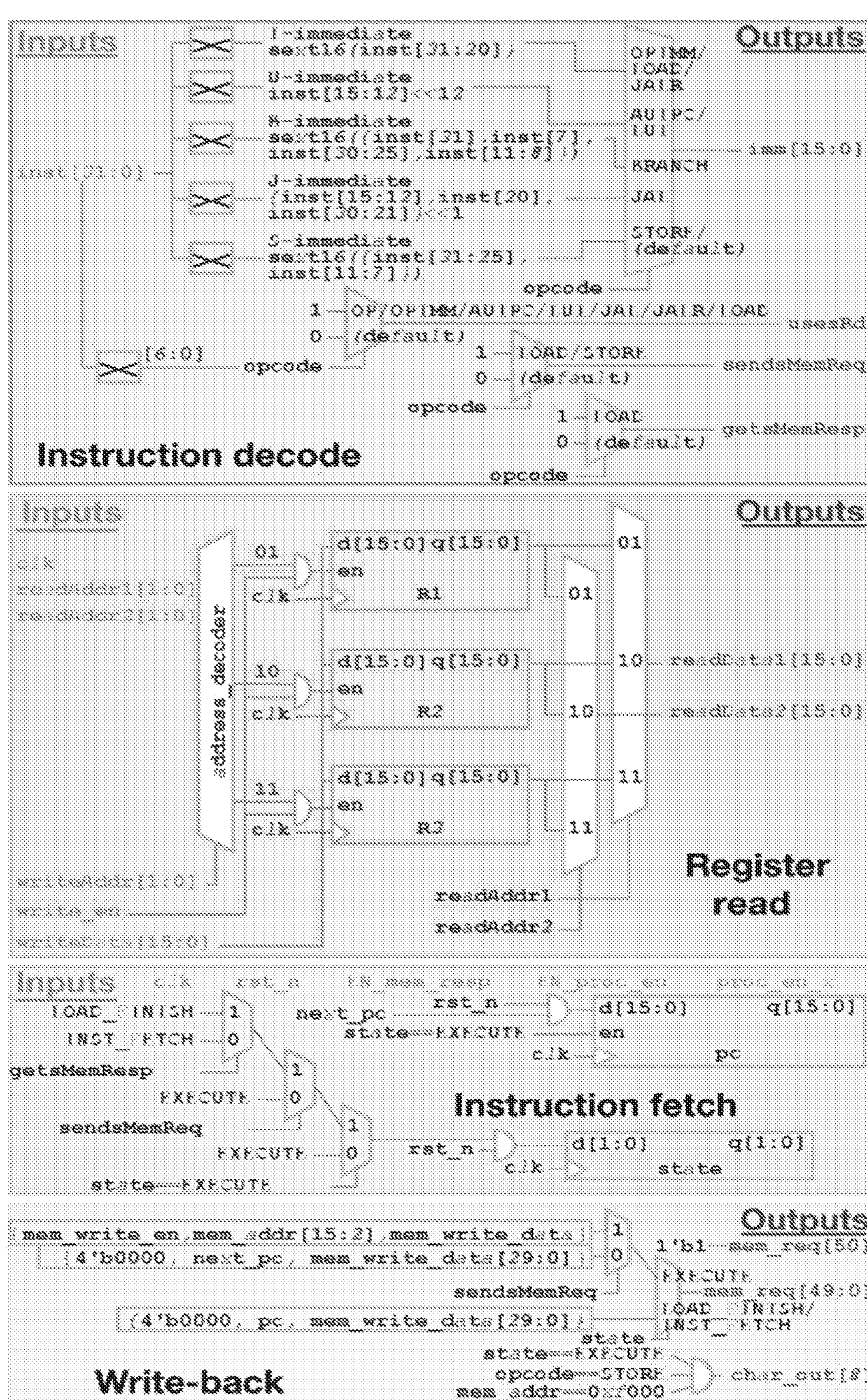


FIG. 20A

Instruction from memory

Program counter

Characters

CLK

Expected

Measured

Hello, world! I am RV16XNano, made from CNTs.

FIG. 20B

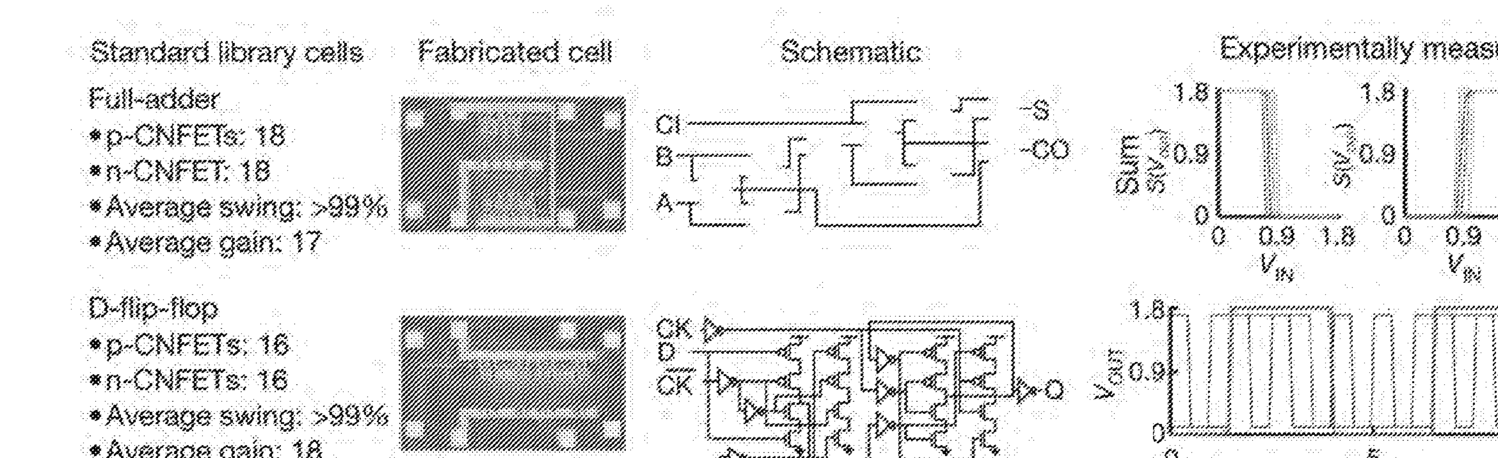


FIG. 21A

Design infrastructure

Fabricate CNFET arrays

② Calibrate compact models to CNFETs (for use in Synopsys HSPICE, Cadence Spectre)

③ Design rule check (Mentor Graphics Calibre)

④ Layout versus schematic

⑤ Parasitic extraction (calibrate to experimental test structures)

⑥ Process design kit integration (with Cadence Virtuoso, with CNFET Pcell, via rules, metal routing)

Process design kit

① Create cell views for all standard library cells (schematic, functional Verilog, layout)

② Design rule check, layout versus schematic, parasitic extraction sign-off (for all standard cells)

③ Standard cell timing/ power characterization (Cadence Liberate)

④ Create abstract standard cell views (for synthesis/ place and route)

Standard library cells

Physical design

① RISC-V specs https://riscv.org/ specifications

② BlueSpec: High-level description of RV16X-NANO

③ Compile BlueSpec to RTL

④ Functional verification of RV16X-NANO

⑤ Logic synthesis (Cadence Genus)

DREAM-enforcing standard cell library

⑥ Functional verification on netlist (Synopsys VCS)

⑦ Placement-and-route (Cadence Innovus)

⑧ Design sign-off (design rule check, layout versus schematic, parasitic extraction power/timing/noise margin)

GDSII (layout design)

Fabrication

Bottom metal layers (signal routing)

Deposit CNTs (low-temperature solution deposition)

RINSE (CNT defect removal)

MIXED (CNFET CMOS fabrication)

Top metal layers (power distribution)

Wafer dicing and packaging ⑥

Testing (programming and running code)

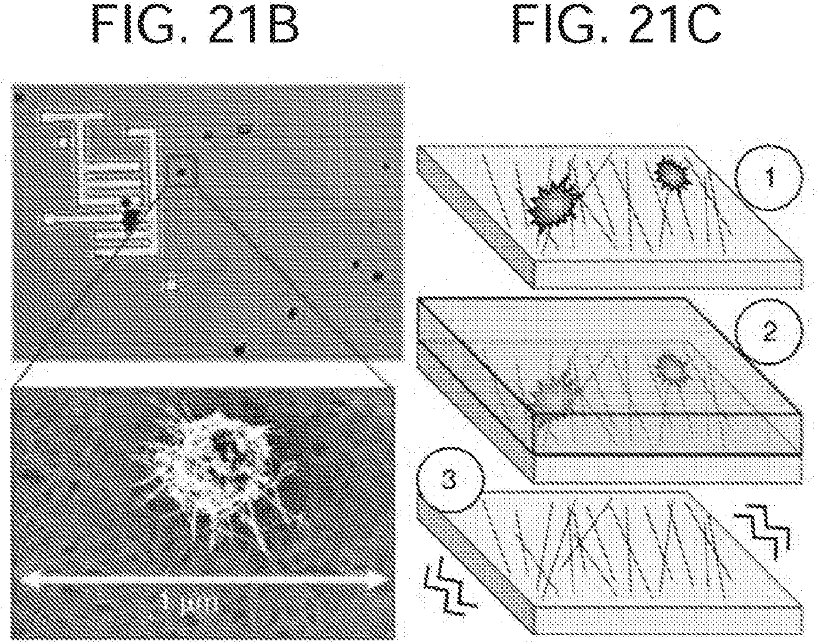


FIG. 21B FIG. 21C

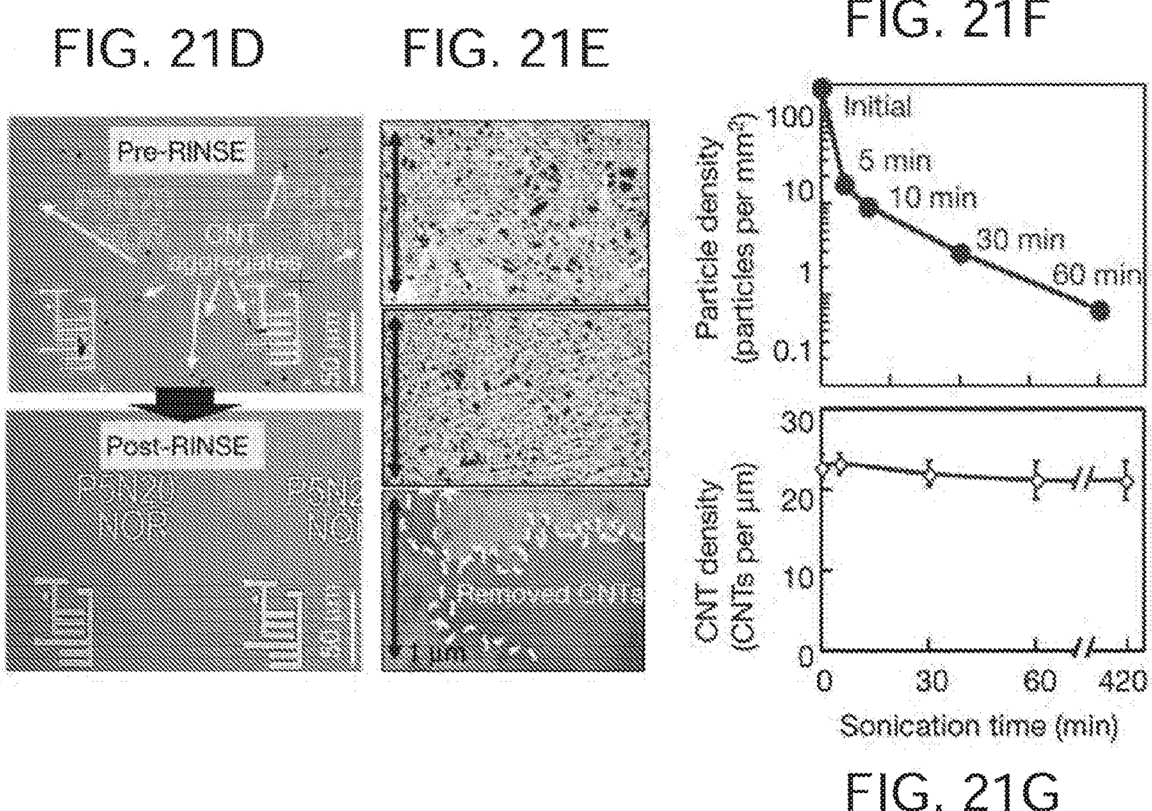


FIG. 21D FIG. 21E FIG. 21F

FIG. 21G

FIG. 22A

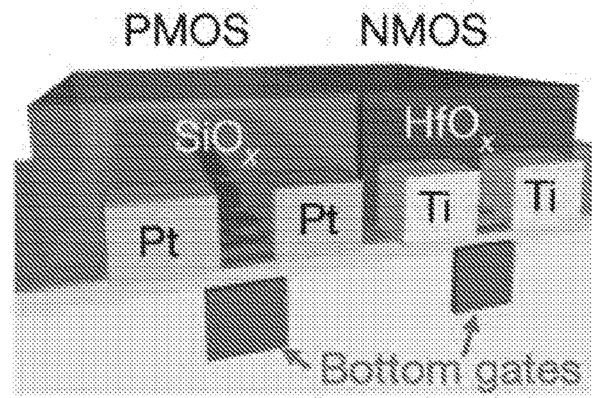


FIG. 22B

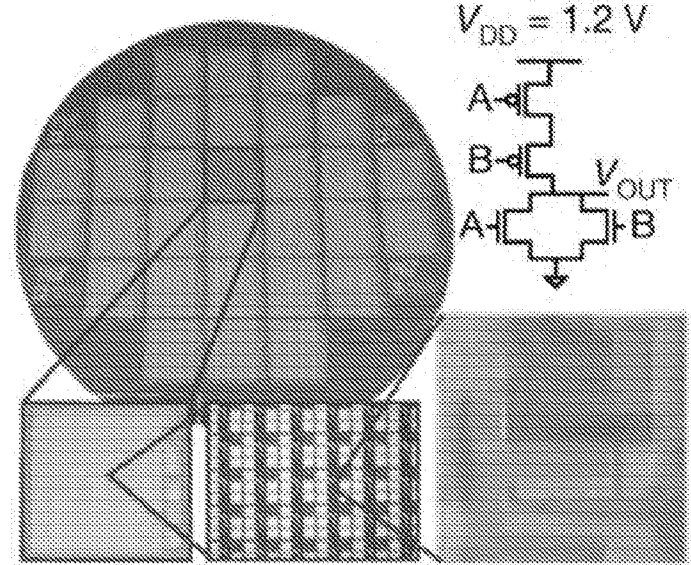


FIG. 22C

PMOS NMOS

I_D (μA)

6
4
2
0

−1.8 0 1.8

V_{DS}

FIG. 22D

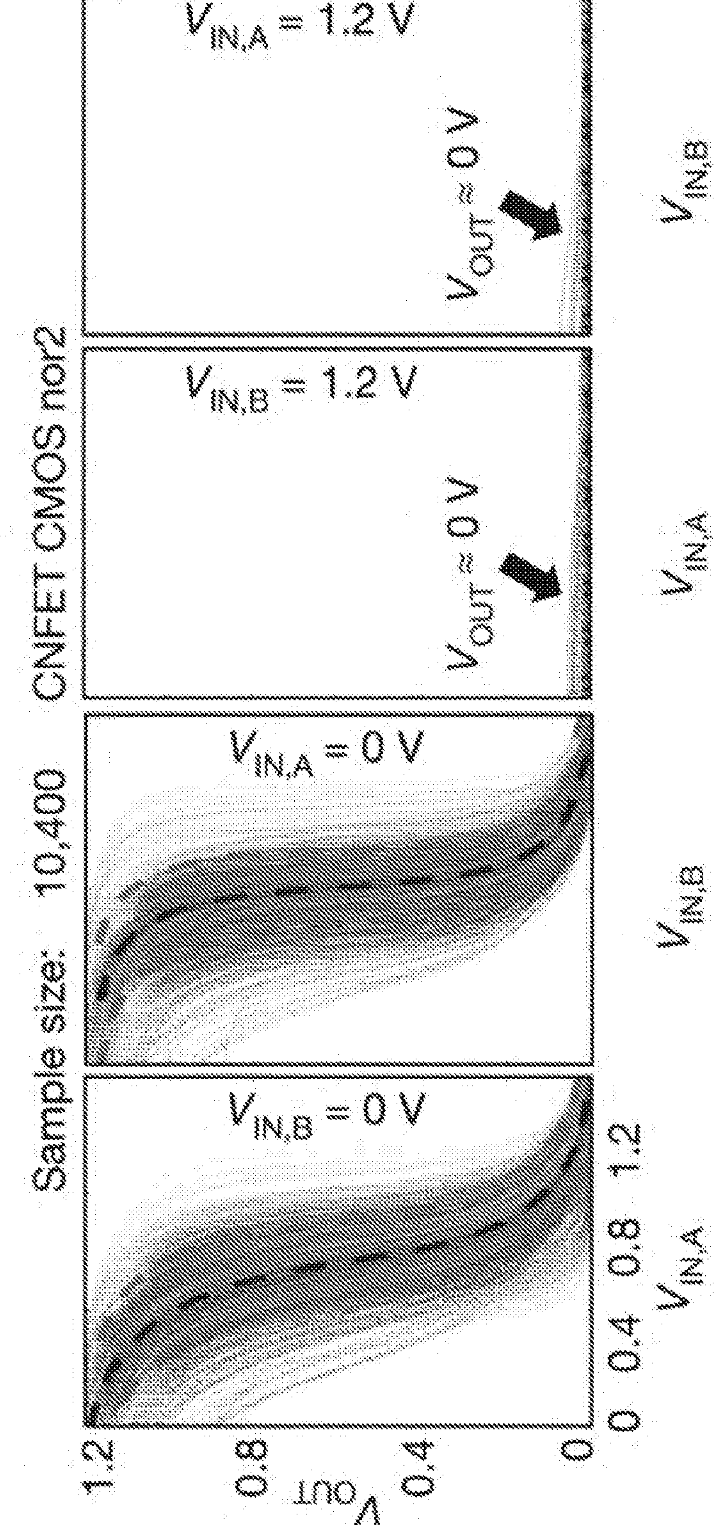


FIG. 23A

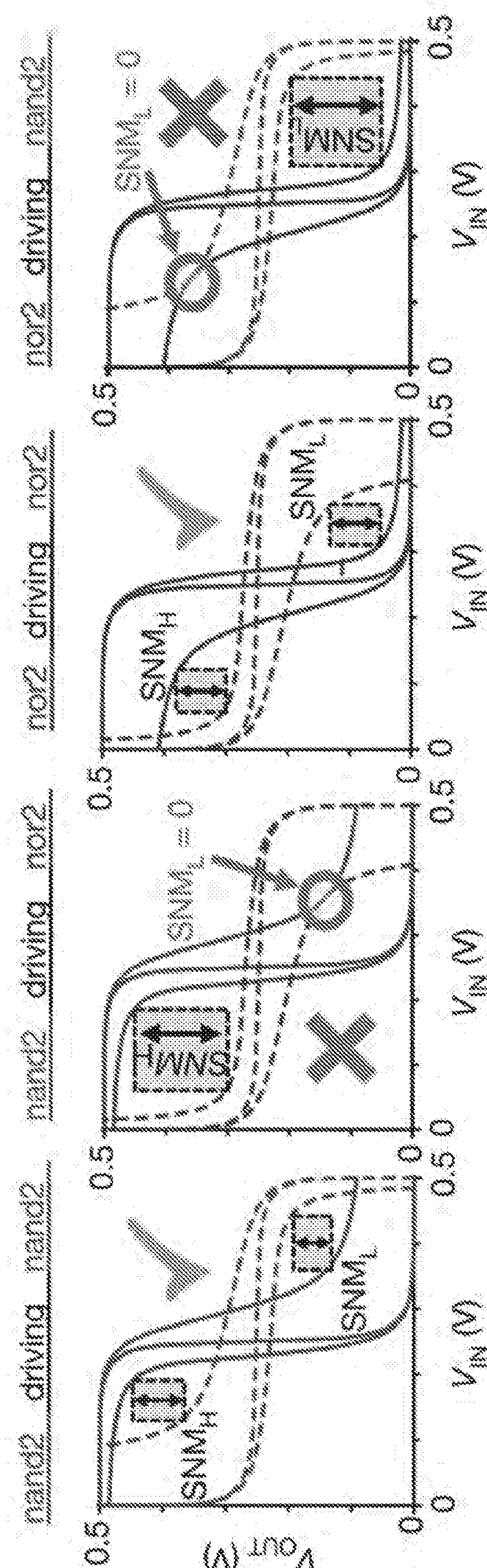


FIG. 23B

SNM (mV)		Loading logic stage						
		(1)	(2)	(3)	(4)	(5)	...	(n)
Driving logic stage	(1) and3stage2	n/a	137	137	111	111		139
	(2) nand2	133	136	108	111	82		113
	(3) nor2	133	108	136	82	111		111
	(4) and3stage1	91	n/a	n/a	n/a	n/a		n/a
	(5) nor3	91	66	96	40	99		69
	...							
	(*n*) oai21	132	110	107	84	82		112

FIG. 23C

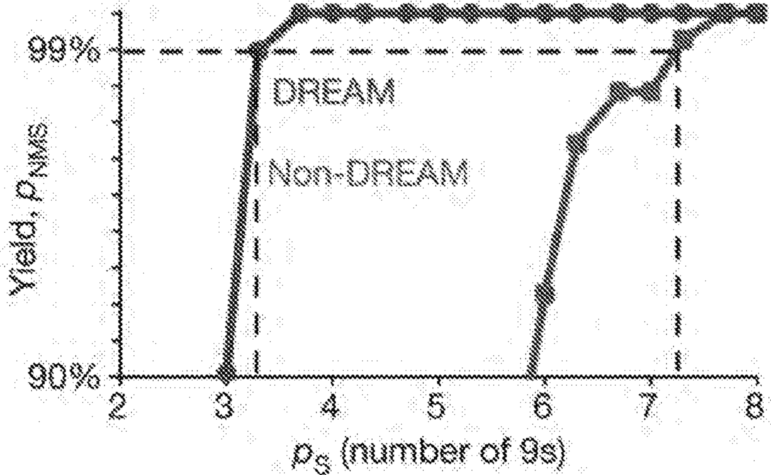


FIG. 23D

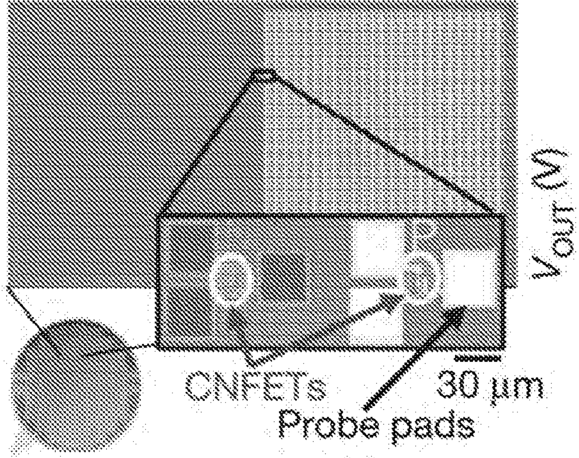


FIG. 23E

nor2 driving nor2

nand2 driving nor2

SNM_H

SNM_L

$SNM_L < 0$

Mirrored VTCs

VTCs

V_{OUT} (V)

V_{IN} (V)

FIG. 23F

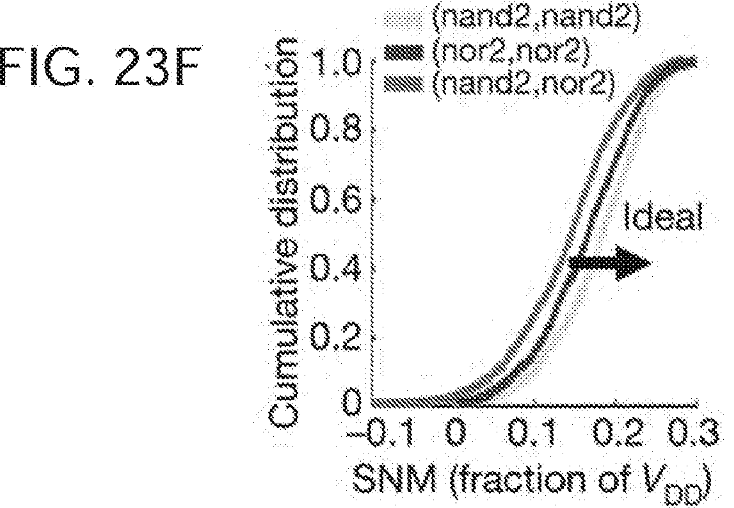


FIG. 24A M1 metal layer: for signal routing

FIG. 24B Interlayer Dielectric (300 °C)

FIG. 24C Via definition (M1 to M2): BCl_3/Cl_2 Reactive Ion Etch

FIG. 24D M2 metal layer: for signal routing + local bottom gates

FIG. 24E Gate dielectric:
Atomic layer deposition (ALD):
(Al_2O_3 + HfO_2, 300 °C)

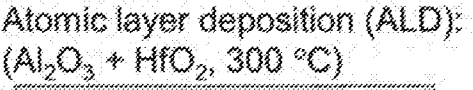
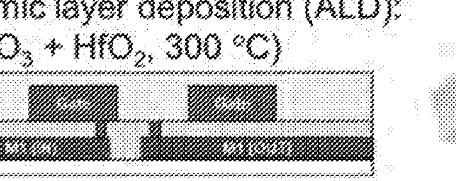



FIG. 24F Via definition (M2 to M3):
BCl_3/Cl_2 Reactive Ion Etch

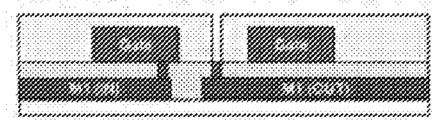
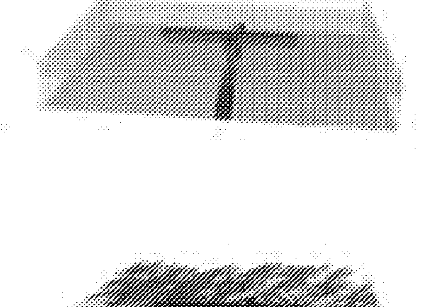



FIG. 24G CNT deposition:
~99.99% s-CNT solution

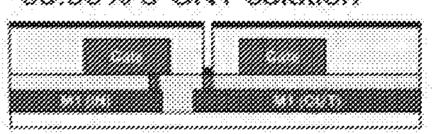


FIG. 24H Active Etch: remove CNTs outside CNFETs
O_2 plasma etch

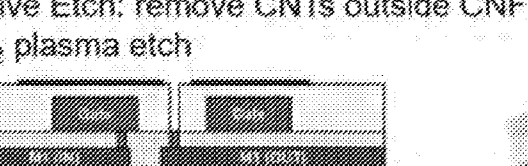
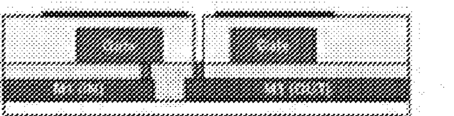
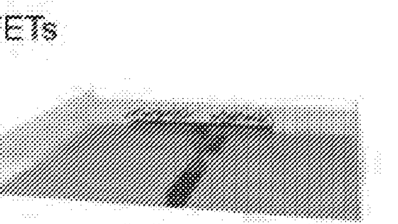
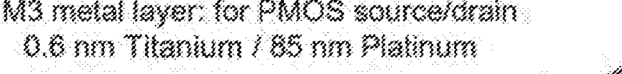




FIG. 24I



M3 metal layer: for PMOS source/drain
0.6 nm Titanium / 85 nm Platinum

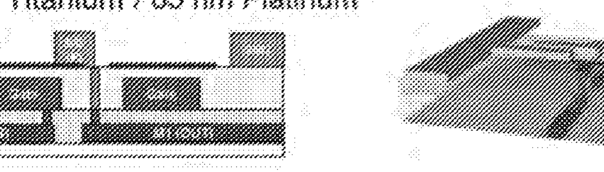
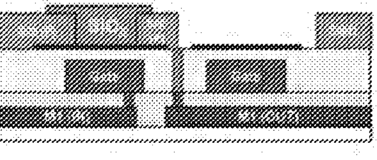


FIG. 24J

PMOS passivation:
100 nm SiO_2



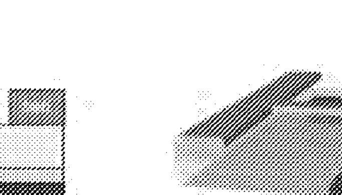


FIG. 24K

M4 metal layer: NMOS source/drain
90 nm Titanium

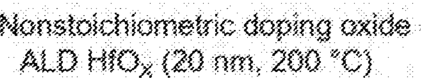
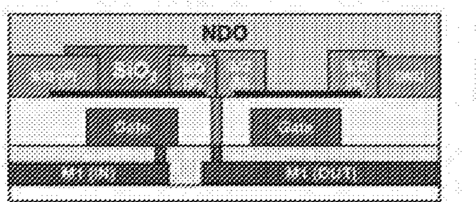


FIG. 24L

Nonstoichiometric doping oxide (NDO):
ALD HfO_x (20 nm, 200 °C)



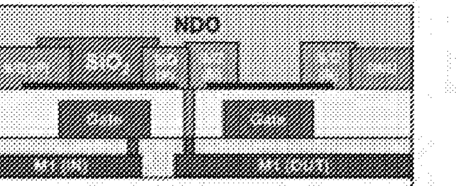


FIG. 24M Via definition (M4 to M5):
+ remove NDO over PMOS CNFET

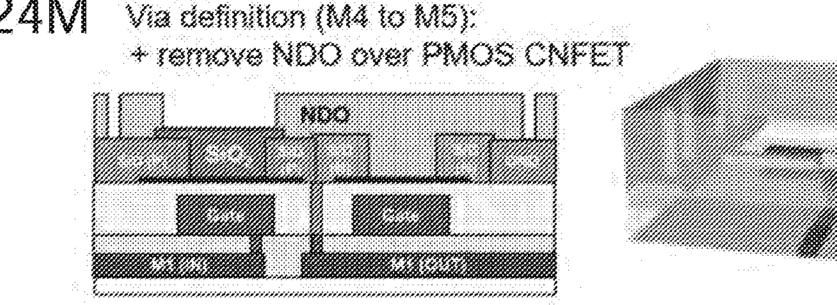


FIG. 24N M5 metal layer: power distribution

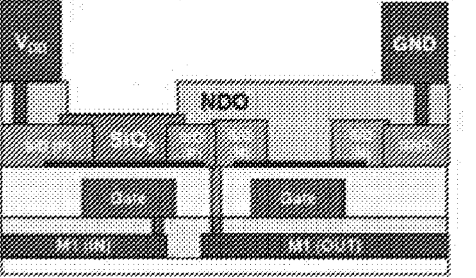


FIG. 25

FIG. 25-contd.

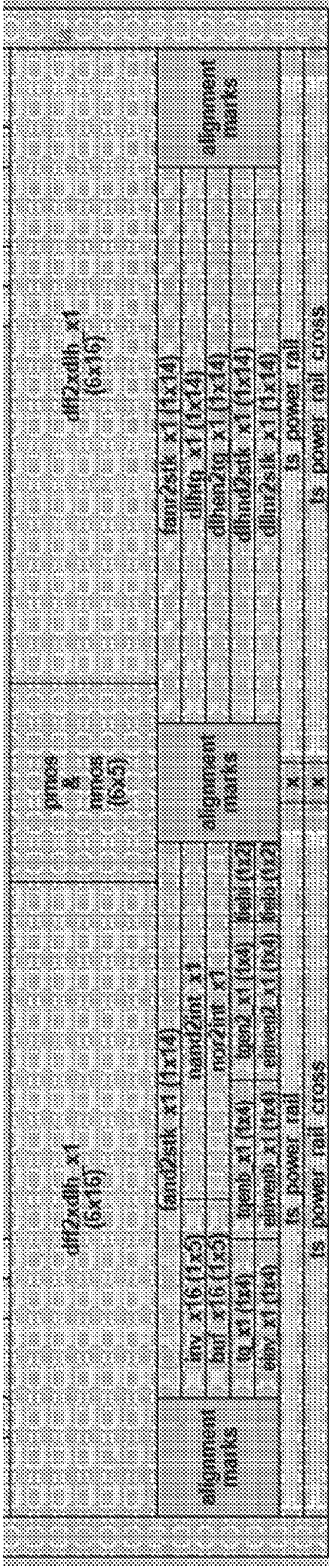


FIG. 25-contd.

FIG. 26

library cell (63)	description
and2_x1	2-input AND
and2nr2_x1	2-input AND (comprising nor2/inv logic stages)
buf_x1	buffer, drive strength 1x
buf_x2	buffer, drive strength 2x
buf_x4	buffer, drive strength 4x
buf_x8	buffer, drive strength 8x
buf_x16	buffer, drive strength 16x
decap_x3	capacitance between power rails, size 1x
decap_x4	capacitance between power rails, size 2x
decap_x5	capacitance between power rails, size 4x
decap_x6	capacitance between power rails, size 8x
decap_x8	capacitance between power rails, size 16x
dff2xdlh_x1	positive edge-triggered D-flip-flop (comprising 2x D-latches), input separate clocks for master/slave
dffck2dlh_x1	positive edge-triggered D-flip-flop (comprising 2x D-latches), input clock and inverted clock
dffck2nd2stk_x1	positive edge-triggered D-flip-flop (comprising nand2/inv logic stages), input clock and inverted clock, 2x cell height
dffck2nr2stk_x1	positive edge-triggered D-flip-flop (comprising nor2/inv logic stages), input clock and inverted clock, 2x cell height
dffck2tg_x1	positive edge-triggered D-flip-flop (comprising D-latch and transmission gate), input clock and inverted clock
dffdlh_x1	positive edge-triggered D-flip-flop (comprising 2x D-latches), inverted clock generated locally
dffnd2stk_x1	positive edge-triggered D-flip-flop (comprising nand2/inv logic stages), 2x cell height
dffnr2stk_x1	positive edge-triggered D-flip-flop (comprising nand2/inv logic stages), 2x cell height
dfftg_x1	positive edge-triggered D-flip-flop (comprising D-latch and transmission gate), inverted clock generated internally
dlhen2tg_x1	high-enable D-latch (comprising transmission gates), input enable and inverted enable
dlhnd2stk_x1	high-enable D-latch (comprising nand2/inv logic stages)

FIG. 26-contd.

dlhtg_x1	high-enable D-latch (comprising transmission gates), inverted enable generated internally
dllnr2stk_x1	high-enable D-latch (comprising nor2/inv logic stages)
einv_x1	tri-state inverter, inverted enable generated internally
einven2_x1	tri-state inverter, input enable and inverted enable
einvenb_x1	tri-state inverter, enable (and inverted enable) buffered internally
fand2stk_x1	full-adder (comprising nand2/inv logic stages)
fanr2stk_x1	full-adder (comprising nor2/inv logic stages)
fill_x1	fill cell (extends power rails), size 1x
fill_x2	fill cell (extends power rails), size 2x
fill_x4	fill cell (extends power rails), size 4x
fill_x8	fill cell (extends power rails), size 8x
fill_x16	fill cell (extends power rails), size 16x
inv_x1	inverter, drive strength 1x
inv_x2	inverter, drive strength 2x
inv_x4	inverter, drive strength 4x
inv_x8	inverter, drive strength 8x
inv_x16	inverter, drive strength 16x
mux2nd2_x1	2-input multiplexer (comprising nand2/inv logic stages)
mux2nr2_x1	2-input multiplexer (comprising nor2/inv logic stages)
mux2s2tg_x1	2-input multiplexer (comprising transmission gates), input select and inverted select
mux2s2tgstk_x1	2-input multiplexer (comprising transmission gates), input selected and inverted select, 2x cell height
mux2sbtg_x1	2-input multiplexer (comprising transmission gates), select (and inverted select) buffered internally
mux2sbtgstk_x1	2-input multiplexer (comprising transmission gates), select (and inverted select) buffered internally, 2x cell height
mux2tg_x1	2-input multiplexer (comprising transmission gates), inverted select generated internally

FIG. 26-contd.

mux2tgstk_x1	2-input multiplexer (comprising transmission gates), inverted select generated internally, 2x cell height
nand2_x1	2-input NOT-AND
nand2nr2_x1	2-input NOT-AND (comprising nor2/inv logic stages)
nor2_x1	2-input NOT-OR
nor2nd2_x1	2-input NOT-OR (comprising nand2/inv logic stages)
or2_x1	2-input OR
or2nd2_x1	2-input OR (comprising nand2/inv logic stages)
tg_x1	transmission gate, inverted enable generated internally
tgen2_x1	transmission gate, input enable and inverted enable
tgenb_x1	transmission gate, enable (and inverted enable) buffered internally
tiehi_x2	output is tied high (to VDD)
tielo_x2	output is tied low (to VSS)
xnor2nd2_x1	2-input EXCLUSIVE-NOT-OR (comprising nand2/inv logic stages)
xnor2nr2_x1	2-input EXCLUSIVE-NOT-OR (comprising nor2/inv logic stages)
xor2nd2_x1	2-input EXCLUSIVE-OR (comprising nand2/inv logic stages)
xor2nr2_x1	2-input EXCLUSIVE-OR (comprising nor2/inv logic stages)

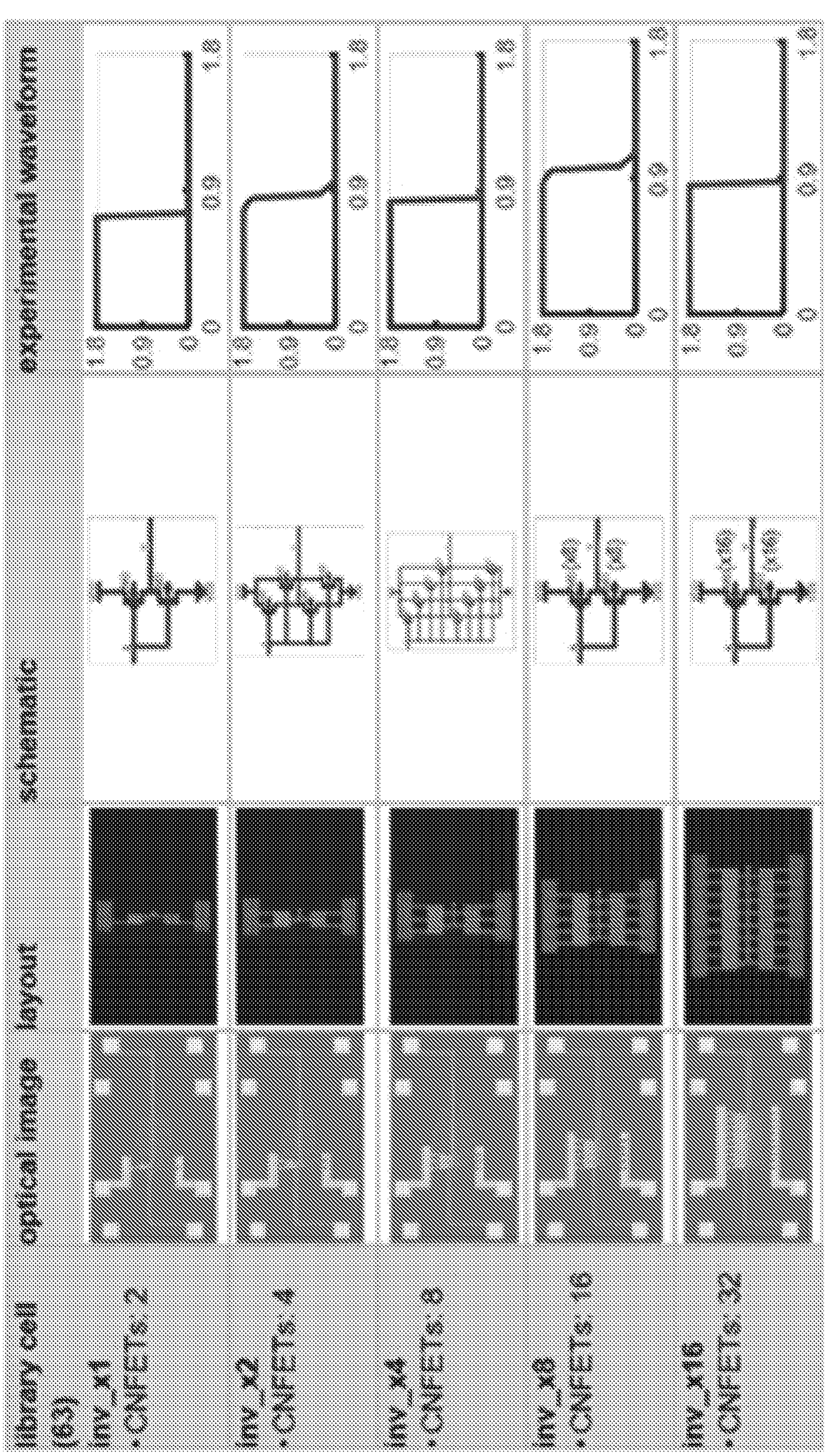


FIG. 26-contd.

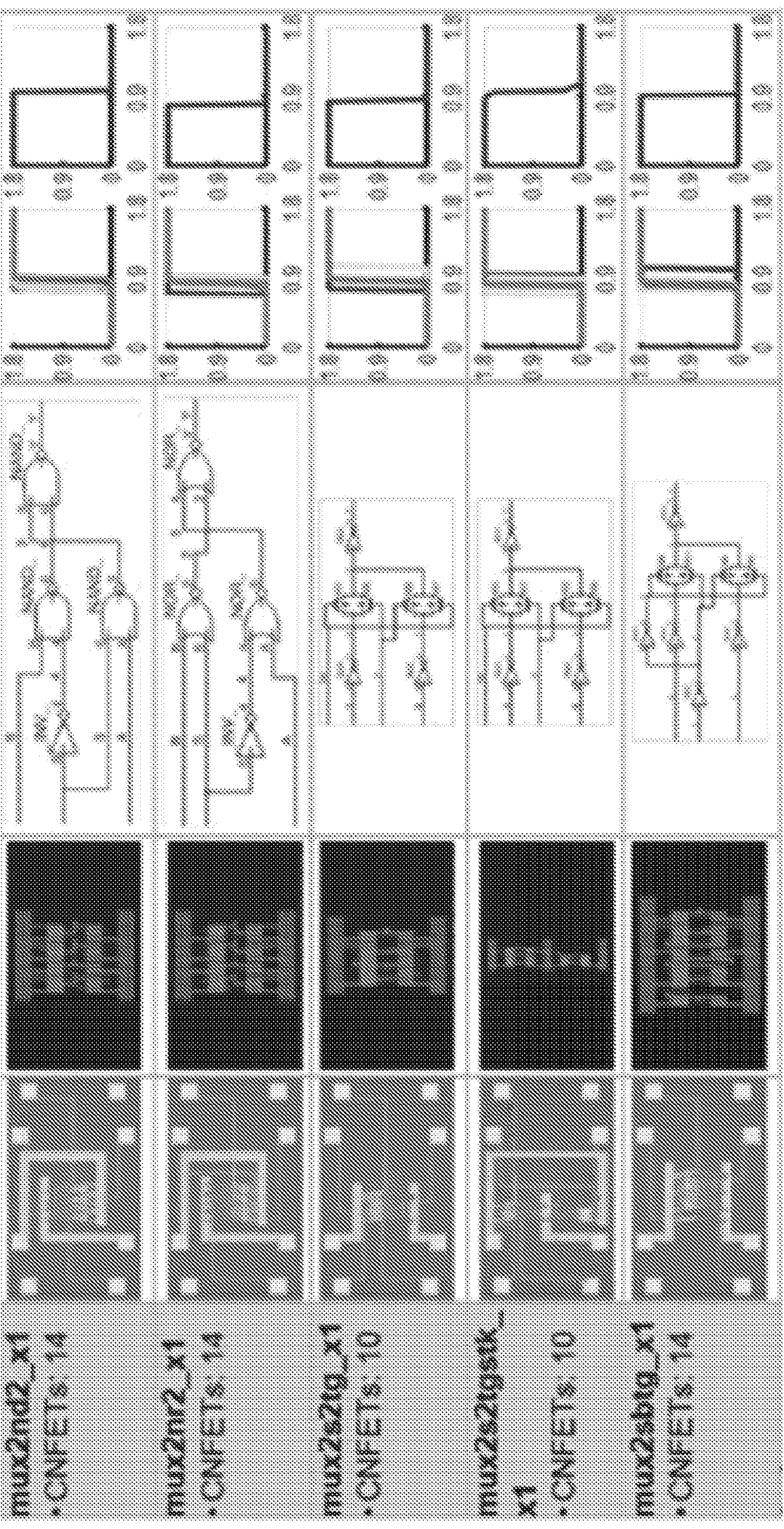


FIG. 26-contd.

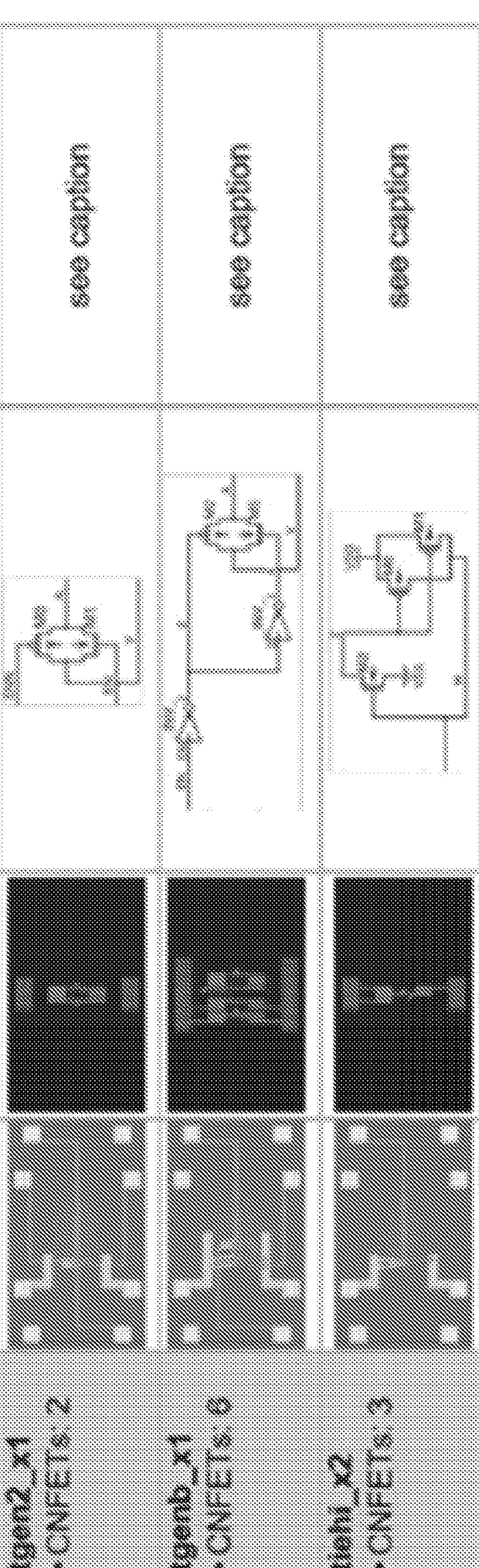
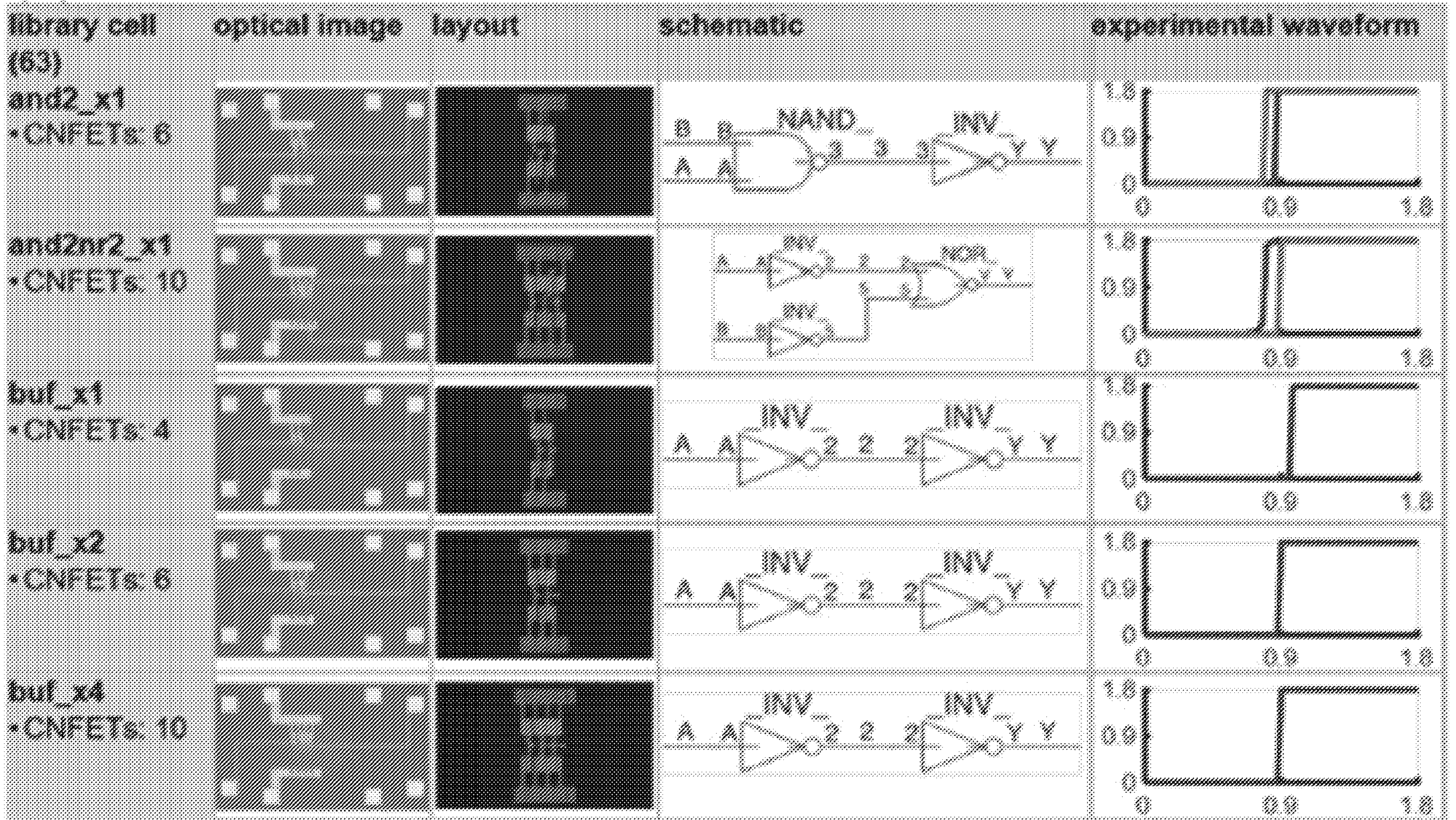


FIG. 26-contd.

FIG. 26-contd.



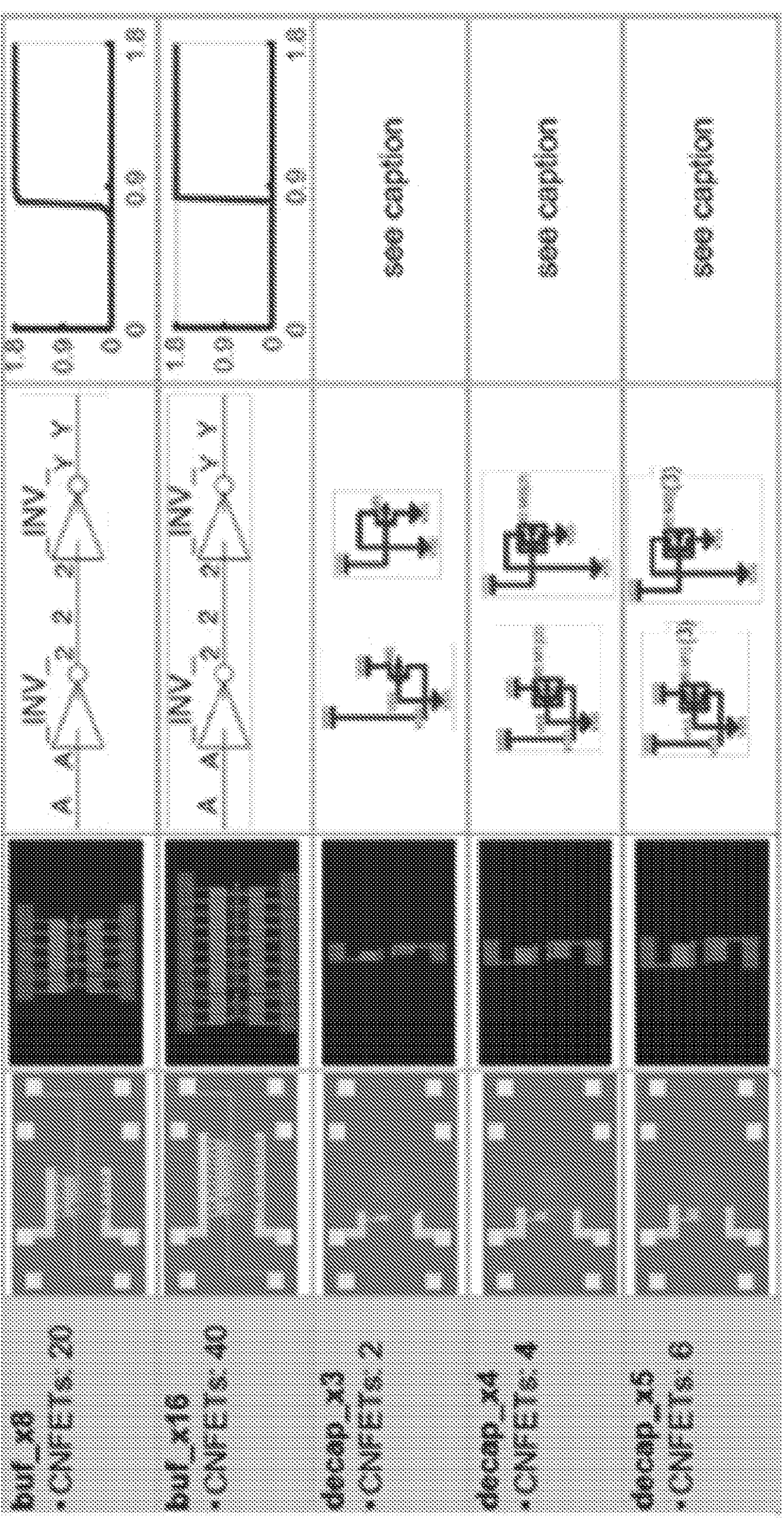


FIG. 26-contd.

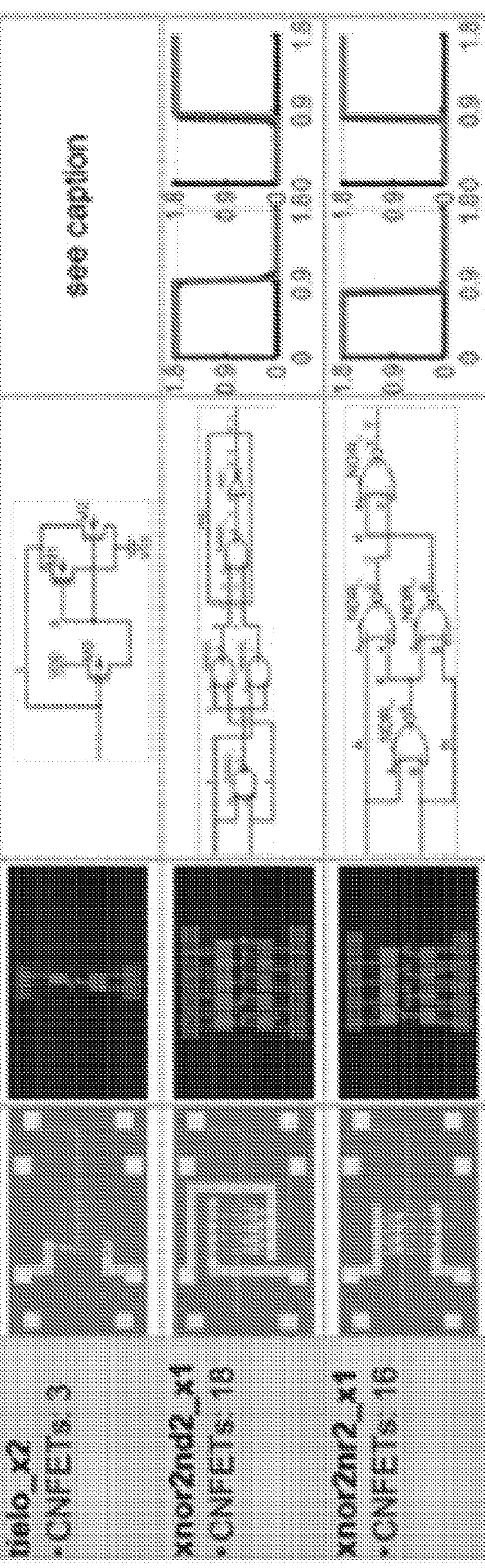
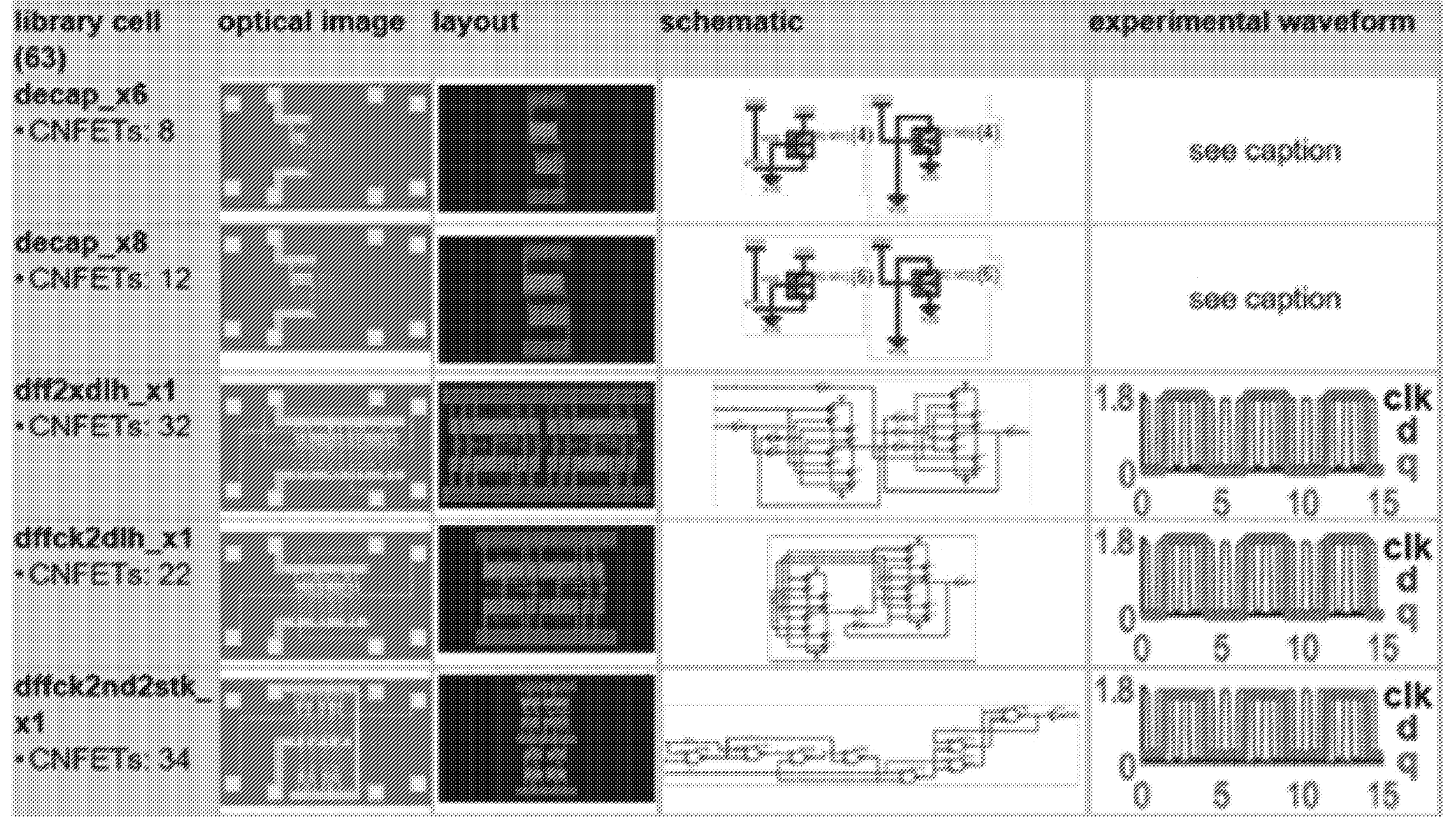


FIG. 26-contd.

FIG. 26-contd.



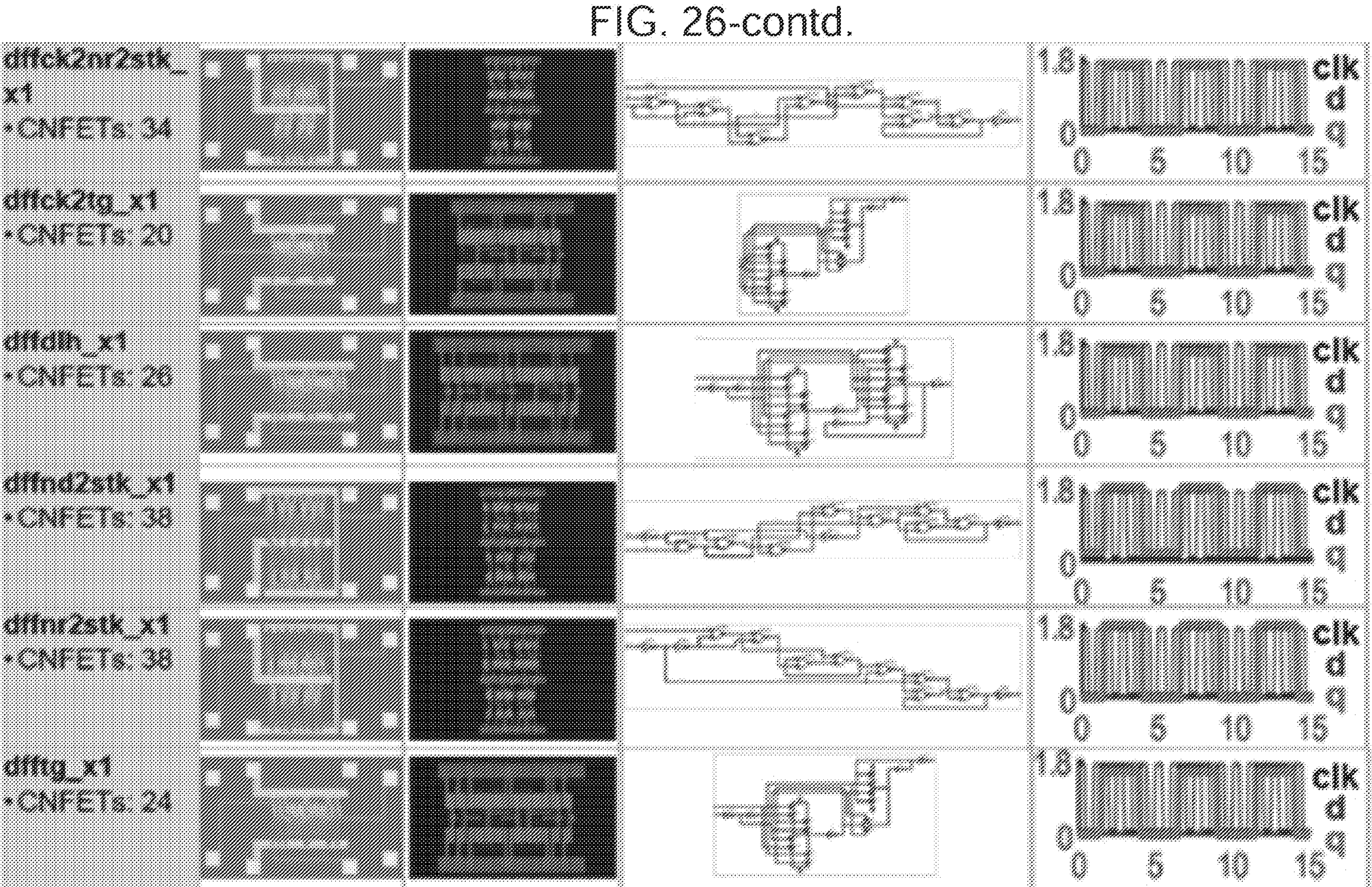


FIG. 26-contd.

FIG. 26-contd.

dlhen2tg_x1
• CNFETs: 12
1.8 0 0 5 10 15 clk d q

dlhnd2stk_x1
• CNFETs: 18
1.8 0 0 5 10 15 clk d q

dlhtg_x1
• CNFETs: 16
1.8 0 0 5 10 15 clk d q

dllnr2stk_x1
• CNFETs: 18
1.8 0 0 5 10 15 $\overline{clk}$ d q

einv_x1
• CNFETs: 6
1.8 0.9 0 0 0.9 1.8

einven2_x1
• CNFETs: 4
1.8 0.9 0 0 0.9 1.8

FIG. 26-contd.

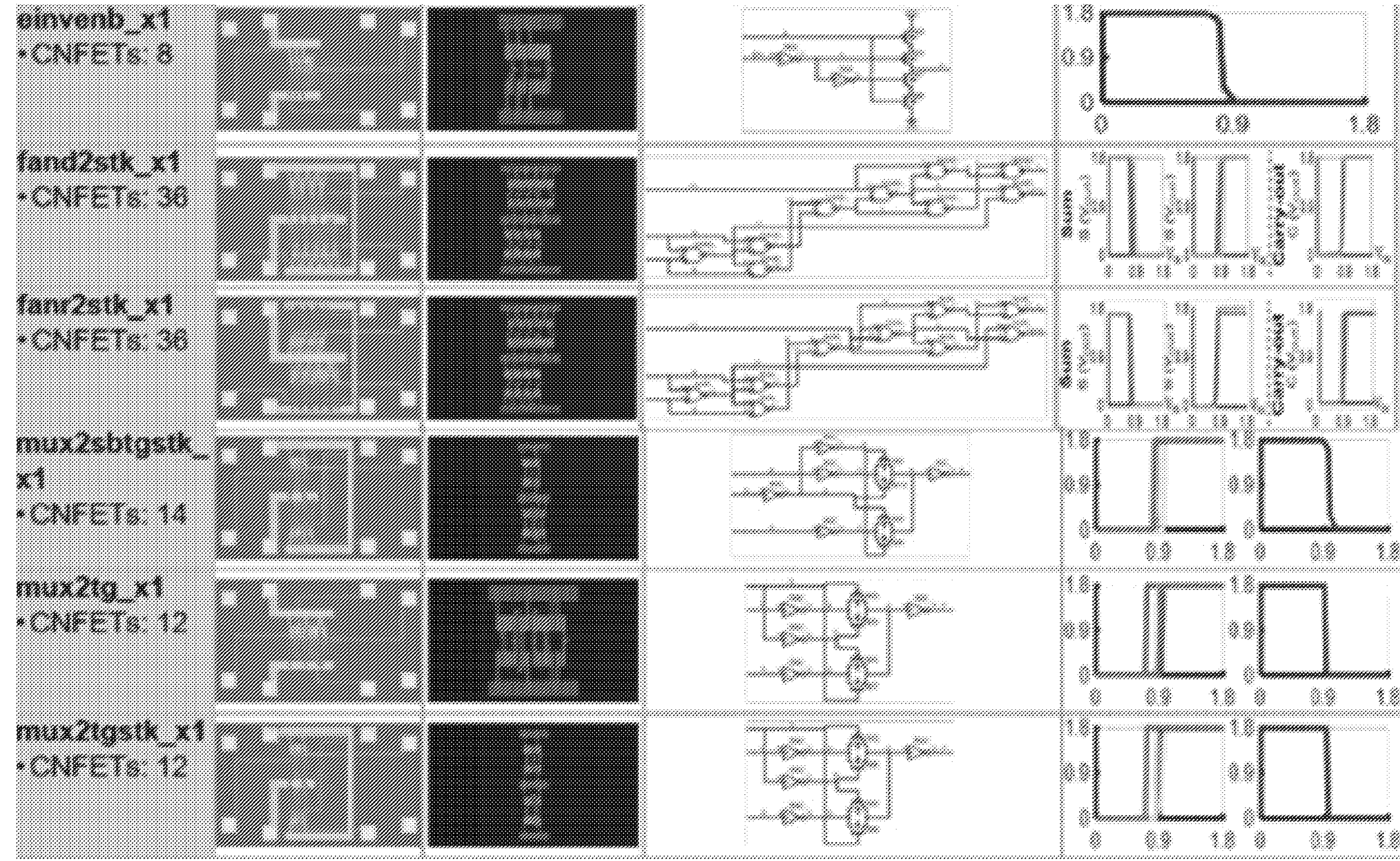
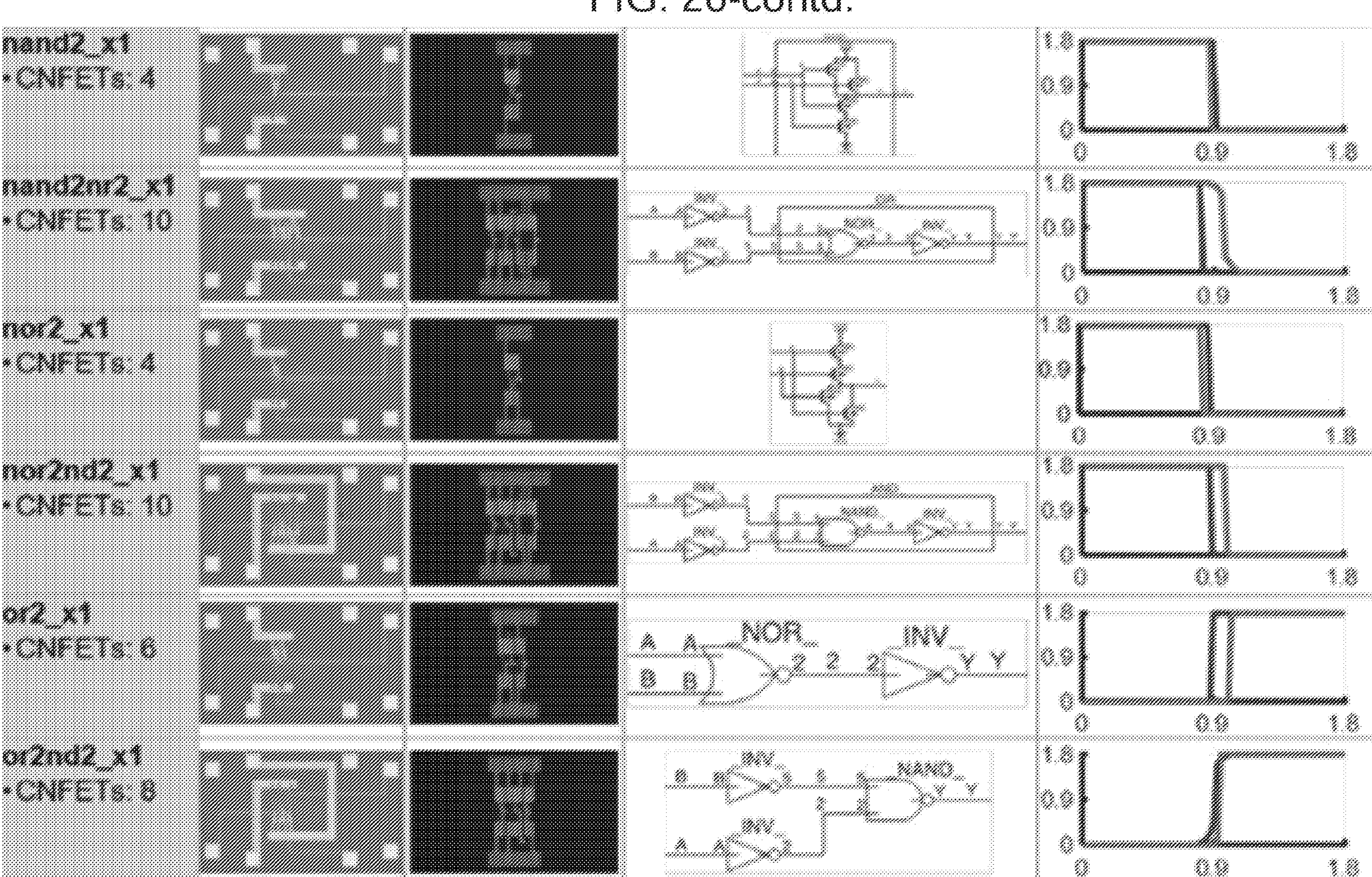


FIG. 26-contd.



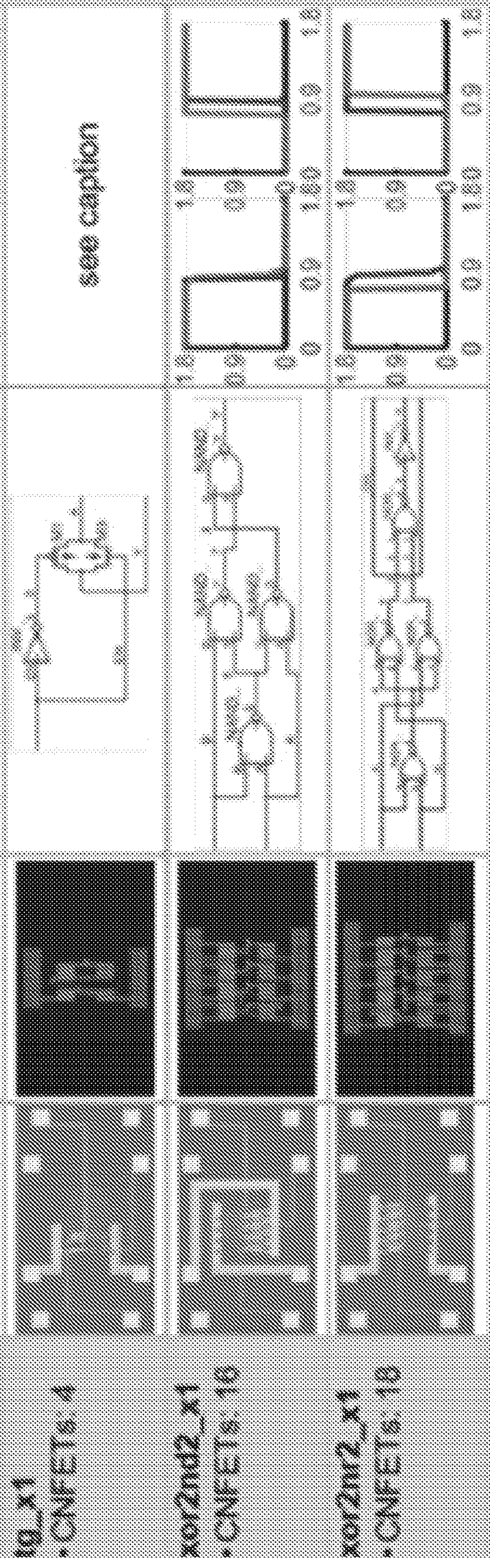


FIG. 26-contd.

FIG. 27

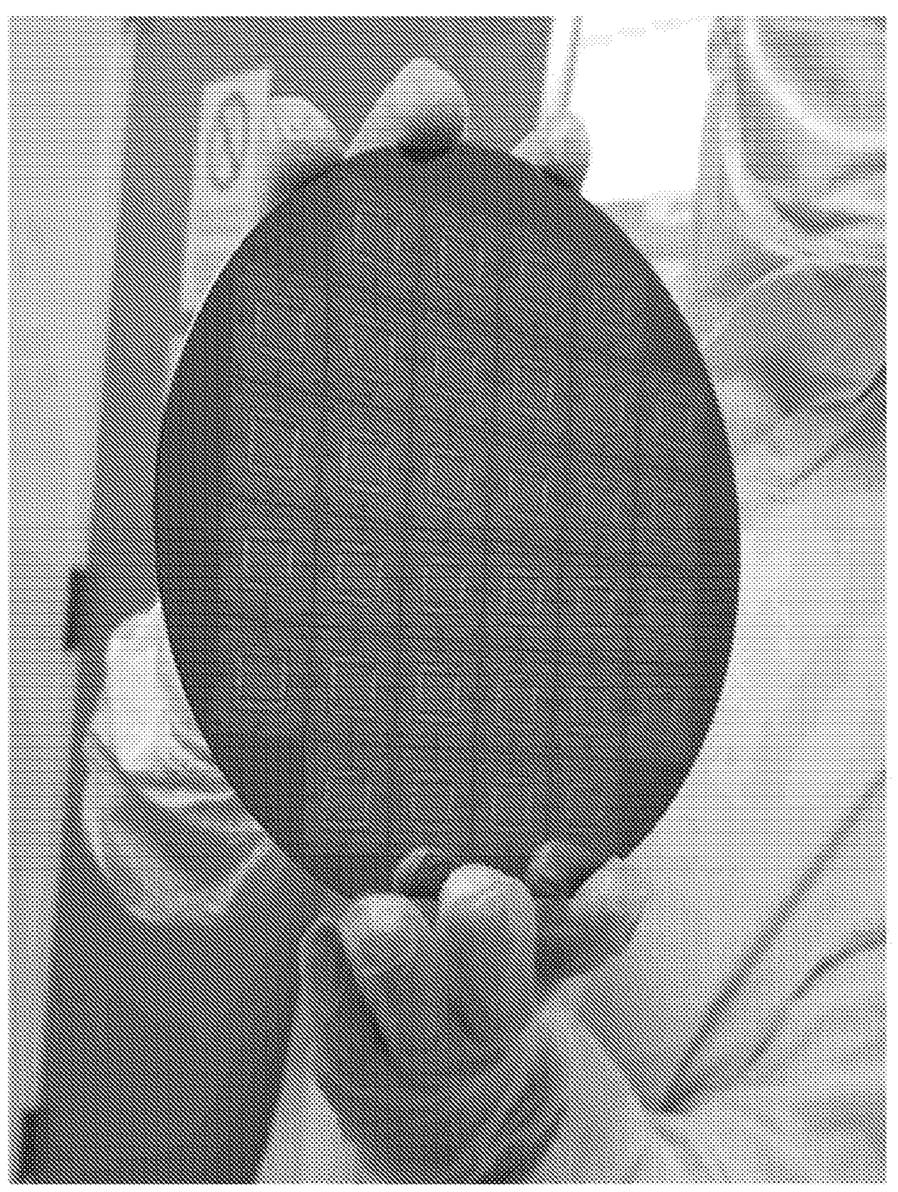
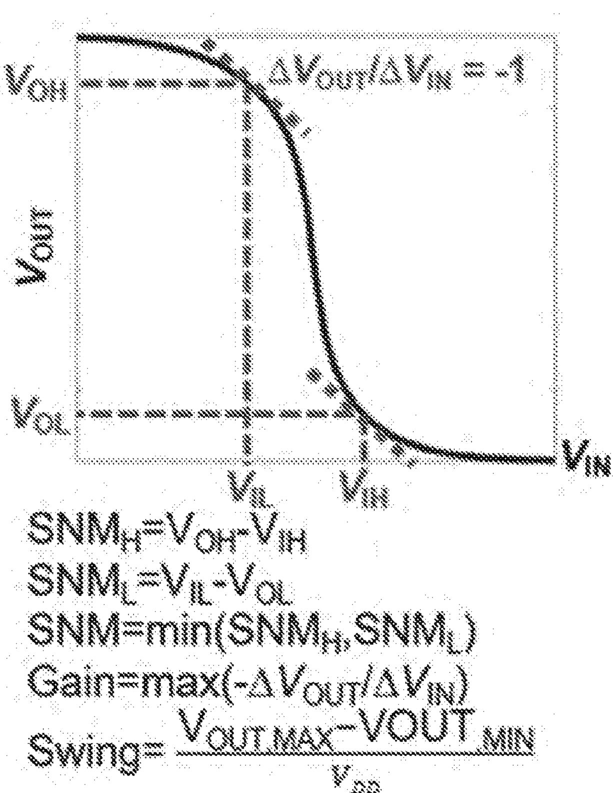


FIG. 28A

FIG. 28B

FIG. 28C

FIG. 29A



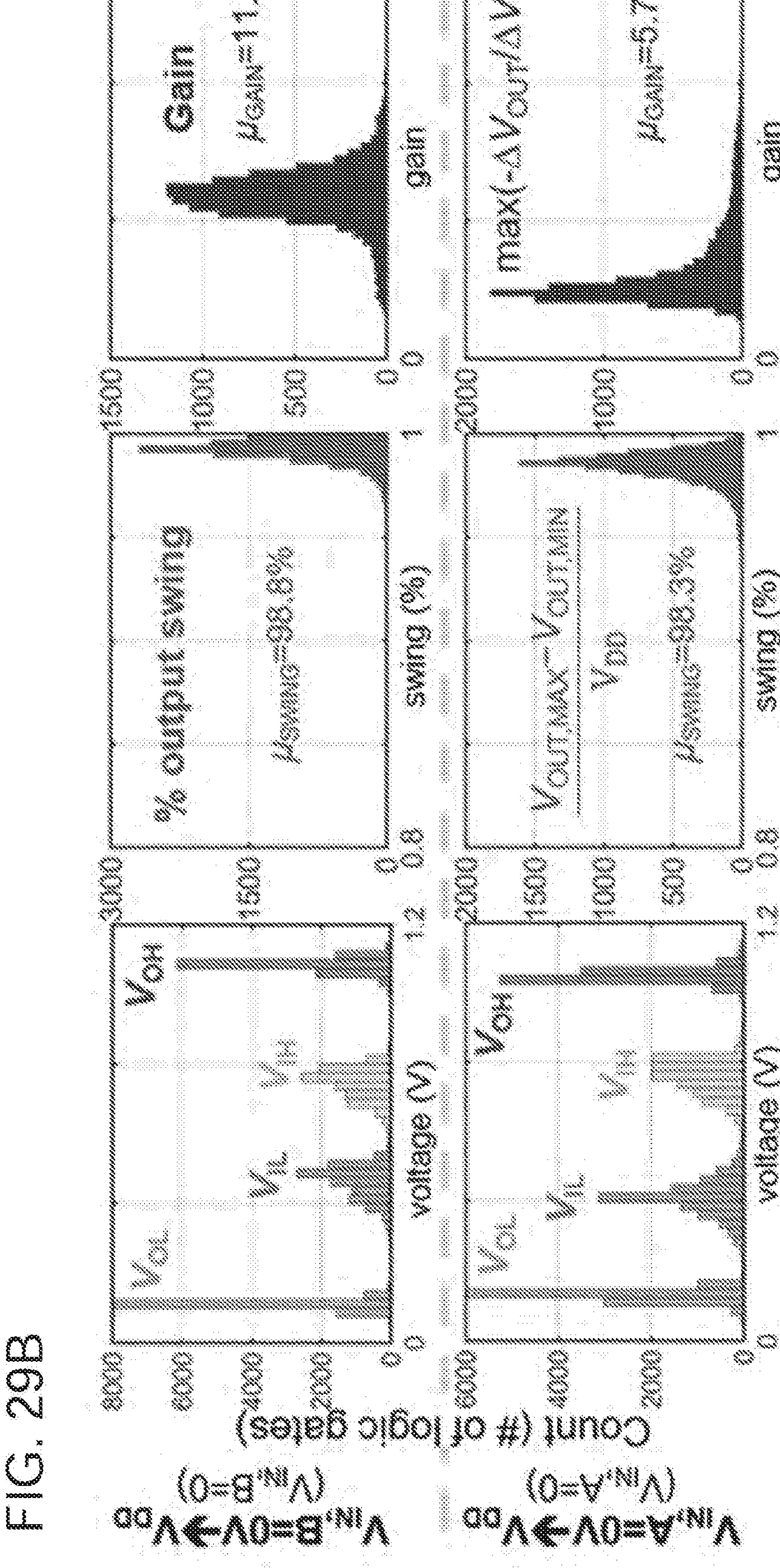


FIG. 29B

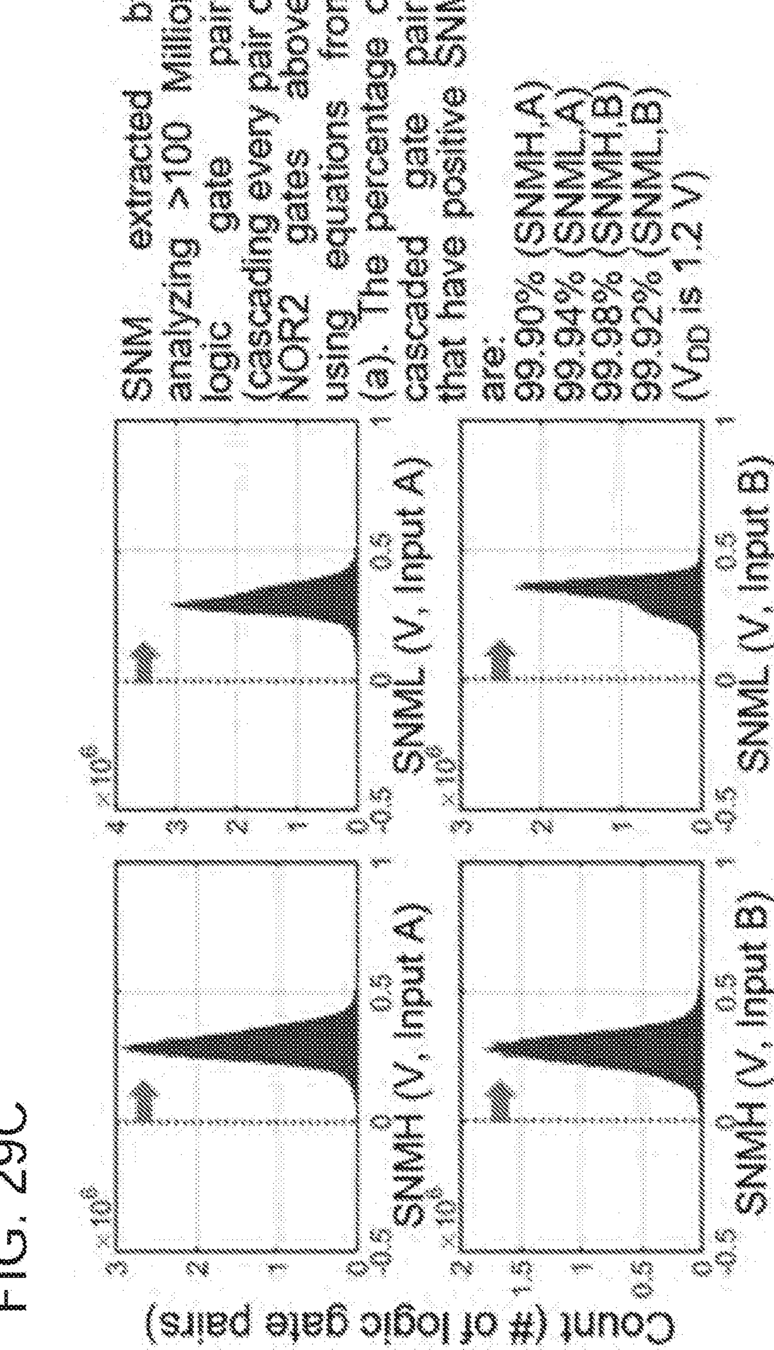
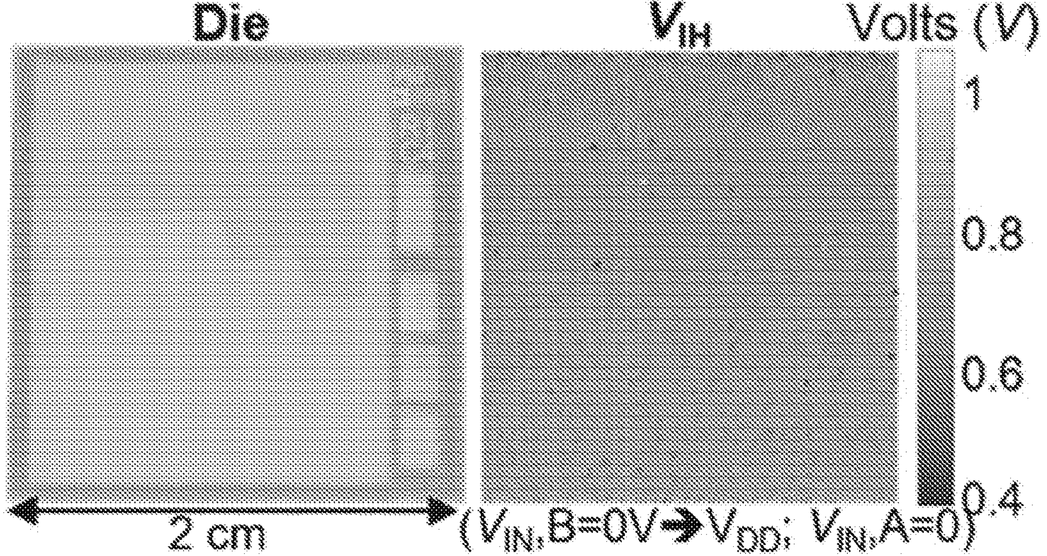


FIG. 29C

FIG. 29D



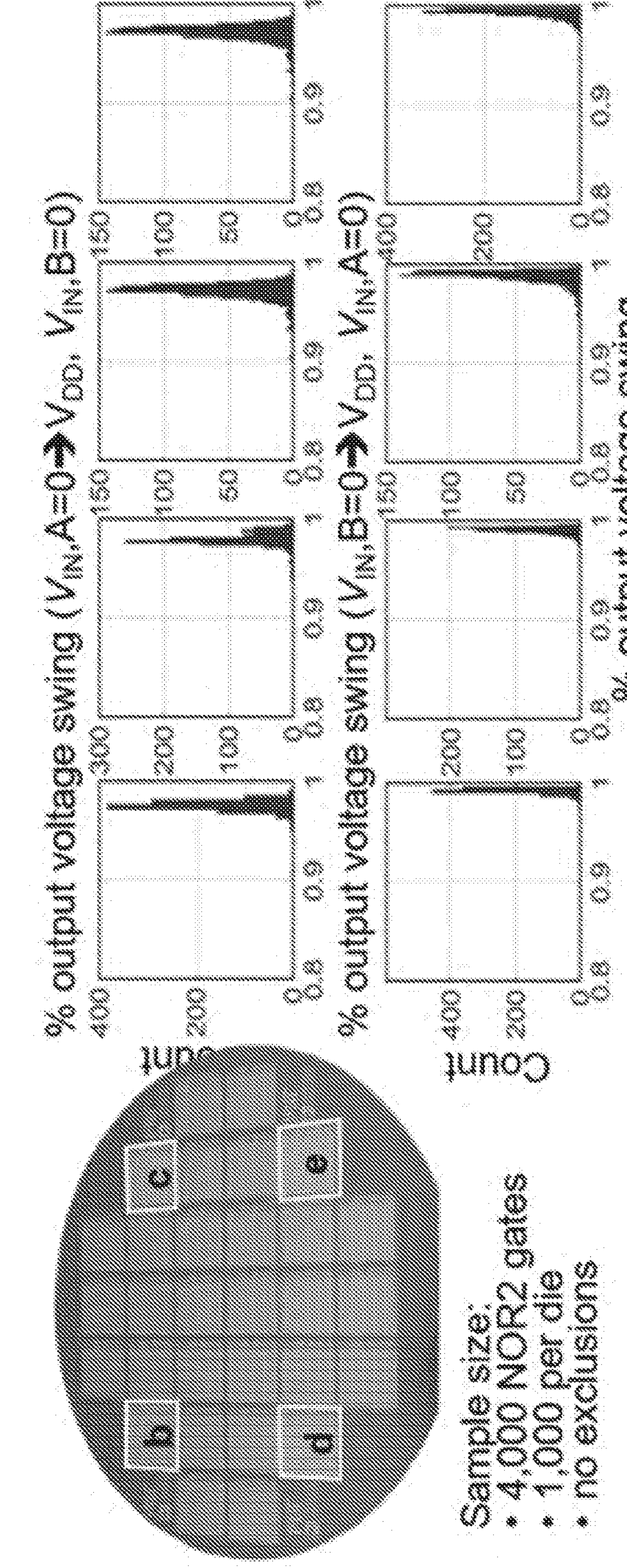


FIG. 29E

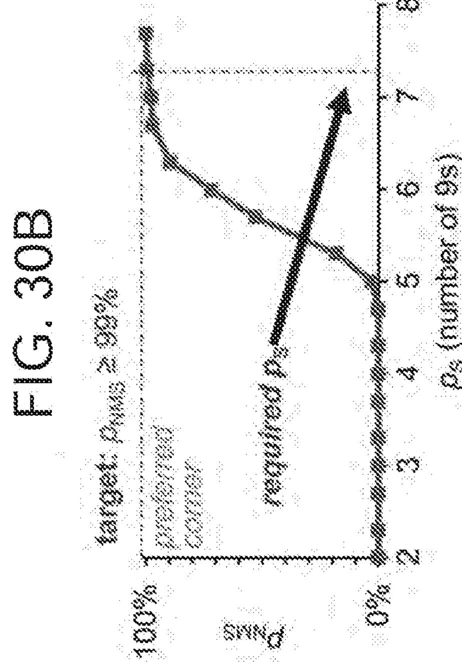


FIG. 30B

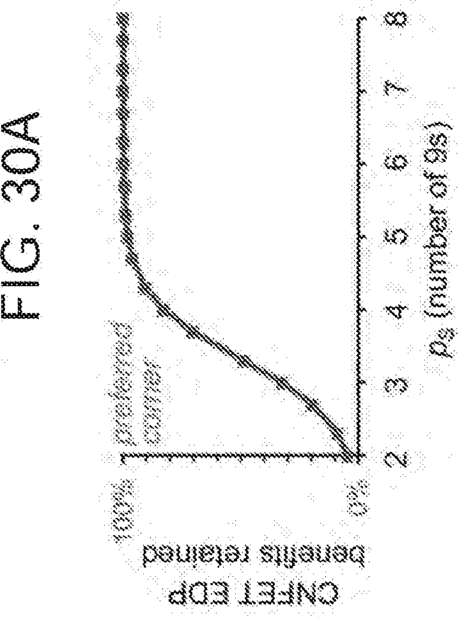


FIG. 30A

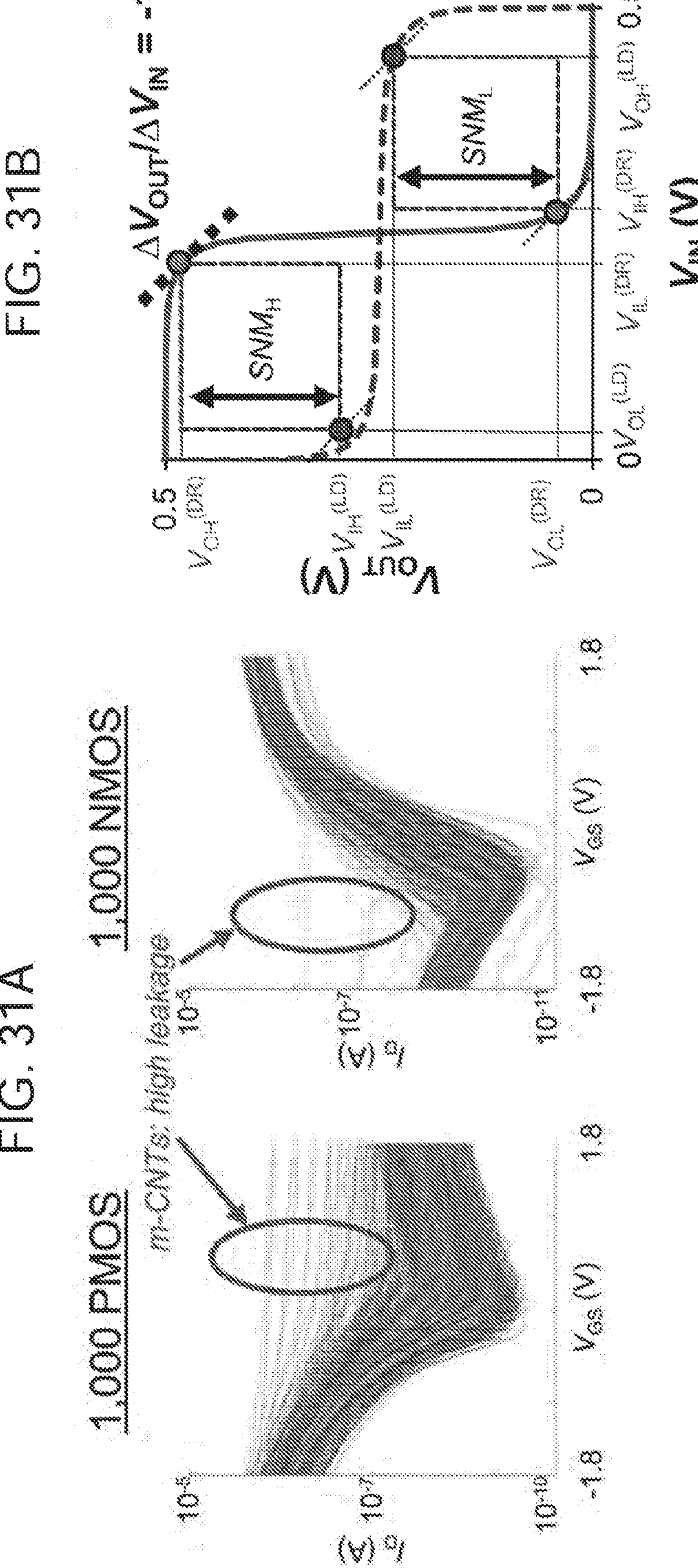


FIG. 31A
1,000 PMOS
m-CNTs: high leakage
1,000 NMOS
I_D (A)
10^-5
10^-7
10^-10
10^-11
-1.8
1.8
V_GS (V)
FIG. 31B
ΔV_OUT/ΔV_IN = -1
SNM_H
SNM_L
V_OUT (V)
0.5
V_OH^(DR)
V_IH^(LD)
V_IL^(LD)
V_OL^(DR)
0
V_OL^(LD)
V_IL^(DR)
V_IH^(DR)
V_OH^(LD)
V_IN (V)

FIG. 31E

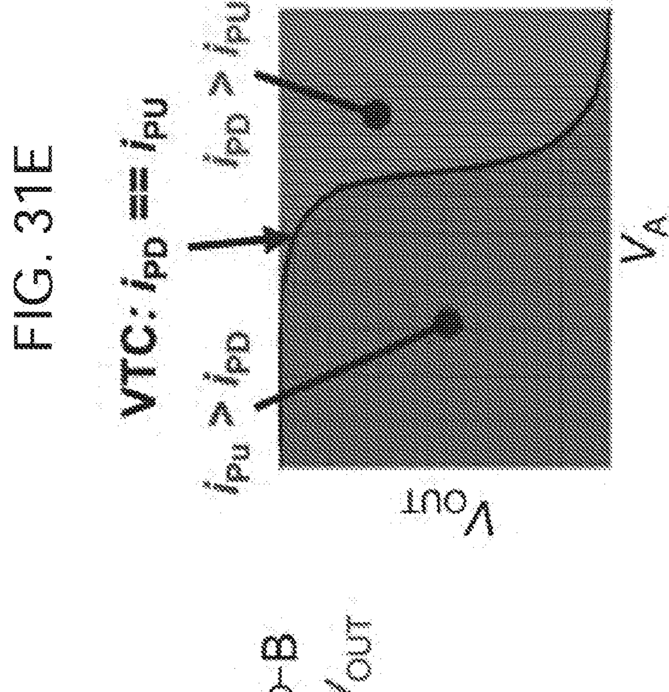


FIG. 31D

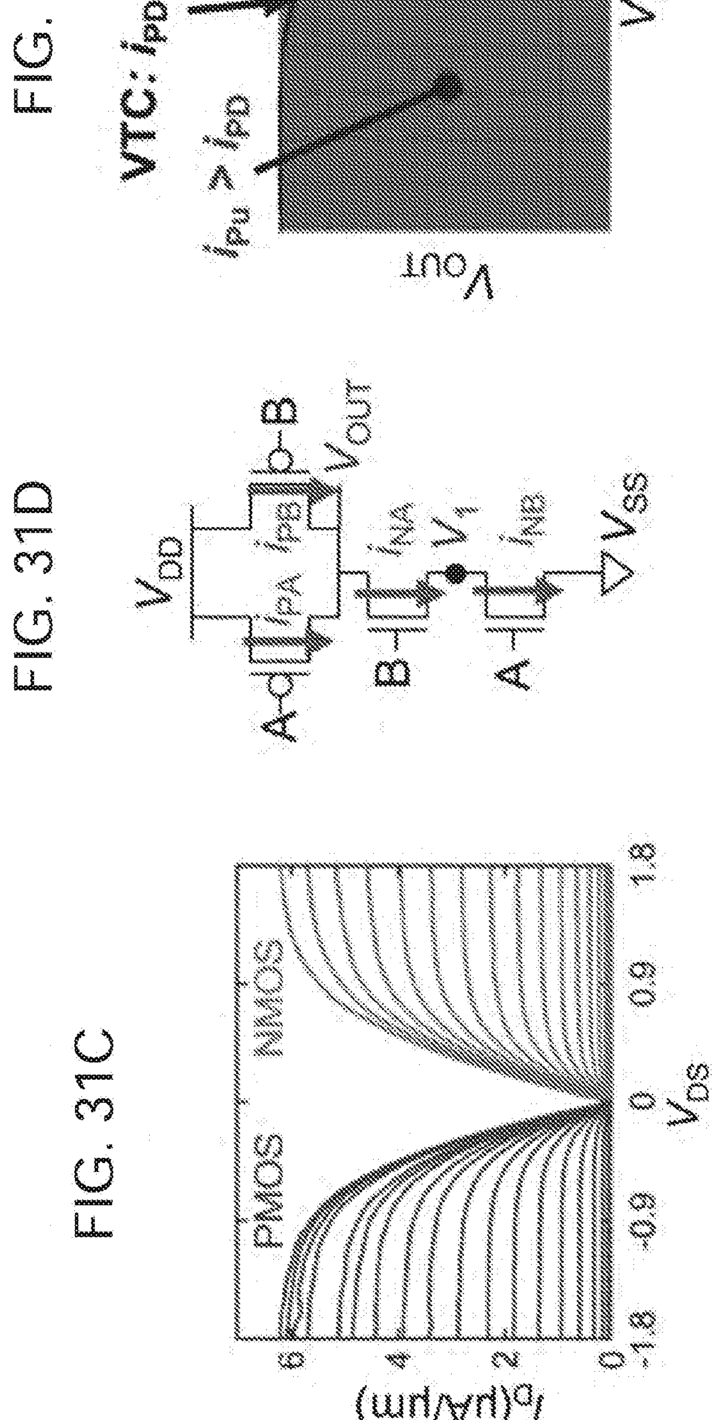


FIG. 31C

FIG. 32A

nand2
nor2
layers
gate
local interconnect
active region
via "V0"
metal "M1"
s-CNTs
m-CNTs
CNFET active regions aligned

FIG. 32B

D flip-flop

FIG. 32C

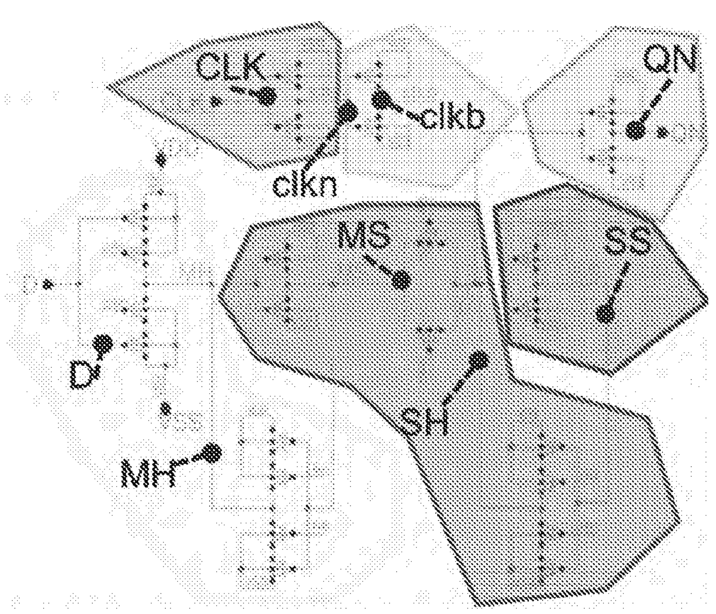


FIG. 32D

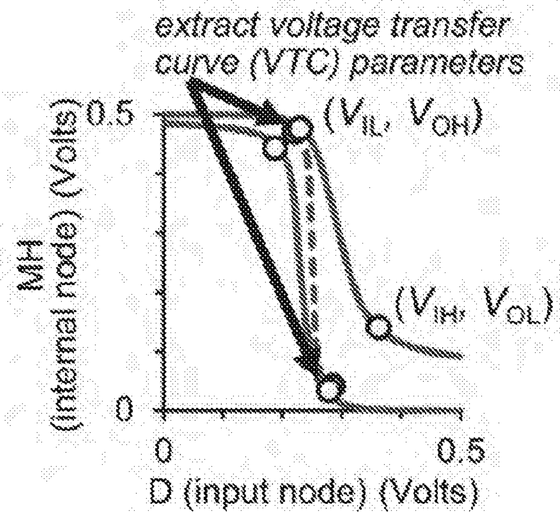
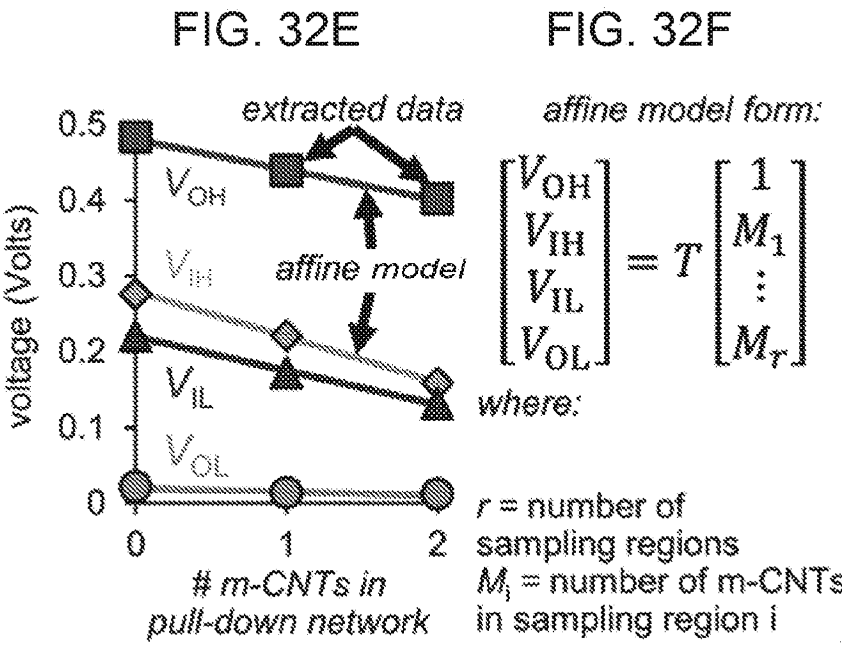


FIG. 32E FIG. 32F



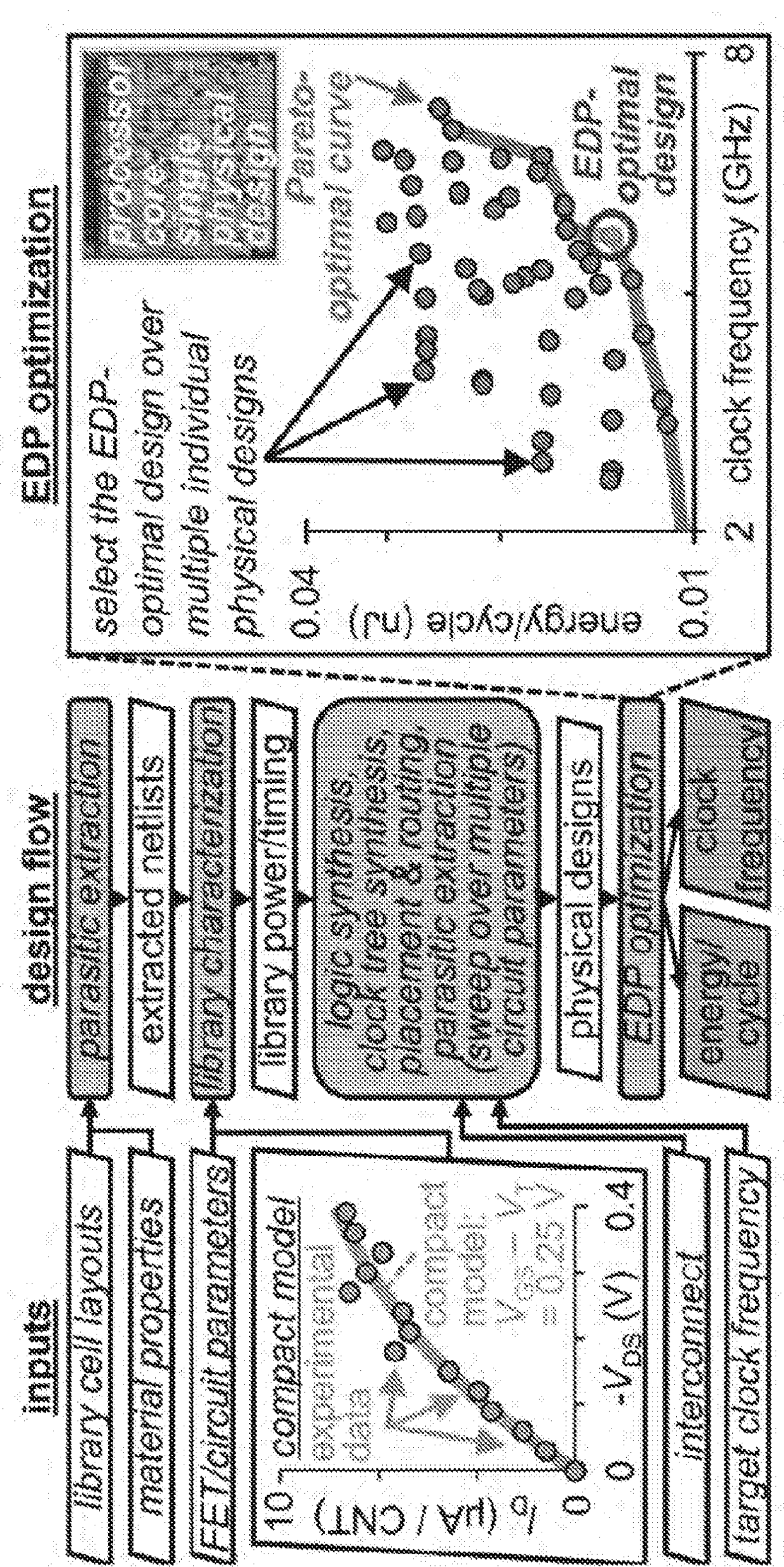


FIG. 32G

FIG. 32H

standard cells: row 1

standard cells: row 2

U3 U4 U5 U6

P3.1 P4.1 P4.2 P5.1 N3.1 N4.1 N4.2 N5.1 N6.1 P6.1

region with aligned CNTs	Variable number of s-CNTs	Variable number of m-CNTs
region 1	S1	M1
region 2	S2	M2
region 3	S3	M3
region 4	S4	M4
region 5	S5	M5
region 6	S6	M6
region 7	S7	M7
region 8	S8	M8
region 9	S9	M9
region 10	S10	M10
region 11	S11	M11
region 12	S12	M12

FIG. 32I

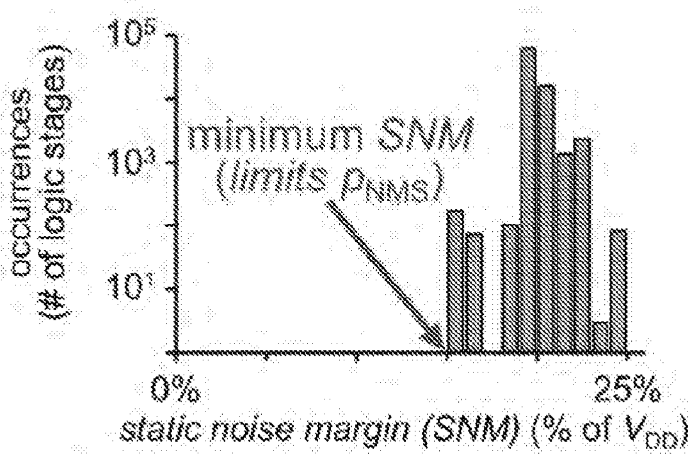


FIG. 32J

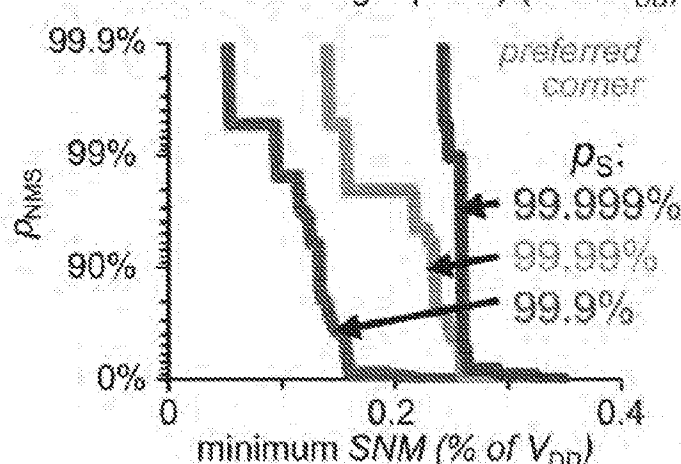


FIG. 32K

parameter	value
technology node	"7 nm"
contacted gate pitch	54 nm
gate, contact length	9 nm, 9 nm
contact resistance	3.3 kΩ/CNT
equivalent oxide thickness (EOT)	0.7 nm
CNT pitch, diameter	2 nm, 1.7 nm
m-CNT resistance	40 kΩ
I_{OFF} target	100 nA/μm

FIG. 33

inst	category	summary	assembly
addi	register-immediate arithmetic	add constant, no overflow exception	addi rd, rs1, imm
add	register-register arithmetic	addition with 3 GPRs, no overflow exception	add rd, rs1, rs2
andi	register-immediate arithmetic	bitwise AND with constant	andi rd, rs1, imm
and	register-register arithmetic	bitwise AND with 3 GPRs	and rd, rs1, rs2
auipc	register-immediate arithmetic	load (pc + constant) into GPR	auipc rd, imm
beq	conditional branch	branch if 2 GPRs are equal	beq rs1, rs2, imm
bgeu	conditional branch	branch based on unsigned comparison of 2 GPRs	bgeu rs1, rs2, imm
bltu	conditional branch	branch based on unsigned comparison of 2 GPRs	bltu rs1, rs2, imm
bge	conditional branch	branch based on signed comparison of 2 GPRs	bge rs1, rs2, imm
blt	conditional branch	branch based on signed comparison of 2 GPRs	blt rs1, rs2, imm
bne	conditional branch	branch if 2 GPRs are not equal	bne rs1, rs2, imm
jalr	unconditional jump	jump to relative address, place return address in GPR	jalr rd, rs1, imm
jal	unconditional jump	jump to address, place return address in GPR	jal rd, imm
lh	memory instruction	load short from memory into GPR	lh rd, imm(rs1)
lui	register-immediate arithmetic	load upper bits of constant into GPR	lui rd, imm
ori	register-immediate arithmetic	bitwise OR with constant	ori rd, rs1, imm
or	register-register arithmetic	bitwise OR with 3 GPRs	or rd, rs1, rs2
sh	memory instruction	store short into memory	sh rs2, imm(rs1)
slli	register-immediate arithmetic	shift left logical by constant	slli rd, rs1, imm
sll	register-register arithmetic	shift left logical by GPR value	sll rd, rs1, rs2
sltiu	register-immediate arithmetic	set GPR based on unsigned comparison of GPR and constant	sltiu rd, rs1, imm
slti	register-immediate arithmetic	set GPR based on signed comparison of GPR and constant	slti rd, rs1, imm
sltu	register-register arithmetic	set GPR based on unsigned comparison of 2 GPRs	sltu rd, rs1, rs2
slt	register-register arithmetic	set GPR based on signed comparison of 2 GPRs	slt rd, rs1, rs2
srai	register-immediate arithmetic	shift right arithmetic by constant	srai rd, rs1, imm
sra	register-register arithmetic	shift right arithmetic by GPR value	sra rd, rs1, rs2
srli	register-immediate arithmetic	shift right logical by constant	srli rd, rs1, imm
srl	register-register arithmetic	shift right logical by GPR value	srl rd, rs1, rs2
sub	register-register arithmetic	subtraction with 3 GPRs, no overflow exception	sub rd, rs1, rs2
xori	register-immediate arithmetic	bitwise XOR with constant	xori rd, rs1, rs2
xor	register-register arithmetic	bitwise XOR with 3 GPRs	xor rd, rs1, rs2
inst	format instruction (type format		

	~imm)	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
addi	I-I	imm[11:0]												~~rs1[4:2]~~			rs1		funct3=ADD			~~rd[4:2]~~			rd		opcode=OPIMM						
add	R	0	0	0	0	0	0	0	~~rs2[4:2]~~			rs2		~~rs1[4:2]~~			rs1		funct3=ADD			~~rd[4:2]~~			rd		opcode=OP						
andi	I-I	imm[11:0]												~~rs1[4:2]~~			rs1		funct3=AND			~~rd[4:2]~~			rd		opcode=OPIMM						
and	R	0	0	0	0	0	0	0	~~rs2[4:2]~~			rs2		~~rs1[4:2]~~			rs1		funct3=AND			~~rd[4:2]~~			rd		opcode=OP						
auipc	I-U	~~imm[31:16]~~																imm[15:12]				~~rd[4:2]~~			rd		opcode=AUIPC						
beq	S-B		imm[10:5]						~~rs2[4:2]~~			rs2		~~rs1[4:2]~~			rs1		funct3=BEQ			imm[4:1]					opcode=BRANCH						
bgeu	S-B		imm[10:5]						~~rs2[4:2]~~			rs2		~~rs1[4:2]~~			rs1		funct3=BGEU			imm[4:1]					opcode=BRANCH						
bltu	S-B		imm[10:5]						~~rs2[4:2]~~			rs2		~~rs1[4:2]~~			rs1		funct3=BLTU			imm[4:1]					opcode=BRANCH						
bge	S-B		imm[10:5]						~~rs2[4:2]~~			rs2		~~rs1[4:2]~~			rs1		funct3=BGE			imm[4:1]					opcode=BRANCH						
blt	S-B		imm[10:5]						~~rs2[4:2]~~			rs2		~~rs1[4:2]~~			rs1		funct3=BLT			imm[4:1]					opcode=BRANCH						
bne	S-B		imm[10:5]						~~rs2[4:2]~~			rs2		~~rs1[4:2]~~			rs1		funct3=BNE			imm[4:1]					opcode=BRANCH						
jalr	I-I	imm[11:0]												~~rs1[4:2]~~			rs1		0	0	0	~~rd[4:2]~~			rd		opcode=JALR						
jal	U-J		imm[10:1]											~~imm[20:16]~~				imm[15:12]				~~rd[4:2]~~			rd		opcode=JAL						
lh	I-I	imm[11:0]												~~rs1[4:2]~~			rs1		funct3=LH			~~rd[4:2]~~			rd		opcode=LOAD						
lui	I-U	~~imm[31:16]~~																imm[15:12]				~~rd[4:2]~~			rd		opcode=LUI						
ori	I-I	imm[11:0]												~~rs1[4:2]~~			rs1		funct3=OR			~~rd[4:2]~~			rd		opcode=OPIMM						
or	R	0	0	0	0	0	0	0	~~rs2[4:2]~~			rs2		~~rs1[4:2]~~			rs1		funct3=OR			~~rd[4:2]~~			rd		opcode=OP						
sh	S-S	imm[11:5]							~~rs2[4:2]~~			rs2		~~rs1[4:2]~~			rs1		funct3=SH			imm[4:0]					opcode=STORE						
slli	I-I	0	0	0	0	0	0	0		imm[3:0]				~~rs1[4:2]~~			rs1		funct3=SLL			~~rd[4:2]~~			rd		opcode=OPIMM						
sll	R	0	0	0	0	0	0	0	~~rs2[4:2]~~			rs2		~~rs1[4:2]~~			rs1		funct3=SLL			~~rd[4:2]~~			rd		opcode=OP						
sltiu	I-I	imm[11:0]												~~rs1[4:2]~~			rs1		funct3=SLTU			~~rd[4:2]~~			rd		opcode=OPIMM						
slti	I-I	imm[11:0]												~~rs1[4:2]~~			rs1		funct3=SLT			~~rd[4:2]~~			rd		opcode=OPIMM						
sltu	R	0	0	0	0	0	0	0	~~rs2[4:2]~~			rs2		~~rs1[4:2]~~			rs1		funct3=SLTU			~~rd[4:2]~~			rd		opcode=OP						
slt	R	0	0	0	0	0	0	0	~~rs2[4:2]~~			rs2		~~rs1[4:2]~~			rs1		funct3=SLT			~~rd[4:2]~~			rd		opcode=OP						
srai	I-I	0	1	0	0	0	0	0		imm[3:0]				~~rs1[4:2]~~			rs1		funct3=SR			~~rd[4:2]~~			rd		opcode=OPIMM						
sra	R	0	1	0	0	0	0	0	~~rs2[4:2]~~			rs2		~~rs1[4:2]~~			rs1		funct3=SR			~~rd[4:2]~~			rd		opcode=OP						
srli	I-I	0	0	0	0	0	0	0		imm[3:0]				~~rs1[4:2]~~			rs1		funct3=SR			~~rd[4:2]~~			rd		opcode=OPIMM						
srl	R	0	0	0	0	0	0	0	~~rs2[4:2]~~			rs2		~~rs1[4:2]~~			rs1		funct3=SR			~~rd[4:2]~~			rd		opcode=OP						
sub	R	0	1	0	0	0	0	0	~~rs2[4:2]~~			rs2		~~rs1[4:2]~~			rs1		funct3=ADD			~~rd[4:2]~~			rd		opcode=OP						
xori	I-I	imm[11:0]												~~rs1[4:2]~~			rs1		funct3=XOR			~~rd[4:2]~~			rd		opcode=OPIMM						
xor	R	0	0	0	0	0	0	0	~~rs2[4:2]~~			rs2		~~rs1[4:2]~~			rs1		funct3=XOR			~~rd[4:2]~~			rd		opcode=OP						

FIG. 33-contd.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 19/63932

A. CLASSIFICATION OF SUBJECT MATTER
IPC - G01N 27/12; G01N 27/414; G01N 33/543 (2020.01)

CPC - G01N 27/124; G01N 27/414; B82Y 15/00; C07K 14/705

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011/0147715 A1 (ROGERS et al), 23 June 2011 (23..06.2011), figutre 8; para [0013], [0015], [0083], [0088].	24
A	US 2004/0099438 A1 (ARTHUR et al), 27 May 2004 (24.05.2004), figures 1-3; para [0015], [0027]-[0028], [0032], [0043]-[0044].	1-23
A	LI et al, 'Facile method for enhancing conductivity of printed carbon nanotubes electrode via simple rinsing process', Organic Electronics, volume 47, 09 May 2017 (09.05.2017), pg 174-180.	1-16
A	US 2006/0204427 A1 (GHENCIU et al), 14 September 2006 (14.09.2006), para [0034], [0059], [0061].	1-16
A	GEIER et al, 'Solution-processed carbon nanotube thin-film complementary static random access memory', Nature Nanotechnology, volume 10, 07 September 2015 (07.09.2015), pg 944-949.	17-23
A	US 2012/0129273 A1 (JOHNSON, JR et al), 24 May 2012 (24.05.2012), figure 4; para [0005], [0020]-[0021], [0046].	17
X, P	HILLS et al, 'Modern microprocessor built from complementary carbon nanotube transistors', Nature, volume 572, 28 August 2019 (28.08.2019), pg 595-602.	1-23
A	US 2016/0133843 A1 (THE BOARD OF TRUSTEES OF THE UNIVERSITY OF ILLINOIS et al), 12 May 2016 (12.05.2016), entire document.	1-23

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 January 2020	19 FEB 2020
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