United States Patent

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[54] **DATA BUS TRANSFER SYSTEM**
9 Claims, 10 Drawing Figs.

[52] **U.S. Cl.** **307/259,** 307/224, 307/241
[51] **Int. Cl.** **H03k 17/74**
[50] **Field of Search** ..... 307/221, 224, 241—4, 256, 259

[56] **References Cited**
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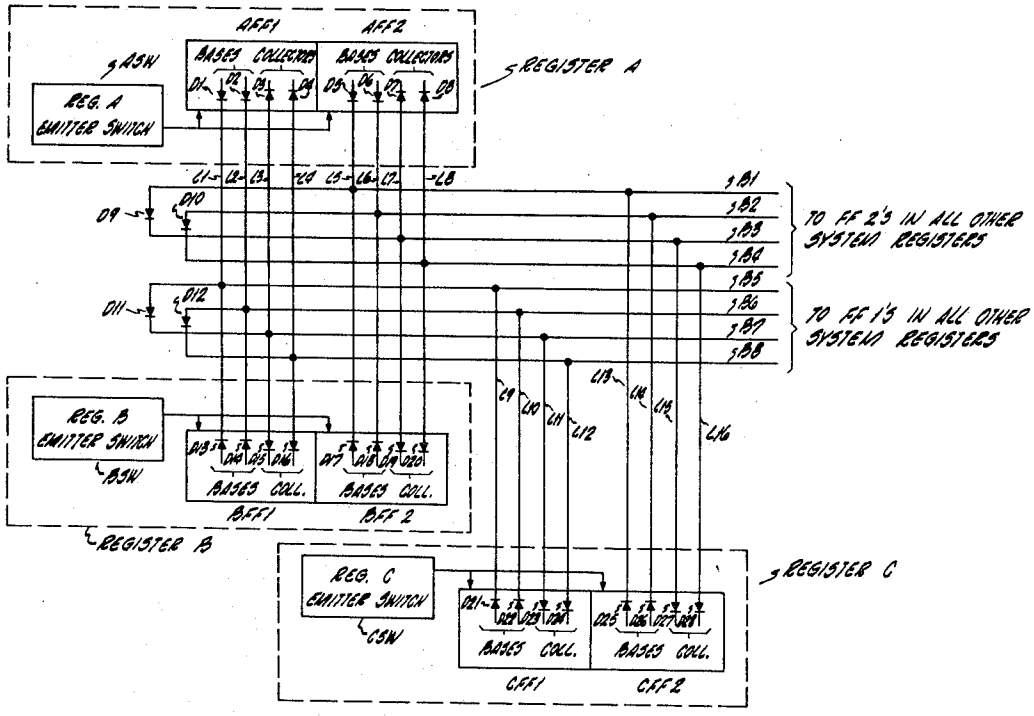
ABSTRACT: The transfer of information in digital form over data busses from one register to another is completed through multiple diode connections between the registers. Switches in the registers are used to change the bias applied via flip-flop circuits to the diodes connected between the registers thereby causing the diodes to become conductive and transfer data from flip-flops in one register to flip-flops in a second register.



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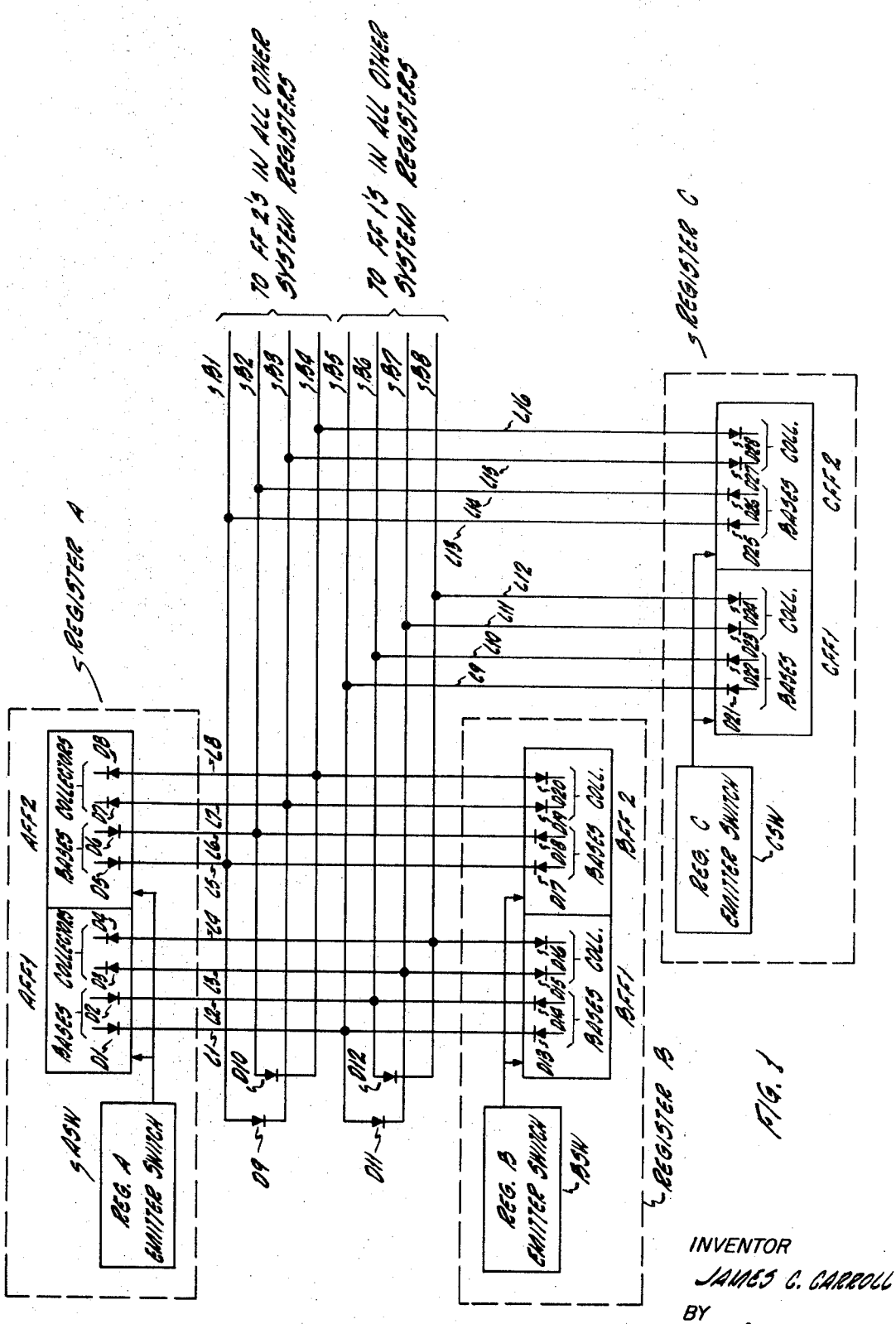

FIG. 1

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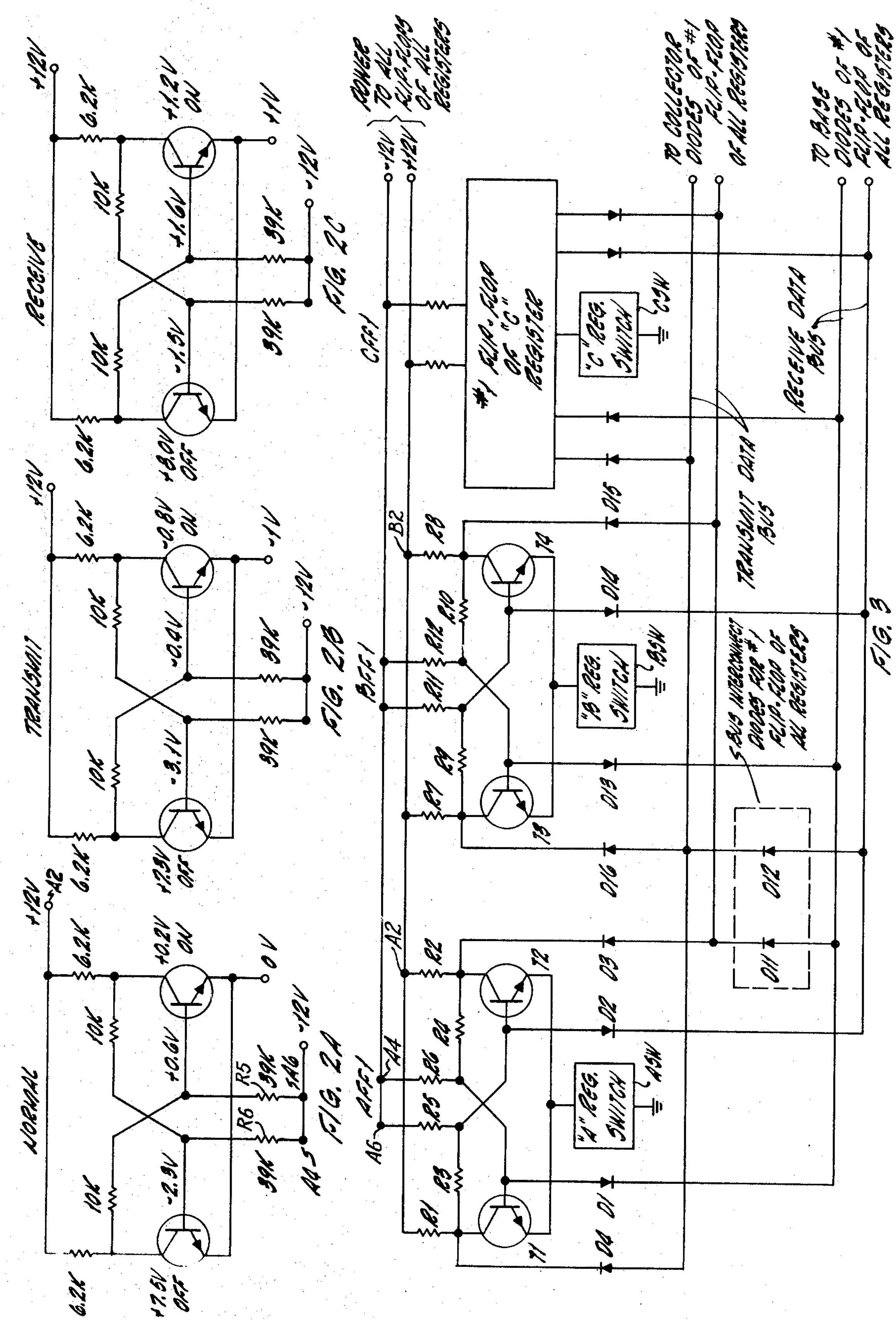
NORMAL
TRANSMIT
RECEIVE
FIG. 2A
FIG. 2B
FIG. 2C
POWER TO ALL FLIP-FLOPS OF ALL REGISTERS
TO COLLECTOR DIODES OF #1 FLIP-FLOP OF ALL REGISTERS
TO BASE DIODES OF #1 FLIP-FLOP OF ALL REGISTERS
#1 FLIP-FLOP OF "C" REGISTER
"C" REG. SWITCH
"B" REG. SWITCH
"A" REG. SWITCH
RECEIVE DATA BUS
TRANSMIT DATA BUS
BUS INTERCONNECT DIODES FOR #1 FLIP-FLOP OF ALL REGISTERS
FIG. 3

CASE	T1	T2	T3	T4	ASSY	T1Vc	T2V3	VDA	T2Vc	T3V3	VDE	T3Vc	T2V2	VDC	T3Vc	T3V3	VDD	XFER
1	OFF	ON	ON	OFF	NMC	+7.6	-2.3	-9.9	+0.2	+0.6	+0.4	+0.2	+0.6	+0.4	+2.6	-2.3	-9.9	NO
2					XMIT	+7.3	-2.3	-9.6	-0.8	+0.6	+1.4	+0.2	+0.4	-0.6	+2.6	-3.1	-10.7	NO
3					REC	+8.0	-2.3	-10.3	+1.2	+0.6	-0.6	+0.2	+1.6	+1.4	+2.6	-1.5	-9.1	NO
4					NMC	+7.6	-3.1	-10.7	+0.2	-0.4	-0.6	-0.8	+0.6	+1.4	+2.9	-2.3	-9.6	NO
5					XMIT	+7.3	-3.1	-10.4	-0.8	-0.4	+0.4	-0.8	-0.4	+1.4	+2.3	-3.1	-10.4	NO
6					REC	+8.0	-3.1	-11.1	+1.2	-0.4	-1.6	-0.8	+1.6	+2.4	+2.3	-1.5	-8.8	B→A
7					NMC	+7.6	-1.5	-9.1	+0.2	+1.6	+2.4	+1.2	+0.6	-0.6	+2.9	-2.3	-10.3	NO
8					XMIT	+7.3	-1.5	-8.8	-0.8	+1.6	+2.1	+1.2	-0.4	-1.6	+2.0	-3.1	-11.1	A→B
9					REC	+8.0	-1.5	-9.5	+1.2	+1.6	+2.4	+1.2	+1.6	+1.4	+2.0	-1.5	-9.5	NO
10				ON	NMC	+7.6	+0.6	-7.0	+0.2	-2.3	-2.5	+2.6	+0.6	-7.0	+0.2	-2.3	-2.5	NO
11			OFF		XMIT	+7.3	+0.6	-6.7	-0.8	-2.3	-1.5	+2.6	-0.4	-7.2	+0.2	-3.1	-3.3	NO
12					REC	+8.0	+0.6	-7.4	+1.2	-2.3	-4.5	+2.6	+1.6	-6.0	+0.2	-1.5	-1.7	NO
13					NMC	+7.6	-0.4	-8.0	+0.2	-3.1	-3.9	+2.3	+0.6	-6.7	-0.8	-2.3	-1.5	NO
14					XMIT	+7.3	-0.4	-7.7	-0.8	-3.1	-2.9	+2.3	-0.4	-7.7	-0.8	-3.1	-2.3	NO
15					REC	+8.0	-0.4	-8.4	+1.2	-3.1	-4.8	+2.3	+1.6	-5.7	-0.8	-1.5	-0.7	NO
16					NMC	+7.6	+1.6	-6.0	+0.2	-1.5	-1.7	+3.0	+0.6	-7.4	+1.2	-2.3	-3.5	NO
17					XMIT	+7.3	+1.6	-5.7	-0.8	-1.5	-0.7	+3.0	-0.4	-8.4	+1.2	-3.1	-4.8	NO
18					REC	+8.0	+1.6	-7.4	+1.2	-1.5	-2.7	+3.0	+1.6	-6.4	+1.2	-1.5	-2.7	NO

VDA = VOLTAGE ACROSS DIODE STRING BETWEEN T1 COLLECTOR AND T4 BASE, I.E. D4, D12 & D16
VDB = " " " " " " T2 " " T3 " " D3, D11 & D13
VDC = " " " " " " T3 " " T2 " " D16, D12 & D2
VDD = " " " " " " T4 " " T1 " " D15, D11 & D1

MINUS (-) SIGN INDICATES REVERSE BIAS; PLUS (+) SIGN INDICATES FORWARD BIAS; A FORWARD BIAS IN EXCESS OF 1.8V WILL EFFECT A TRANSFER, I.E. CAUSE THE RECEIVING ELEMENT TO ASSUME WITH THE TRANSMITTING ONE.

FIG. 4

THREE FLIP-FLOPS EACH FORMED BY CROSS-CONNECTING TWO DTL SINGLE INPUT INVERTERS
TO BASE DIODES OF NO. 1 FLIP-FLOP OF ALL REGISTERS
TO COLLECTOR DIODES OF NO. 1 FLIP-FLOP OF ALL REGISTERS
CAF1
BAF1
AAF1
EFF1
EBF1
OAF1
FIG. 5
TYPICAL WAVEFORM AT (A)
+1V
0V
-1V
NORMAL
TRANSMIT
NORMAL
RECEIVE
NORMAL
FIG. 6B
+6V
+5V
+4V
CORRESPONDING WAVEFORM AT (B)
REGISTER "A"
PULSE TRANSFORMER WITH CENTER TAPPED PRIMARY AND BIFILAR SECONDARY
(B)
(A)
+5V VCC
+VCC
TRANSMIT
RECEIVE
FIG. 6A

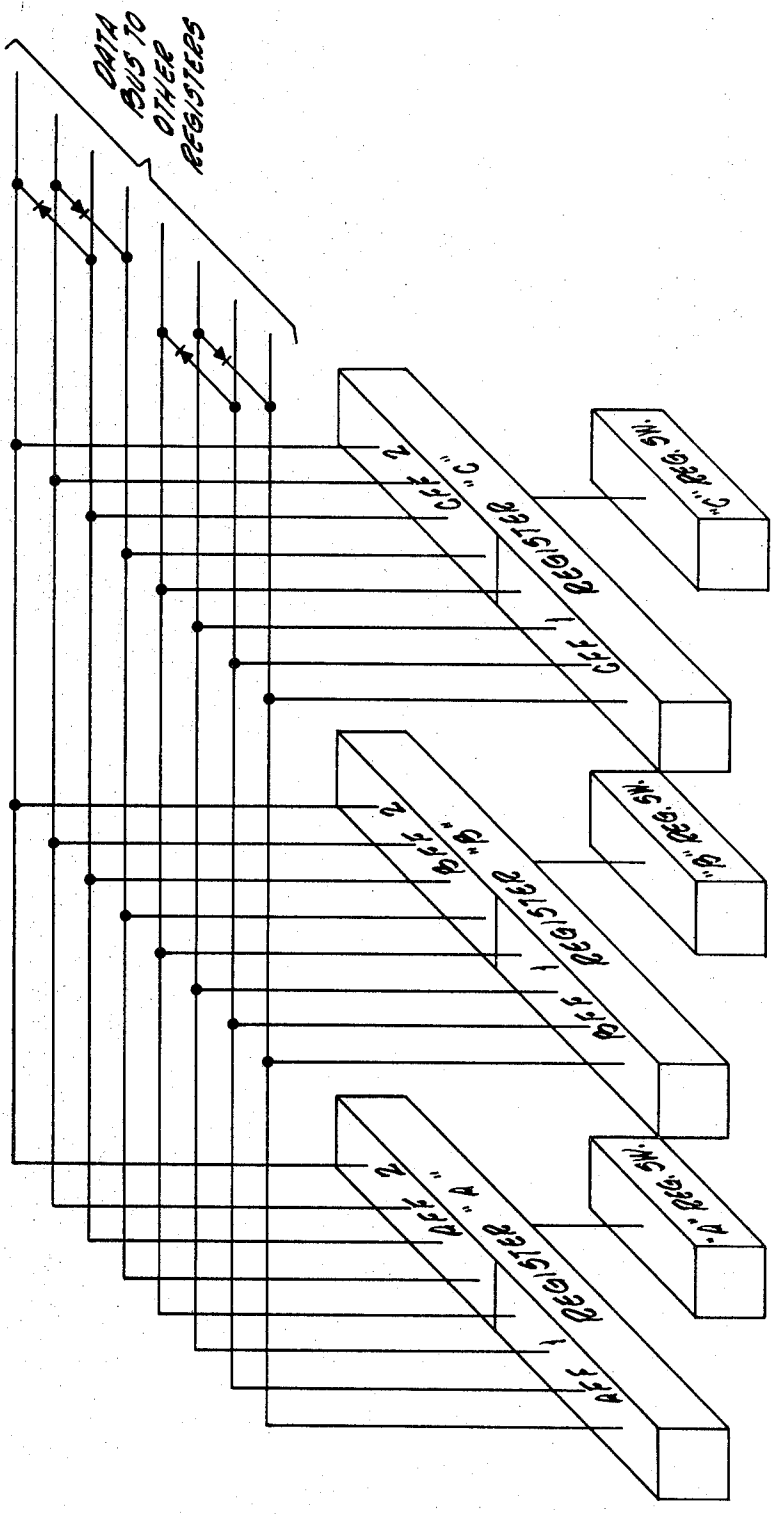
DATA BUS TO OTHER REGISTERS
REGISTER "A" FF 1
FF 2
REG. "A"
REGISTER "B" FF 1
FF 2
REG. "B"
REGISTER "C" FF 1
FF 2
REG. "C"

FIG. 1

DATA BUS TRANSFER SYSTEM

The present invention relates to the transfer of data from one register to another over data busses and data bus gates.

The prior art devices which appear to be most closely related to the present invention require the use of elaborate gating devices to enable the transfer of information over data busses from one register to another. These prior art devices therefore require a large amount of support equipment and are generally economical only with very large data processing systems.

It is a primary object of this invention to provide improved and more economical means for setting one register from another over interconnecting data busses. The following description provides an explanation of the nature and operation of an embodiment of this invention in which:

FIG. 1 illustrates, in a block diagram, a data transfer system according to the present invention,

FIGS. 2A, 2B and 2C illustrate the operation of a basic bistable multivibrator or flip-flop in three different modes and show specific collector, base, and emitter biases for each mode,

FIG. 3 shows the use of single flip-flop circuits from FIGS. 2A—2C in a data transfer system utilizing several registers. Though only one flip-flop position is shown in the figure, as many positions as required per register would be similarly equipped with flip-flops, steering diodes and bus interconnecting diodes,

FIG. 4 includes a tabulation of the system voltages when a flip-flop, such as is shown in FIGS. 2A—2C, is incorporated in the transfer system of FIG. 3 and exposed to all combinations of the three register operating modes, i.e. normal, transmit and receive modes,

FIG. 5 depicts how integrated circuit logic elements, connected to function as reset-set flip-flops, can be utilized as active elements in the data transfer system. Here the 01 flip-flops of six registers are shown in block diagram form, while the steering and bus interconnecting diodes, external to the IC package are shown in schematic form,

FIG. 6A shows how the IC registers of FIG. 5 are switched into the transmit or receive mode as required by system operation. The operation differs from that depicted in FIG. 2 in that both the ground and the +Vcc busses to the register in question are raised or lowered by one volt with respect to normal bus voltages to effect receiving or transmitting. This leaves the +Vcc bus to "ground" bus voltage in the register proper constant regardless of operating mode. FIG. 6B illustrates waveforms related to FIG. 6A, and

FIG. 7 presents a three dimensional representation of a system using at least three registers of two flip-flops each. Data bus interconnecting diodes are shown while the flip-flop input and output steering diodes are shown as part of the flip-flops themselves.

Turning first to the diagram in FIG. 1, registers A, B and C are indicated by dashed blocks with input-output interfaces represented by flip-flops in blocks AFF1, AFF2, BFF1, BFF2, CFF1 and CFF2. The registers are interconnected through the diodes D1, D2...D28, and over the lines L1, L2...L16 and the busses B1, B2...B8. Due to the existence of these interconnections it is possible to transfer information from one register to another. Transfer is effected by increasing the bias potential across three normally nonconductive diodes in series, to enable them to conduct and transfer data from one register to another.

As an example of the transfer of a single bit of information between registers in the system illustrated in FIG. 1, consider the effect of an appropriate change in bias applied by a register emitter switch ASW to the emitters (FIG. 2A) of a flip-flop AFF1 at the same time that another appropriate bias change is applied from a register emitter switch BSW to the emitters of flip-flop BFF1. Assuming that the flip-flops are operating in suitable transmit and receive modes, a change will occur in the bias on diodes D1 and D2 at the same time that appropriate changes occur in the bias on diodes D15 and D16. These changes in bias so effect the connections, as shown in FIG. 1, over D1–L1–B5–D11–L3–D15 and/or over D2–L2–B6–D12–L4–D16 that data represented by the conductive state of BFF1 will be transferred to the bases indicated in block AFF1. In a similar way, signals can be transferred between any of these registers over the indicated lines, diodes and busses to other registers, including other registers connected to the busses but not expressly illustrated.

In order to establish the precise conditions needed for operation of embodiments of the present invention, an unusual number of details concerning specific operating voltages and other circuit conditions are shown in FIGS. 2A, 2B and 2C. It will be clear from this figure that in an operating embodiment of the invention there are three possible operating modes for each register determined by the voltage on the emitter bus common to all flip-flops in the register in question. These states, as shown respectively in FIGS. 2A, 2B and 2C are normal, transmit and receive. The normal state occurs when the emitter bus is at ground potential OV and the register can neither transmit its contents to or receive the contents from any other register on the data bus. The transmit state exists when the emitter bus is at a −1V potential with respect to ground and the register can nondestructively transmit its contents to one or more registers operating in the receive mode via the data bus. The receive state is present when the emitter bus is at a +1V potential with respect to ground and the register will be set to agree with the transmitting register through the data bus. If only one of the registers on the bus is operating in a transmit or receive mode and all remaining registers on the bus are in the normal mode, no transfer of data will occur in any direction.

A brief tabulation of the potentials applied to respective elements of a transistorized flip-flop to provide normal, transmit and receive modes of operation is presented below, where the voltages referred to are all with respect to ground:

	Collector		Base		Emitter, On/Off
	On	Off	On	Off	
Mode:					
Normal	+0.2	+7.5	+0.6	−2.3	0.0
Transmit	−0.8	+7.3	−0.4	−3.1	−1.0
Receive	+1.2	+8.0	+1.6	−1.5	+1.0

Further details concerning the nature of the present invention may be gleaned from a more detailed review of the interconnections and operations of exemplary flip-flops AFF1 and BFF1 as illustrated in FIG. 3. The labels in FIG. 3 are repeated from FIG. 1 to the extent the same circuits and circuit elements are illustrated in both Figures.

In FIG. 3 the flip-flops AFF1 and BFF1 are shown to include transistors which have been labeled T1, T2, T3 and T4. Pairs of these transistors, i.e. T1 paired with T2 and T3 paired with T4 serve as the dynamic elements of the flip-flop circuits and are set in their normal condition (see FIG. 2A) initially either by signals from circuits (not shown) in their respective registers or by transferred signals originating from one of the other registers.

Assume that the flip-flops AFF1 and BFF1 in FIG. 3 are biased so that they are in the normal state indicated in FIG. 2A. Under these circumstances, the particular bias conditions shown prevail on the respective emitter circuits until a demand is placed on the respective registers for a transfer of information. Once the computer circuits (not shown) determine that the transfer of information should be made from one register to another, the settings of appropriate switches ASW and BSW are changed to alter the potentials on the emitters of AFF1 and BFF1 thereby setting these flip-flops respectively in transmit and receive modes and causing conduction through selected diodes over connecting lines between AFF1 and BFF1.

The operation of the emitter switches ASW and BSW is important to an understanding of this invention. Each of these switches is arranged to connect all of the emitters of the

transistors of the flip-flops in the associated register to ground, as indicated by zero on the emitters of FIG. 2A, or to connect them to +1 or −1 potentials, as indicated in FIGS. 2B and 2C. The effect of lowering the emitter potentials of transistors in flip-flop AFF1 of Register A by one volt (placing it in the transmit mode) and raising the emitter potentials of transistors in BFF1 of Register B by 1 volt (placing it in the receive mode) is to initiate the transfer of information (one or zero) from AFF1 to BFF1. Bias on the interconnecting diodes at this time is such that current can flow through three diodes in series between AFF1 and BFF1.

For purposes of further explanation assume first a particular set of conditions for the circuits of FIG. 3. Assume that AFF1 and BFF1 are each in the condition representing the Normal state as defined in FIG. 2A. Assume further that AFF1 is in a condition representing its "one" state and that BFF1 is in a condition representing a "zero" state. Assume further that in the "one" state of AFF1 the transistor T2 is "on" and that in the "zero" state of BFF1 the transistor T3 is "on" (see the first line of FIG. 4). Transistors T1 and T4 are "off" at this time.

Under the circumstances referred to above, with exemplary transistors, the bases of T2 and T3 must be +0.6 volts relative to the emitters to remain "on." With T2 and T3 each conducting and with biases of +12 volts at terminals A2 and −12 volts at terminals A4 and A6 the effective potentials on their collectors are each +0.2 volts.

Assuming the conditions referred to in the foregoing paragraphs, in order to transfer information in Register A to Register B the registers must be set in Transmit and Receive states respectively. To set the registers, the switch BSW is operated to raise the potential on the emitters in Register B to +1 volt and, at the same time the corresponding switch ASW lowers the voltage applied to the emitters in Register A from ground to −1 volt. With a decrease in its emitter voltage to −1 volt, the potential on the collector of T2 will also drop 1 volt to a new value of −0.8 volts (line 8 of FIG. 4). An increase of +1 volt in the emitter voltage of T3 at the same time will cause the base potential of T3 to rise by one volt to a new value of +1.6 volts. The difference between these two potentials (of 2.4 volts) is applied over diodes D3, D11 and D13 causing them to conduct. The diodes conduct with a potential drop of 0.6 volt each or a total of 1.8 volts when they are in series. The collector of T2 serves under these circumstances as a current sink to pull down the potential on base T3 to a value limited by the initial potential on the collector of − 0.8 volt plus the +1.8 volts drop across the diodes or one (+1) volt. This causes T3 to turn "off." When T3 turns "off" T4 turns "on" and the conversion of BFF1 to the "one" state of AFF1 is completed.

The flip-flop schematics and power supply voltages shown in FIGS. 1, 2A, 2B, 2C and 3 are typical and are only used to facilitate circuit descriptions. This data transfer technique has been applied to RTL, DTL, and TTL integrated circuits, as shown in FIG. 5, with excellent results. Both "ready-made" flip-flops of the JK and D configurations have been used as well as flip-flops made by cross connecting standard gate functions. In these applications, external steering diodes must be provided when they are not part of the IC proper. When IC's are used, transfer is effected by simultaneously raising or lowering both the positive and negative power supply busses of the register in question by the use of a pulse transformer with a bifilar secondary as shown in FIG. 6A, rather than by just varying the emitter bus voltage as is done in FIG. 2. This technique has also been applied to flip-flops of the type shown in FIGS. 2A, 2B and 2C when it is desirable to keep all bias voltages within the flip-flop proper constant regardless of the mode of the register. In this instance, a trifilar secondary would be used on the pulse transformer, and the −12V, +12V, and "ground" busses of the register would be powered through the three secondary windings.

In many digital systems, such as computers, the necessity to shift digital information one bit or one word to the right or to the left often comes up. Using the data transfer scheme presented here, data can be parallel transmitted to an intermediate register which in turn transmits the data back to the original register skewed as many bits as desired to the left or right. Even though two registers are required for this operation, the simplicity of each register is such that the combination is usually no more complex than a shift register required to implement the same operation. In addition, the intermediate register with the skewed output can communicate with any other register on the data bus and can shift that register's contents without the necessity of first transferring its contents to a specific register designated as a shift register, shifting the data, and then returning it to the original register. Binary complementation can be implemented in the same manner except the intermediate register outputs would be reversed on a per flip-flop basis such that parallel transfer from the original register to the intermediate register would occur and then the transfer back to the original register would be complemented by the output reversal.

While the principles of the invention have been described in connection with specific apparatus and applications, it is to be understood that this description is made only by way of example and not as a limitation on the scope of the invention.

I claim:

1. A data bus transfer system comprising
a data bus,
a plurality of registers,
each register including bistable switching means coupled via diodes to the data bus,
bias control switching means coupled to said bistable switching means to control the level of the voltage applied by said bistable means to the diodes,
said bistable switching means having three possible modes of operation determined by the level of the voltage applied by the bias control switching means to the bistable switching means, in which a first voltage level causes a normal mode in the bistable during which no conduction can occur in the diodes, a second voltage level causes a transmit mode in the bistable during which the bistable is able to transmit data to the diodes, and a third voltage level produces a receive mode in the bistable in which it is able to receive data over the diodes from registers in the transmit mode.

2. A data bus transfer system as claimed in claim 1, in which the data bus, the diodes and bistable switching means in each register are interconnected to permit transfer of data from a first register to at least one other register.

3. A data bus transfer system as claimed in claim 1, in which the bistable switching means are formed by flip-flop circuits in each register.

4. A data bus transfer system as claimed in claim 3, in which the bias control switching means includes register switches to introduce bias changes to the flip-flop circuits and thereby control the mode of operation of the flip-flop circuits forming the bistable switching means.

5. A data bus transfer system as claimed in claim 3, in which the bias control switching means controls the modes of operation of the bistable switching means, and
the bistable switching means, in response to the changes in the mode of operation, provide a change in biasing potential across the diodes to enable the transfer of information from one register to another.

6. A data bus transfer system as claimed in claim 1, in which the bistable switching means includes a flip-flop circuit in each register, and
means are provided, including the diodes and the data bus connected in series, for interconnecting electrodes of a flip-flop circuit of the first register and a flip-flop circuit of the second register.

7. A data bus transfer system as claimed in claim 1, in which at least three registers are included, and the diodes are interconnected to permit transfer of data from a first register to a second register and to the third register as required.

8. A data bus transfer system comprising:
a plurality of registers,

first switching means forming a part of each of the registers,

register switches forming a part of each of the registers,

the register switches serving to control the interconnection of the first switching means of a first register with the first switching means of a second register through switching elements and data busses,

the switching elements including serially connected diodes biased normally to a nonconductive state, and

means, including the register switches in the first and second registers, operable to change the operation of the

respective first switching means of the first and second registers to bias selective diodes to a conductive state and cause the diodes to transfer information over the data busses from the first register to the second register.

9. A data bus transfer system as claimed in claim 8, in which the data busses, the diodes and the register switches are interconnected to permit transfer of data from a first register to more than one other register.