

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
5 February 2009 (05.02.2009)

PCT

(10) International Publication Number
WO 2009/016497 A2

(51) International Patent Classification: Not classified

(74) Agent: REEVE, Anna, Elizabeth; Marks & Clerk, 90 Long Acre, London WC2E 9RA (GB).

(21) International Application Number:
PCT/IB2008/002032

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(22) International Filing Date: 1 August 2008 (01.08.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/832,519 1 August 2007 (01.08.2007) US

(71) Applicant (for all designated States except US): ADVANCED MICRO DEVICES, INC. [US/US]; One AMD Place, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

(71) Applicant (for BB only): ATI INTERNATIONAL SRL [BB/BB]; Heart Foundation Building, 3 Railway View, Jemmott's Lane, St Michael (BB).

(72) Inventors; and

(75) Inventors/Applicants (for US only): CHAN, Vincent [CA/CA]; 83 Sun Valley Drive, Richmond Hill, Ontario L4S 2G6 (CA). McLELLAN, Neil [US/CA]; 2 Rean Drive #2104, Toronto, Ontario M2K 3B8 (CA). O'NEIL, Kevin [CA/CA]; 30 Buntly Lane, Toronto, Ontario M2K 1W6 (CA).

Declaration under Rule 4.17:

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

Published:

— without international search report and to be republished upon receipt of that report

(54) Title: DIE STACKING APPARATUS AND METHOD

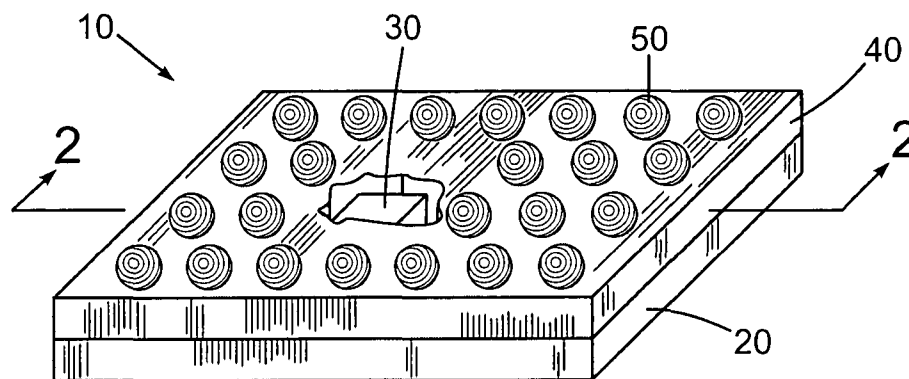


FIG. 1

(57) Abstract: Various stacked semiconductor devices and methods of making the same are provided. In one aspect, a method of manufacturing is provided that includes providing a first semiconductor die that has a first bulk semiconductor side and a first opposite side. A second semiconductor die is provided that has a second bulk semiconductor side and a second opposite side. The second opposite side of the second semiconductor die is coupled to the first opposite side of the first semiconductor die. Electrical connections are formed between the first semiconductor die and the second semiconductor die.

WO 2009/016497 A2

DIE STACKING APPARATUS AND METHOD

BACKGROUND OF THE INVENTION

1. Field of the Invention

5 [0001] This invention relates generally to semiconductor processing, and more particularly to semiconductor device mounting apparatus and methods.

2. Description of the Related Art

10 [0002] Conventional integrated circuits are frequently implemented on a semiconductor substrate or die that consists of a small rectangular piece of semiconductor material, typically silicon, fashioned with two opposing principal sides. The active circuitry for the die is concentrated near one of the two principal sides. The side housing the active circuitry is usually termed the "active circuitry side," while the side opposite the active circuitry side is often termed the "bulk silicon side." Depending on the thermal output of the die, it may be desirable to mount a heat transfer device, such as a heat sink, on the bulk silicon side of the die. This mounting may be directly on the bulk silicon side or on a lid that is positioned over the die.

15 [0003] A conventional die is usually mounted on some form of substrate, such as a package substrate or a printed circuit board. Electrical connectivity between the die and the underlying substrate or board is established through a variety of conventional mechanisms. In a so-called flip-chip configuration, the active circuitry side of the die is provided with a plurality of conductor balls or bumps that are designed to establish a metallurgical bond with a corresponding plurality of conductor pads positioned on the substrate or circuit board. The die is flipped over and seated with the active circuitry side facing downwards on the underlying substrate. A subsequent thermal process is performed to establish the requisite metallurgical bond between the bumps and the pads. One of the principal advantages of a flip-chip mounting strategy is the relatively short electrical pathways between the integrated circuit and the substrate. These relatively low inductance pathways yield a high speed performance for the electronic device.

20

25

[0004] In some circumstances it may make sense from a performance standpoint to stack one semiconductor die on another semiconductor die. For example, it may be advantageous to mount a memory device on a processor device. However, electrical interconnects must be established between the stacked dice. Several conventional techniques for stacking dice have been
5 considered.

[0005] In one conventional variant, a relatively small semiconductor die is positioned on the bulk semiconductor side of a much larger semiconductor die. Bonding wires are used to establish the electrical conductivity between the upper die and the lower die. The difficulty associated with this approach is that the bonding wires tend to be relatively long electrical
10 pathways and thus exhibit higher than desired inductance and proportionally slower electrical performance. In addition, the bulk semiconductor side is not available for heat sink mounting.

[0006] In another conventional variant, a relatively small die is flip-chip mounted on the bulk silicon side of a larger semiconductor die. Electrical interconnects between the upper and lower die are provided by a plurality of conductor traces that are formed on the bulk silicon side of the
15 lower die. As with the first-mentioned conventional design, the conductor traces represent relatively high inductance pathways and thus limit speed performance. Furthermore, the bulk silicon side is not available for a heat sink.

[0007] In still another conventional design, a second die is mounted on the bulk silicon side of a larger die. Electrical interconnects between the two are established through a plurality of
20 silicon vias. This design also requires a plurality of external traces and thus represents longer than desired electrical pathways for signal transfer. In addition, the bulk silicon side is not available for a heat sink.

[0008] A fourth conventional design consists of a first die upon which a couple of additional dice are positioned. The multiple smaller dice are electrically interconnected with each other and
25 with the larger base die by way of a metal layer that is patterned on the base die and the two top-mounted dice. The metal layer is not unlike a larger scale version of a typical metallization layer used in a semiconductor die. In this regard, a dielectric layer is typically formed over the base die and the multiple top-mounted dice. The dielectric layer is lithographically patterned with

openings to selected portions of the base and top-mounted dice. The metallization layer is thereafter deposited over the dielectric layer. This conventional technique requires a very high degree of die alignment, which is not always possible and thus may result in limited yields.

[0009] The present invention is directed to overcoming or reducing the effects of one or more of the foregoing disadvantages.

5

SUMMARY OF THE INVENTION

[0010] In accordance with one aspect of the present invention, a method of manufacturing is provided that includes providing a first semiconductor die that has a first bulk semiconductor side and a first opposite side. A second semiconductor die is provided that has a second bulk semiconductor side and a second opposite side. The second opposite side of the second semiconductor die is coupled to the first opposite side of the first semiconductor die. Electrical connections are formed between the first semiconductor die and the second semiconductor die.

[0011] In accordance with another aspect of the present invention, a method of manufacturing is provided that includes providing a first semiconductor die that has a first bulk semiconductor side and a first opposite side. A plurality of second semiconductor dice is provided, each of which includes a second bulk semiconductor side and a second opposite side. The second opposite sides of the plurality of second semiconductor dice are coupled to the first opposite side of the first semiconductor die. Electrical connections between the first semiconductor die and the plurality of second semiconductor dice are formed.

[0012] In accordance with another aspect of the present invention, an apparatus is provided that includes a first semiconductor die that has a first bulk semiconductor side and a first opposite side. A second semiconductor die has a second bulk semiconductor side and a second opposite side. The second opposite side of the second semiconductor die is coupled to the first opposite side of the first semiconductor die. The second semiconductor die includes electrical connections with the first semiconductor die.

[0013] In accordance with another aspect of the present invention, an apparatus is provided that includes a first semiconductor die that has a first bulk semiconductor side and a first opposite side. A plurality of second semiconductor dice is included. Each of the second semiconductor dice includes electrical connections with the first semiconductor die and has a second bulk semiconductor side, and a second opposite side that is coupled to the first opposite side of the first semiconductor die.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The foregoing and other advantages of the invention will become apparent upon reading the following detailed description and upon reference to the drawings in which:

[0015] FIG. 1 is a pictorial view of an exemplary embodiment of a semiconductor device that includes stacked semiconductor dice;

[0016] FIG. 2 is a sectional view of FIG. 1 taken at section 2-2;

[0017] FIG. 3 is a sectional view of an exemplary embodiment of semiconductor die illustrating an exemplary conductor layer fabrication;

[0018] FIG. 4 is a sectional view like FIG. 3 depicting an exemplary process of fabricating conductor structures on the semiconductor die;

[0019] FIG. 5 is a sectional view like FIG. 4 depicting an exemplary process of stacking two exemplary semiconductor dice;

[0020] FIG. 6 is a sectional view like FIG. 5 depicting an exemplary process of encapsulating portions of the semiconductor device;

[0021] FIG. 7 is a sectional view like FIG. 6, but depicts additional processing of the exemplary semiconductor device;

[0022] FIG. 8 is an exploded pictorial view of an exemplary embodiment of a semiconductor device depicting some exemplary mounting configurations;

[0023] FIG. 9 is a plan view of an alternate exemplary embodiment of a semiconductor device including multiple semiconductor dice stacked on another semiconductor die; and

[0024] FIG. 10 is a sectional view of another alternate exemplary embodiment of a semiconductor device including stacked semiconductor dice.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

[0025] In the drawings described below, reference numerals are generally repeated where identical elements appear in more than one figure. Turning now to the drawings, and in particular to FIG. 1, therein is shown a pictorial view of an exemplary embodiment of a semiconductor device 10 that includes a semiconductor die 20 and a semiconductor die 30 mounted on the semiconductor die 20. An insulation or encapsulation layer 40 is positioned on the semiconductor die 20. A portion of the insulation layer 40 is shown cut away to reveal a portion of the semiconductor die 30. The conductor structures 45 are designed to provide interconnects between the semiconductor device 10 and another device as described elsewhere herein. The semiconductor dice 20 and 30 may be any of a myriad of different types of circuit devices used in electronics, such as, for example, microprocessors, graphics processors, application specific integrated circuits, memory devices or the like, and may be single or multi-core. The semiconductor dice 20 and 30 may be fabricated using silicon, germanium or other semiconductor materials. If desired, the semiconductor dice 20 and 30 may be fabricated as semiconductor-on-insulator substrates. Several conductor structures 45 are coupled to the semiconductor die 20. The conductor structures 45 may be fabricated as solder structures of lead-based or lead-free solders and shaped as bumps, balls or other structures. In an exemplary embodiment, a silver-tin-copper solder may be used. Optionally, another type of conductor structure may be used.

[0026] Additional details of the semiconductor device 10 may be understood by referring now also to FIG. 2, which is a sectional view of FIG. 1 taken at section 2-2. The semiconductor die 20 includes a bulk semiconductor side 50 and an opposite side 55. Chip circuitry of the semiconductor die 20, represented schematically by the dashed box 60 may be fabricated near the side 55. The semiconductor die 30 includes a bulk semiconductor side 65 and an opposite side 70. Chip circuitry of the semiconductor die 30, represented schematically by the dashed box 75, may be fabricated near the side 70. Thus, the opposite side 70 of the semiconductor die 30 is coupled to the opposite side 55 of the semiconductor die 20. This arrangement provides certain advantages described in more detail below.

[0027] Exemplary electrical connections between the semiconductor die 20 and the semiconductor die 30 will now be described. The semiconductor die 20 may be provided with plural conductor structures 80 proximate the side 55. The conductor structures 80 may be bond pads or other types of conductor structures composed of, for example, copper, nickel, gold, platinum, silver, alloys of these or the like. In an exemplary embodiment, the conductor structures 80 are composed of an alloy of copper, nickel and gold. The semiconductor die 30 may be provided with plural conductor structures 90 proximate the side 70. The conductor structures 90 may be bond pads or other types of conductor structures, and composed of the same types of materials used for the conductor structures 80. Ohmic contact between the pluralities of conductor structures 80 and 90 may be provided by another plurality of conductors 100 interposed between the sets of conductor structures 80 and 90. The conductors 100 may be composed of solder or other conductor materials. If solder is used, the conductor structures 100 may be fabricated as bumps, balls or other structures and be lead-based or lead-free. In an exemplary embodiment, a silver-tin-copper solder may be used.

[0028] This illustrative embodiment provides very short electrical pathways and thus fast signal and power transfer between the semiconductor die 20 and the semiconductor die 30. In addition, the bulk semiconductor side 50 is unfettered, leaving open the possibility of mounting a heat sink (not shown) thereon.

[0029] The semiconductor die 20 may be electrically connected to the conductor structures 45 by plural conductor structures 110 positioned proximate the side 55, a metal layer 120 positioned on or proximate the side 55 and plural conductors 130 coupled between the conductor structures 45 and the metallization layer 120. Optionally, a pathway between a given conductor 110 and a given conductor 45 may be provided with a conductor 120, but without the metallization layer 125. Such an arrangement is shown for the conductor 110, the conductor 125 and the conductor 45 located at the position labeled A in FIG. 2. Thus, the conductors 130 may have corresponding conductors 45 and vice versa. The conductor structures 110 may be bond pads or other types of conductor structures composed of the same types of materials used for the conductor structures 110. The metal layer 120 may be a so-called redistribution layer that provides electrical

pathways between the various conductor structures 110 of the semiconductor die 20 and the conductor structures 45. When viewed from above, the metallization layer 120 may take on the form of electrical traces that are well known for use on printed circuit boards and other types of electrical substrates. The benefits of routing may be achieved with two or more of the conductors 130 and the conductors 110 connected to the layer 120, however, the number and arrangement of conductor structures 110 and 130 tied to the layer 120 are matters of design discretion. The metal layer 120 may be composed of a myriad of conductor materials, such as copper, nickel, gold, platinum, silver, alloys of these or the like. The conductors 130 may be posts, pillars or other type of mechanical structures and may be composed of, for example, copper, nickel, gold, platinum, silver, alloys of these or the like. In an exemplary embodiment, the conductor structures 130 are composed of an alloy of copper, nickel and gold. The conductors 130 should project farther away from the side 55 of the semiconductor die 20 than does the side 65 so that clearance for the semiconductor die 30 is provided.

[0030] The encapsulation layer 40 surrounds the metallization layer 120 and the conductor structures 130 and thus provides lateral support for the conductor structures 130. In addition, the encapsulation layer serves as an underfill material for the region between the semiconductor device 30 and the semiconductor device 20. The encapsulation layer 40 may be fabricated from well-known encapsulation materials, such as epoxy resin with or without fillers such as silica or the like. If desired, the encapsulation layer 40 may be fabricated as a laminate structure.

Optionally, a separate underfill material (not shown) of epoxy resin or other well known under fill materials, may be positioned between the semiconductor dice 20 and 30.

[0031] An exemplary process for fabricating the semiconductor device 10 may be understood by referring now to FIGS. 3-7 and initially to FIG. 3. The metallization layer 120 is formed on the surface 55 of the semiconductor device 20. A variety of techniques may be used, such as plating, chemical vapor deposition, physical vapor deposition or the like. It is preferable that the metallization layer 120 includes an opening 140 to accommodate the positioning of the semiconductor device 30 shown in FIGS. 1 and 2. Thus, the metallization layer 120 will establish ohmic contact with the conductor structures 110 but not with the conductor structures

80 that are destined for electrical connectivity with the semiconductor device 30 depicted in FIGS. 1 and 2. If desired, the metallization layer 120 may be built up as a laminate structure.

[0032] The formation of the conductor structures 130 is depicted in FIG. 4. In an exemplary embodiment, a mask of resist or other mask material 160 is formed on the semiconductor die 20 and patterned with openings, one of which is shown and labeled 165, in which a metallic material may be deposited to establish the conductor structures 130. As noted above, the conductor structures 130 may be composed of, for example, copper, nickel, gold, platinum, silver, alloys of these or the like. Following the formation process for the structures 130, the resist film 160 may be removed by well-known ashing or other resist stripping techniques.

[0033] Referring now to FIG. 5, the semiconductor device 30 may be flip-chip mounted on the semiconductor die 20 in the opening 140 of the metallization layer 120 by way of the conductor balls or bumps 100. As noted above, electrical pathways are established between the semiconductor die 30 and the semiconductor die 20 by way of the conductor structures 90 on the device 30, the bumps 100 and the conductor structures 80 on the semiconductor die 20. The conductor structures 100 may be coupled first to the semiconductor device 30 or to the device 20 as desired. Following the initial mounting, a reflow process may be performed to temporarily liquify the conductor structures 120. In an exemplary embodiment, the semiconductor device 10 may be heated from about 35°C up to about 240°C in about 20 to 120 seconds and then allowed to cool. Optionally, the conductor structures 100 may be formed by reflowing complementary solder structures on both the pads 80 and 90. As noted above, the conductor structures 130 should project farther away from the side 55 of the semiconductor die 20 than does the semiconductor die 30.

[0034] The formation of the encapsulation layer 40 will now be described in conjunction with FIGS. 6 & 7. The encapsulation layer 40 may be applied to the semiconductor device 10 to encapsulate not only the semiconductor device 30 but also the underlying conductor structures 130 and the metallization layer 100. If desired, the semiconductor die 30 may be less than completely encapsulated. The encapsulation layer 40 may be composed of well-known epoxy materials, such as epoxy resin with or without silica fillers and phenol resins or the like.

Optionally, the layer 40 may be formed from a synthetic rubber mixture of epoxy resin, phenol resin, fused silica, and synthetic rubber. It is anticipated that the encapsulation layer 40 may be initially deposited with a greater height than that of the conductor structures 130 as shown.

[0035] In order to establish ohmic contact between the subsequently positioned conductor structures 45 (See FIGS. 1 & 2) and the conductor structures 130, it may be necessary to perform a material removal process, such as a grinding or chemical mechanical planarization process on the encapsulation layer 40. FIG. 7 depicts the semiconductor device 10 following the material removal process. The tops 170 of the conductors structures 130 are exposed and ready for attachment of the conductors 45 depicted in FIGS. 1 and 2. The conductor structures 45 may be formed by a variety of processes. If solder balls are used, a drop-in process may be used. Bumps may be formed by well-known plating or stencil processes. If other than solder structures are used, then other well-known techniques may be used.

[0036] With the semiconductor device 30 mounted on the side 55 of the semiconductor device 20, the bulk semiconductor side 50 of the semiconductor die 20 is still available for positioning of a heat sink. As shown in FIG. 8, which is an exploded pictorial, the semiconductor device 10 may be positioned on another device 180 such that the bulk semiconductor side 50 of the semiconductor die 20 may receive a heat sink 185. The device 180 may be a substrate, a printed circuit board, or other type of substrate. The heat sink 185 may be a fin, pipe or other configuration and may include fluid cooling. Additionally, the device 180 may, in turn, be mounted to another electronic device, such as another printed circuit board, or other type of substrate as desired. For example, the device 180 may be a package substrate and the device 190 may be a printed circuit board. The devices 180 and 190 may be part of some overall system, such as a computer system, or a component of a computer system, such as a discrete board or card.

[0037] In the embodiment disclosed in FIGS. 1 and 2, a single semiconductor die 30 is mounted on the semiconductor die 20. However, it should be understood that multiple semiconductor devices may be mounted on another semiconductor device in the same fashion as the semiconductor die 30 is mounted on the semiconductor die 20 depicted in FIGS. 1 and 2. In

this regard, FIG. 9 depicts an overhead view of a semiconductor die or device 195 upon which three semiconductor dice or devices 200, 210 and 215 are mounted. The devices 195, 200, 210 and 215 may be any of a myriad of different types of circuit devices used in electronics, such as, for example, microprocessors, graphics processors, application specific integrated circuits, memory devices or the like, and may be single or multi-core. If the semiconductor die 195 is implemented as a multi-core device, then each of the semiconductor devices may be positioned over and electrically tied to a particular core. For example, the devices 200 and 210 are positioned near and electrically coupled to respective cores that are represented schematically by the dashed boxes 217 and 219. Optionally, groups of such devices 200, 210 etc. may be tied to a given core.

[0038] In the foregoing illustrative embodiments, conductor bumps or balls are used to establish electrical connectivity between one semiconductor device mounted on another. However, other types of conductor structures may be used. FIG. 10 depicts an alternate exemplary embodiment in which a semiconductor die 220 is provided with the same conductor structures 80, 110 and 130, metallization layer 120 and encapsulation layer 40. External conductivity may be provided by the aforementioned conductor structures 45. However, electrical connections between a mounted semiconductor die 230 and the semiconductor die 220 may be established by way of conductor posts or pillars 240 that are positioned between corresponding conductor structures 90 of the semiconductor die 230 and corresponding conductor structures 80 of the semiconductor die 220. The conductor posts 250 may be composed of, for example, copper, nickel, gold, platinum, silver, alloys of these or the like. Various fabrication techniques may be used, such as plating, chemical vapor deposition, physical vapor deposition or the like.

[0039] It should be understood that the fabrication processes described herein may be performed on an individual single die or currently on multiple die that are part of some larger semiconductor workpiece, such as a wafer. The wafer can then be singulated into individual dice.

[0040] While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.

CLAIMS

What is claimed is:

1. A method of manufacturing, comprising:
5 providing a first semiconductor die having a first bulk semiconductor side and a first opposite side;
providing a second semiconductor die having a second bulk semiconductor side and a second opposite side;
coupling the second opposite side of the second semiconductor die to the first opposite
10 side of the first semiconductor die; and
forming electrical connections between the first semiconductor die and the second semiconductor die.
2. The method of claim 1, wherein the forming the electrical connections comprises forming
15 solder structures or conductor pillars.
3. The method of claim 1, comprising forming a plurality of conductor structures electrically connected to the first semiconductor die.
- 20 4. The method of claim 3, wherein the forming the plurality of conductor structures comprises forming a plurality of conductors coupled to a corresponding plurality of solder structures.
- 25 5. The method of claim 3, comprising forming a metal layer coupled to the first semiconductor die and electrically coupled to at least two of the plurality of conductor structures.

6. The method of claim 1, wherein the providing the first semiconductor die comprises providing a processor.

7. The method of claim 6, wherein the providing the second semiconductor die comprises providing a memory device.

8. The method of claim 1, comprising coupling a first substrate to the first or second semiconductor die.

9. The method of claim 8, comprising coupling a second substrate to the first substrate.

10. A method of manufacturing, comprising:
providing a first semiconductor die having a first bulk semiconductor side and a first opposite side;
providing a plurality of second semiconductor dice, each of the plurality of second semiconductor dice having a second bulk semiconductor side and a second opposite side;
coupling the second opposite sides of the plurality of second semiconductor dice to the first opposite side of the first semiconductor die; and
forming electrical connections between the first semiconductor die and the plurality of second semiconductor dice.

11. The method of claim 10, wherein the forming the electrical connections comprises forming solder structures.

12. The method of claim 10, comprising forming a plurality of conductor structures electrically connected to the first semiconductor die.

13. The method of claim 12, wherein the forming the plurality of conductor structures comprises forming a plurality of conductors coupled to a corresponding plurality of solder structures.
- 5 14. The method of claim 12, comprising forming a metal layer coupled to the first semiconductor die and electrically coupled to at least two of the plurality of conductor structures.
- 10 15. The method of claim 10, wherein the providing the second semiconductor die comprises providing a plurality of memory devices.
16. The method of claim 10, comprising coupling a first substrate to the first semiconductor die.
- 15 17. The method of claim 16, comprising coupling a second substrate to the first substrate.
18. The method of claim 10, wherein the providing the first semiconductor die comprises providing a semiconductor die including a plurality of cores, and wherein the forming the electrical connections comprises electrically connecting at least one of the plurality of the
20 second semiconductor dice to at least one of the cores.
19. An apparatus, comprising:
a first semiconductor die having a first bulk semiconductor side and a first opposite side;
and
25 a second semiconductor die having a second bulk semiconductor side and a second opposite side, the second opposite side of the second semiconductor die being coupled to the first opposite side of the first semiconductor die, the second semiconductor including electrical connections with the first semiconductor die.

20. An apparatus, comprising:
a first semiconductor die having a first bulk semiconductor side and a first opposite side;
and
a plurality of second semiconductor dice, each of the second semiconductor dice
5 including electrical connections with the first semiconductor die and having a
second bulk semiconductor side and a second opposite side, the second opposite
side being coupled to the first opposite side of the first semiconductor die.
21. The apparatus of claim 20, wherein the first semiconductor die comprises a processor.
- 10 22. The apparatus of claim 21, wherein each of the plurality of second semiconductor dice
comprises a memory device.
23. The apparatus of claim 20, comprising a first substrate coupled to the first or second
15 semiconductor die.
24. The apparatus of claim 23, comprising a second substrate coupled to the first substrate.

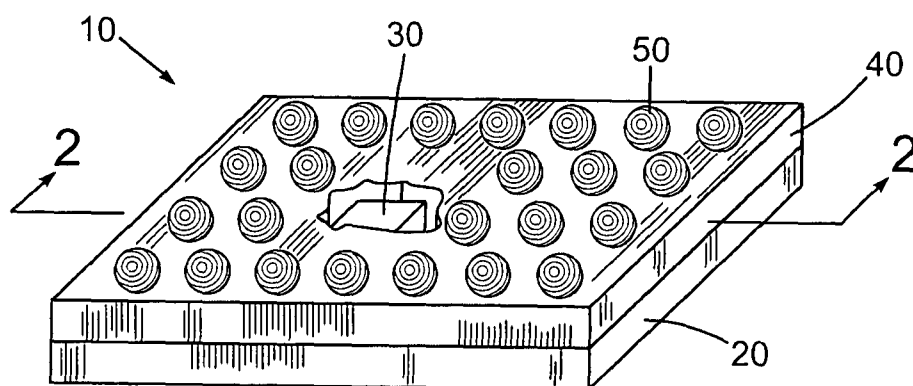
$\frac{1}{4}$ 

FIG. 1

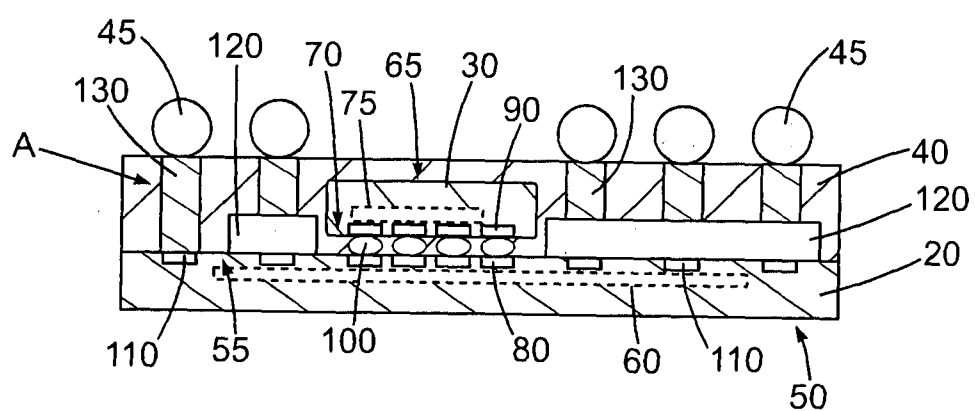


FIG. 2

2/4

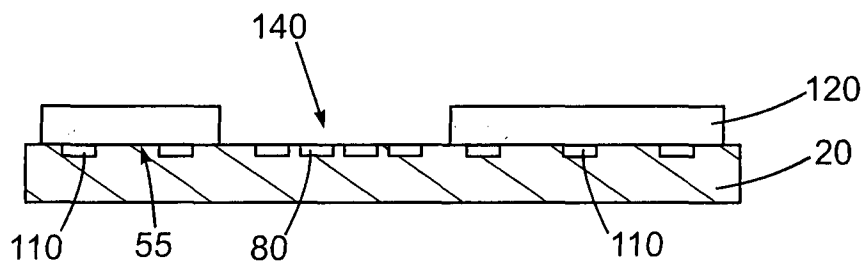


FIG. 3

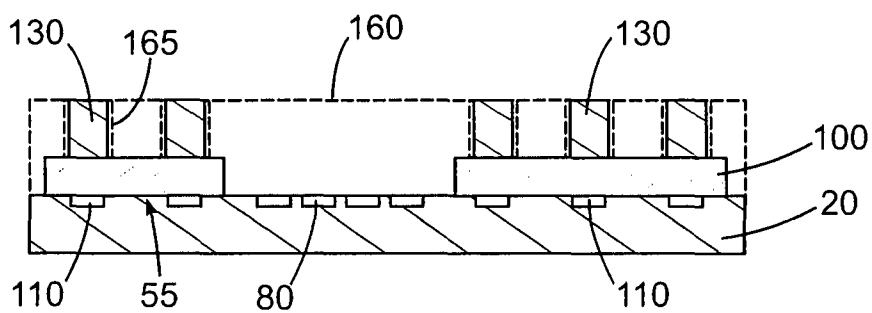


FIG. 4

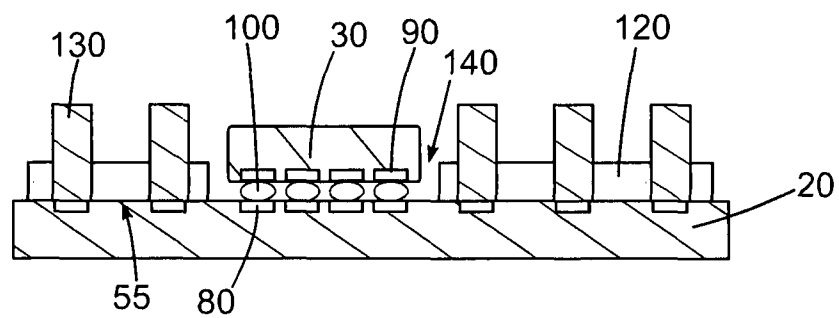


FIG. 5

3/4

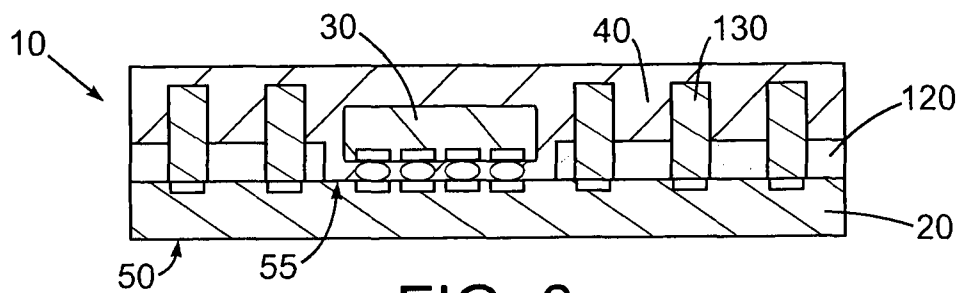


FIG. 6

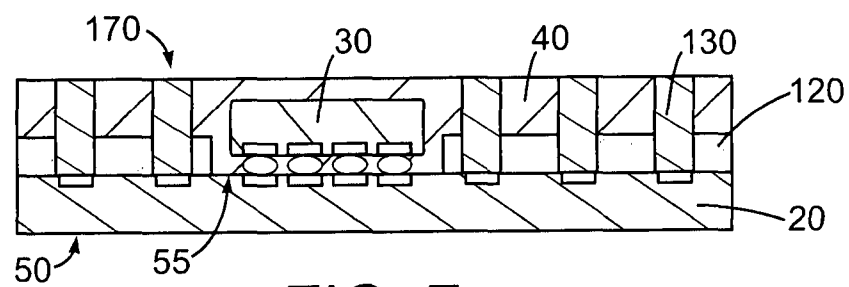


FIG. 7

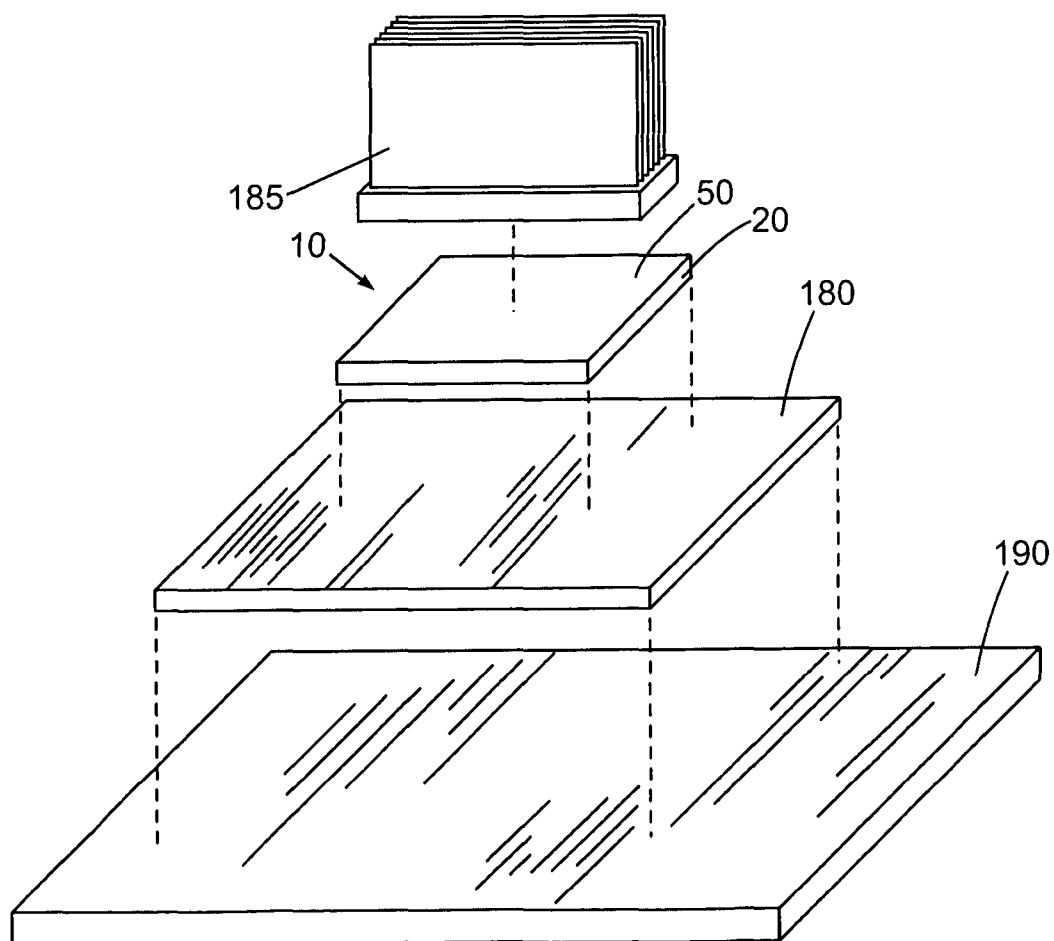


FIG. 8

4/4

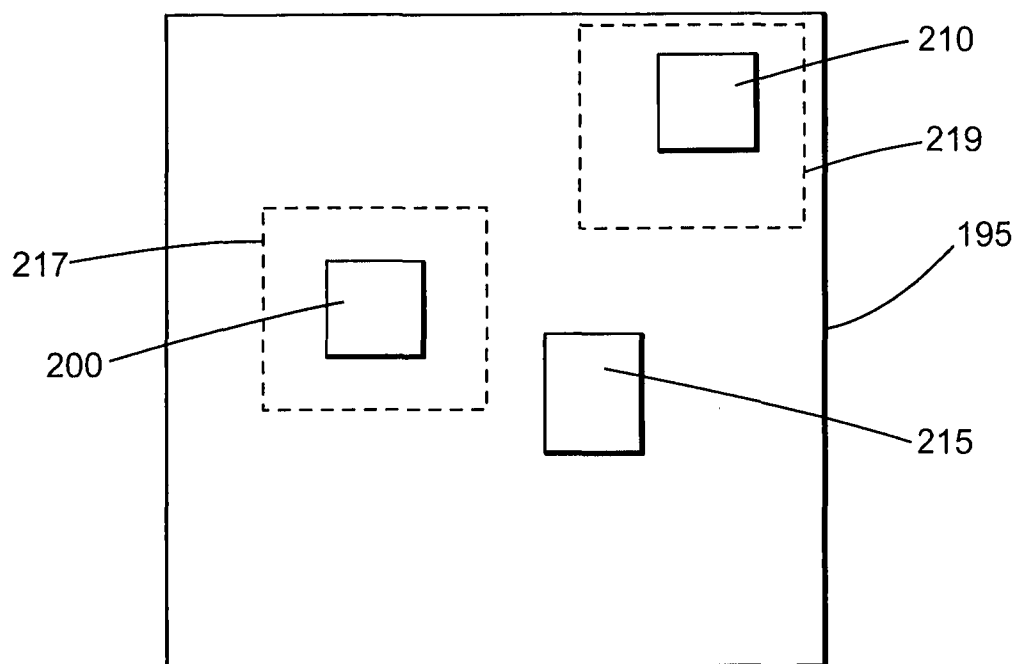


FIG. 9

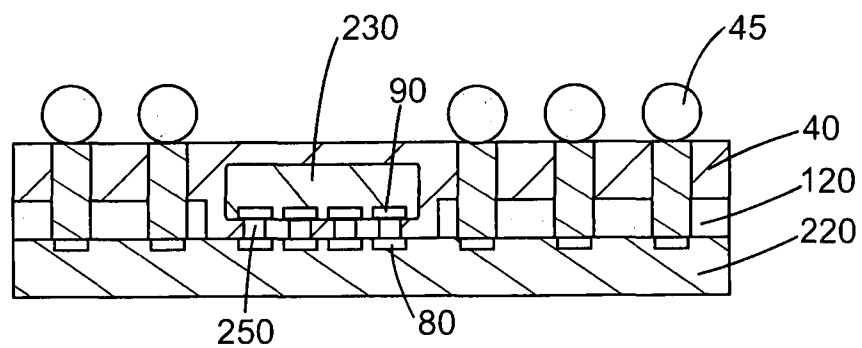


FIG. 10