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(71) Applicant: **SANDISK TECHNOLOGIES, INC.** [US/US]; Two Legacy Town Center, 6900 North Dallas Parkway, Plano, Texas 75024 (US).

(72) Inventors: **MAKALA, Raghuveer S.**; c/o SanDisk Corporation, 951 SanDisk Drive, Milpitas, California 95035 (US). **LEE, Yao-Sheng**; c/o SanDisk Corporation, 951 SanDisk Drive, Milpitas, California 95035 (US). **ALSMEIER, Johann**; c/o SanDisk Corporation, 951 SanDisk Drive, Milpitas, California 95035 (US). **CHIEN, Henry**; c/o SanDisk Corporation, 951 SanDisk Drive, Milpitas, California 95035 (US). **TERAHARA, Masanori**; c/o SanDisk Corporation, 951 SanDisk Drive, Milpitas, California 95035 (US). **WATATANI, Hirofumi**; c/o SanDisk Corporation, 951 SanDisk Drive, Milpitas, California 95035 (US).

(74) Agents: **RADOMSKY, Leon** et al.; The Marbury Law Group, PLLC, 11800 Sunrise Valley Dr., 15th Floor, Reston, Virginia 20191 (US).

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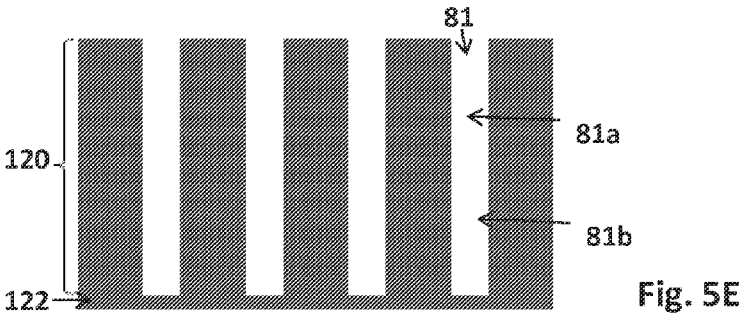


Fig. 5E

(57) Abstract: A method of making a semiconductor device includes forming a stack of alternating layers of a first material and a second material over a substrate, etching the stack to form at least one opening extending partially through the stack and forming a masking layer on a sidewall and bottom surface of the at least one opening. The method also includes removing the masking layer from the bottom surface of the at least one opening while leaving the masking layer on the sidewall of the at least one opening, and further etching the at least one opening to extend the at least one opening further through the stack while the masking layer remains on the sidewall of the at least one opening.

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SPACER PASSIVATION FOR HIGH ASPECT RATIO ETCHING OF MULTILAYER STACKS FOR THREE DIMENSIONAL NAND DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims benefit of U.S. non-provisional application serial number 14/135,931 filed on December 20, 2013, which claims benefit of U.S. provisional patent application serial number 61/807,277 filed on April 1, 2013, and which applications are incorporated herein by reference in their entireties.

FIELD

[0002] The present invention relates generally to the field of semiconductor devices and specifically a method of making three dimensional vertical NAND devices and other three dimensional devices.

BACKGROUND

[0003] Three dimensional vertical NAND strings are disclosed in an article by T. Endoh, et. al., titled "Novel Ultra High Density Memory With A Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell", IEDM Proc. (2001) 33-36. However, this NAND string provides only one bit per cell. Furthermore, the active regions of the NAND string is formed by a relatively difficult and time consuming process involving repeated formation of sidewall spacers and etching of a portion of the substrate, which results in a roughly conical active region shape.

SUMMARY

[0004] An embodiment relates to a method of making a semiconductor device includes forming a stack of alternating layers of a first material and a second material over a substrate, etching the stack to form at least one opening extending partially through the stack and

forming a masking layer on a sidewall and bottom surface of the at least one opening. The method also includes removing the masking layer from the bottom surface of the at least one opening while leaving the masking layer on the sidewall of the at least one opening, and further etching the at least one opening to extend the at least one opening further through the stack while the masking layer remains on the sidewall of the at least one opening.

[0005] Another embodiment relates to a method of making a semiconductor device including forming a stack of alternating layers of a first material and a second material over a substrate and etching the stack to form at least one opening in the stack. The at least one opening comprises a tapered opening having an upper portion which is wider than a lower portion. The method also includes forming a masking layer on a sidewall of the upper portion of the at least one opening while the lower portion of the at least one opening is not covered by the masking layer, and further etching the lower portion of the at least one opening to widen the lower portion of the at least one opening while the masking layer remains on the sidewall of the upper portion of the at least one opening.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIGs. 1A-1B are respectively side cross sectional and top cross sectional views of a NAND string of one embodiment. Figure 1A is a side cross sectional view of the device along line Y-Y' in Figure 1B, while Figure 1B is a side cross sectional view of the device along line X-X' in Figure 1A.

[0007] FIGs. 2A-2B are respectively side cross sectional and top cross sectional views of a NAND string of another embodiment. Figure 2A is a side cross sectional view of the device along line Y-Y' in Figure 2B, while Figure 2B is a side cross sectional view of the device along line X-X' in Figure 2A.

[0008] FIG. 3 is side cross sectional view of a NAND string of an embodiment with a U-shaped channel.

[0009] FIG. 4 is side cross sectional view of a NAND string of another embodiment.

[0010] FIGs. 5A-5E, 6A-6F, 7A-7F and 8A-8E illustrate embodiment methods of making NAND strings.

DETAILED DESCRIPTION

[0011] The embodiments of the invention provide a monolithic, three dimensional array of semiconductor devices, such as an array of vertical NAND strings located in high aspect ratio openings which are formed using a sidewall spacer.

[0012] The present inventors realized that vertical NAND device fabrication relies heavily on reactive ion etching ("RIE") of very high aspect ratio (e.g., at least a 40:1, such as 40:1 to 100:1 height to width ratio) of memory openings in a stack of alternating layers. This etching suffers from several drawbacks, such as etch profile variation resulting in variation of critical diameter between the top and bottom of the memory opening, bowing across the length of the memory opening, hard mask erosion, and critical diameter non-uniformity between memory openings at the center, middle and edge of the substrate. These drawbacks limit the number of memory layers that can be controllably etched within acceptable process. variations.

[0013] The embodiments of the present invention provide a solution to the aforementioned drawbacks by using a spacer passivation of memory opening sidewalls to improve the etch profiles of the multilayer stacks. In a first embodiment, the memory opening is partially etched in the stack followed by a conformal spacer deposition in the memory opening. The spacer protects the sidewalls of already etched features (e.g. upper layers of the stack) from being over etched. The memory opening etching is then continued

to form the bottom part of the opening.

[0014] In a second embodiment, the memory opening is completely etched through the stack followed by a non-conformal spacer deposition in the memory opening. The deposition of the non-conformal spacer is tuned so that the thickness drops from a finite value (at the upper end of the memory opening) to near-zero thickness towards the lower end of the opening (preferably at about 2/3rds depth of the etched opening). An over etch step is then used to widen the critical diameter of the opening that is not protected by the spacer (in the lower end of the opening, such as in the lower third of the opening). In both embodiments, an additional step may be used to remove the spacer after the memory opening etching is completed.

[0015] The NAND strings are vertically oriented, such that at least one memory cell is located over another memory cell. This allows vertical scaling of NAND devices to provide a higher density of memory cells per unit area of silicon or other semiconductor material.

[0016] A monolithic three dimensional memory array is one in which multiple memory levels are formed above a single substrate, such as a semiconductor wafer, with no intervening substrates. The term "monolithic" means that layers of each level of the array are directly deposited on the layers of each underlying level of the array. In contrast, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device. For example, non-monolithic stacked memories have been constructed by forming memory levels on separate substrates and adhering the memory levels atop each other, as in Leedy, U.S. Pat. No. 5,915,167, titled "Three Dimensional Structure Memory." The substrates may be thinned or removed from the memory levels before bonding, but as the memory levels are initially formed over separate substrates, such memories are not true monolithic three dimensional memory arrays.

[0017] In some embodiments, the monolithic three dimensional NAND string 180 comprises a semiconductor channel 1 having at least one end portion extending substantially perpendicular to a major surface 100a of a substrate 100, as shown in Figures 1A, 2A and 4. For example, the semiconductor channel 1 may have a pillar shape and the entire pillar-shaped semiconductor channel extends substantially perpendicularly to the major surface of the substrate 100, as shown in Figures 1A, 2A and 4. In these embodiments, the source/drain electrodes of the device can include a lower electrode 102 provided below the semiconductor channel 1 and an upper electrode 202 formed over the semiconductor channel 1, as shown in Figures 1A and 2A.

[0018] Alternatively, the semiconductor channel 1 may have a U-shaped pipe shape, as shown in Figure 3. The two wing portions 1a and 1b of the U-shaped pipe shape semiconductor channel may extend substantially perpendicular to the major surface 100a of the substrate 100, and a connecting portion 1c of the U-shaped pipe shape semiconductor channel 1 connects the two wing portions 1a, 1b extends substantially parallel to the major surface 100a of the substrate 100. In these embodiments, one of the source or drain electrodes 202_1 contacts the first wing portion of the semiconductor channel from above, and another one of a source or drain electrodes 202_2 contacts the second wing portion of the semiconductor channel 1 from above. An optional body contact electrode (not shown) may be disposed in the substrate 100 to provide body contact to the connecting portion of the semiconductor channel 1 from below. The NAND string's select or access transistors are not shown in Figures 1-4 for clarity.

[0019] In some embodiments, the semiconductor channel 1 may be a filled feature, as shown in Figures 2A-2B, 3 and 4. In some other embodiments, the semiconductor channel 1 may be hollow, for example a hollow cylinder filled with an insulating fill material 2, as

shown in Figures 1A-1B. In these embodiments, an insulating fill material 2 may be formed to fill the hollow part surrounded by the semiconductor channel 1. The U-shaped pipe shape semiconductor channel 1 shown in Figure 3 and/or the channel 1 shown in Figure 4 may alternatively be a hollow cylinder filled with an insulating fill material 2, shown in Figures 1A-1B.

[0020] The substrate 100 can be any semiconducting substrate known in the art, such as monocrystalline silicon, IV-IV compounds such as silicon-germanium or silicon-germanium-carbon, III-V compounds, II-VI compounds, epitaxial layers over such substrates, or any other semiconducting or non-semiconducting material, such as silicon oxide, glass, plastic, metal or ceramic substrate. The substrate 100 may include integrated circuits fabricated thereon, such as driver circuits for a memory device.

[0021] Any suitable semiconductor materials can be used for semiconductor channel 1, for example silicon, germanium, silicon germanium, or other compound semiconductor materials, such as III-V, II-VI, or conductive or semiconductive oxides, etc. The semiconductor material may be amorphous, polycrystalline or single crystal. The semiconductor channel material may be formed by any suitable deposition methods. For example, in one embodiment, the semiconductor channel material is deposited by low pressure chemical vapor deposition (LPCVD). In some other embodiments, the semiconductor channel material may be a recyrstallized polycrystalline semiconductor material formed by recrystallizing an initially deposited amorphous semiconductor material.

[0022] The insulating fill material 2 may comprise any electrically insulating material, such as silicon oxide, silicon nitride, silicon oxynitride, or other high-k insulating materials.

[0023] The monolithic three dimensional NAND string further comprise a plurality of control gate electrodes 3, as shown in Figures 1A-1B, 2A-2B, 3 and 4. The control gate

electrodes 3 may comprise a portion having a strip shape extending substantially parallel to the major surface 100a of the substrate 100. The plurality of control gate electrodes 3 comprise at least a first control gate electrode 3a located in a first device level (e.g., device level A) and a second control gate electrode 3b located in a second device level (e.g., device level B) located over the major surface 100a of the substrate 100 and below the device level A. The control gate material may comprise any one or more suitable conductive or semiconductor control gate material known in the art, such as doped polysilicon, tungsten, copper, aluminum, tantalum, titanium, cobalt, titanium nitride or alloys thereof. For example, the control gate material in Figures 1A, 2A and 3 may comprise a conductive metal or metal alloy, such as tungsten and/or titanium nitride, while the control gate material in Figure 4 may comprise doped polysilicon.

[0024] A blocking dielectric 7 is located adjacent to the control gate(s) 3 and may surround the control gate 3, as shown in Figures 1A, 2A and 3. Alternatively, a straight blocking dielectric layer 7 may be located only adjacent to an edge (i.e., minor surface) of each control gate 3, as shown in Figure 4. The blocking dielectric 7 may comprise a layer having plurality of blocking dielectric segments located in contact with a respective one of the plurality of control gate electrodes 3, for example a first dielectric segment 7a located in device level A and a second dielectric segment 7b located in device level B are in contact with control electrodes 3a and 3b, respectively, as shown in Figure 3. Alternatively, the blocking dielectric 7 may be a straight, continuous layer, as shown in Figure 4.

[0025] The monolithic three dimensional NAND string also comprise a charge storage region 9. The charge storage region 9 may comprise one or more continuous layers which extend the entire length of the memory cell portion of the NAND string, as shown in Figure 4. For example, the charge storage region 9 may comprise an insulating charge trapping

material, such as a silicon nitride layer.

[0026] Alternatively, the charge storage region may comprise a plurality of discrete charge storage regions 9, as shown in Figures 1A, 2A and 3. The plurality of discrete charge storage regions 9 comprise at least a first discrete charge storage region 9a located in the device level A and a second discrete charge storage region 9b located in the device level B, as shown in Figure 3. The discrete charge storage regions 9 may comprise a plurality of vertically spaced apart, conductive (e.g., metal such as tungsten, molybdenum, tantalum, titanium, platinum, ruthenium, and alloys thereof, or a metal silicide such as tungsten silicide, molybdenum silicide, tantalum silicide, titanium silicide, nickel silicide, cobalt silicide, or a combination thereof), or semiconductor (e.g., polysilicon) floating gates. Alternatively, the discrete charge storage regions 9 may comprise an insulating charge trapping material, such as silicon nitride segments.

[0027] The tunnel dielectric 11 of the monolithic three dimensional NAND string is located between charge storage region 9 and the semiconductor channel 1.

[0028] The blocking dielectric 7 and the tunnel dielectric 11 may be independently selected from any one or more same or different electrically insulating materials, such as silicon oxide, silicon nitride, silicon oxynitride, or other insulating materials. The blocking dielectric 7 and/or the tunnel dielectric 11 may include multiple layers of silicon oxide, silicon nitride and/or silicon oxynitride (e.g., ONO layers).

[0029] Figures 5A-5E illustrate a method of making a high aspect ratio opening in a stack of alternating layers using sidewall spacer passivation of the opening according to a first embodiment of the invention.

[0030] Referring to Figure 5A, a stack 120 of alternating layers 19 and 121 are formed over the major surface of the substrate 100. Layers 19, 121 may be deposited over the

substrate by any suitable deposition method, such as sputtering, CVD, PECVD, MBE, etc. The layers 19, 121 may be 6 to 100 nm thick and there may be 32-64 pairs of layers 19, 121 in the stack 120. Layers 19 and 121 are comprised of different materials from each other.

[0031] The first layers 19 comprise an electrically insulating material. Any suitable insulating material may be used, such as silicon oxide, silicon nitride, silicon oxynitride, a high-k dielectric (e.g., aluminum oxide, hafnium oxide, etc. or an organic insulating material).

[0032] In one aspect of this embodiment, the second layers 121 comprise the control gate material, such as doped polysilicon. In this aspect, layers 121 will be retained in the final device as the control gates 3, and the memory film comprising the blocking dielectric 7, the charge storage region 9 and the tunnel dielectric 11 will be formed through the same front side memory opening as the channel 1 to form the NAND string shown in Figure 4.

[0033] In another aspect of this embodiment, the second layers 121 comprise a sacrificial material, such a semiconductor material, conductive material (e.g., metal) or insulating material (e.g., silicon nitride). The sacrificial layers 121 will be eventually removed from the stack 120 though a back side opening and replaced with the combination of the electrically conductive control gates 3, such as tungsten control gates 3, and clam shaped blocking dielectric segments 7, as shown in Figures 1A, 2A and 3.

[0034] For example, sacrificial layers 121 may comprise silicon, such as amorphous silicon or polysilicon, or another semiconductor material, such as a group IV semiconductor, including silicon-germanium and germanium. Sacrificial layers 121 may comprise intrinsic or undoped (if the as-deposited material inherently has a low p-type or n-type conductivity) semiconductor material, such as intrinsic or undoped polysilicon or amorphous silicon. However, p-type or n-type doped semiconductor materials, such as lightly or heavily doped

materials may also be used if desired. The term heavily doped includes semiconductor materials doped n-type or p-type to a concentration of above 10^{18} cm^{-3}. In contrast, lightly doped semiconductor materials have a doping concentration below 10^{18} cm^{-3} and intrinsic semiconductor materials have a doping concentration below 10^{15} cm^{-3}.

[0035] If desired, an optional lower etch stop layer 122 may be formed below the stack 120. If the stack 120 comprises silicon oxide layers 19 and doped polysilicon layers 121, then the etch stop layer 122 may comprise silicon nitride or another material which has a lower etch rate than the etch rate of layers 19 and 121. For example, the etch stop layer 122 may be made of a mid-k to high-k metal oxide, such as an aluminum based dielectric (e.g., stoichiometric Al_2O_3 or non-stoichiometric aluminum oxide) or a titanium based dielectric (e.g., stoichiometric TiO_2 or non-stoichiometric titanium oxide), or a tantalum based dielectric (e.g., stoichiometric Ta_2O_5 or non-stoichiometric tantalum oxide),or nitrogen doped silicon carbide (e.g., silicon carbonitride, SiC(N)) which is resistant to fluorine based plasma. Alternatively, the etch stop layer may comprise aluminum nitride, aluminum oxynitride, silicon carbide or another suitable etch stop material. The etch stop is typically thin, such as 10-70 nm, such as 20-50 nm thick.

[0036] If desired, an optional intermediate etch stop layer 132 may be located in the stack 120, such as between the top 25% and bottom 25% of the stack height, for example at the 50% of the stack height. Layer 132 may comprise the same or different etch stop material as layer 122. For example, layer 132 may be a silicon nitride layer 132 in a stack of silicon oxide 19 and polysilicon layers 121. In summary, the intermediate etch stop layer 132 may be formed between a lower portion and an upper portion of the stack 120, and/or the lower etch stop layer 122 may be formed under the stack 120.

[0037] Furthermore, an optional hard mask layer or layers 124 may be formed over the

stack. The hard mask layer 124 may be any suitable hard mask material which has a lower etch rate than the stack layers 19, 121. For example, the hard mask layer 124 may comprise amorphous carbon, doped carbon, silicon nitride, silicon carbide, tungsten, tungsten nitride etc.

[0038] As shown in Figure 5B, the stack 120 is etched to form at least one memory opening 81a extending partially through the stack 120 (e.g., through the upper portion 120a of the stack). Preferably, a plurality of memory openings 81a are formed, as shown in Figure 5B.

[0039] The openings 81a may be formed by patterning the hard mask 124 to form at least one hard mask opening 181 which exposes the stack 120, followed by etching the stack 120 through the at least one hard mask opening 181 to form at least one opening 81a extending partially through the upper portion 120a of the stack 120. The openings 81a may be formed by photolithographic patterning of a photoresist (not shown for clarity), etching the hard mask layer 124 using the patterned photoresist as a mask to form openings 181, followed by RIE of the upper portion 120a of the stack 120 through openings 181 using the patterned hard mask layer 124 as a mask.

[0040] Each opening 81a may extend 25% to 75% through the stack 120, such as about half way through the stack, stopping on any suitable layer in the stack. If the optional intermediate etch stop layer 132 is located in the stack 120, then the partial etch stops on layer 132.

[0041] As shown in Figure 5C, a masking layer 134 is formed on a sidewall and bottom surface of the at least one opening 81a. Preferably, layer 134 is formed on sidewalls and bottom surfaces of all openings 81a and over the top surface of the hard mask 124. The masking layer 134 preferably comprises a conformal spacer deposited by atomic layer

deposition (ALD) or chemical vapor deposition (CVD). Layer 134 is deposited conformally in the openings 81a such that it does not fill the entire volume of the openings 81a. As noted above, layer 134 may have a thickness of 3 to 50 nm, such as 5 to 25 nm, and may be made of any suitable protective material, such as amorphous carbon, silicon nitride, silicon oxide, metal oxide or metal nitride (e.g., HfOx, TaOx, AlOx, AlNx, etc.).

[0042] The masking layer 134 is removed from the bottom surface of the at least one opening 81a while leaving the masking layer on the sidewall of the at least one opening 81a, as shown in Figure 5D. Layer 134 may also removed from the top surface of the hard mask layer 124. The removal step preferably comprises a highly directional RIE step, similar to a sidewall spacer etch step, as shown by the arrows in Figure 5D. A low pressure, high bias RIE process can be used for strong ion bombardment.

[0043] After removing layer 134 at the bottom of the openings 81a, the RIE process shown in Figure 5D may optionally be continued to extend the openings 81a into the lower part of the stack to form openings 81b. Alternatively, the RIE process stops after removing layer 134 from the bottom of the upper openings 81a and the etching chemistry is switched to etch the lower openings 81b in the lower part of the stack 120. In either case, the further etching of the at least one opening 81a using the same RIE chemistry or a different etching chemistry extends the at least one opening further through the stack while the masking layer 134 remains on the sidewall of the at least one opening 81a. If the intermediate etch stop layer 132 is present in the stack, then the further etching extends the at least one opening 81a through the intermediate etch stop layer 132 and through the lower portion of the stack 120 to the lower etch stop layer 122 while the masking layer 134 remains on the sidewall of the at least one opening 81a. If desired, the opening may be etched further through the lower etch stop layer 122 to extend to the underlying layer(s) or substrate, as shown in Figure 4. For

example, the opening may extend to the lower electrode 102 shown in Figures 1A and 2A.

[0044] After completion of the further etching of the openings 81, the masking layer 134 is removed from the sidewalls of the openings 81. If the masking layer 134 comprises an amorphous carbon masking layer, then the step of removing the masking layer from the sidewall may comprise ashing the amorphous carbon masking layer. Alternatively, for other masking layer 134 materials, the step of removing the masking layer from the sidewall may comprise selectively wet etching the masking layer 134 without removing the other layers 19, 121 of the stack. This completes the formation of the memory openings 81.

[0045] The completed memory openings 81 composed of upper portions 81a and lower portions 81b are shown in Figure 5E. The openings 81 extend at least to the lower etch stop layer 122 or through the lower etch stop layer 122. The hard mask layer 124 may be partially or fully consumed during the etching of the lower portions 81b of the openings 81, as shown in Figure 5E.

[0046] An array of memory openings 81 (i.e., front side openings) is formed in locations where the memory film and vertical channels of NAND strings will be subsequently formed, as shown in Figure 4. For example, if layers 121 comprise a control gate material, such as doped polysilicon, then the etching of the memory openings 81 patterns layers 121 into control gates 3. The memory film (e.g., blocking dielectric 7, charge storage region 9 and tunnel dielectric 11) and the channels 1 are then deposited into the memory openings 81 to complete the memory levels of the NAND strings, as shown in Figure 4. Specifically, the blocking dielectric 7 is formed in the at least one opening 81, the charge storage layer 9 is formed over the blocking dielectric 7, the tunnel dielectric 11 is formed over the charge storage layer 9, and the semiconductor channel 1 is formed over the tunnel dielectric 11 in the at least one opening 81. If desired, the insulating fill layer 2 may also be deposited into the

memory openings, as shown in Figure 2A.

[0047] Figures 6A-6F illustrate a method of making a high aspect ratio opening in a stack of alternating layers using sidewall spacer passivation of the opening according to a second embodiment of the invention.

[0048] Figure 6A illustrates the same stack 120 of alternating layers of a first material 19 and a second material 121 as in Figure 5A. The stack may also contain the optional lower etch stop 122 and hard mask 124 layers as in Figure 5A. However, the intermediate etch stop layer 132 is preferably omitted in the stack shown in Figure 6A.

[0049] Then, as shown in Figure 6B, the stack 120 is etched to form at least one memory opening 81 in the stack 120. The at least one opening 81 preferably comprises a plurality of openings 81 formed by a method similar to the method described above with respect to Figure 5B. However, the openings 81 in Figure 6B differ from the openings 81a in Figure 5B in that they extend through the entire stack 120, such as to the etch stop layer 122 under the stack, and in that the openings 81 are preferably tapered openings having an upper portion 81a which is wider than a lower portion 81b. The openings 81 may be formed by RIE through openings 181 in the patterned hard mask 124.

[0050] As shown in Figure 6C, a masking layer 234 is formed on a sidewall of the upper portion 81a of the at least one opening 81 in the upper portion 120a of the stack 120. Layer 234 is also formed on the upper surface of the stack 120. The lower portion 81b of the at least one opening 81 is not covered by the masking layer 234. Preferably, layer 234 comprises a non-conformal sidewall spacer because it does not cover the sidewall of the lower portion 81b of the opening 81. This non-conformal layer 234 may be referred to as a "semi-conformal" layer because it covers the hard mask 124 and upper portion 81a of the opening 81. Layer 234 may be made of any suitable protective material, such as amorphous carbon,

silicon nitride, silicon oxide, metal oxide or metal nitride (e.g., HfOx, TaOx, AlOx, AlNx, etc.). Layer 234 deposition is tuned so that the thickness drops from a finite value (e.g., 3-50 nm in the upper portion 81a of the memory opening 81) to zero or near-zero thickness in the lower portion 81b of the opening 81. Preferably, layer 234 thickness drops to zero or below 1 nm between 50% and 75% of the depth of the opening 81, such as at about 65-68% depth of the etched opening 81. In other words, the lower portion 81b of the opening 81 comprises the lower 25 to 50% of the opening, such as the lower third of the opening 81 in the lower portion 120b of the stack 120.

[0051] As shown by the arrows in Figures 6D and 6E, an over etch step is then used to widen the critical diameter of the lower portion 81b of the opening 81 that is not protected by layer 234. Specifically, the over etch comprises further etching the lower portion 81b of the at least one opening 81 to widen the lower portion 81b of the at least one opening while the masking layer 234 remains on the sidewall of the upper portion 81a of the at least one opening 81. Thus, layers 19 and 121 (e.g., control gates) in the upper portion 120a of the stack are protected by layer 234 from further etching while the layers 19 and 121 in the lower portion 120b of the stack are further etched in the step shown in Figures 6D and 6E. The further etching step shown in Figures 6D and 6E may comprise an RIE step and/or a wet etching (e.g., wet clean) step.

[0052] After completion of the further etching of the openings 81, the masking layer 234 is removed from the sidewalls of the openings 81, as shown in Figure 6F. If the masking layer 234 comprises an amorphous carbon masking layer, then the step of removing the masking layer from the sidewall may comprises ashing the amorphous carbon masking layer. Alternatively, for other masking layer 234 materials, the step of removing the masking layer from the sidewall may comprise selectively wet etching the masking layer 234 without

removing the other layers 19, 121 of the stack. This completes the formation of the memory openings 81.

[0053] The completed memory openings 81 composed of upper portions 81a and lower portions 81b are shown in Figure 6F. The openings 81 extend at least to the lower etch stop layer 122 or through the lower etch stop layer 122. The hard mask layer 124 may be partially or fully consumed during the etching of the lower portions 81b of the openings 81, as shown in Figure 6F.

[0054] An array of memory openings 81 (i.e., front side openings) is formed in locations where the memory film and vertical channels of NAND strings will be subsequently formed, as shown in Figure 4. For example, if layers 121 comprise a control gate material, such as doped polysilicon, then the etching of the memory openings 81 patterns layers 121 into control gates 3. The memory film (e.g., blocking dielectric 7, charge storage region 9 and tunnel dielectric 11) and the channels 1 are then deposited into the memory openings 81 to complete the memory levels of the NAND strings, as shown in Figure 4. Specifically, the blocking dielectric 7 is formed in the at least one opening 81, the charge storage layer 9 is formed over the blocking dielectric 7, the tunnel dielectric 11 is formed over the charge storage layer 9, and the semiconductor channel 1 is formed over the tunnel dielectric 11 in the at least one opening 81. If desired, the insulating fill layer 2 may also be deposited into the memory openings, as shown in Figure 2A.

[0055] Figures 7A-7F show alternative steps of the method of the second embodiment. In this method, an additional hard mask layer is formed over the masking layer 234.

[0056] Figure 7A illustrates the same stack 120 of alternating layers of the first material 19 and the second material 121 as in Figure 6A. The stack may also contain the lower etch stop 122 and hard mask 124 layers as in Figure 6A. Then, as shown in Figure 7B, the stack

120 is etched to form at least one memory opening 81 in the stack 120 using RIE, similar to the step described above with respect to Figure 6B. The RIE step is followed by stripping the hard mask layer 124 by ashing or selective wet etching.

[0057] As shown in Figure 7C, the masking layer 234 is formed on a sidewall of the upper portion 81a of the at least one opening 81 in the upper portion 120a of the stack 120, similar to the step described above with respect to Figure 6B. Layer 234 is also formed on the upper surface of the stack 120.

[0058] Then, as shown in Figure 7D, an additional hard mask 244 is formed over a portion of the masking layer 234 located over the upper surface of the stack 120. The hard mask 244 is formed non-conformally such that it is formed only on the upper surface of the stack 120, but not in the openings 81. This forms hard mask openings 181 in the hard mask 244. The hard mask 244 may comprise an amorphous carbon hard mask.

[0059] The method then proceeds similar to the method illustrated in Figures 6D-6F. Specifically, the lower portion 81b of the at least one opening 81 is etched through the openings 181 in the additional hard mask 244 to widen the lower portion 81b of the at least one opening 81, as shown in Figure 7E. Finally, as shown in Figure 7F, layer 234 and the hard mask 244 are removed similar to the step described above with respect to Figure 6F.

[0060] In the above methods, amorphous carbon hard mask shape may be improved by an optional flash step. This may improve the masking layer deposition and memory opening profile.

[0061] The first and second embodiments described above contain doped semiconductor layers 121 which form the control gates 3 of the NAND strings, as shown in Figure 4. In alternative embodiments layers 121 may be sacrificial layers which are removed and replaced by conductive control gates 3, as shown in Figures 8A-8E.

[0062] A portion of the stack 120 containing insulating first layers 19 (e.g., 19a, 19b, etc.) and sacrificial second layers 121 (e.g., 121a, 121b, etc.) is shown in Figure 8A. The front side opening (i.e., the memory opening 81) is formed in the stack 120 using the method of the first or the second embodiment described above.

[0063] Next, in an optional step as shown in Figure 8B, the second material 121 is selectively etched compared to the first material 19 to form front side recesses 62 in the second material 121 (i.e., layers 121a, 121b, etc). The recesses 62 may be formed by selective, isotropic wet or dry etching which selectively etches the second material 121 compared to the first material 19. The depth of each recess 62 may be 3 to 20 nm. This step may be omitted if desired.

[0064] As shown in Figure 8C, a plurality of discrete semiconductor, metal or silicide charge storage regions 9 are selectively formed on portions of the second material layers 121 exposed in the front side opening 81. The charge storage regions 9 comprise a plurality of charge storage segments or regions (e.g., 9a and 9b) located on the exposed edges of the second material 121 in the front side recesses 62.

[0065] In one embodiment, the charge storage regions 9 are selectively formed by selective growth of the regions on the exposed edges of the semiconductor second material layers 121 but not on the exposed insulating first material layers 19. Any suitable selective growth methods may be used to form the charge storage regions 9, such as chemical vapor deposition.

[0066] In one aspect of the selective growth embodiment, charge storage regions 9 comprise doped polysilicon regions which are selectively grown by CVD on the portions of the undoped or intrinsic second material layers 121 (e.g., undoped or intrinsic semiconductor having a polycrystalline or amorphous structure, such as polysilicon, amorphous silicon,

silicon germanium or germanium) exposed in the front side opening 81. For example, the doped polysilicon regions 9 may comprise boron doped, p-type polysilicon regions (e.g., lightly or heavily doped) which are selectively, epitaxially grown on polysilicon layer 121 edges exposed in the front side openings 81. The doped polysilicon regions 9 are not grown on portions of the first material layers 19 (e.g., silicon oxide) exposed in the front side opening 81.

[0067] Any suitable silicon selective epitaxial growth (SEG) conditions may be used to form regions 9. For example, a chemical vapor deposition (CVD) SEG process which combines a silicon source gas and a silicon growth inhibitor gas which inhibits silicon growth on the oxide layers 19 may be used. Exemplary silicon source gases include silane and chloro-silanes (e.g., SiH_4, SiH_2Cl_2, and/or $SiHCl_3$). Exemplary inhibitor gases which inhibit silicon growth on SiO_2 include HCl and/or Cl_2. H_2 may be used as a carrier gas while B_2H_6, AsH_3 and/or PH_3 gases may be added to introduce dopants to the silicon regions 9. Any suitable SEG temperatures and pressures may be used, such as a temperature of 500 to 800C and a pressure of 10 mTorr to 100 Torr (i.e., LPCVD). Similar process conditions may be used to form germanium or silicon-germanium charge storage regions 9, where germane (GeH_4) is substituted for silane or provided in addition to silane, at lower temperatures (e.g., 340 to 380C) and pressure of about 10 mTorr -5 Torr, such as about 1 Torr.

[0068] In another aspect of the selective growth embodiment, charge storage regions 9 comprise selectively grown metal or silicide charge storage regions, such as on the portions of the second material layers exposed in the front side opening. Any metal (i.e., pure metal or conductive metal alloy) or metal silicide which may be selectively grown on exposed semiconductor layer 121 in the opening 81 may be used. For example, the charge storage

regions 9 may comprise selectively grown tungsten, molybdenum or tantalum regions that are selectively grown on the semiconductor material (e.g., silicon) 121 but not on insulating material (e.g., silicon oxide) 19 from a metal halide source gas (e.g., tungsten hexafluoride) in a CVD process.

[0069] Selective deposition of refractory metals, such as W, Mo or Ta, on silicon may be performed by metal halide source gas reduction by SiH_4, where a ratio of SiH_4 to metal halide is less than one. For example, as disclosed in U.S. patent numbers 5,084,417 and 5,807,788, incorporated herein by reference in their entirety, in the selective CVD process, the metal halide source gas may comprise WF_6, MoF_6 or $TaCl_5$ and the deposition temperature and pressure may range from 370 to 550C and 100 to 500 mTorr, respectively. The ratio of the SiH_4/metal halide flow rates may range between 0.4 and 0.6.

[0070] If the front side recesses 62 are present, then the regions 9 may be selectively grown in the front side recesses 62 until their edges are about even with the edges of the insulating material 19 such that they form a relatively straight sidewall of the front side opening 81 (e.g., as much as a timed selective growth permits). Alternatively, the selective growth of regions 9 is terminated before regions 9 completely fill the recesses 62. Thus, regions 9 may partially fill recesses 62 and may remain horizontally recessed in the opening 81 compared to insulating material layers 19. Alternatively, the selective growth of regions 9 is terminated after regions 9 completely fill the recesses 62 such that the regions 9 protrude horizontally into the front side opening 81 past layers 19, as shown in Figure 8C.

[0071] In another embodiment, the regions 9 are selectively formed by doping of the semiconductor layers 121 exposed in the front side opening 81. For example, when layers 121 comprise intrinsic or undoped semiconductor layers, a timed gas phase diffusion doping may be carried out to dope the edge portions 9 of layers 121 facing the opening 81 by

providing a doping gas through the opening 81. The doping is terminated before the entire volume of layers 121 are doped, such that portions of layers 121 located behind regions 9 and facing away from the opening 81 remain undoped. For example, for Group IV semiconductor material (e.g., silicon) layers 121, the doping gas may comprise a boron containing gas, such as diborane, to form p-type doped regions 9, or a phosphorus or arsenic containing gas, such as phosphine or arsene, to form n-type doped regions 9.

[0072] In the next step shown in Figure 8C, a tunnel dielectric layer 11 is deposited over the charge storage regions 9a, 9b and the insulating first material layers 19 between the charge storage regions in the front side opening 81. Then, the channel 1 is formed by depositing channel material 1, such as a lightly doped or intrinsic polysilicon over the tunnel dielectric layer 11 in the front side opening 81. If desired, a high temperature anneal may be performed after forming the channel.

[0073] As discussed above, the entire opening 81 may be filled to form the device illustrated in Figures 2A and 2B. Alternatively, a layer of channel material may first be deposited in the opening 81 followed by deposition of an insulating fill material 2 to form the device illustrated in Figures 1A and 1B. If desired, the channel 1 may be U-shaped as illustrated in Figure 3.

[0074] The channel 1 may be formed by filling the front side opening 81 with a lightly doped semiconductor material (e.g., polysilicon) and then etched back from the top to form the pillar shaped (or U-shaped) channel 1 in the opening 81. In the embodiment of Figure 3, the space between the wings of the U-channel 1 is filled with a gap fill insulating layer 103, such as silicon oxide or another material. Layer 103 may be formed by etching the stack 120 to form a rail shaped cut, followed by depositing an oxide layer followed by etch back or chemical mechanical polishing to form a planar top surface exposing the top surfaces of the

channels 1. The channels are then connected to source and drain electrodes 102, 202 as shown in Figures 1-3, the select gate electrodes (not shown for clarity) are connected to select gate contacts and the control gate electrodes 3 are connected to word line contacts as known in the art.

[0075] In the next step shown in Figure 8D, the stack 120 is patterned to form one or more back side openings 84 in the stack. The back side opening(s) 84 may be formed by photolithography and anisotropic etching of the stack. Preferably, the opening(s) 84 have a slit trench shape.

[0076] Then, at least a portion of the second material layers 121 are removed through the back side opening 84 to form back side recesses 64 between the first material layers 19. For example, layers 121 may be removed completely by selective wet etching using a liquid etching medium which selectively etches the material of layers 121 compared to the materials of layers 19 and regions 9. For example, if layers 121 comprise undoped or intrinsic polysilicon, layers 19 comprise silicon oxide and regions 9 comprise doped polysilicon, silicide or metal, then an undoped polysilicon selective etch may be used which stops on doped polysilicon (e.g., p-type polysilicon) regions 9 which act as an etch stop. Alternatively, the selective etch may be a timed etch which is timed to remove only a portion of the sacrificial second material layers 121 through the back side opening 84. In this case, a remaining portion of the second material layers 121 rather than regions 9 remain exposed in the back side recesses 64.

[0077] Then, as shown in Figure 8E, the blocking dielectric layer 7 (also known as an inter-poly dielectric, IPD) is then formed in the back side recesses 64 through the back side opening 84 such that the blocking dielectric coats the sides of the back side recesses 64 and the back side of layers 19 exposed in the back side opening 84. The blocking dielectric layer

7 may comprise a silicon oxide layer deposited by conformal atomic layer deposition (ALD) or chemical vapor deposition (CVD). Other high-k dielectric materials, such as hafnium oxide, aluminum oxide, or multi-layer dielectrics (e.g., ONO) may be used instead or in addition to silicon oxide. Optionally, an insulating capping layer (e.g., silicon nitride) may be deposited into the openings before the blocking dielectric 7 and may comprise a back portion of a multi-layer blocking dielectric. The blocking dielectric 7 may have a thickness of 6 to 20 nm. An optional anneal, such as a rapid thermal anneal, may be conducted after the blocking dielectric formation.

[0078] The blocking dielectric layer 7 comprises a plurality of clam-shaped blocking dielectric segments 7a, 7b in the back side recesses 64 connected to each other by vertical portions 7c of the blocking dielectric layer 7 located on the exposed edges of the first material layers 19 in the back side opening 84. As used herein a "clam" shape is a side cross sectional shape configured similar to an English letter "C". A clam shape has two segments which extend substantially parallel to each other and to the major surface 100a of the substrate 100. The two segments are connected to each other by a third segment which extends substantially perpendicular to the first two segments and the surface 100a. Each of the three segments may have a straight shape (e.g., a rectangle side cross sectional shape) or a somewhat curved shape (e.g., rising and falling with the curvature of the underlying topography). The term substantially parallel includes exactly parallel segments as well as segments which deviate by 20 degrees or less from the exact parallel configuration. The term substantially perpendicular includes exactly perpendicular segments as well as segments which deviate by 20 degrees or less from the exact perpendicular configuration. The clam shape preferably contains an opening bounded by the three segments and having a fourth side open.

[0079] The opening in the clam shaped blocking dielectric segments is then filled by a control gate 3 material. As described above, the control gate material may comprise a thin barrier layer/adhesion layer such as titanium nitride or tungsten nitride and metal, such as tungsten or a combination of tungsten and titanium nitride layers. The control gate material may be deposited by CVD and fills the remaining volume of the back side recesses 64 inside the clam shaped blocking dielectric 7 segments and the entire back side opening 84. The deposition of the control gate material is followed by etching the control gate material to remove it from the back side opening 84 using anisotropic etching, while leaving the control gate material inside the back side recesses 64 in the clam shaped blocking dielectric 7 segments. The remaining control gate material inside the back side recesses 64 forms the control gates 3 of the vertical NAND string.

[0080] While the formation of the high aspect ratio openings was described above with respect to forming memory openings 81 for a vertical NAND string, the methods described above may be applied to any other suitable device. For example, the methods of the first or the second embodiments described above may be used to form any high aspect ratio opening, such as trenches, slits, holes, spaces between mesas or pillars, or other three dimensional shapes in any memory, logic or other semiconductor device.

[0081] Although the foregoing refers to particular preferred embodiments, it will be understood that the invention is not so limited. It will occur to those of ordinary skill in the art that various modifications may be made to the disclosed embodiments and that such modifications are intended to be within the scope of the invention. All of the publications, patent applications and patents cited herein are incorporated herein by reference in their entirety.

WHAT IS CLAIMED IS:

1. A method of making a semiconductor device, comprising:

forming a stack of alternating layers of a first material and a second material over a substrate;

etching the stack to form at least one opening extending partially through the stack;

forming a masking layer on a sidewall and bottom surface of the at least one opening;

removing the masking layer from the bottom surface of the at least one opening while leaving the masking layer on the sidewall of the at least one opening; and

further etching the at least one opening to extend the at least one opening further through the stack while the masking layer remains on the sidewall of the at least one opening.

2. The method of claim 1, wherein removing the masking layer from the bottom surface of the at least one opening comprises using directional reactive ion etching to remove the masking layer from the bottom surface of the at least one opening.

3. The method of claim 1, wherein the masking layer comprises a conformal masking layer.

4. The method of claim 3, wherein the conformal masking layer comprises an amorphous carbon, silicon nitride, silicon oxide, metal oxide or metal nitride masking layer.

5. The method of claim 1, further comprising removing the masking layer from the sidewall of the at least one opening after the step of further etching.

6. The method of claim 5, wherein the masking layer comprises an amorphous carbon masking layer and the step of removing the masking layer from the sidewall comprises ashing the amorphous carbon masking layer.

7. The method of claim 5, wherein the step of removing the masking layer from the sidewall comprises selectively wet etching the masking layer.

8. The method of claim 1, further comprising:

forming a first etch stop layer between a lower portion and an upper portion of the stack;

forming a second etch stop layer under the stack;

forming a hard mask over the stack; and

patterning the hard mask to form at least one hard mask opening which exposes the stack;

wherein etching the stack comprises etching the stack through the at least one hard mask opening to form at least one opening extending partially through the upper portion of the stack to the first etch stop layer;

wherein forming the masking layer comprises forming the masking layer over an upper surface of the hard mask in addition to forming the masking layer on the sidewall and the bottom surface of the at least one opening; and

wherein further etching comprises further etching the at least one opening to extend the at least one opening further through the first etch stop layer and through the lower portion of the stack to the second etch stop layer while the masking layer remains on the sidewall of the at least one opening.

9. The method of claim 1, further comprising:

forming a blocking dielectric in the at least one opening;

forming a charge storage layer over the blocking dielectric;

forming a tunnel dielectric over the charge storage layer; and

forming a semiconductor channel over the tunnel dielectric in the at least one opening.

10. The method of claim 9, wherein:

the semiconductor device comprises a monolithic three dimensional NAND string;

the first material comprises a conductive or semiconductor control gate material; and

the second material comprises an insulating material.

11. A method of making a semiconductor device, comprising:

forming a stack of alternating layers of a first material and a second material over a substrate;

etching the stack to form at least one opening in the stack, the at least one opening comprising a tapered opening having an upper portion which is wider than a lower portion;

forming a masking layer on a sidewall of the upper portion of the at least one opening while the lower portion of the at least one opening is not covered by the masking layer; and

further etching the lower portion of the at least one opening to widen the lower portion of the at least one opening while the masking layer remains on the sidewall of the upper portion of the at least one opening.

12. The method of claim 11, wherein:

the step of etching the stack comprises using reactive ion etching; and

the step of further etching comprises wet etching or reactive ion etching the first and second material layers of the stack exposed in the lower portion of the at least one opening while the masking layer protects the first and the second material layers in the upper portion of the opening from the further etching.

13. The method of claim 11, wherein the masking layer comprises a non-conformal sidewall spacer.

14. The method of claim 13, wherein the masking layer comprises an amorphous carbon, silicon nitride, silicon oxide, metal oxide or metal nitride masking layer.

15. The method of claim 11, further comprising removing the masking layer from the sidewall of the at least one opening.

16. The method of claim 15, wherein the masking layer comprises an amorphous carbon masking layer and the step of removing the masking layer from the sidewall comprises ashing the amorphous carbon masking layer.

17. The method of claim 15, wherein the step of removing the masking layer from the sidewall comprises selectively wet etching the masking layer.

18. The method of claim 11, further comprising:

forming an etch stop layer under the stack;

forming a hard mask over the stack; and

patterning the hard mask to form at least one hard mask opening which exposes the stack;

wherein etching the stack comprises etching the stack through the at least one hard mask opening to form the at least one opening extending through the entire stack to the etch stop layer; and

wherein forming the masking layer comprises forming the masking layer over an upper surface of the hard mask in addition to forming the masking layer on the sidewall of the upper portion of the at least one opening.

19. The method of claim 11, further comprising:

forming a blocking dielectric in the at least one opening;

forming a charge storage layer over the blocking dielectric;

forming a tunnel dielectric over the charge storage layer; and

forming a semiconductor channel over the tunnel dielectric in the at least one opening.

20. The method of claim 19, wherein:

the semiconductor device comprises a monolithic three dimensional NAND string;

the first material comprises a conductive or semiconductor control gate material; and

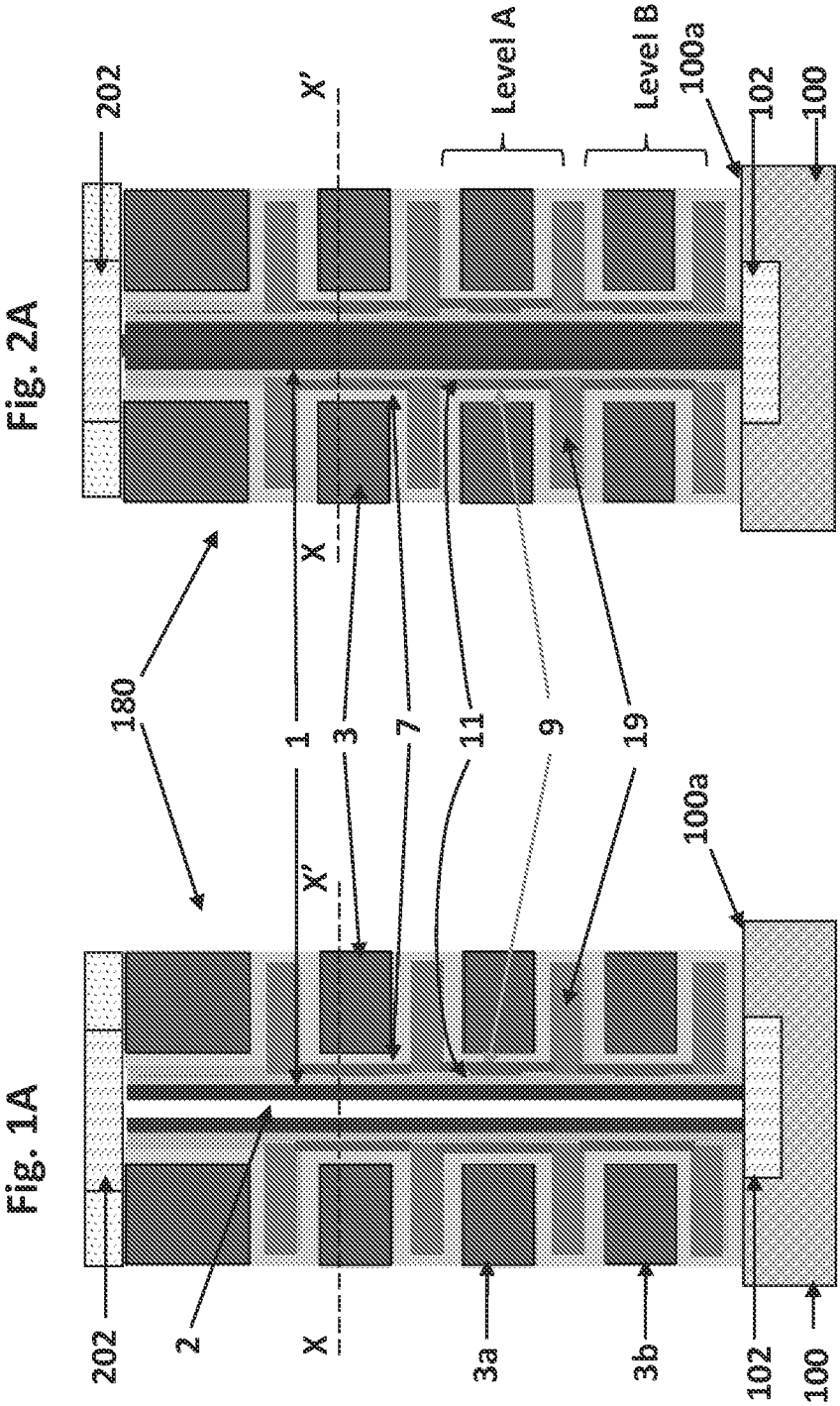
the second material comprises an insulating material.

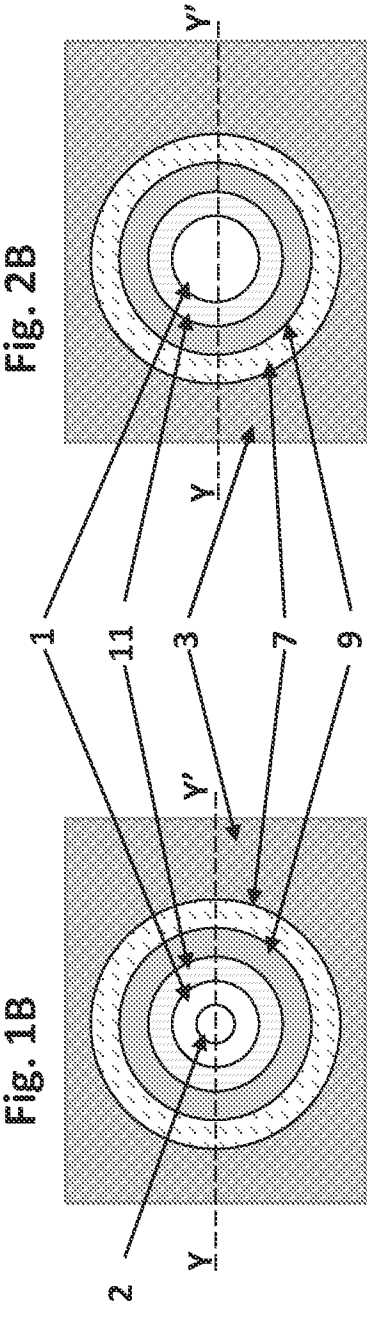
21. The method of claim 11, further comprising:

forming the masking layer over an upper surface of the stack in addition to forming the masking layer on the sidewall of the upper portion of the at least one opening; and

forming an additional hard mask over a portion of the masking layer located over the upper surface of the stack;

wherein further etching comprises further etching the lower portion of the at least one opening through the additional hard mask to widen the lower portion of the at least one opening.


Fig. 2A
202
X'
Level A
Level B
100a
102
100
180
X
1
3
7
11
9
19
Fig. 1A
202
2
X
3a
3b
102
100
100a
X'


Fig. 2B
Y'
Y
1
11
3
7
9
Fig. 1B
Y'
Y
2

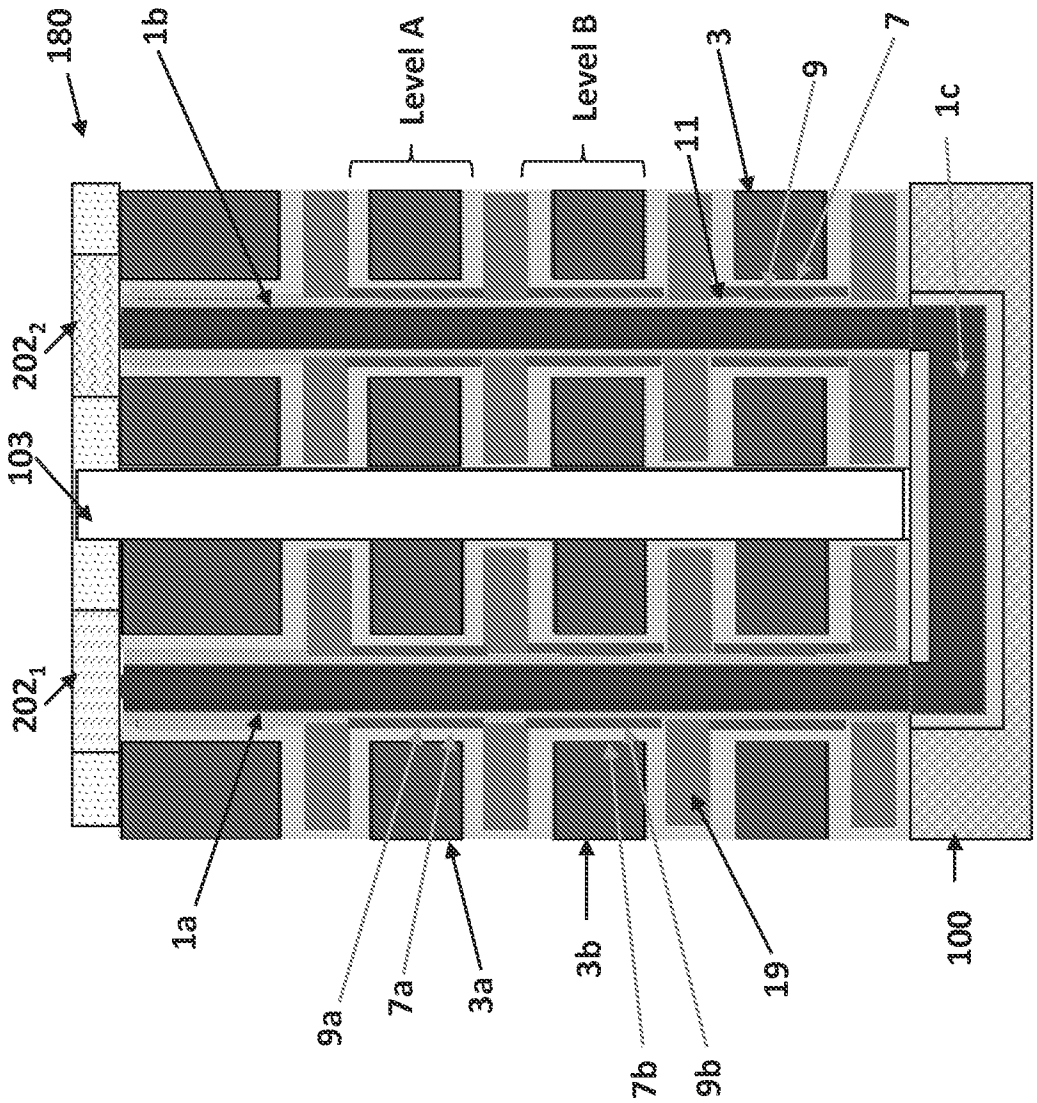

180
1b
Level A
Level B
3
9
7
11
1c
202_2
103
202_1
1a
9a
7a
3a
3b
7b
9b
19
100

Fig. 3

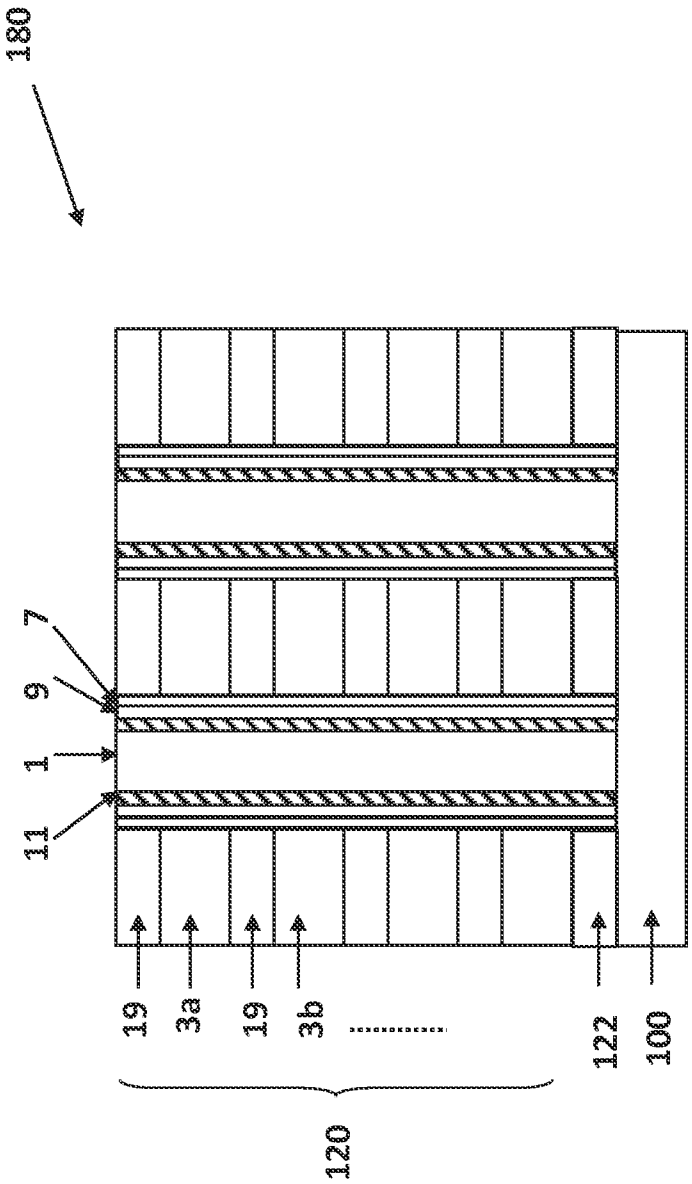


Fig. 4

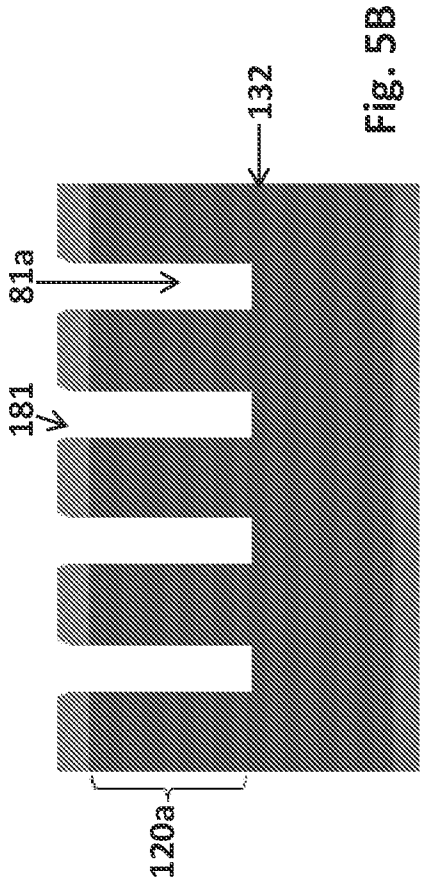


Fig. 5B

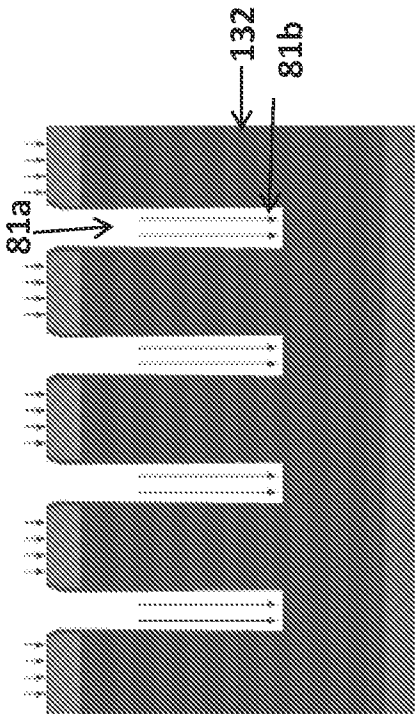


Fig. 5D

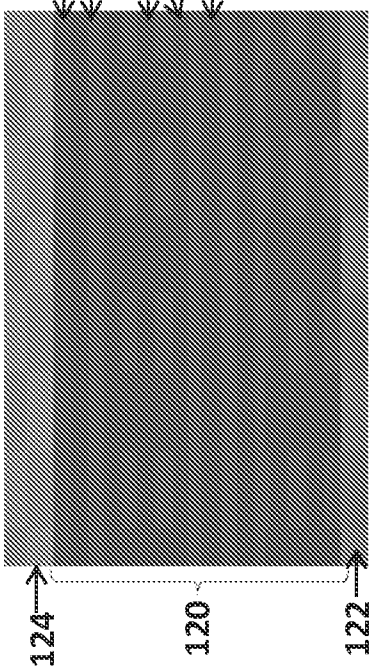


Fig. 5A

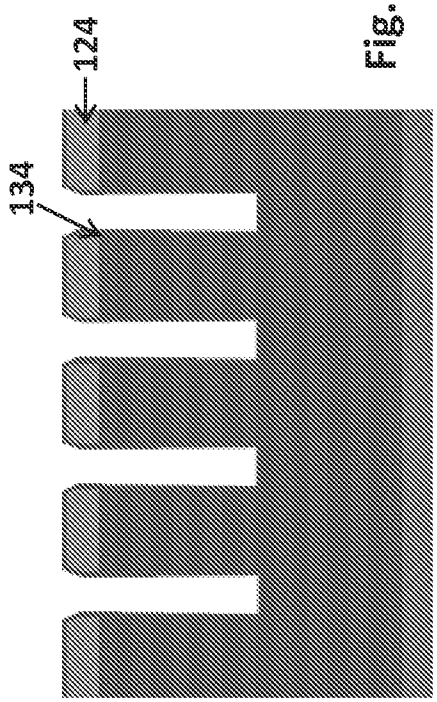


Fig. 5C

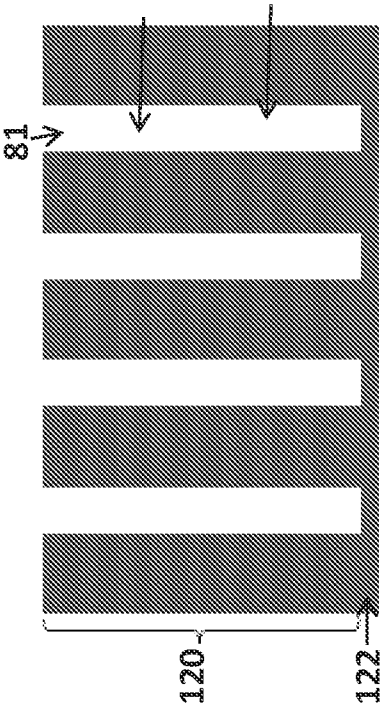


Fig. 5E

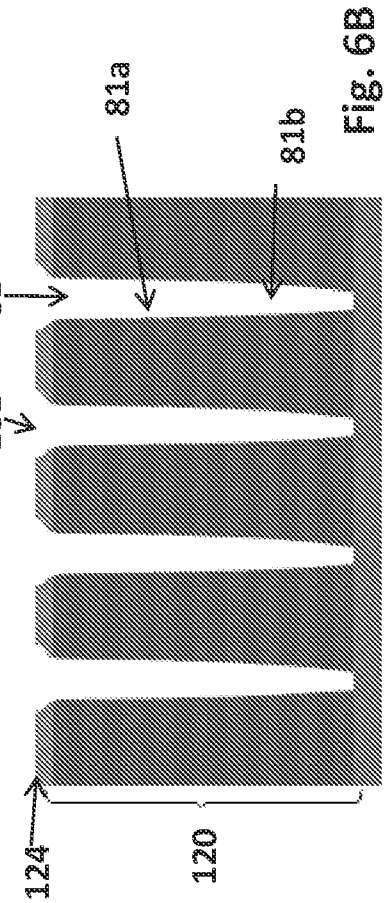


Fig. 6B

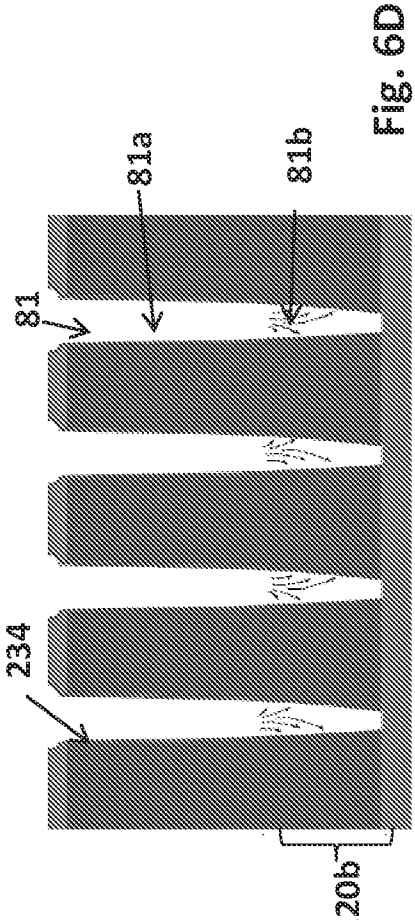


Fig. 6D

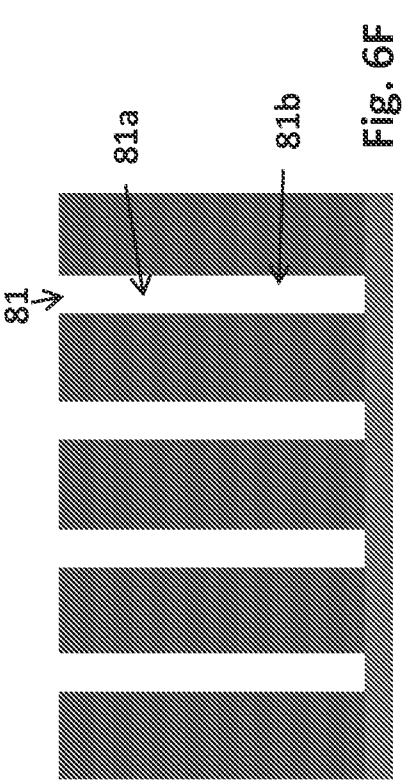


Fig. 6F

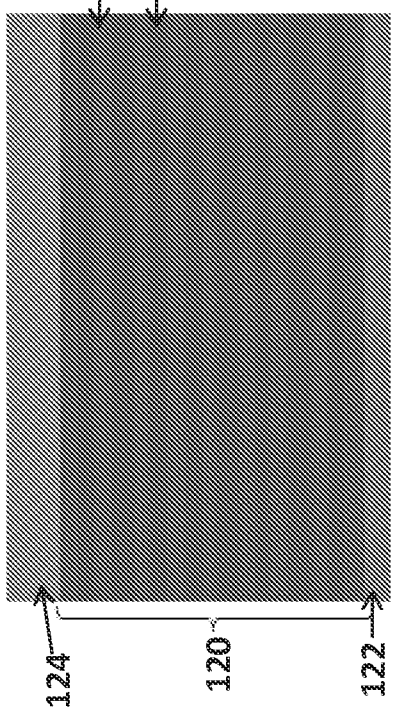


Fig. 6A

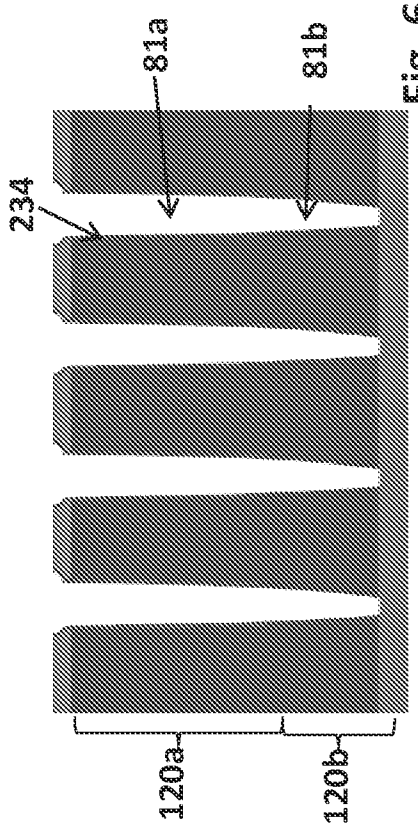


Fig. 6C

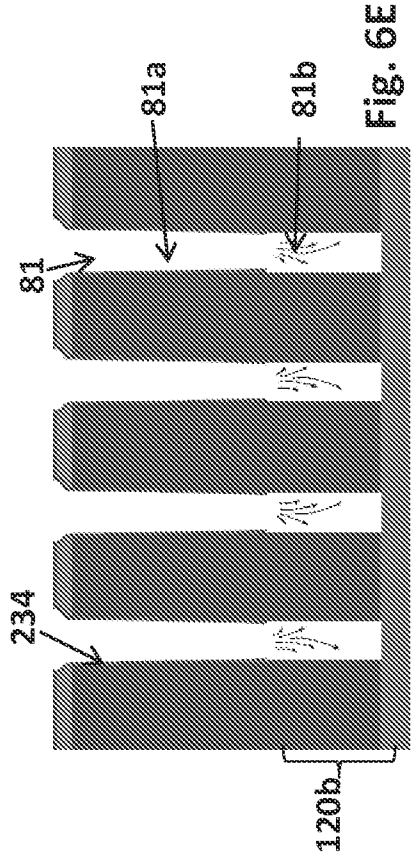


Fig. 6E

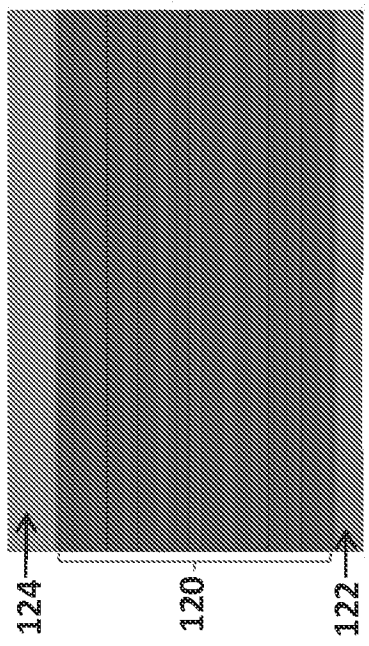


Fig. 7A

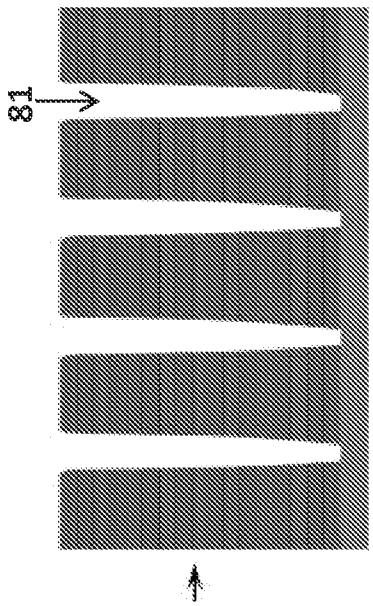


Fig. 7B

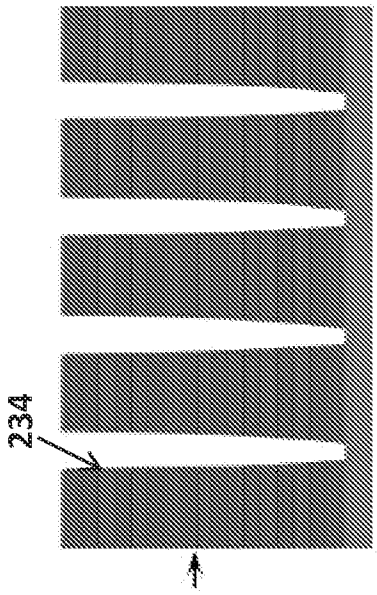


Fig. 7C

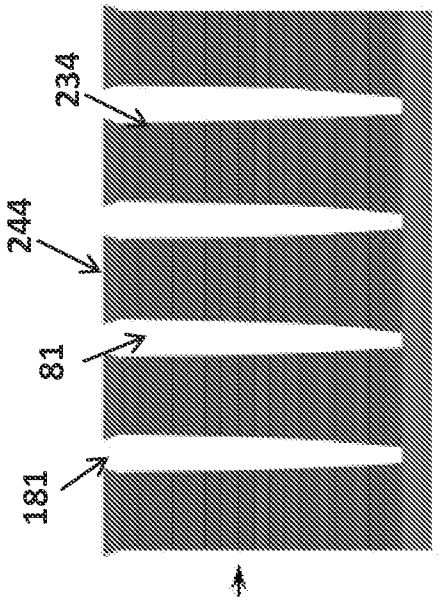


Fig. 7D

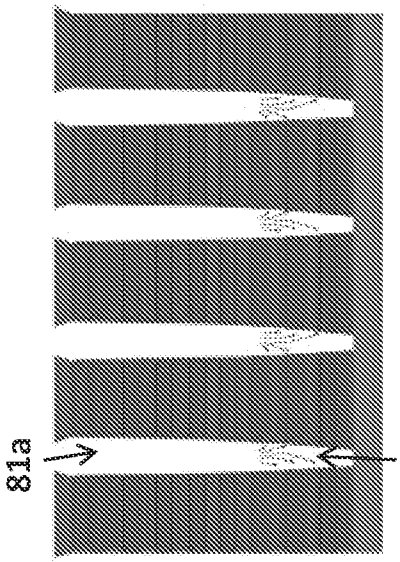


Fig. 7E

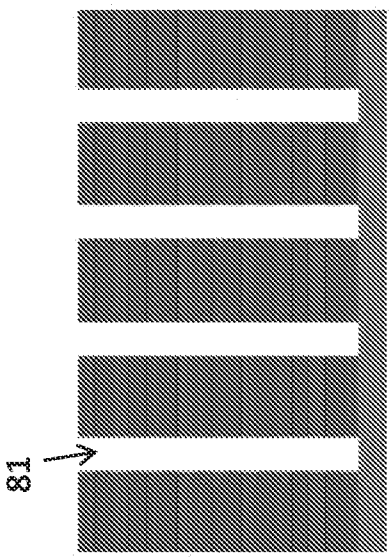


Fig. 7F

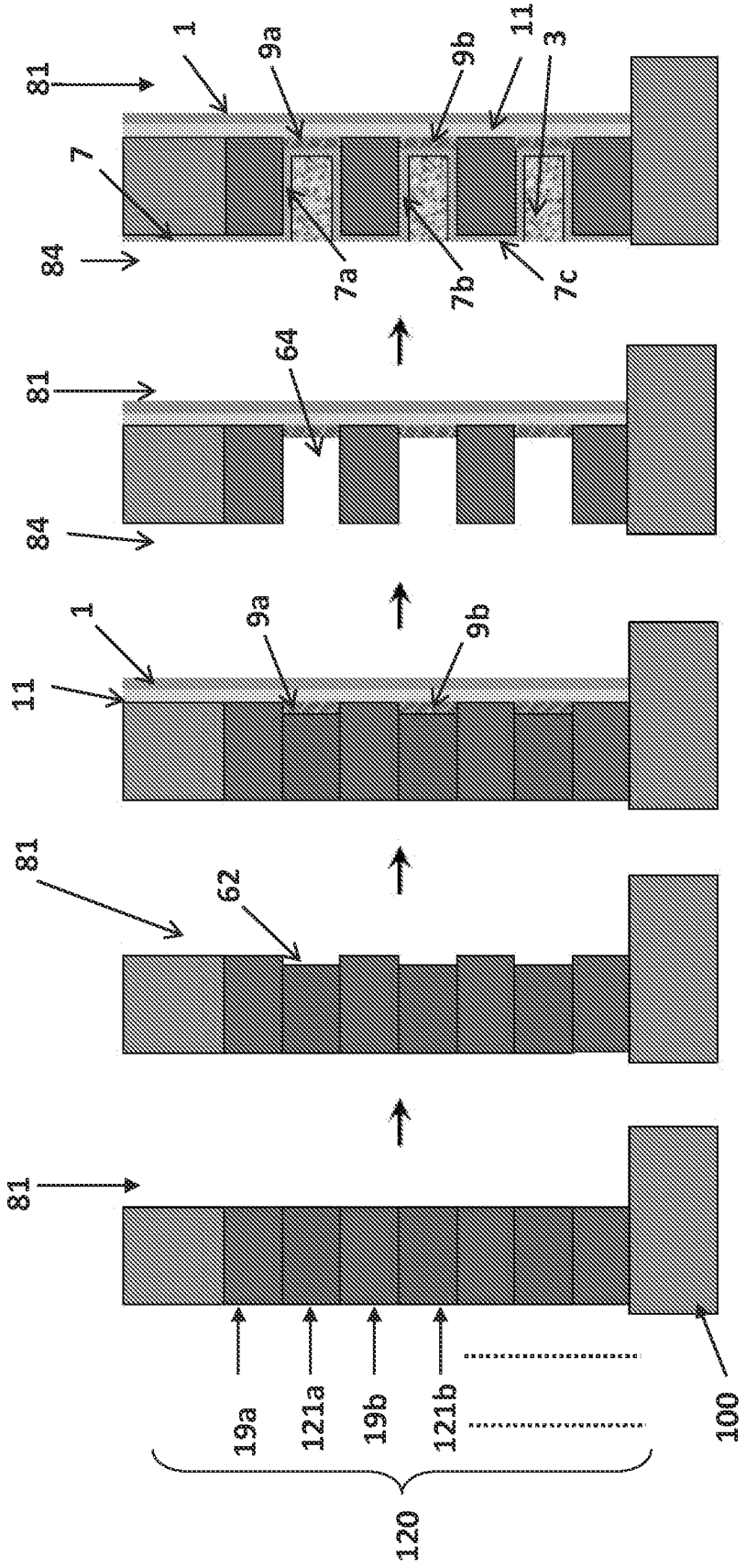


Fig. 8E

Fig. 8D

Fig. 8C

Fig. 8B

Fig. 8A

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/032123

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L27/115
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2012/146127 A1 (LEE KI-HONG [KR] ET AL) 14 June 2012 (2012-06-14) paragraphs [0052] - [0078]; figures 3A-3K	1-10
X	US 2009/283819 A1 (ISHIKAWA MASAO [JP] ET AL) 19 November 2009 (2009-11-19) paragraphs [0019] - [0051]; figures 1-8	1-3,5-10
X	WO 2012/003301 A2 (SANDISK TECHNOLOGIES INC [US]; ALSMEIER JOHANN [US]; PURAYATH VINOD [U) 5 January 2012 (2012-01-05) page 22, line 25 - page 25, line 17; figures 23-27	1-4,9,10
X	US 2012/156848 A1 (YANG SANG-RYOL [KR] ET AL) 21 June 2012 (2012-06-21) paragraphs [0063] - [0122]; figures 4A,4B, 5, 6A-6H	11-21

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 September 2014	22/09/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Ley, Marc

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/032123

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☒ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-10

A method of making a semiconductor device, comprising: forming a stack of alternating layers of a first material and a second material over a substrate;etching the stack to form at least one opening extending partially through the stack;forming a masking layer on a sidewall and bottom surface of the at least one opening;removing the masking layer from the bottom surface of the at least one opening while leaving the masking layer on the sidewall of the at least one opening; andfurther etching the at least one opening to extend the at least one opening further through the stack while the masking layer remains on the sidewall of the at least one opening.

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2. claims: 11-21

A method of making a semiconductor device, comprising: forming a stack of alternating layers of a first material and a second material over a substrate;etching the stack to form at least one opening in the stack, the at least one opening comprising a tapered opening having an upper portion which is wider than a lower portion;forming a masking layer on a sidewall of the upper portion of the at least one opening while the lower portion of the at least one opening is not covered by the masking layer; and further etching the lower portion of the at least one opening to widen the lower portion of the at least one opening while the masking layer remains on the sidewall of the upper portion of the at least one opening.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2014/032123

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012146127 A1	14-06-2012	NONE	
US 2009283819 A1	19-11-2009	JP 2009277770 A	26-11-2009
		US 2009283819 A1	19-11-2009
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		EP 2589070 A2	08-05-2013
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		TW 201214631 A	01-04-2012
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