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(21) Application No. 51153/76 (22) Filed 8 Dec. 1976
 (31) Convention Application No. 7 537 552
 (32) Filed 9 Dec. 1975 in
 (33) France (FR)
 (44) Complete Specification published 18 June 1980
 (51) INT CL³ H03K 4/56, 4/00
 (52) Index at acceptance H3T 2B2 2B3 2E 2T3F 3F1 3J 3N 3V LV
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(54) VARIABLE TIME BASE CONTROL CIRCUITS FOR
 OSCILLOSCOPES

(71) We COMPTEURS SCHLUMBERGER, 12 Place des Etats-Unis, 92120 Montrouge, France, a French body corporate, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

5 This invention relates to variable time-base control circuits for oscilloscopes.

10 The most commonly met oscilloscope time-base control circuit is based on a Miller integrator, which comprises a high gain amplifier, a resistance connected between a fixed reference voltage and the input of the amplifier, and a capacitance negative feedback connected between the output and the input of the amplifier. As the 15 capacitance commences to charge, the output voltage V_s at the output of the amplifier increases linearly at a rate given by $dV_s/dt = V_{ref}/RC$, where V_{ref} is the reference voltage and R and C are the 20 respective values of the resistance and the capacitance. When the voltage V_s reaches a predetermined level, a reset circuit rapidly 25 discharges the capacitance, which then commences to charge again. The integrator 30 thus produces, at the output of the amplifier, an output voltage of sawtooth waveform, the slope of the flanks of this sawtooth waveform determining the time-base of the oscilloscope, i.e. the horizontal 35 scanning rate of the electron beam in the cathode ray tube of the oscilloscope.

In order to vary the time-base of the 40 oscilloscope, the respective values of the resistance and the capacitance in the integrator are selectively varied. Typically, this is achieved by providing a plurality of resistors and capacitors of different values, and a switch for connecting different ones, or different combinations of, these resistors 45 and capacitors into the circuit of the integrator. The switch is normally a multi-position, multipole rotary switch mounted on the front panel of the oscilloscope, and

connected to the integrator by a large number of wires.

50 The use of such a switch has several disadvantages. Firstly, during manufacture of the oscilloscope, the connection of the switch to the integrator by means of a large number of wires is time-consuming, and therefore contributes significantly to the manufacturing costs. Additionally, the wires themselves introduce stray capacitances, which can cause stability problems, while the large number of contacts in the switch has an adverse effect on reliability. Furthermore, the use of such a switch substantially precludes the possibility of making the oscilloscope electronically programmable.

55 It is an object of the present invention to provide a variable time-base control circuit for an oscilloscope, in which the above-mentioned disadvantages are substantially alleviated.

60 It is a further object of the invention to provide such a time-base control circuit which is particularly suitable for electronically programmable operation.

65 According to the present invention, therefore, there is provided a variable time-base control circuit for an oscilloscope, the circuit comprising:

a reference voltage source;
 an integrator arranged to receive and integrate the reference voltage produced by the source so as to periodically produce a ramp voltage whose slope determines the time-base of the oscilloscope, the integrator comprising a high gain amplifier, resistance means connected between the reference voltage source and the input of the amplifier, capacitance means negative-feedback connected between the output and the input of the amplifier, at least one of the resistance means and the capacitance means being switchably variable in value, and reset means for resetting the integrator to an initial state each time said ramp voltage reaches a predetermined level; and switch means for varying the value of said at least one of the resistance means and the

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5 capacitance means, whereby to vary the slope of said ramp voltage; wherein the switch means comprises at least one semi-conductor switching device, connected in the integrator in such a manner that when the or each switching device is in a conductive state, either it passes substantially no current at least throughout the production of each ramp voltage or it passes a substantially constant current at least throughout the production of each ramp voltage.

10 Thus the or each semiconductor switching device, which advantageously 15 comprises a MOSFET, can be implemented together with a substantial part of the remainder of the circuit as a single integrated circuit, thereby reducing manufacturing costs; further the use of one or 20 more semiconductor switching devices makes the circuit particularly suitable for electronically programmable operation.

25 The invention will now be described, by way of non-limitative example, with reference to the accompanying drawings, of which:

30 Figure 1 is a simplified block circuit diagram of a variable time-base control circuit in accordance with the present invention for use in an oscilloscope.

35 Figure 2 is a diagram showing the voltage waveforms which appear at two points in the circuit of Figure 1;

40 Figure 3 is an equivalent diagram of a semiconductor switching device forming part of the circuit of Figure 1;

45 Figure 4 is a block circuit diagram of a control system for controlling the circuit of Figure 1.

50 The variable time-base control circuit illustrated in Figure 1 is indicated generally at 10, and comprises a high gain inverting amplifier 12 having an input 14 and an output 16. The output 16 of the amplifier 12 is connected to one terminal of each of two capacitors C1 and C2 of different value, and to one input 18 of a voltage comparator 20. The second input 22 of the comparator 20 is connected to receive a positive reference voltage from a voltage source 24, while the output 26 is connected to the reset input 28 of a bistable circuit 30. The set input 32 of the bistable circuit 30 is connected to receive a trigger signal from a trigger circuit 55 (not shown) of the oscilloscope, while the \bar{Q} (or reset) output 34 thereof is connected to the anode of a diode D1.

60 The other terminal of each of the capacitors C1 and C2 is connected to the input 14 of the amplifier via a respective one of two semiconductor switching devices $\alpha 1$ and $\alpha 2$, and to the cathode of the diode D1 via a respective one of two semiconductors switching devices $\beta 1$ and $\beta 2$. The other 65 terminal of the capacitor C1 is also

connected via respective semiconductor switching devices $\gamma 11$ and $\gamma 12$ to one end of each of two resistors R1 and R2 of different value, while the other terminal of the capacitor C2 is connected via respective semiconductor switching devices $\gamma 21$ and $\gamma 22$ to these same ends of the resistors R1 and R2. These same ends of the resistors R1 and R2 are also connected via respective semiconductor switching devices $\delta 1$ and $\delta 2$ to earth, while the other end of each of the resistors R1 and R2 is connected to receive a negative reference voltage from a voltage source 36. ..

70 The output 16 of the amplifier 12 is connected via a suitable power amplifier (not shown) to the horizontal - or X - deflection plates of the cathode ray tube of the oscilloscope in known manner to control the time-base, i.e. the horizontal scanning rate of the electron beam in the cathode ray tube, of the oscilloscope.

75 Each of the semiconductor switching devices α , β , γ and δ preferably comprises a respective insulated gate field effect transistor (MOSFET).

80 It will be appreciated that by rendering conductive an appropriate combination of the switching devices α and γ , either one of the capacitors C1 and C2 can be selectively 85 negative-feedback connected round the amplifier 12, and either one of the resistors R1 and R2 can be selectively connected to the input 14 of the amplifier 12, so as to 90 form an integrator. The possible combinations of the switching devices α and γ , which combinations are selected by a 95 control system to be described hereinafter with reference to Figure 4, are shown in the following table:

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Table

Switching devices rendered conductive	Capacitor and resistor selected
$\alpha 1$ and $\gamma 11$	C1 and R1
$\alpha 1$ and $\gamma 12$	C1 and R2
$\alpha 2$ and $\gamma 21$	C2 and R1
$\alpha 2$ and $\gamma 22$	C2 and R2

110 The integrator thus formed integrates the negative reference voltage from the source 36 to produce at the output 16 of the amplifier 12 a linear positive-going ramp voltage V_s whose slope dV_s/dt is given by $dV_s/dt = V_{ref}/RC$, where V_{ref} is the voltage source 36 and R and C are the respective values of the particular capacitor and resistor selected by the switching devices α and γ .

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5 The switching devices β_1 and β_2 are arranged to be conductive concurrently with the switching devices α_1 and α_2 respectively. The switching device δ_1 is arranged to be rendered conductive concurrently with the switching devices γ_12 or γ_22 , while the switching device δ_2 is arranged to be rendered conductive concurrently with the switching devices γ_{11} or γ_{21} , in order to ensure that the voltage applied to the switching devices γ which are not conductive (i.e. the switching devices associated with whichever of the resistors R1, R2 is not selected) is relatively small.

10 15 The switching devices β and δ are also controlled by the control system of Figure 4.

Assuming that the bistable circuit 30 is initially in its reset state, the voltage at the Q output 34 thereof is positive, as shown at 40 in Figure 2(a), and is therefore operative to forward bias the diode D1 and clamp the voltage at the input 14 of the amplifier 12 at a level which saturates the amplifier 12. The output voltage V_s is thus held at a low, possibly negative level, as shown at 42 in Figure 2(b). The application of a suitable trigger signal to the set input 32 of the bistable circuit 30 causes the voltage at the Q output thereof to fall to its low value, as shown at 44 in Figure 2(a). The diode D1 thus becomes reverse-biased, releasing the voltage at the input 14 of the amplifier 12. The aforementioned integration of the reference voltage produced by the source 36 therefore commences, and the voltage V_s increases linearly, as shown at 46 in Figure 2(b), at a rate determined as described above.

40 When the voltage V_s reaches equality with the voltage produced by the source 24, the comparator 20 produces an output signal which resets the bistable circuit 30, as shown at 48 in Figure 2(a). The diode D1 again becomes forward-biased, and the voltage V_s rapidly returns to its initial low level, as shown at 50 in Figure 2(b), and remains there until the next successive trigger signal causes the whole sequence of events described above to be repeated. The circuit 10 thus produces at the output 16 of the amplifier 12 an output voltage of sawtooth waveform. The slope of the positive-going flanks of this sawtooth output voltage has four possible values, selectable by means of the switching devices α and γ , and is operative to determine the time base of the oscilloscope.

60 65 The switching devices α , β , γ and δ are all connected in the integrator formed by the amplifier 12 and the selected combination of the capacitors C1, C2 and the resistors R1, R2 in such a manner that, when they are in a conductive state, their respective resistances R_{on} , which vary with the current passing through the devices, have substan-

tially no effect on the slope of the positive-going flanks of the sawtooth output voltage produced by the circuit 10.

70 Thus the switching devices α are connected directly in series with the input 14 of the amplifier 12, which normally has an extremely high input impedance. It is possible that the switching devices α may slightly retard the start of the positive-going flanks of the sawtooth output voltage, but this retardation can be substantially eliminated by increasing the speed of response of the amplifier 12.

75 80 The switching devices β pass a current only during the return (or negative-going) flanks of the sawtooth output voltage produced by the circuit 10. Since the voltage on the terminal of the selected one of the capacitors C1, C2 connected to the respective switching device in use is maintained constant by the negative feedback loop round the amplifier 12, an abrupt step at the start of the positive-going flanks of the sawtooth output voltage, due to the disappearance of the current in the respective switching device β , is avoided.

85 90 The switching devices γ are connected in series with respective ones of the resistors R1 and R2, and therefore pass a constant current. The variations of their respective resistances R_{on} are therefore negligible.

95 100 Finally, the switching devices δ , as already mentioned, serve to connect one end of the resistor R1 or R2 which is not selected for connection to the integrator to earth, and therefore do not affect the operation of the integrator.

105 110 Thus to summarise, during the positive-going flanks of the sawtooth output voltage produced by the circuit 10, the switching devices α , β and γ pass either a substantially zero current (devices α , β) or a substantially constant current (devices γ), while the switching device δ which is conductive at any instant is associated with the non-selected one of the resistors R1, R2.

115 120 The circuit 10 is shown with two capacitors C1 and C2 and two resistors R1, and R2 merely for the sake of clarity. In general there can be M capacitors and N resistors, in which case there will be M switching devices α , M switching devices β , MN switching devices γ and N switching devices δ , all arranged in a manner exactly analogous to that shown in Figure 1.

125 130 The switching devices α , β , γ and δ are preferably implemented, together with the aforementioned control system, as a single large scale integrated circuit on a common substrate. In this case, since each of the MOSFET switching devices α , β , γ and δ has an equivalent circuit of the form shown in Figure 3 and therefore includes respective diodes D2 and D3 connecting its source terminal S and its drain terminal D to the

substrate, care must be taken to ensure that none of these substrate diodes is inadvertently rendered conductive when its respective switching device is intended to be non-conductive. To this end, the circuit 10 can be arranged to produce a negative-going sawtooth output voltage. This is achieved by interchanging the respective polarities of the voltage sources 24 and 36, reversing the connection of the diode D1, and arranging the bistable circuit 30 to produce a negative voltage at its Q output 34 when in its reset state.

Under certain circumstances, the switching devices β can cause minor problems, in particular by slowing down the return portion of the sawtooth output voltage or by distorting the first cycle of the sawtooth output voltage after a change of time-base. These problems can be alleviated by arranging the switching devices β to open before, and close after, the corresponding switching devices α and γ , during each change of time-base. Alternatively, and particularly for high rates of increase of the leading edge of the sawtooth output voltage, the switches β can be replaced by respective diode gates (thus rendering the diode D1 unnecessary), the direction in which these diodes are connected depending on the polarity of the sawtooth output being produced: for example, in the circuit 10 of Figure 1, a respective diode oriented in the same direction as the diode D1 would replace each of the switching devices β_1 and β_2 , and the diode D1 would be omitted.

The control system for controlling the switching devices α , β , γ and δ is indicated generally at 60 in Figure 4, and comprises a variable frequency clock pulse generator 62 whose frequency is manually adjustable by means of a variable resistor RV1 over a typical range of 1 to 2Hz. The pulses produced by the generator 62 are applied to a three-position manually operable switch 64, which is mounted on the front panel of the oscilloscope. The switch 64 has a first position in which the pulses are transmitted to the forward count input 66 of a reversible counter 68, a second position in which the pulses are transmitted to the reverse count input 70 of the counter 68, and a third or neutral position (illustrated in Figure 1) in which the pulses are not transmitted to the counter 68. The user of the oscilloscope can therefore change the count in the counter 68 upwardly or downwardly at will by means of the switch 64.

Each possible value of the count in the counter 68 is arranged to correspond to a respective time-base or horizontal scanning rate of the oscilloscope, preferably in a logical sequence, e.g. a sequence in which increasing count values correspond to

increasing horizontal scanning rates. The count outputs 72 of the counter 68 are connected to a set of multiplexing gates 74, having a first state in which they connect the outputs 72 to the common inputs 76 of first and second decoders 78, 80. Each of the decoders 78, 80 may conveniently be constituted by a respective read-only memory (ROM). The decoder 78 has a plurality of outputs 82 each connected to a respective one of the switching devices α , β , γ and δ , and decodes the count applied thereto via the gates 74 so as to produce at its outputs 82 a combination of energising signals which will render conductive that combination of the switching devices α , β , γ and δ which causes the circuit 10 to produce the horizontal scanning rate corresponding to the count in the counter 68. The decoder 80 similarly has a plurality of outputs 84, which are connected via respective buffer amplifiers 86 to a display unit (not shown) forming part of the oscilloscope, and decodes the count applied thereto via the gates 74 so as to produce at its outputs 84 the correct energising signals for causing the display unit to display to the user of the oscilloscope the horizontal scanning rate corresponding to the count in the counter 68. The display unit may take the form of a plurality of annunciator lights on the front panel of the oscilloscope, each of which corresponds to a respective horizontal scanning rate of the oscilloscope, or it may comprise means for displaying the currently-selected horizontal scanning rate directly on the screen of the cathode ray tube of the oscilloscope.

The control system 60 also includes a set of programmable inputs 88, whereby a digital control signal corresponding to any of the possible values of the count in the counter 68 may be entered into a latch 90, and a switch 92 for enabling programmable operation of the control system. The outputs 94 of the latch 90 are connected to the set of multiplexing gates 74, and closure of the switch 92 is effective to change the gates 74 from their first state to a second state in which they connect the outputs 94 of the latch 90 to the common inputs 76 of the decoders 78, 80.

Thus the control system 60 can be used to control the horizontal scanning rate of the oscilloscope, via the circuit 10, either manually or in response to digital control signals. In the former case, the user of the oscilloscope merely moves the switch 64 from its third position to either its first or its second position and holds it there until the desired horizontal scanning rate is displayed by the display unit (or until the oscilloscope displays a satisfactory trace). In the latter case, a digital control signal representative

of the value of the count in the counter corresponding to the desired horizontal scanning rate is entered into the latch 90.

5 **WHAT WE CLAIM IS:—**

1. A variable time-base control circuit for an oscilloscope, the circuit comprising:

 a reference voltage source;

 an integrator arranged to receive and integrate the reference voltage produced by the source so as to periodically produce a ramp voltage whose slope determines the time-base of the oscilloscope, the integrator comprising a high gain amplifier, resistance means connected between the reference voltage source and the input of the amplifier, capacitance means negative-feedback connected between the output and the input of the amplifier, at least one of the resistance means and the capacitance means being switchably variable in value, and reset means for resetting the integrator to an initial state each time said ramp voltage reaches a predetermined level; and

 switch means for varying the value of said at least one of the resistance means and the capacitance means, whereby to vary the slope of said ramp voltage;

 wherein the switch means comprises at least one semiconductor switching device, connected in the integrator in such a manner that when the or each switching device is in a conductive state, either it passes substantially no current at least throughout the production of each ramp voltage or it passes a substantially constant current at least throughout the production of each ramp voltage.

2. A circuit as claimed in claim 1, characterised in that the capacitance means comprises M capacitors each having one terminal connected to the output of the amplifier, the resistance means comprises N resistors each having one terminal connected to the reference voltage source, where M and N are both integers greater than one, and the switch means comprises M first semiconductor switching devices each connected between the input of the amplifier and the other terminal of a respective one of the capacitors, MN second semiconductor switching devices each connected between the other terminal or a respective one of the resistors and the other terminal of a respective one of the capacitors, and a control system for selectively rendering conductive different combinations of at least one of said first switching devices and at least one of said second switching devices, said combinations being such that at least one of said capacitors is connected between the output and the input of the amplifier and at least one of said resistors is connected between

the reference voltage source and the input of the amplifier.

3. A circuit as claimed in claim 2, characterised in that the switch means further comprises N third semiconductor switching devices each connected between the other terminal of a respective one of the resistors and earth, for connecting to earth the other end of each resistor not currently connected to the other end of a capacitor by one of said second semiconductor switching devices.

4. A circuit as claimed in claim 2 or claim 3, characterised in that the reset means comprises a switchable voltage source whose polarity is opposite to that of the reference voltage source, and the switch means additionally comprises M further semiconductor switching devices each connected between said second voltage source and the other terminal of a respective one of the capacitors and each arranged to be rendered conductive concurrently with the respective first switching device connected to the same capacitor.

5. A circuit as claimed in claim 2 or claim 3, characterised in that the reset means comprises a switchable voltage source whose polarity is opposite to that of the reference voltage source, and M diodes each connected between said voltage source and the other terminal of a respective one of the capacitors.

6. A circuit as claimed in any of claims 2 to 5, characterised in that the control system comprises a source of pulses, a counter connectable to receive and count said pulses, manually operable means for controlling the supply of said pulses to the counter, so as to permit the count therein to be selectively set to any one of a plurality of different values each of which corresponds to a respective one of said different combinations of the first and second switching devices, and a decoder responsive to the value of the count in the counter to render conductive the respective combination of the first and second switching devices corresponding to that value.

7. A circuit as claimed in claim 6, characterised in that said counter is a reversible counter, and said manually operable means is adapted to select the direction of counting of the counter.

8. A circuit as claimed in claim 6 or 7, characterised in that said decoder comprises a read-only memory (ROM).

9. A circuit as claimed in any preceding claim, characterised in that the or each semiconductor switching device comprises a MOSFET.

10. A circuit as claimed in any preceding claim, characterised in that the or each

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semiconductor switching device and a substantial part of the remainder of the circuit are implemented as a single integrated circuit.

5 11. A variable time-base control circuit for an oscilloscope, the circuit being substantially as herein described with reference to the accompanying drawings.

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Printed for Her Majesty's Stationery Office by the Courier Press, Leamington Spa, 1980.
Published by the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from
which copies may be obtained.

FIG. 1

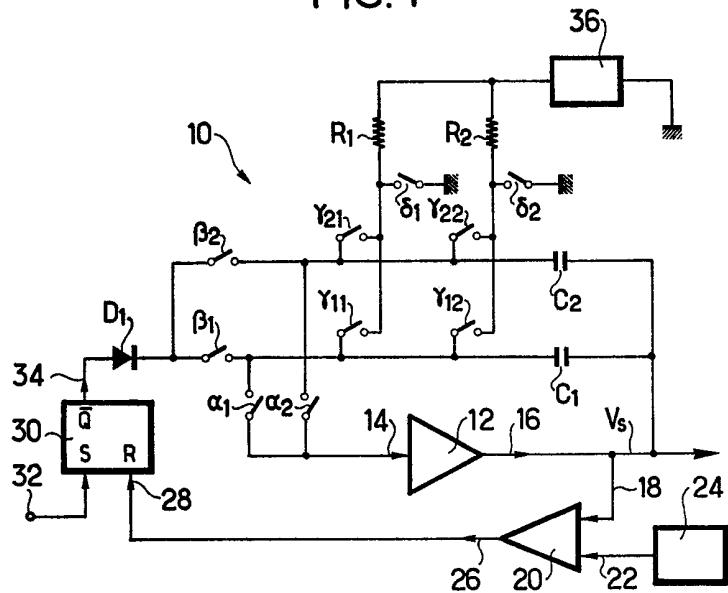


FIG. 2

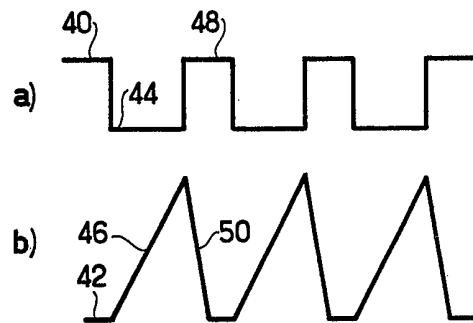


FIG. 3

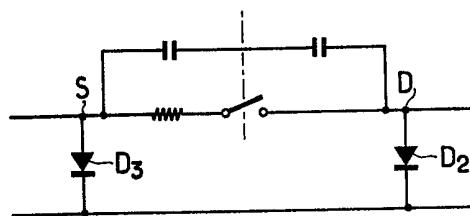


FIG. 4

