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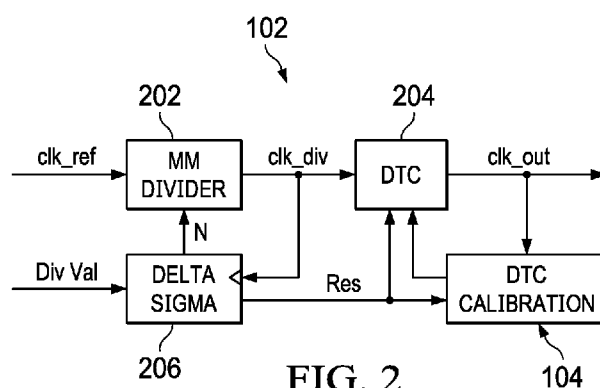


FIG. 2

(57) Abstract: In some examples, a circuit includes a clock divider (102) and a calibration circuit (104) coupled to the clock divider. The clock divider includes digital-to-time converter (DTC) (204). The calibration circuit configured to determine a gain error and a parametric integrated nonlinearity (INL) error of the DTC, determine a gain adjustment value and a INL adjustment value to compensate for the gain error and the INL error, and modify operation of the DTC according to the gain adjustment value and the INL adjustment value to correct for the gain error and the INL error.

CALIBRATION OF PARAMETRIC ERROR OF DIGITAL-TO-TIME CONVERTERS

BACKGROUND

[0001] Various electrical components in an electronic system operate at different clock frequencies. As a result, a first clock signal having a first frequency may be divided to form a second clock signal having a second frequency. Some approaches to performing this division may be limited in their usefulness.

SUMMARY

[0002] In some examples, a circuit includes a multi-modulus (MM) divider, a delta-sigma modulator, a digital-to-time converter (DTC), and a calibration circuit. The MM divider has a first input configured to receive an input clock signal, a second input, and an output. The delta-sigma modulator has a first input configured to receive a divide value, a second input coupled to the output of the MM divider, a first output coupled to the second input of the MM divider, and a second output. The DTC has a first input, a second input, a third input, and an output, the first input coupled to the output of the MM divider, the second input coupled to the second output of the delta-sigma modulator. The calibration circuit has a first input coupled to the DTC output, a second input coupled to the second delta-sigma modulator, and an output coupled to the third DTC input.

[0003] In some examples, a circuit includes a clock divider and a calibration circuit coupled to the clock divider. The clock divider includes digital-to-time converter (DTC). The calibration circuit configured to determine a gain error and a parametric integrated nonlinearity (INL) error of the DTC, determine a gain adjustment value and a INL adjustment value to compensate for the gain error and the INL error, and modify operation of the DTC according to the gain adjustment value and the INL adjustment value to correct for the gain error and the INL error.

[0004] In some examples, a system includes a controller, a clock divider, a calibration circuit, and a component. The controller is configured to provide a control signal. The clock divider is coupled to the controller, and includes a DTC configured to modify a received clock signal according to the control signal to form a modified clock signal. The calibration circuit is coupled to the clock divider. The calibration circuit is configured to determine a gain error and a parametric integrated nonlinearity (INL) error of the DTC, determine a gain adjustment value and a INL adjustment value

to compensate for the gain error and the INL error, and modify operation of the DTC according to the gain adjustment value and the INL adjustment value to correct for the gain error and the INL error. The component is coupled to the clock divider and configured to receive the modified clock signal from the clock divider and operate according to the modified clock signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. 1 is a block diagram of an electronic device, in accordance with various examples.

[0006] FIG. 2 is a block diagram of a clock divider with a calibration circuit, in accordance with various examples.

[0007] FIG. 3 is a block diagram of a clock divider with a calibration circuit, in accordance with various examples.

[0008] FIG. 4 is a block diagram of a calibration phase-locked loop (PLL), in accordance with various examples.

[0009] FIG. 5 is a block diagram of a calibration PLL, in accordance with various examples.

[0010] FIG. 6 is a block diagram of a calibration PLL, in accordance with various examples.

[0011] FIG. 7 is a block diagram of a calibration PLL, in accordance with various examples.

[0012] FIG. 8 is a block diagram of a calibration PLL, in accordance with various examples.

[0013] FIG. 9 is a block diagram of a calibration PLL, in accordance with various examples.

[0014] FIG. 10 is a block diagram of a PLL that includes a clock divider with a calibration circuit, in accordance with various examples.

[0015] FIG. 11 is a block diagram of a PLL that includes a clock divider with a calibration circuit, in accordance with various examples.

[0016] FIG. 12 is a block diagram of a detector, in accordance with various examples.

[0017] FIG. 13 is a block diagram of a detector, in accordance with various examples.

[0018] FIG. 14 is a block diagram of a detector, in accordance with various examples.

[0019] FIG. 15 is a timing diagram of signals in a clock divider, in accordance with various examples.

[0020] FIG. 16 is a diagram of basis functions, in accordance with various examples.

[0021] FIG. 17 is a diagram of expanded basis functions, in accordance with various examples.

[0022] FIG. 18 is a diagram of simplified basis functions, in accordance with various examples.

[0023] FIG. 19 is a transient simulation of gain and parametric integrated nonlinearity (INL) correction in a clock divider, in accordance with various examples.

[0024] FIG. 20A is a phase noise spectrum in a clock divider with INL cancellation disabled, in accordance with various examples.

[0025] FIG. 20B is a phase noise spectrum in a clock divider with INL cancellation enabled, in accordance with various examples.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0026] Some approaches to clock division exist, such as integer frequency division. However, integer frequency division may be limited in its usefulness due to an integer relationship existing between input and output clock signals which limits a resolution of selectable output clock signal frequencies. To avoid such limits on output frequency resolution, one solution is the implementation of a fractional output divider (FOD). A fractional output divider dynamically varies its divide value in time for dividing an input clock signal such that the average divided clock frequency is not constrained to an integer relationship between input and divided clock signals, where the divided clock signal has an average frequency corresponding to a programmed value. However, the dynamically varying divide value can lead to instantaneous phase error in the divided clock signal, which can result in jitter in the divided clock signal. The jitter may be considered instantaneous variations in time between rising edges of the divided clock signal and corresponding rising edges of an ideal clock signal having a frequency that is the same as the average frequency of the divided clock signal.

[0027] In some examples, the ideal clock signal is a clock signal that is periodic (e.g., each clock cycle has a same period). The phase error may cause the divided clock to have periods that vary from clock cycle to clock cycle and do not match the period of the ideal clock signal. The mismatch may be corrected, such as by a digital-to-time converter (DTC) modifying the divided clock signal according to a residual error signal that quantifies the phase or time error between the input and divided clock signal. However, implementations of the DTC can introduce correction errors as the DTC modifies the divided clock signal to cancel the residual error signal due to the dynamic variation of the divide value. Such correction errors include gain error, parametric integrated nonlinearity (INL) error, and mismatch error. Gain error corresponds to an error in a full-scale range in time of the DTC compared to an ideal full-scale range corresponding to an input clock period or an integer multiple of the input clock period. INL corresponds to error under an assumption of zero gain error that can be described as a function of the input residue that controls the DTC. Mismatch error corresponds to error of individual settings of the input residue that is not readily amenable to being

described as a function of the input residue that controls the DTC.

[0028] Because the mismatch error is not readily amenable to being described as a function of the input residue that controls the DTC, correction of the mismatch error is sometimes performed via a look up table (LUT). In examples in which the mismatch error is relatively stable across temperature variations, the measurements and calculations to determine the entry values of the LUT can be performed offline. In such examples, the remaining errors of concern are gain error and INL error, which can vary significantly with temperature. Therefore, gain error and INL error may be corrected in a substantially continuous manner, rather than offline. In some examples, the correction of gain error and INL error in a continuous manner is accompanied by offline calibration of mismatch error via a LUT.

[0029] Examples of this description provide a circuit useful to correct for gain and INL error introduced in forming a clock signal. For example, circuits of this description may estimate gain and INL error values, determine gain and INL adjustment values, and modify the DTC gain and INL according to the gain and INL adjustment values to calibrate the gain and INL errors of the DTC such that their impact on the output clock signal is reduced. In some examples, such calibration may provide for an output clock signal that is periodic in nature, being approximately equivalent to an ideal clock signal, while avoiding the constraint of an integer relationship between input and output clock signals and mitigating effects of gain or INL error introduced into the output clock signal in the process of forming the output clock signal.

[0030] FIG. 1 is a block diagram of an electronic device 100, in accordance with various examples. The electronic device 100 may be any suitable device, the scope of which is not limited herein. For example, the electronic device 100 may be a device in which it is useful to have a second clock signal having a second frequency that varies from a first frequency of a first clock signal, such as via frequency division techniques or frequency multiplication techniques. Accordingly, the electronic device 100 includes a clock divider 102. The clock divider 102 may be of various forms, such as a FOD. The FOD may be implemented in an open loop context, such as a frequency divider, or in a closed loop context, such as within a phase-locked loop. The clock divider 102 includes a calibration circuit 104. In various examples, the calibration circuit 104 estimates, calculates, or otherwise determines an error of, or associated with, the clock divider 102, determines an adjustment value based on the error, and corrects such error through correction or calibration of the clock divider 102 based on the adjustment value.

[0031] The electronic device 100 also includes a controller 106. The controller 106 may couple to the clock divider 102 and/or the calibration circuit 104 and provide various control signals or other data to the clock divider 102 and/or the calibration circuit 104. The signals may include at least a reference clock (e.g., the input clock for the clock divider 102) and a frequency to which the clock divider 102 is to divide the input clock (or a value by which the clock divider 102 is to divide the input clock) to form the output clock. In other examples, the reference clock is provided by another component (not shown) such as an oscillator or phase locked loop, such as a fractional-N or integer-N frequency synthesizer. In some examples, the controller 106 receives the output clock from the clock divider 102. In other examples, the electronic device 100 includes a component 108. The component 108 may couple to the clock divider 102 and receive the output clock signal from the clock divider 102. In various examples, the component 108 is any suitable component, such as a radio transceiver, a frequency divider, a phase-locked loop (e.g., such as fractional-N or integer-N frequency synthesizer), a component useful in communication or other signaling, or any other component which may benefit from receiving an output clock signal having a frequency that varies from the input clock and is set with high resolution.

[0032] FIG. 2 is a block diagram of the clock divider 102 with the calibration circuit 104, in accordance with various examples. In some examples, the clock divider 102 as shown in FIG. 2 is an open loop FOD. In some examples, the clock divider 102 includes a multi-modulus (MM) divider 202, a digital delta-sigma modulator 206, a DTC 204, and the calibration circuit 104. In some examples, the MM divider 202 has a first input configured to receive an input clock signal, such as a reference clock signal, indicated in FIG. 2 as `clk_ref`. The MM divider 202 also has a second input and an output. The delta-sigma modulator 206 has a first input configured to receive a divide value that includes integer and fractional components, indicated in FIG. 2 as `Div Val`. The divide value may be in a digital format or domain and is converted by the delta-sigma modulator 206 to a sequence of divide values, indicated in FIG. 2 as `N`, such that the average of the sequence corresponds to `Div Val`. The delta-sigma modulator 206 has a first output coupled to the second input of the MM divider 202 and provides `N` to the MM divider 202 via the coupling. The delta-sigma modulator 206 also includes a second input coupled to the output of the MM divider 202 and a second output. The DTC 204 has a first input coupled to the output of the MM divider 202, a second input coupled to the second output of the delta-sigma modulator 206, a third input, and an output. In some examples, the DTC 204 receives a residual error signal, indicated in FIG. 2 as `Res`, from the delta-sigma modulator

206. The DTC 204 provides an output clock signal, indicated in FIG. 2 as `clk_out`, at its output. The calibration circuit 104 has a first input coupled to the output of the DTC 204, a second input coupled to the second output of the delta-sigma modulator 206, and an output coupled to the third input of the DTC 204. In some examples, the calibration circuit 104 has a third input coupled to the output of the MM divider 202.

[0033] In an example of operation, the delta-sigma modulator 206 receives `Div Val`, determines, based on `Div Val`, `N`, and provides `N` to the MM divider 202. The delta-sigma modulator 206 further provides `Res` at its second output. The MM divider 202 receives `clk_ref` and `N`, and based thereon, provides a divided clock signal, indicated in FIG. 2 as `clk_div`. The DTC 204 receives `clk_div` and `Res`, and based thereon, provides `clk_out`. The calibration circuit 104 receives `clk_div`, `clk_out`, and `Res`, and based thereon, determines gain and INL error adjustment values for calibrating the clock divider 102 to mitigate gain and INL errors introduced into `clk_out` by the DTC 204. In some examples, the calibration circuit 104 also corrects for mismatch errors in the DTC 204, as described above, such as via a LUT.

[0034] FIG. 3 is a block diagram of the clock divider 102 with the calibration circuit 104, in accordance with various examples. The clock divider 102 and the calibration circuit 104 are coupled and operate as described above with respect to FIG. 2, the description of which is not repeated with respect to FIG. 3. In some examples, the calibration circuit 104 includes a calibration phase-locked loop (PLL) 302, a correlation circuit 304, a filter and accumulation circuit 306, an INL compensation circuit 308, and a gain compensation circuit 310. The calibration PLL 302 has an input coupled to the output of the DTC 204 and an output. The correlation circuit 304 has a first input coupled to the output of the calibration PLL 302, a second input coupled to the second output of the delta-sigma modulator 206, a first output, and a second output. The filter and accumulation circuit 306 has a first input coupled to the first output of the correlation circuit 304, a second input coupled to the second output of the correlation circuit 304, a first output, and a second output. The INL compensation circuit 308 has a first input coupled to the output of the MM divider 202, a second input coupled to the second output of the delta-sigma modulator 206, a third input coupled to the second output of the filter and accumulation circuit 306, and an output coupled to the second input of the DTC 204. In some examples, the coupling between the output of the INL compensation circuit 308 and the second input of the DTC 204 replaces the coupling between the second output of the delta-sigma modulator 206 and the second input of the DTC 204, described above with respect to FIG. 2. The gain

compensation circuit 310 has an input coupled to the first output of the filter and accumulation circuit 306 and an output coupled to the third input of the DTC 204. In some examples, a LUT (not shown) is coupled between the second output of the delta-sigma modulator 206 and the DTC 204 to correct for mismatch errors in the DTC.

[0035] In an example of operation, the calibration PLL 302 receives `clk_out` and determines a phase error signal, indicated in FIG. 3 as `PDcal`, based on `clk_out`. `PDcal` provides an instantaneous phase error of `clk_out` to correlation circuit 304, which performs a correlation based on `PDcal`, `Res`, and basis functions for gain error and INL error. In some applications, `PDcal` indicates whether the phase error is positive or negative, such as may be determined by a bang-bang phase detector (not shown), or any other suitable component. `PDcal` is then correlated with a signal based on `Res` and basis functions. For example, `Res` is mapped by the correlation circuit 304 according to one or more basis functions, the resulting signals of which may be filtered and may have an offset applied. In some examples, the filtering is high-pass in nature. In some examples, filtering and offset application are optional and either may be omitted. The correlation is subsequently performed by the correlation circuit 304, which first multiplies `PDcal` by the signals created by mapping `Res` according to one or more basis functions and then filters by a correlation filter of the correlation circuit 304 to obtain correlation error values. For example, based on the correlation, the correlation circuit 304 provides a gain correlation error value (`Corr_gain`) and an INL correlation error value (`Corr_INL`). The filter and accumulation circuit 306 receives the gain correlation error value and the INL correlation error value and determines a gain adjustment value (`Gain_adj`) and an INL adjustment value (`INL_adj`). The filter and accumulation circuit 306 provides `Gain_adj` to the DTC 204 and provides `INL_adj` to the INL compensation circuit 308. In some examples, `Gain_adj` is provided to a delta-sigma digital-to-analog converter (DAC) (not shown) of the gain compensation circuit 310 to control the DTC 204 to correct for the determined gain error. For example, a resistance, current, voltage, or capacitance of the DTC 204 may be modified according to `Gain_adj` to correct for the determined gain error. The INL compensation circuit 308 receives `clk_div` (such as for clocking operation of the INL compensation circuit 308), `Res`, and `INL_adj` and, based thereon, determines a compensation residual error signal. In some examples, the INL compensation circuit 308 includes an adder that adds `INL_adj` to `Res` to determine the compensation residual error signal. The INL compensation circuit 308 may also include registers that store data associated with determination of the compensation residual error signal and the registers may be clocked by `clk_div`. The compensation

residual error signal may be determined by the INL compensation circuit 308 via computation (e.g., such as via an adder, as described above), a LUT, or both, based on its received input signals. The INL compensation circuit 308 provides the compensation residual error signal to the DTC 204. In other examples, the addition of INL_adj and Res is performed within the DTC 204 such that the INL compensation circuit 308 is omitted and the DTC 204 directly receives INL_adj in place of the compensation residual error signal. Based on the compensation residual error signal and Gain_adj, the DTC 204 applies compensation to the determination and providing of clk_out, reducing the effect of gain error and/or INL error of the DTC 204 on a value of clk_out.

[0036] FIG. 4 is a block diagram of the calibration PLL 302, in accordance with various examples. In some examples, the calibration PLL 302 includes a linear phase detector (PD) 402, a loop filter 404, a bang-bang phase detector (BB PD) 408, a tune control circuit 410, a voltage-controlled oscillator (VCO) 412, a divider 414. In some examples, the linear PD 402 has a first input configured to receive clk_out (e.g., such as coupled to the output of the DTC 204 to receive clk_out), a second input, and an output. The loop filter 404 has an input coupled to the output of the linear PD 402 and an output. The BB PD 408 has a first input configured to receive clk_out (e.g., such as coupled to the output of the DTC 204 to receive clk_out), a second input, and an output. The BB PD 408 provides PDcal at its output. The tune control circuit 410, which may be omitted in some implementations, has an input coupled to the output of the BB PD 408 and an output. The VCO 412 has an output and has an input coupled to the output of loop filter 404 or the tune control circuit 410, which could include analog circuits and/or digital logic. The divider 414 has an input coupled to the output of the VCO 412 and an output coupled to the second input of the linear PD 402 (unless it is omitted) and the second input of the BB PD 408. The divider 414 provides a divider output signal, indicated in FIG. 4 as Div Out, at its output.

[0037] In an example of operation, the linear PD 402 provides a frequency lock between clk_out and Div Out, maintaining a linear relationship between the two during steady-state operation of the calibration PLL 302. An output signal of the linear PD 402 is filtered by the loop filter 404 and provided to the VCO 412. The BB PD 408 shifts the phase of Div Out such that the BB PD 408 alternates between positive and negative phase error values during steady-state operation. As such, the BB PD 408 provides PDcal, indicating whether the phase error of clk_out is negative or positive with respect to Div Out. For example, a first value of PDcal indicates the phase error of clk_out is positive and a second value of PDcal indicates that the phase error of clk_out is negative.

Accordingly, PDcal dithers between two output values having an approximately even probability of occurring during steady-state operation of the calibration PLL 302. For example, if PDcal more frequently indicates that the phase of clk_out is negative, the tune control circuit 410 sends a corrective signal to the VCO 412, which sums with the output of the loop filter 404, to shift the phase of VCO 412 to cause PDcal to achieve an approximately even probability of negative and positive values. Similar functionality is performed if PDcal more frequently indicates that the phase of clk_out is positive. The divider 414 divides the output signal of the VCO 412 by a programmed value to provide Div Out at the same frequency as clk_out while facilitating operation of the VCO 412 at a frequency within operational limits of the VCO 412.

[0038] FIG. 5 is a block diagram of the calibration PLL 302, in accordance with various examples. In some examples, the calibration PLL 302 includes a linear PD 502, a loop filter 504, a BB PD 506, a tune control circuit 508, a VCO 510, and a divider 512. In some examples, the linear PD 502 includes a d-flip flop 514, a d-flip flop 516, an AND gate 518, and a delay circuit 520. The loop filter 504 includes a resistor 522, an inverter 524, a resistor 526, a capacitor 528, a resistor 530, and a capacitor 532. The VCO 510 includes a varactor 534 and a varactor 536. In some examples, the d-flip flop 514 has a data input that receives a logic 1 value, a clock input that receives clk_out, a reset input, and an output. The d-flip flop 516 has a data input that receives a logic 1 value, a clock input that receives Div Out, a reset input, and an output. The AND gate 518 has a first input coupled to the output of the d-flip flop 514, a second input coupled to the output of the d-flip flop 516, and an output. The delay circuit 520 has an input coupled to the output of the AND gate 518, and an output coupled to the reset inputs of the d-flip flop 514 and the d-flip flop 516. The resistor 522 is coupled between the output of the d-flip flop 514 and a node 540. The inverter 524 has an input coupled to the output of the d-flip flop 516 and an output coupled through the resistor 526 to the node 540. The capacitor 528 is coupled between the node 540 and a ground voltage potential. The resistor 530 is coupled between the node 540 and a node 542. The capacitor 532 is coupled between the node 542 and the ground voltage potential. The varactor 534 has an input coupled to the node 542 and an output. The varactor 536 has an input coupled to the output of the tune control circuit 508 and an output. Output signals provided at respective outputs of the varactor 534 and the varactor 536 are summed to provide a signal, indicated in FIG. 5 as Fvco, having a frequency determined based on capacitances of the varactor 534 and the varactor 536. The linear PD 502 and the loop filter 504 allows phase and frequency locking of Div Out to clk_out according to linear dynamics,

while the BB PD 506 and tune control circuit 508 provide phase alignment of clk_out and Div Out such that PDcal dithers between two output values having an approximately even probability of occurring during steady-state operation, as described above.

[0039] FIG. 6 is a block diagram of the calibration PLL 302, in accordance with various examples. In some examples, the calibration PLL includes a linear PD 602, a loop filter 604, a BB PD 606, a BB control circuit 608, a digital delta-sigma DAC 610, a DAC and filter circuit 612, a VCO 614, and a divider 616. In some examples, the VCO 614 is substantially similar to the VCO 510 of FIG. 5, the description of which is not repeated herein with respect to FIG. 6. In some examples, the linear PD 602, the loop filter 604, the BB PD 606, and the divider 616 are substantially similar to the linear PD 402, the loop filter 404, the BB PD 408, and the divider 414, described above with respect to FIG. 4, the description of which is not repeated herein with respect to FIG. 6. The BB control circuit 608 has an input coupled to the output of the BB PD 606 and an output. The digital delta-sigma modulator 610 has an input coupled to the output of the BB control circuit 608 and an output. The DAC and filter circuit 612 has an input coupled to the output of the digital delta-sigma modulator 610 and an output coupled to the VCO 614.

[0040] In an example of operation, the BB control circuit 608 provides a BB tuning signal based on PDcal as provided by BB PD 606. The BB control circuit 608 may provide the BB tuning signal according to any suitable processing, such as via a decimator, accumulator, gear shifting, etc. The digital delta-sigma modulator 610 and the DAC and filter circuit 612 convert the BB tuning signal from a digital format or domain to an analog signal suitable for controlling the VCO 614. In some examples, DAC and filter circuit 612 may be omitted and the VCO 614 may include an array of capacitors (not shown) coupled to digital delta-sigma modulator 610 to achieve a more digital implementation for providing the BB tuning signal.

[0041] FIG. 7 is a block diagram of the calibration PLL 302, in accordance with various examples. In some examples, the calibration PLL 302 of FIG. 7 includes the elements of the calibration PLL 302 of FIG. 6, and are labeled accordingly. The description of these components is not repeated herein with respect to FIG. 7. The calibration PLL 302 also includes a measurement circuit 702 and a frequency control circuit 704. The measurement circuit 702 has a first input configured to receive clk_out, a second input coupled to the output of the divider 616, and an output. The frequency control circuit 704 has an input coupled to the output of the measurement circuit 702 and an output coupled to the input of the DAC and filter circuit 612. The measurement circuit 702 and the

frequency control circuit 704 form an auxiliary frequency control path that increases a frequency tuning range of the VCO 614. In some examples, the DAC and filter circuit 612 may be omitted and the VCO 614 may include an array of capacitors coupled to the digital delta-sigma modulator 610 and the frequency control circuit 704 to achieve a more digital implementation for providing the BB tuning signal and auxiliary frequency control path.

[0042] FIG. 8 is a block diagram of the calibration PLL 302, in accordance with various examples. In some examples, the calibration PLL 302 of FIG. 8 includes the elements of the calibration PLL 302 of FIG. 7, and are labeled accordingly. The description of these components is not repeated herein with respect to FIG. 8. The calibration PLL 302 also includes a divide value selection circuit 802. The divide value selection circuit 802 has a first input coupled to the input of the DAC and filter circuit 612, a second input configured to receive a enable signal, and an output coupled to the divider 616. In some examples, the divide value selection circuit 802 selects a value by which the divider 616 divides an output signal of the VCO 614 such that the BB tuning signal is kept within a programmed range of limits of the VCO 614, such as to achieve proper operation for frequency control of the VCO 614.

[0043] FIG. 9 is a block diagram of the calibration PLL 302, in accordance with various examples. In some examples, the calibration PLL 302 of FIG. 9 includes some of the elements of the calibration PLL 302 of FIG. 7, and are labeled accordingly. The description of these components is not repeated herein with respect to FIG. 9. The calibration circuit 302 includes multiple VCOs 902, each of which may be coupled as the VCO 614. In some examples, a VCO of the VCOs 902 that operates at a lowest frequency suitable for a particular application of the calibration PLL 302 may provide a VCO output signal, thereby reducing power consumption of the calibration PLL 302 in comparison to other examples, such as those of FIGS. 6-9.

[0044] FIG. 10 is a block diagram of a PLL 1000 that includes the clock divider 102 with the calibration circuit 104, in accordance with various examples. In some examples, the PLL 1000 includes the clock divider 102 within its closed loop feedback and performs frequency multiplication from F_{ref} to F_{vco} according to Div Val. In some examples, the PLL 1000 includes detector 1002, a VCO 1006, a divider 1008, a MM divider 1010, a DTC 1012, and a delta-sigma modulator 1014. In some examples, the PLL 1000 of FIG. 10 may provide filtering, via the detector 1002, of jitter introduced by the DTC 1012 that is not provided by the clock divider 102 of FIG. 2, described above herein.

[0045] In an example implementation, the detector 1002 has a first input configured to receive a reference signal F_{ref} , a second input, a first output, and a second output. The VCO 1006 has an input coupled to the first output of the detector 1002 and an output. The divider 1008 has an input coupled to the output of the VCO 1006 and an output at which the divider 1008 is configured to provide clk_out . In some implementations, the divider 1008 may be omitted in examples in which high output signal frequencies are to be provided by the PLL 1000. In some examples, the divider 1008 may include multiple frequency dividers to create multiple output signals which may be at different frequencies. The MM divider 1010 has a first input coupled to the output of the VCO 1006, a second input, and an output. The DTC 1012 has a first input coupled to the output of the MM divider 1010, a second input, a third input, and an output coupled to the second input of the detector 1002. The delta-sigma modulator 1014 has an input coupled to the output of the MM divider 1010, a first output coupled to the second input of the MM divider 1010, and a second output. The calibration circuit 104 has a first input coupled to the second output of the detector 1002, a second input coupled to the second output of the delta-sigma modulator 1014, and an output coupled to the DTC 1012.

[0046] In an example of operation of the PLL 1000, the detector 1002 compares an output of the DTC 1012, indicated in FIG. 10 as clk_out , to F_{ref} . Based on the comparison, the detector 1002 provides $PDcal$ to the calibration circuit 104 and a control signal, indicated in FIG. 10 as $Vctrl$, that is provided to the VCO 1006 to achieve phase lock at steady state. A frequency of an output signal of the VCO 1006 is determined by the frequency of F_{ref} multiplied by $Div\ Val$. $Fvco$, as provided by the VCO 1006, may be directly provided as an output of the PLL 1000, or may be divided down to one or more frequencies by divider 1008. Also, PLL 1000 may omit a calibration PLL and provide filtering of high frequency noise introduced by the DTC 1012.

[0047] The MM divider 1010 receives the output of the VCO 1006 and receives N from the delta-sigma modulator 1014, and based thereon, provides a divided clock signal, indicated in FIG. 10 as clk_div . The DTC 1012 receives clk_div and calibration signals, and based thereon, provides clk_out . The calibration circuit 104 receives $PDcal$ from the detector 1002 and receives Res from the delta-sigma modulator 1014, and based thereon, performs correlations according to basis functions that are each a function of Res , as described above herein, to determine and provide the calibration signals. Based on the calibration signals, the DTC 1012 applies compensation to the determination and providing of clk_out , reducing the effect of gain error and/or INL error of the

DTC 1012 on a value of clk_out . In some examples, the PLL 1000 continually adjusts the calibration signals provided by the calibration circuit 104 such that correlation values determined by the compensation circuit for gain and INL errors of the DTC 1012 converge to an average of zero.

[0048] FIG. 11 is a block diagram of the PLL 1000 with the calibration circuit 104, in accordance with various examples. The PLL 1000 is coupled and operates as described above with respect to FIG. 10, some of the description of which is not repeated with respect to FIG. 11. In some examples, the calibration circuit 104 includes a correlation circuit 1016, a filter and accumulation circuit 1018, an INL compensation circuit 1020, and a gain compensation circuit 1022.

[0049] In an example implementation, the detector 1002 has a first input configured to receive F_{ref} , a second input, a first output, and a second output. The VCO 1006 has an input coupled to the first output of the detector 1002 and an output. The divider 1008 has an input coupled to the output of the VCO 1006 and an output at which the divider 1008 is configured to provide clk_out . In other examples, the divider 1008 is omitted as F_{vco} is provided as clk_out . The MM divider 1010 has a first input coupled to the output of the VCO 1006, a second input, and an output. The DTC 1012 has a first input coupled to the output of the MM divider 1010, a second input, a third input, and an output coupled to the second input of the detector 1002. The delta-sigma modulator 1014 has an input coupled to the output of the MM divider 1010, a first output coupled to the second input of the MM divider 1010, and a second output. The correlation circuit 1016 has a first input coupled to the second output of the detector 1002, a second input coupled to the second output of the delta-sigma modulator 1014, a first output, and a second output. The filter and accumulation circuit 1018 has a first input coupled to the first output of the correlation circuit 1016, a second input coupled to the second output of the correlation circuit 1016, a first output, and a second output. The INL compensation circuit 1020 has a first input coupled to the second output of the delta-sigma modulator 1014, a second input coupled to the second output of the filter and accumulation circuit 1018, and an output coupled to the third input of the DTC 1012. The gain compensation circuit 1022 has an input coupled to the first output of the filter and accumulation circuit 1018 and an output coupled to second input of the DTC 1012. In some examples, the gain compensation circuit 1022 functions substantially similar to the gain compensation circuit 310 of FIG. 3, and such description is not repeated again herein with respect to FIG. 10.

[0050] In an example of operation of the PLL 1000, the detector 1002 compares an output of the DTC 1012, indicated in FIG. 11 as clk_out , to a reference signal, indicated in FIG. 11 as F_{ref} .

Based on the comparison, the detector 1002 provides PDcal to the correlation circuit 1016 and a control signal, indicated in FIG. 11 as Vctrl, to the VCO 1006. A frequency of Fvco is determined by the frequency of F_ref multiplied by the divide value of divider 1008, which is determined by a programmed value. Out, as provided by the VCO 1006, may be directly provided as an output of the PLL 1000, or may be divided down to one or more frequencies by divider 1008. Also, PLL 1000 may omit a calibration PLL and provide filtering of high frequency noise introduced by the DTC 1012.

[0051] The MM divider 1010 receives Fvco and receives N from the delta-sigma modulator 1014, and based thereon, provides a divided clock signal, indicated in FIG. 11 as clk_div. The DTC 1012 receives clk_div, a compensation residual error signal, and Gain_adj and based thereon, provides clk_out. The correlation circuit 1016 receives PDcal from the detector 1002 and receives Res from the delta-sigma DAC 1014, and based thereon, performs correlations according to basis functions that are each a function of Res, as described above herein, to determine and provide correlation values for gain and INL, respectively indicated in FIG. 11 as Corr_gain and Corr_INL. The filter and accumulation circuit 1018 receives Corr_gain and Corr_INL, and based thereon, determines gain and INL adjustment values, respectively indicated in FIG. 11 as INL_adj and Gain_adj. The INL compensation circuit 1020 receives Res and INL_adj, and based thereon, determines and provides the compensation residual error signal to the DTC 1012. Based on the compensation residual error signal and the Gain_adj, the DTC 1012 applies compensation to the determination and providing of clk_out, reducing the effect of gain error and/or INL error of the DTC 1012 on a value of clk_out. For example, the DTC 1012 may convert Gain_adj from a digital value to an analog value via a delta-sigma DAC (not shown) and control a resistance, current, voltage, or capacitance of the DTC 1012 based on the resulting analog value provided by the delta-sigma DAC to correct for the determined gain error. In some examples, the PLL 1000 continually adjusts the calibration signals provided by the calibration circuit 104 such that correlation values determined by the compensation circuit for gain and INL errors of the DTC 1012 converge to an average of zero. In some examples, a LUT (not shown) is coupled between the second output of the delta-sigma modulator 1014 and the DTC 1012 to provide correction for mismatch errors in the DTC 1012.

[0052] FIG. 12 is a block diagram of the detector 1002, in accordance with various examples. In some examples, the detector 1002 includes a linear PD 1202, a loop filter 1204, a BB PD 1208, and a tune control circuit 1210. In some examples, the linear PD 1202, loop filter 1204, BB PD 1208,

and tune control circuit 1210 are coupled and operate substantially similar to the linear PD 402, loop filter 404, BB PD 408, and tune control circuit 410, described above with respect to FIG. 4, with the signal Div in FIG. 12 replacing the signal Div Out of FIG. 4. Accordingly, the description of these components is not repeated herein with respect to FIG. 12.

[0053] FIG. 13 is a block diagram of the detector 1002, in accordance with various examples. In some examples, the detector 1002 includes a linear PD 1302, a loop filter 1304, an offset delay circuit 1306, and a BB PD 1308. The linear PD 1302 has a first input configured to receive F_{ref} , a second input configured to receive Div, and an output. The loop filter 1304 has a first input coupled to the output of the linear PD 1302, and an output at which Vctrl is provided. The offset delay circuit 1306 has a first input configured to receive Div, a second input configured to receive an offset calibration signal, and an output. The BB PD 1308 has a first input configured to receive F_{ref} , a second input coupled to the output of the offset delay circuit 1306, and an output at which PDcal is provided.

[0054] In an example of operation, the linear PD 1302 provides phase lock between F_{ref} and Div, maintaining a steady-state phase error between F_{ref} and Div according to characteristics (including mismatch) of detector 1002. An output signal of the linear PD 1302 is filtered by the loop filter 1304 and provided as Vctrl. The offset delay circuit 1306 delays Div according to the offset calibration signal, which may be received from a control circuit (not shown) that monitors PDcal to shift the phase of Div such that PDcal eventually achieves an approximately even probability of negative and positive values during steady-state operation of the detector 1002. Based on the shifting, the BB PD 1308 provides PDcal, indicating whether the instantaneous phase of F_{ref} is negative or positive with respect to the delayed Div. For example, a first value of PDcal indicates that the phase of F_{ref} is negative and a second value of PDcal indicates that the phase of F_{ref} is positive.

[0055] FIG. 14 is a block diagram of the detector 1002, in accordance with various examples. In some examples, the detector 1002 includes a linear PD 1402, a loop filter 1404, and an analog-to-digital converter (ADC) 1406. The linear PD 1402 has a first input configured to receive F_{ref} , a second input configured to receive Div, and an output. The loop filter 1404 has a first input coupled to the output of the linear PD 1402, a first output at which Vctrl is provided, and a second output. The ADC 1406 has a first input coupled to the second output of the loop filter 1404, a second input configured to receive an offset calibration signal, and an output at which PDcal is provided.

[0056] FIG. 15 is a timing diagram 1500 of signals in the clock divider 102, in accordance with

various examples. The timing diagram 1500 shows `clk_ref`, `clk_div`, and `clk_out`, as described above herein. As shown by the diagram 1500, `clk_div` may have periods of different time duration (e.g., jitter) that are corrected by a DTC as controlled by `Res` and the described error correction techniques in forming `clk_out`.

[0057] FIG. 16 is a diagram 1600 of basis functions that are less computationally complex to implement, in accordance with various examples. The diagram 1600 shows a gain basis function 1605 and an INL basis function 1610. In some examples, the gain basis function 1605 and the INL basis function 1610 are orthogonal and each have zero mean value. In other examples, the basis function 1605 and the basis function 1610 may be non-orthogonal and/or a non-zero mean component may be introduced.

[0058] FIG. 17 is a diagram 1700 of expanded basis functions, in accordance with various examples. The diagram 1700 shows a gain basis function 1705, a fundamental INL basis function 1710, and a 2nd harmonic INL basis function 1715. In some examples, the gain basis function 1705, the fundamental INL basis function 1710, and the 2nd harmonic INL basis function 1715 are orthogonal and each have zero mean value. In other examples, the basis function 1705, the basis function 1710, and the basis function 1715 may be non-orthogonal and/or a non-zero mean component may be introduced.

[0059] FIG. 18 is a diagram 1800 of simplified basis functions, in accordance with various examples. The diagram 1800 shows a gain basis function 1805 and an INL basis function 1810. In some examples, the gain basis function 1805 and the INL basis function 1810 are orthogonal and each have zero mean value. In other examples, the basis function 1805 and the basis function 1810 may be non-orthogonal and/or a non-zero mean component may be introduced. In some examples, the simplified basis functions are computationally simpler (e.g., require less computational complexity and/or power) than the basis functions of FIG. 16 and/or FIG. 17. In other examples, more complex basis functions may be useful, such as if performance increases resulting from the more complex basis functions is worthwhile relative to the increased computational complexity and/or power associated with computation of the more complex basis functions.

[0060] FIG. 19 is a transient simulation 1900 of gain and INL correction in a clock divider, in accordance with various examples. In some examples, the clock divider is the clock divider 102, as described above herein. The transient simulation 1900 shows `PDcal`, `Gain_adj`, and `INL_adj`.

[0061] FIG. 20A is a phase noise spectrum 2000 of `clk_out` with INL cancellation disabled, in

accordance with various examples. In some examples, clk_out is provided by the clock divider 102, as described above herein. As shown in FIG. 20A, the left-side vertical axis is representative of spectral density ($L(f)$) in units of decibels relative to the carrier (dBc) per Hertz (Hz), the right-side vertical axis is representative of dBc, and the horizontal axis is representative of a frequency offset from a carrier frequency, in terms of megahertz (MHz). As shown by the phase noise spectrum 2000, in some examples of the clock divider in which INL cancellation is disabled, a spur having a magnitude, which in this example is approximately -39 dBc, may be present at a carrier frequency of about 156 MHz.

[0062] FIG. 20B is a phase noise spectrum 2005 of clk_out with INL cancellation enabled, in accordance with various examples. In some examples, clk_out is provided by the clock divider 102, as described above herein. A description of units of the axes of FIG. 20B may be the same as those of FIG. 20A. As shown by the phase noise spectrum 2005, in some examples of the clock divider in which INL cancellation is enabled, the spur shown in FIG. 20A is reduced, with this example showing reduction from approximately -39 dBc in value to approximately -80 dBc in value.

[0063] The term “couple” is used throughout the specification. The term may cover connections, communications, or signal paths that enable a functional relationship consistent with this description. For example, if device A provides a signal to control device B to perform an action, in a first example device A is coupled to device B, or in a second example device A is coupled to device B through intervening component C if intervening component C does not substantially alter the functional relationship between device A and device B such that device B is controlled by device A via the control signal provided by device A.

[0064] A device that is “configured to” perform a task or function may be configured (e.g., programmed and/or hardwired) at a time of manufacturing by a manufacturer to perform the function and/or may be configurable (or reconfigurable) by a user after manufacturing to perform the function and/or other additional or alternative functions. The configuring may be through firmware and/or software programming of the device, through a construction and/or layout of hardware components and interconnections of the device, or a combination thereof.

[0065] A circuit or device that is described herein as including certain components may instead be adapted to be coupled to those components to form the described circuitry or device. For example, a structure described as including one or more semiconductor elements (such as transistors), one or more passive elements (such as resistors, capacitors, and/or inductors), and/or one or more sources

(such as voltage and/or current sources) may instead include only the semiconductor elements within a single physical device (e.g., a semiconductor die and/or integrated circuit (IC) package) and may be adapted to be coupled to some of the passive elements and/or the sources to form the described structure either at a time of manufacture or after a time of manufacture, such as by an end-user and/or a third-party.

[0066] While certain components may be described herein as being of a particular process technology, these components may be exchanged for components of other process technologies. Circuits described herein are reconfigurable to include the replaced components to provide functionality at least partially similar to functionality available prior to the component replacement. Components shown as resistors, unless otherwise stated, are generally representative of any one or more elements coupled in series and/or parallel to provide an amount of impedance represented by the shown resistor. For example, a resistor or capacitor shown and described herein as a single component may instead be multiple resistors or capacitors, respectively, coupled in parallel between the same nodes. For example, a resistor or capacitor shown and described herein as a single component may instead be multiple resistors or capacitors, respectively, coupled in series between the same two nodes as the single resistor or capacitor.

[0067] The phrase “ground voltage potential” in the foregoing description include a chassis ground, an Earth ground, a floating ground, a virtual ground, a digital ground, a common ground, and/or any other form of ground connection applicable to, or suitable for, the teachings of this description. Unless otherwise stated, “about,” “approximately,” or “substantially” preceding a value means +/- 10 percent of the stated value. Modifications are possible in the described examples, and other examples are possible within the scope of the claims.

CLAIMS

What is claimed is:

1. A circuit, comprising:
 - a multi-modulus (MM) divider having a first input configured to receive an input clock signal, a second input, and an output;
 - a delta-sigma modulator having a first input configured to receive a divide value, a second input coupled to the output of the MM divider, a first output coupled to the second input of the MM divider, and a second output;
 - a digital-to-time converter (DTC) having a first input, a second input, a third input, and an output, the first input coupled to the output of the MM divider, the second input coupled to the second output of the delta-sigma modulator; and
 - a calibration circuit having a first input coupled to the DTC output, a second input coupled to the second delta-sigma modulator, and an output coupled to the third DTC input.
2. The circuit of claim 1, wherein the calibration circuit includes:
 - a correlation circuit having a first input, a second input, a first output, and a second output, the correlation circuit first input configured to receive a phase error signal, the correlation circuit second input coupled to the second output of the delta-sigma modulator;
 - a feedback control circuit having a first input coupled to the correlation circuit first output, a second input coupled to the correlation circuit second output, a first output, and a second output;
 - a parametric integrated nonlinearity (INL) compensation circuit having a first input coupled to the output of the MM divider, a second input coupled to the second output of the delta-sigma modulator, a third input coupled to the second output of the feedback control circuit, and an output coupled to the third input of the DTC; and
 - a gain compensation circuit having an input coupled to the first output of the feedback control circuit and a fourth input of the DTC.
3. The circuit of claim 2, wherein the calibration circuit includes a calibration phase-locked loop (PLL) having an input and an output, the PLL input coupled to the DTC output and the phase error signal provided at the PLL output, wherein the calibration PLL includes:
 - a linear phase detector (PD) having a first input coupled to the output of the DTC, a second input, and an output;
 - a loop filter having an input coupled to the output of the linear PD, and an output;

a bang bang PD having a first input coupled to the output of the DTC, a second input, and an output, the output coupled to the correlation circuit first input;

a tune control circuit having an input coupled to the bang bang PD output and an output;

a voltage-controlled oscillator (VCO) having an input coupled to the loop filter output and the tune control circuit output, and an output;

a divider having an input coupled to the VCO output and an output coupled to the first input of the linear PD and the first input of the bang bang PD.

4. The circuit of claim 1, further comprising:

a detector circuit having a first input, a second input, a first output, and a second output, the detector circuit first input configured to receive a reference signal, the detector circuit second input coupled to the DTC output, and the detector circuit first output coupled to a third input of the calibration circuit; and

voltage-controlled oscillator (VCO) having an input coupled to the detector circuit second output and an output coupled to the first input of the MM divider.

5. The circuit of claim 4, wherein the calibration circuit includes:

a correlation circuit having a first input, a second input, a first output, and a second output, the correlation circuit first input coupled to the detector circuit first output, and the correlation circuit second input coupled to the second output of the delta-sigma modulator;

a feedback control circuit having a first input coupled to the correlation circuit first output, a second input coupled to the correlation circuit second output, a first output, and a second output;

a parametric integrated nonlinearity (INL) compensation circuit having a first input coupled to the feedback control circuit second output, a second input coupled to the feedback control circuit second output, a third input coupled to the second output of the delta-sigma modulator, and an output coupled to the third input of the DTC; and

a gain compensation circuit having an input coupled to the first output of the feedback control circuit and a fourth input of the DTC.

6. The circuit of claim 5, wherein the detector circuit includes:

a linear phase detector (PD) having a first input configured to receive the reference signal, a second input coupled to the output of the DTC, and an output;

a loop filter having an input coupled to the output of the linear PD, and an output coupled to the input of the VCO;

a bang bang PD having a first input configured to receive the reference signal, a second input coupled to the output of the DTC, and an output, the output coupled to the correlation circuit first input; and

a tune control circuit having an input coupled to the bang bang PD output and an output coupled to the input of the VCO.

7. The circuit of claim 4, wherein the calibration circuit is configured to:
compare an output of the DTC to the reference signal to determine a phase error signal;
correlate the phase error signal to multiple basis functions that are each a function of a residual error of the delta-sigma modulator to determine correlation values; and
control gain and parametric integrated nonlinearity (INL) adjustments of the DTC based on the correlation to cause the correlation values to converge to zero average.

8. The circuit of claim 1, wherein the calibration circuit is configured to:
compare an output of the DTC to a second input clock signal to determine a phase error signal;
correlate the phase error signal to multiple basis functions that are each a function of a residual error of the delta-sigma modulator to determine correlation values; and
control gain and parametric integrated nonlinearity (INL) adjustments of the DTC based on the correlation to cause the correlation values to converge to zero average.

9. A circuit, comprising:
a clock divider including a digital-to-time converter (DTC); and
a calibration circuit coupled to the clock divider, the calibration circuit configured to:
determine a gain error and a parametric integrated nonlinearity (INL) error of the DTC;
determine a gain adjustment value and a INL adjustment value to compensate for the gain error and the INL error; and
modify operation of the DTC according to the gain adjustment value and the INL adjustment value to correct for the gain error and the INL error.

10. The circuit of claim 9, wherein to determine the gain error and the INL error of the DTC the calibration circuit is configured to:
compare an output signal of the DTC to a reference signal to determine a phase error signal;
correlate the phase error signal to multiple basis functions that are each a function of a

residual error of a delta-sigma modulator of the clock divider to determine correlation values; and
determine the gain adjustment value and the INL adjustment value based on the determined correlation values, the gain adjustment value and the INL adjustment value determined to cause the correlation values to converge to zero average.

11. The circuit 10, wherein to determine the phase error signal, the calibration circuit includes a bang bang phase detector configured to compare the reference signal to the output signal of the DTC to provide the phase error signal.

12. The circuit of claim 10, wherein the multiple basis functions include at least one basis function for the gain error and at least one basis function for the INL error.

13. The circuit of claim 12, wherein the multiple basis functions have zero direct current components.

14. The circuit of claim 12, wherein the multiple basis functions include a first basis function for a fundamental frequency and a second basis function for a second harmonic frequency.

15. The circuit of claim 10, wherein the calibration circuit is configured to filter the basis functions prior to performing the correlation.

16. The circuit of claim 9, wherein the calibration circuit is configured to correct for a mismatch error of the DTC according to a look-up table.

17. A system, comprising:

a controller configured to provide a control signal;

a clock divider coupled to the controller, the clock divider including a digital-to-time converter (DTC) configured to modify a received clock signal according to the control signal to form a modified clock signal;

a calibration circuit coupled to the clock divider, the calibration circuit configured to:

determine a gain error and a parametric integrated nonlinearity (INL) error of the DTC;

determine a gain adjustment value and a INL adjustment value to compensate for the gain error and the INL error; and

modify operation of the DTC according to the gain adjustment value and the INL adjustment value to correct for the gain error and the INL error; and

a component coupled to the clock divider and configured to receive the modified clock signal from the clock divider and operate according to the modified clock signal.

18. The system of claim 17, wherein to determine the gain error and the INL error of the DTC the calibration circuit is configured to:

compare an output signal of the DTC to a reference signal to determine a phase error signal;
correlate the phase error signal to multiple basis functions that are each a function of a residual error of a delta-sigma modulator of the clock divider to determine correlation values; and
determine the gain adjustment value and the INL adjustment value based on the determined correlation values, the gain adjustment value and the INL adjustment value determined to cause the correlation values to converge to zero average.

19. The system of claim 18, wherein to determine the phase error signal, the calibration circuit includes a bang bang phase detector configured to compare the reference signal to the output signal of the DTC to provide the phase error signal.

20. The system of claim 18, wherein the multiple basis functions are orthogonal to each other, with at least one basis function for the gain error and at least one basis function for the INL error.

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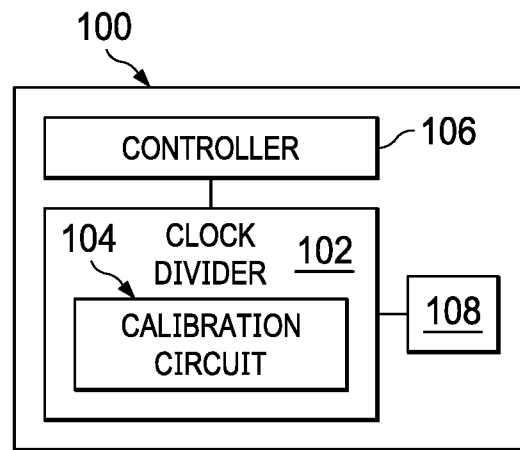


FIG. 1

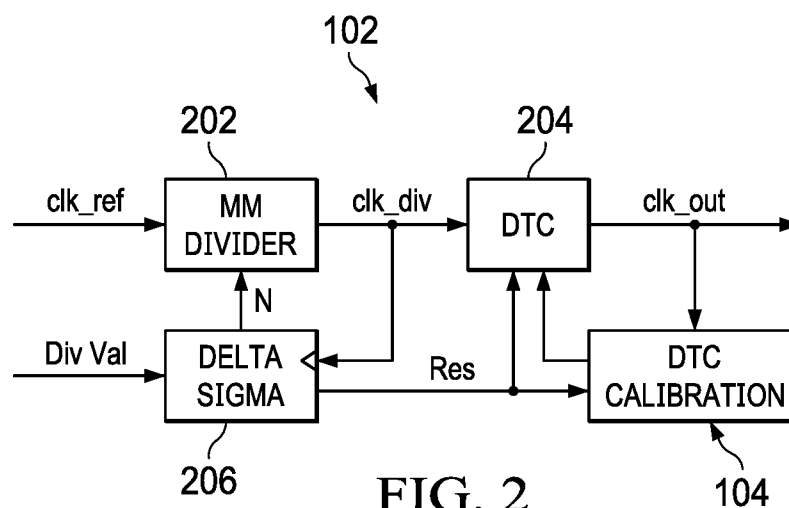
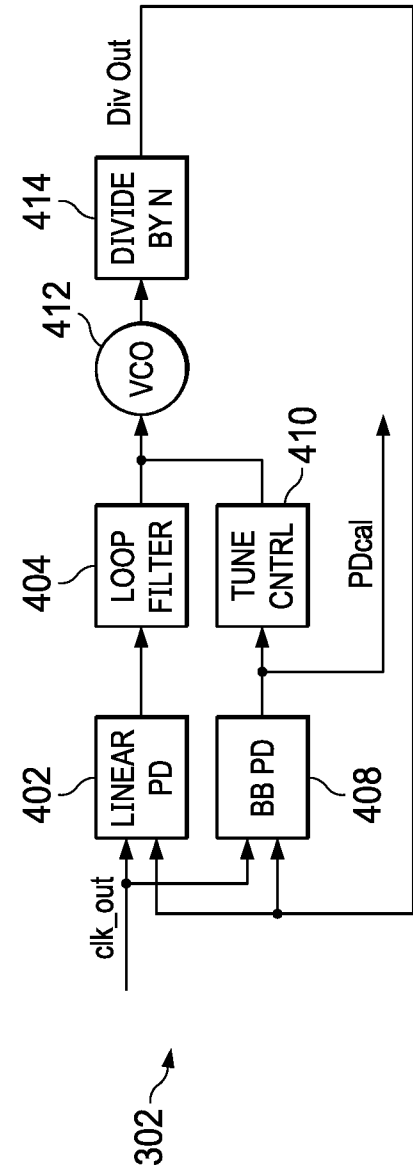
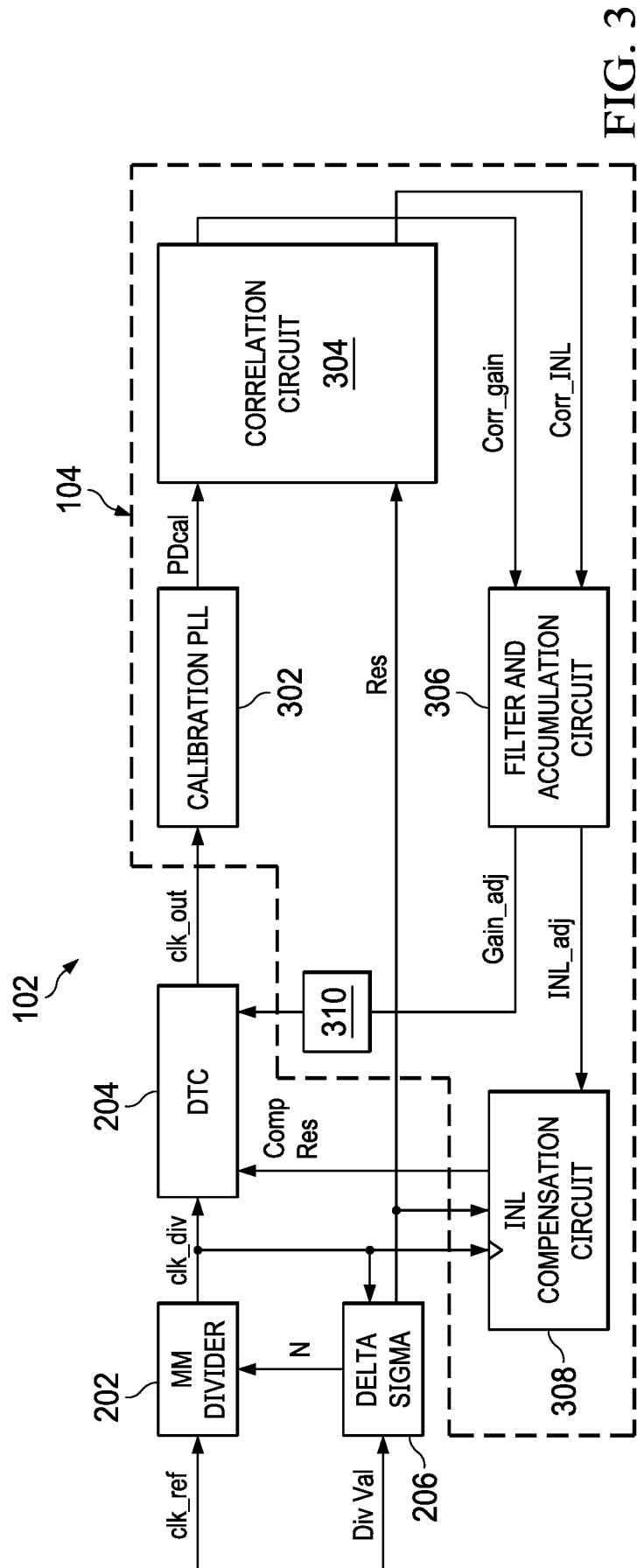


FIG. 2



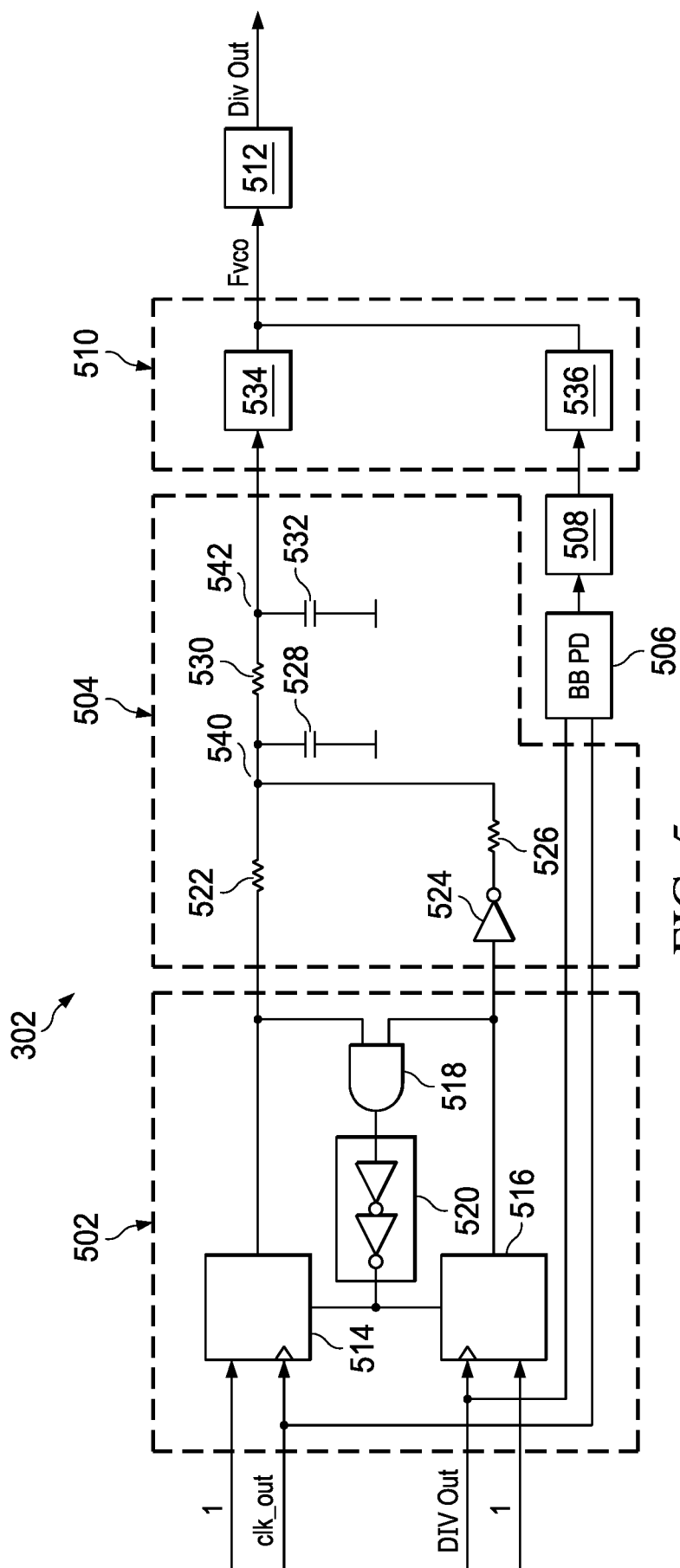
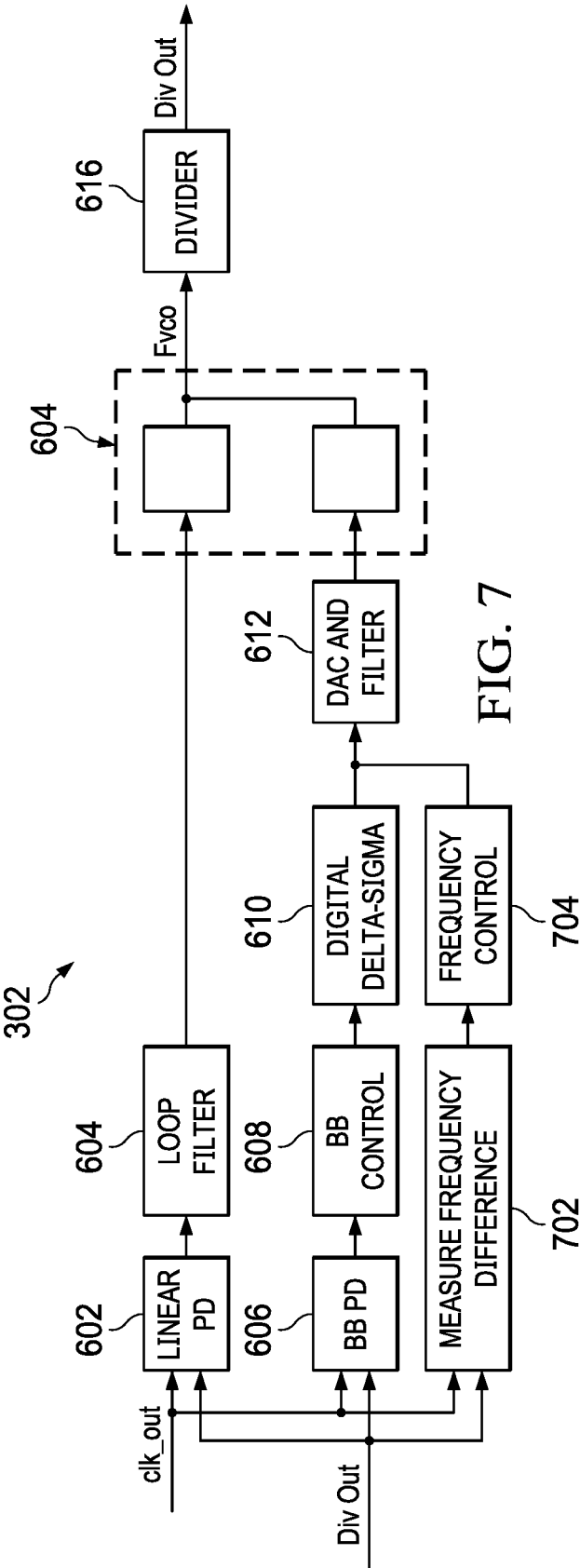
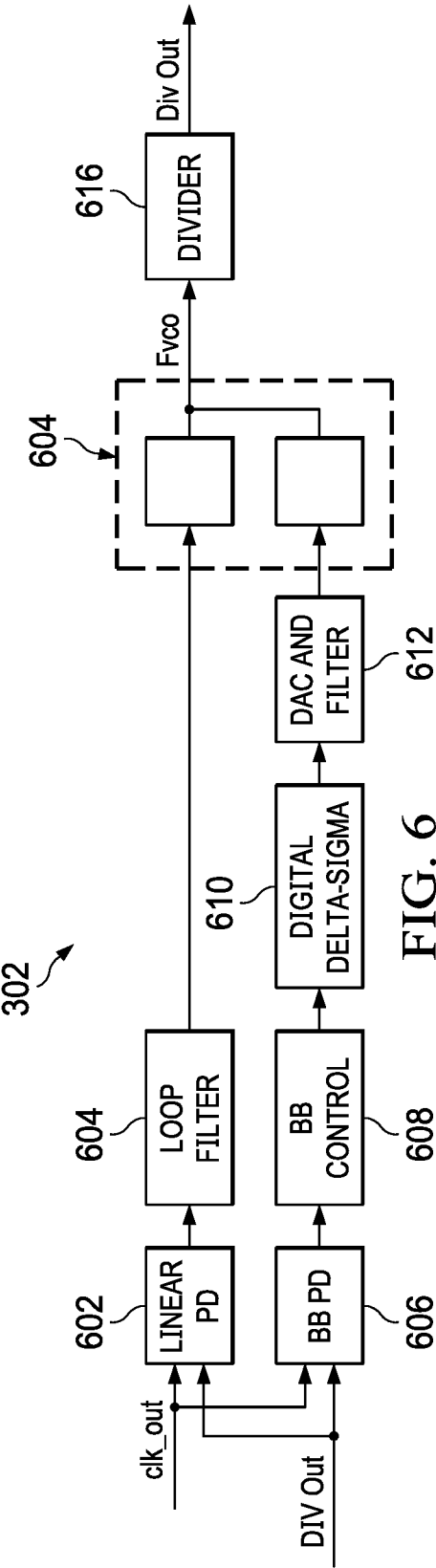
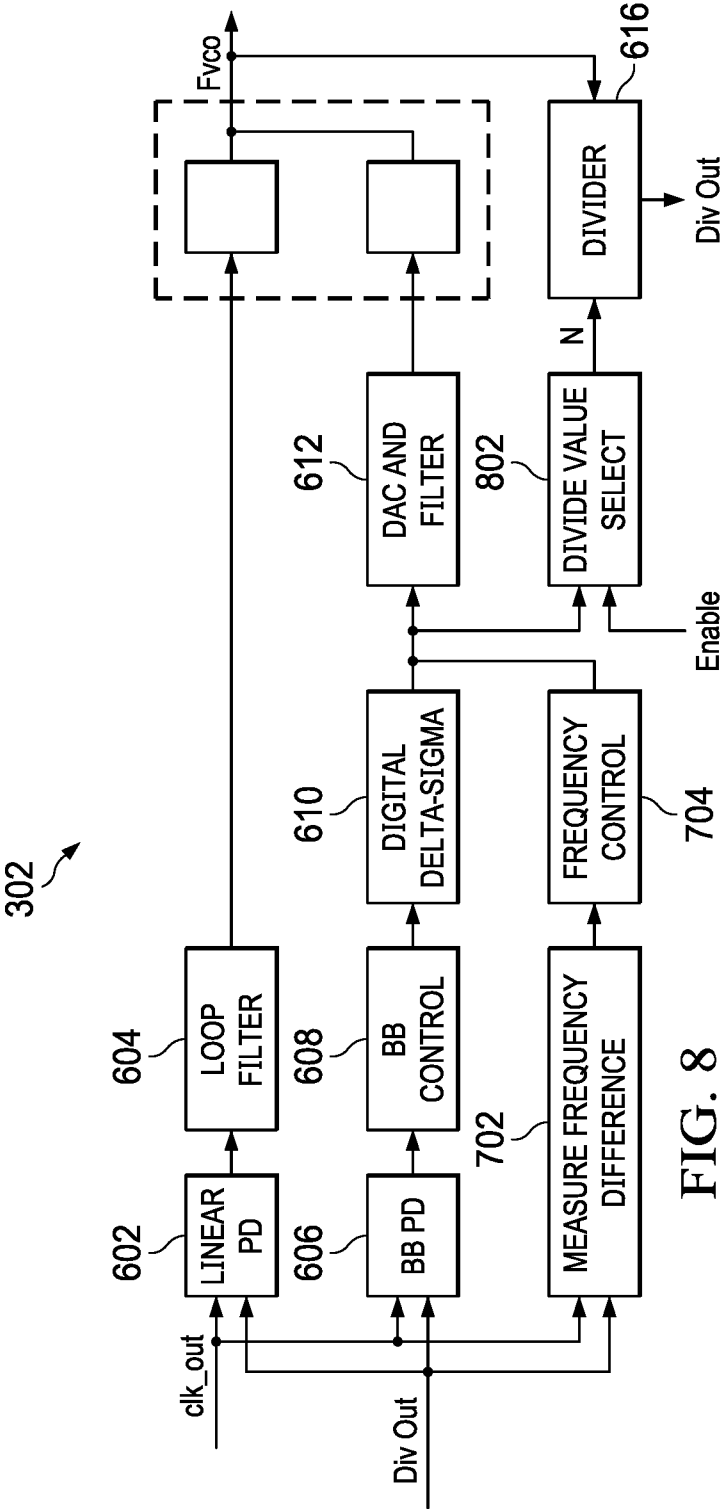
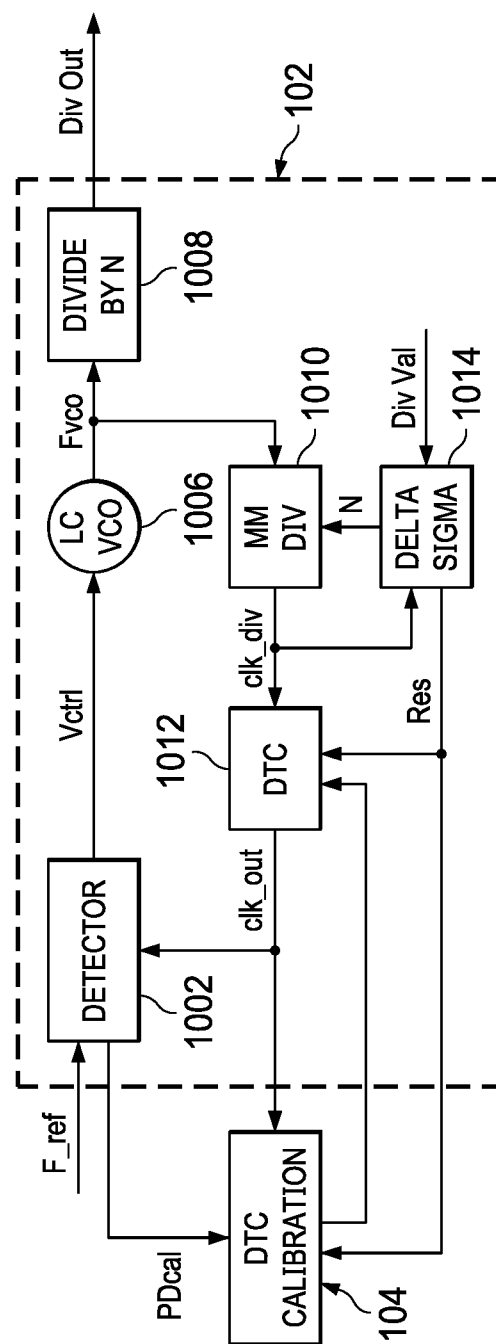
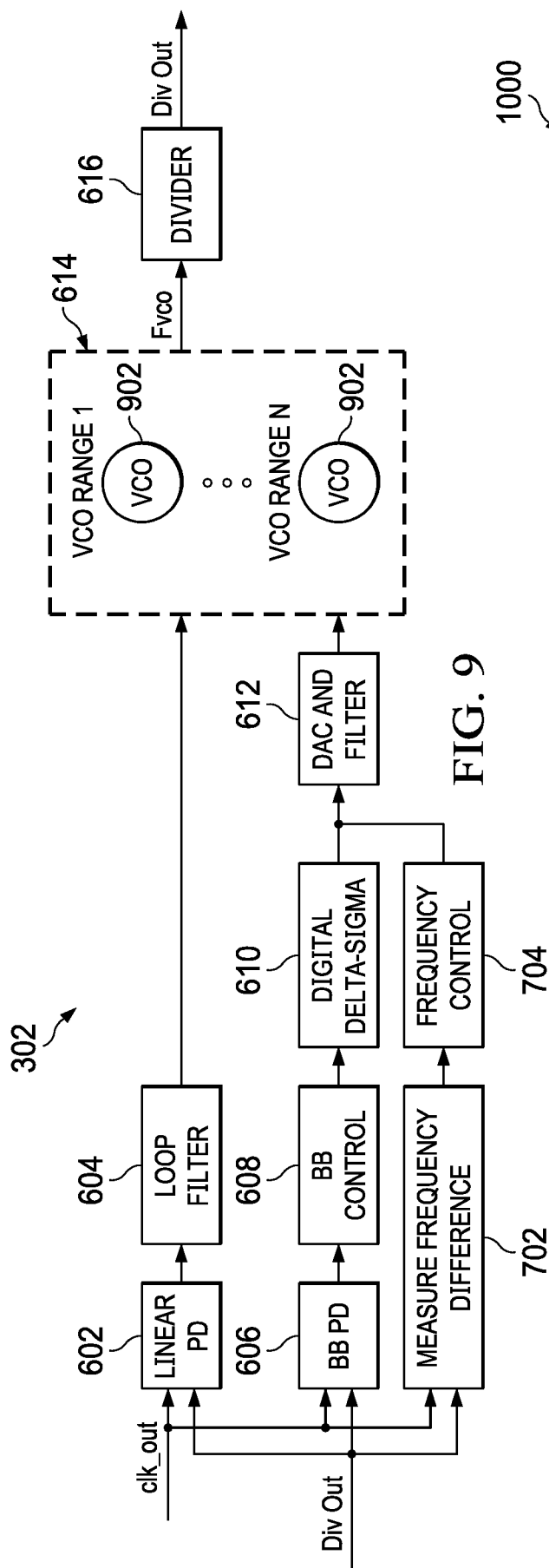


FIG. 5







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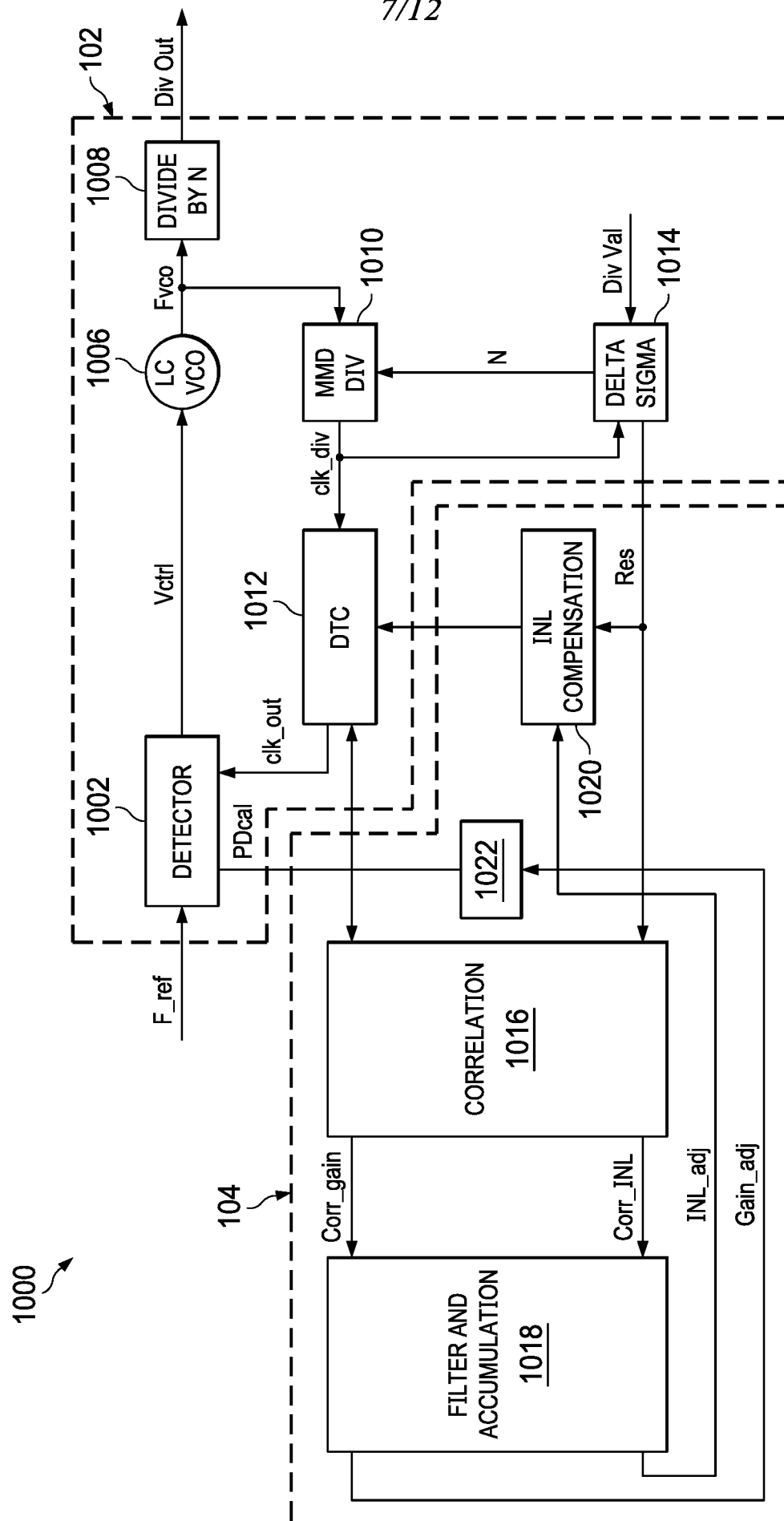


FIG. 11

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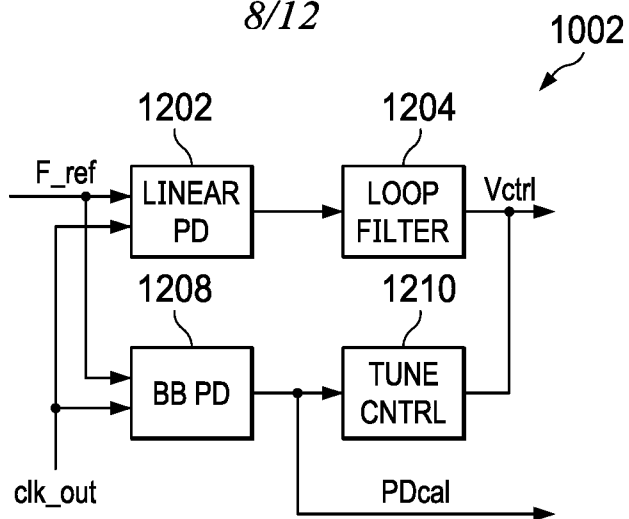


FIG. 12

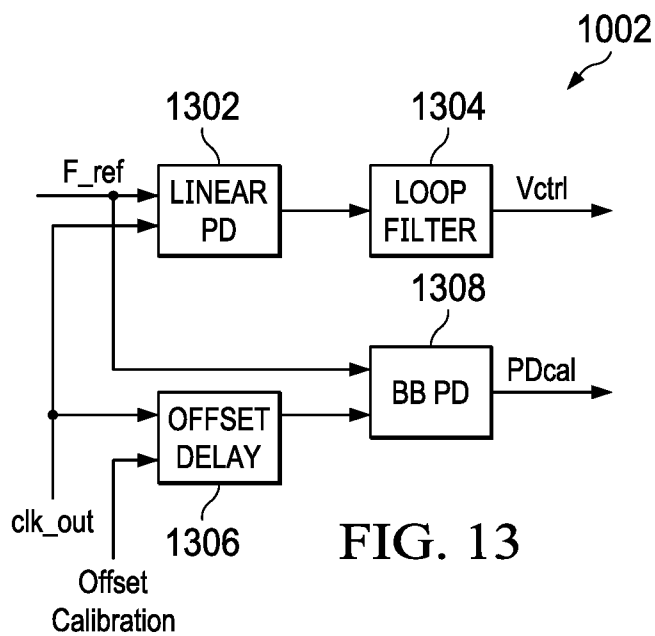


FIG. 13

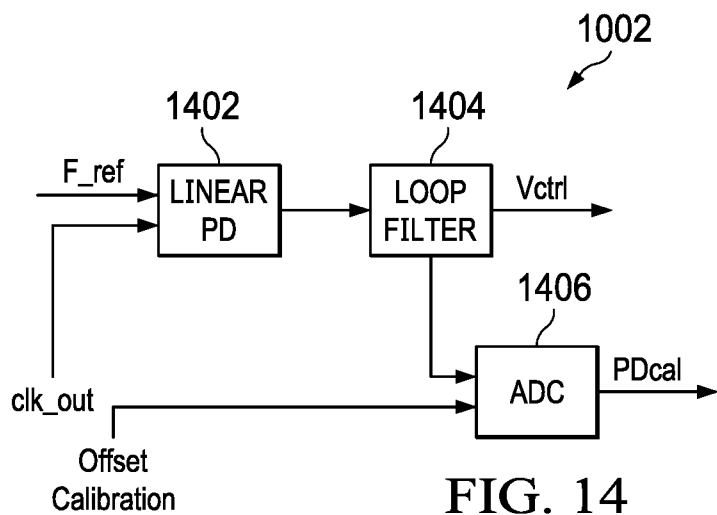


FIG. 14

FIG. 15

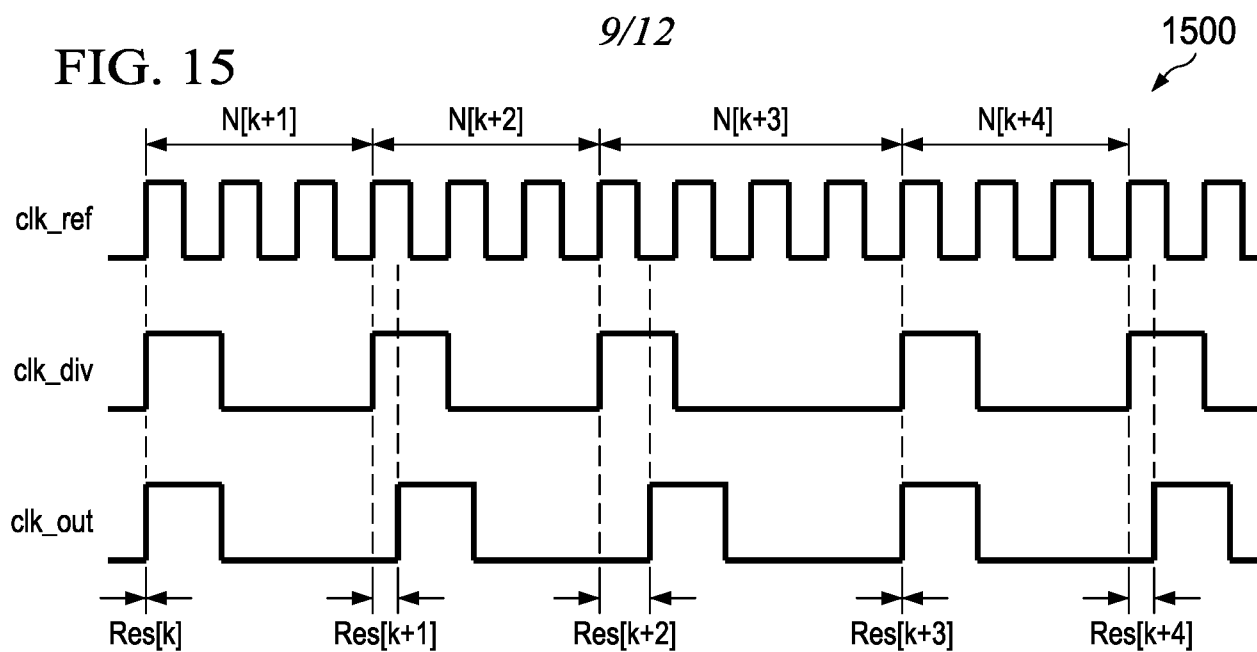


FIG. 16

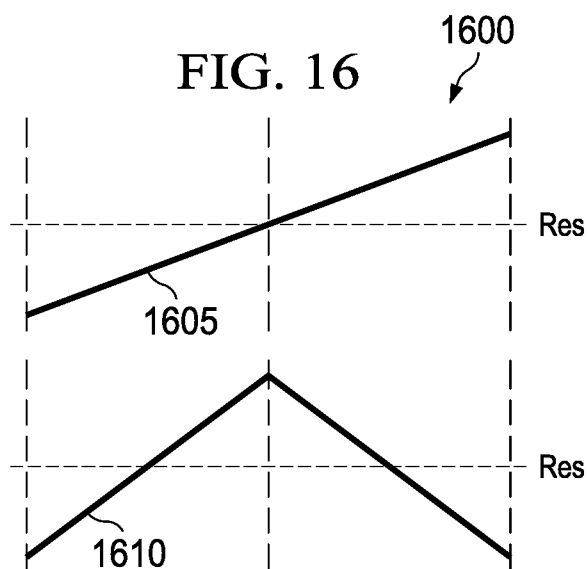


FIG. 17

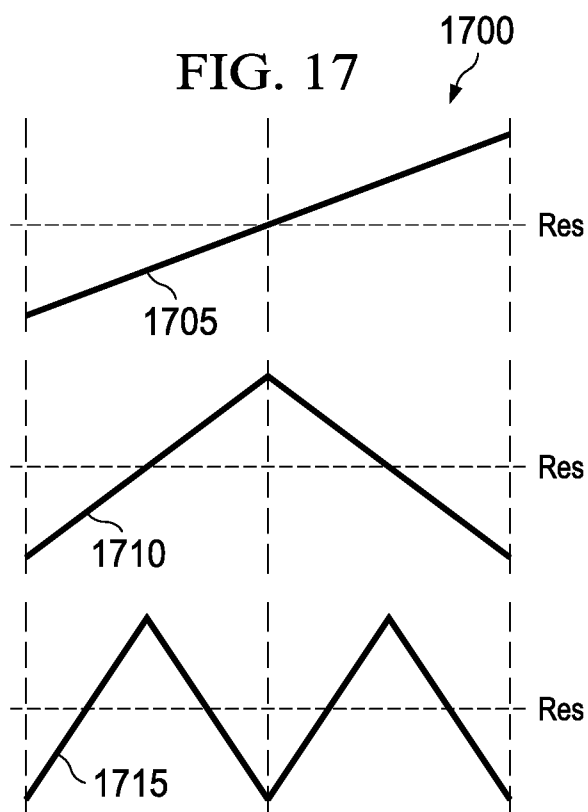
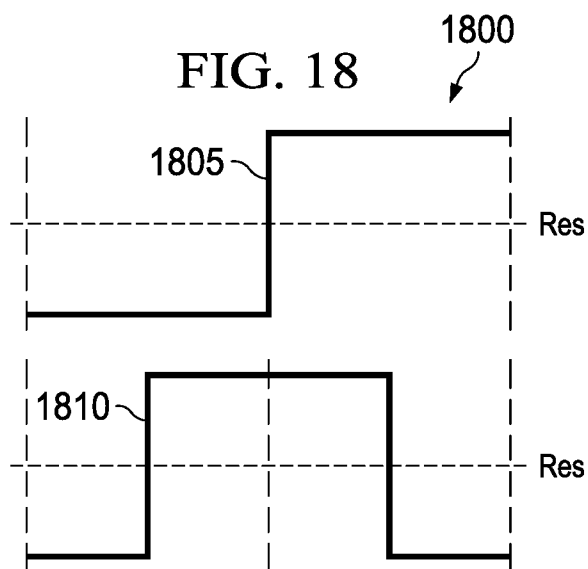


FIG. 18



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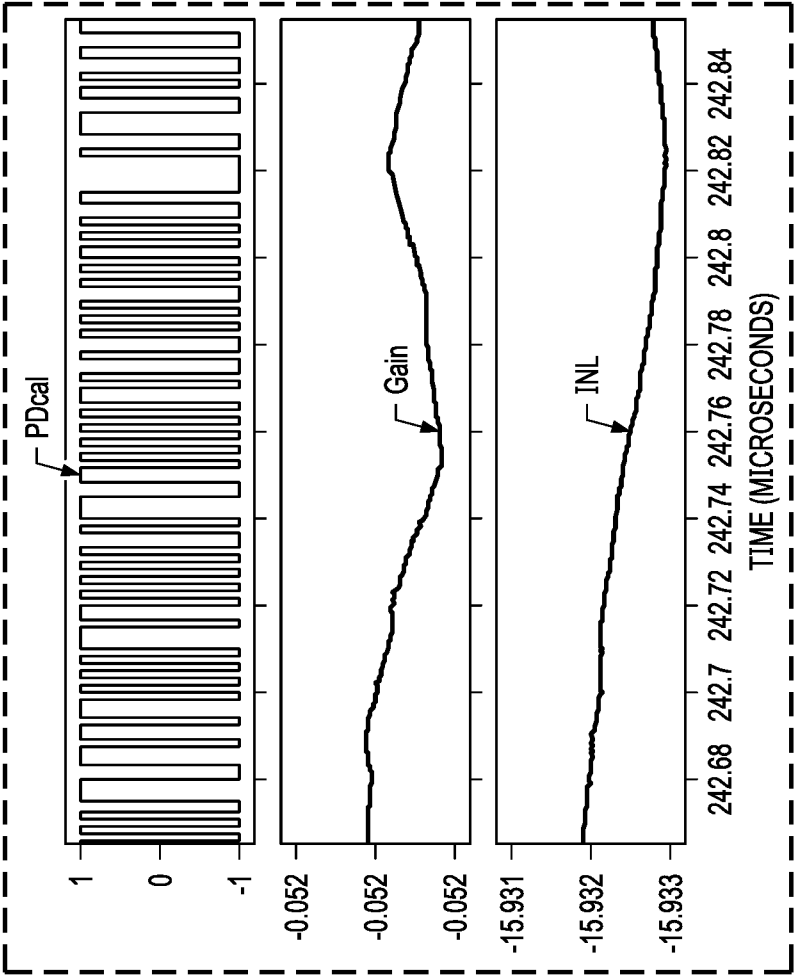
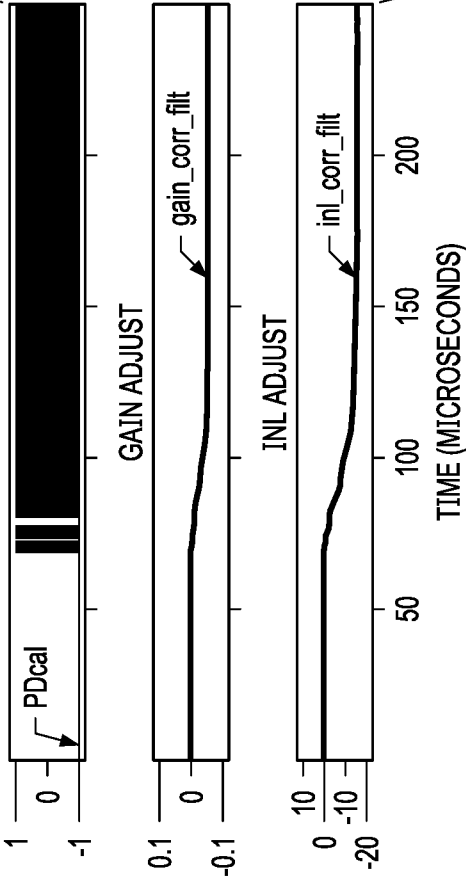
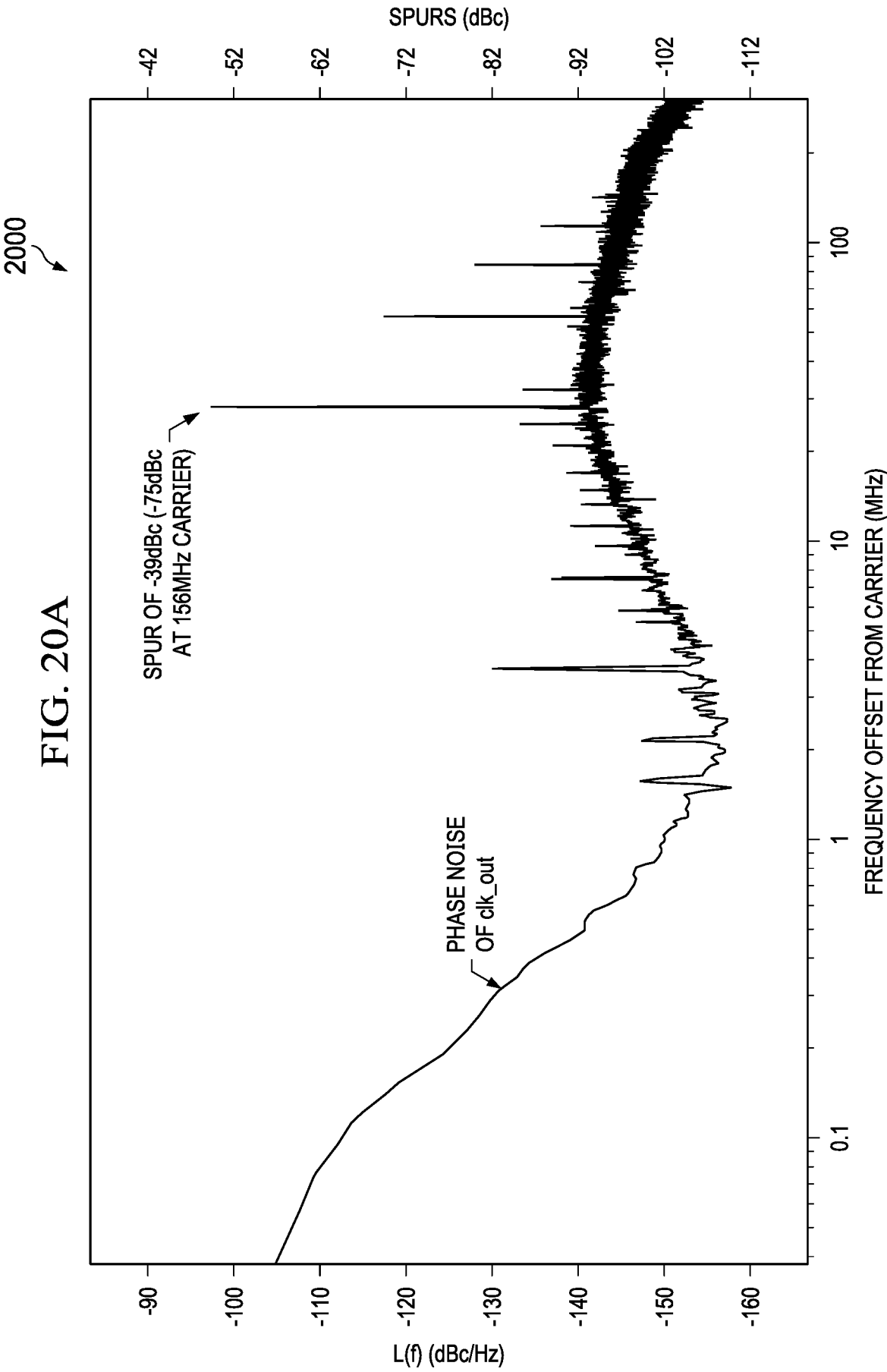
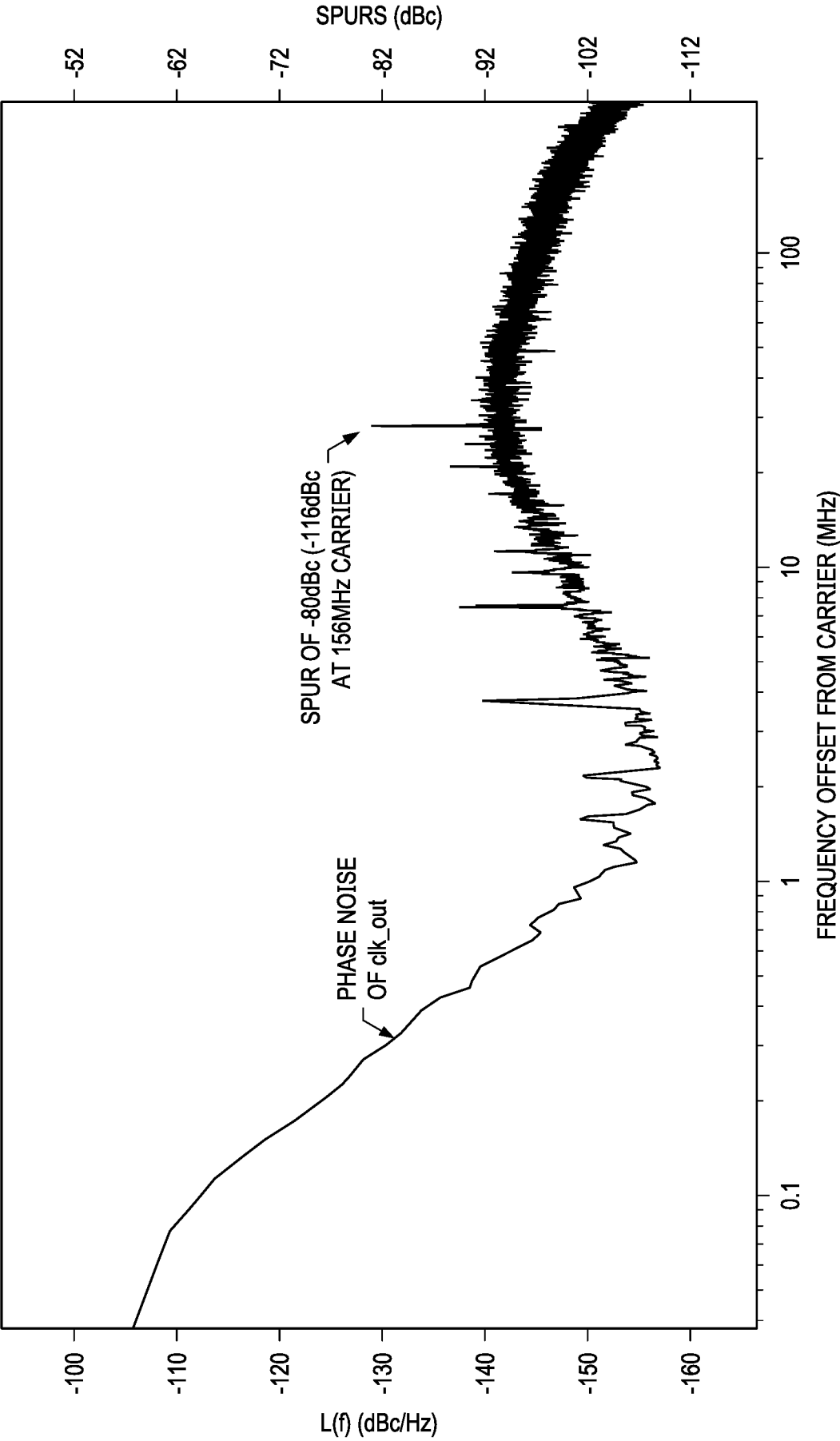


FIG. 19



2005

FIG. 20B



INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2022/012085

A. CLASSIFICATION OF SUBJECT MATTER		
<i>H03M 1/82 (2006.01)</i> <i>H03K 3/02 (2006.01)</i>		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
H03M 1/00, 1/10, 1/66, 1/82, H03K 3/00, 3/02		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	US 8860514 B2 (SILICON LAB INC) 14.10.2014, claim 1, col. 2, lines 40-46, fig. 1	9, 16-17 1-8, 10-15, 18-20
Y	US 8994573 B2 (INTEL MOBILE COMM GMBH) 31.03.2015, col. 10, lines 8-12, 35-38, 43-47, 62-66, fig. 11A	9, 16-17
Y	US 10707883 B2 (SI-WARE SYSTEMS S.A.E.) 07.07.2020, col. 16, lines 58-60	9, 16-17
A	US 2016/0373120 A1 (SI WARE SYSTEMS S A E) 22.12.2016	1-20
A	US 9678481 B1 (INTEGRATED DEVICE TECH) 13.06.2017	1-20
☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.		
* Special categories of cited documents: “A” document defining the general state of the art which is not considered to be of particular relevance “D” document cited by the applicant in the international application “E” earlier document but published on or after the international filing date “L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) “O” document referring to an oral disclosure, use, exhibition or other means “P” document published prior to the international filing date but later than the priority date claimed “T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention “X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone “Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art “&” document member of the same patent family		
Date of the actual completion of the international search		Date of mailing of the international search report
23 March 2022 (23.03.2022)		07 April 2022 (07.04.2022)
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37		Authorized officer G. Razhev Telephone No. 8 499 240 25 91