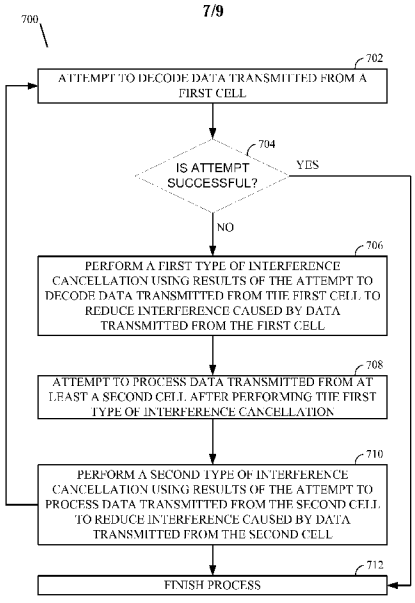

FIG. 7

Certain aspects of the present disclosure relate to a hybrid approach for Physical Downlink Shared Channel (PDSCH) Interference Cancellation (IC). In certain aspects, if the PDSCH information is known for a serving cell but not be known for interfering cell(s), a hybrid approach that involves using Codeword-level IC (CWIC) for the serving cell and using Symbol-level IC (SLIC) for the interfering cells may be used for better IC performance. The hybrid IC approach may start with a UE attempting to decode the serving cell PDSCH. If the decode is unsuccessful, the UE may perform CWIC for the serving cell followed by SLIC using the results of the CWIC stage. After the SLIC stage, the UE may attempt to decode the serving cell PDSCH again. The UE may perform multiple operations of this method until the serving cell PDSCH is successfully decoded or a maximum number of iterations is reached.

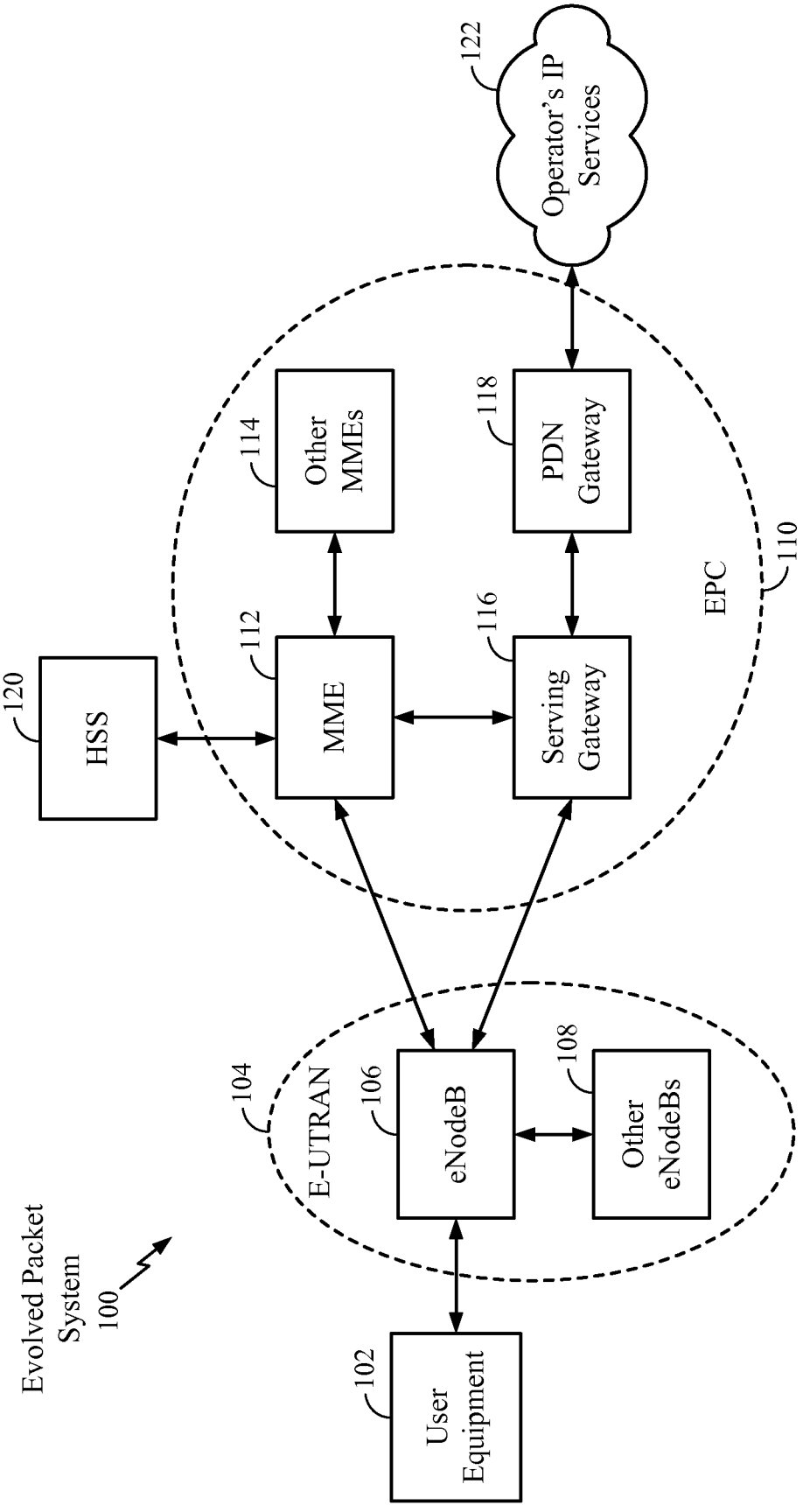
Evolved Packet System
100
User Equipment
102
E-UTRAN
104
eNodeB
106
Other eNodeBs
108
EPC
110
MME
112
Other MMEs
114
Serving Gateway
116
PDN Gateway
118
HSS
120
Operator's IP Services
122

FIG. 1

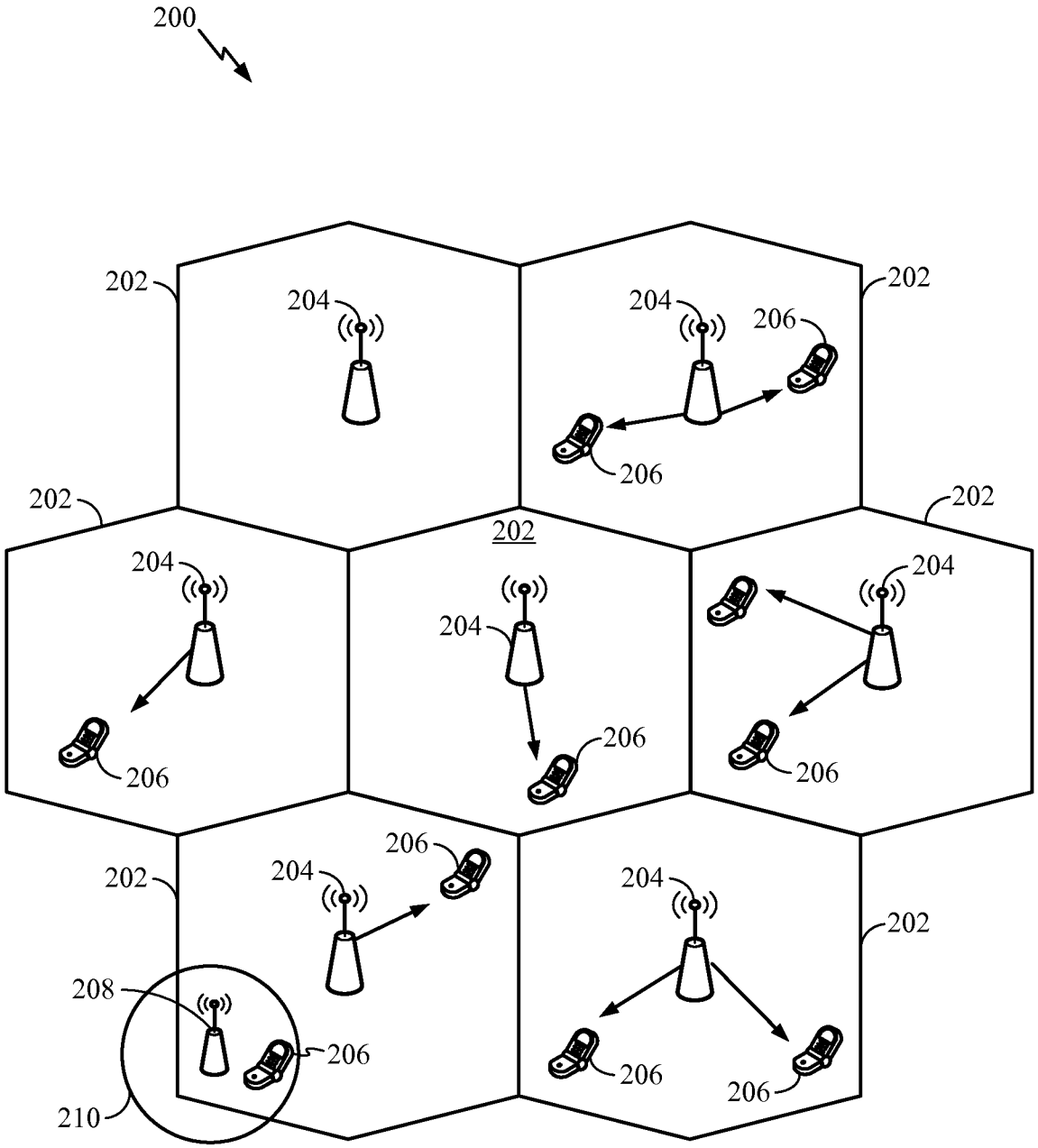

FIG. 2

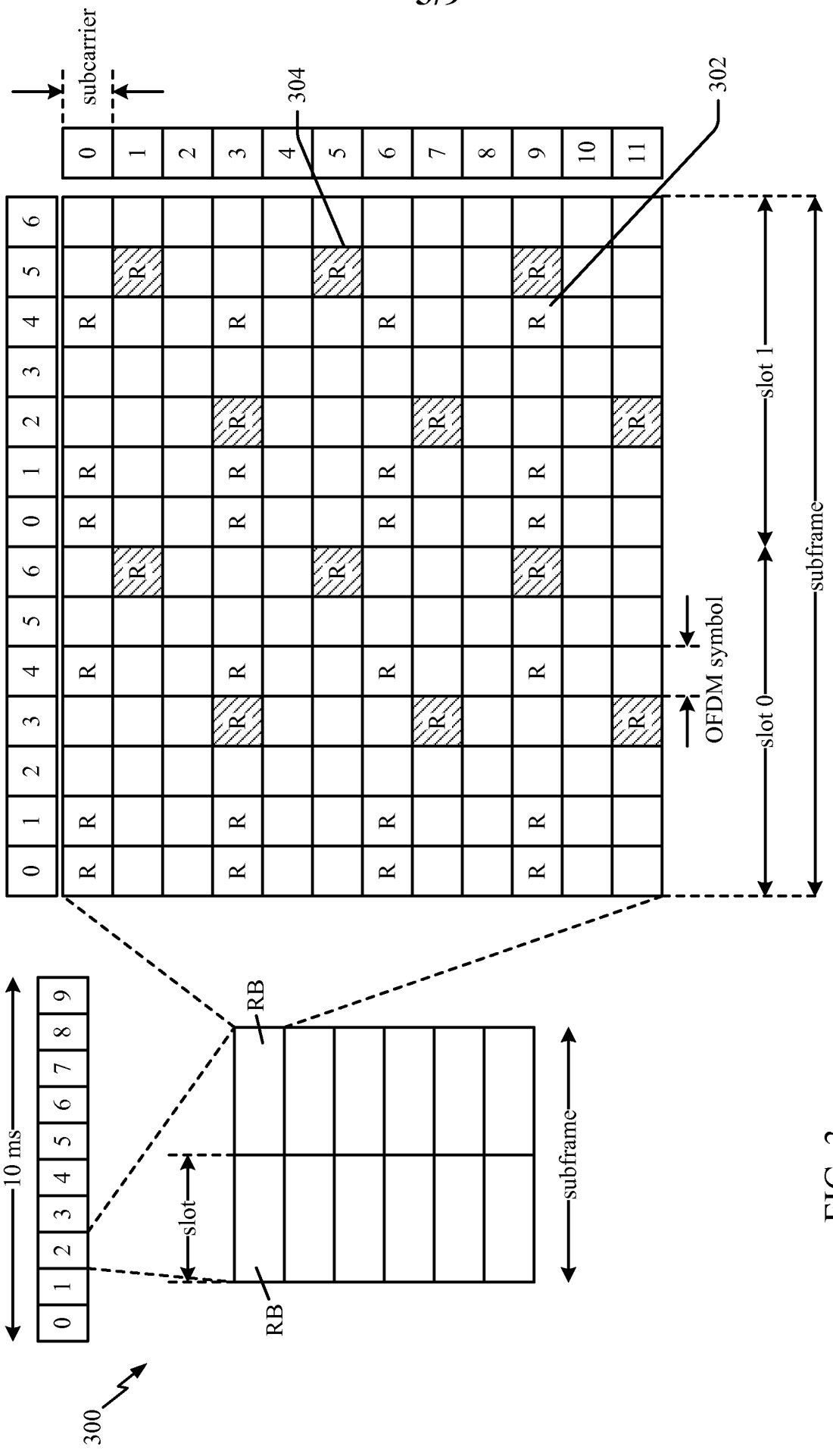
subcarrier
304
302
0 1 2 3 4 5 6 7 8 9 10 11
0 1 2 3 4 5 6
R
OFDM symbol
slot 0
slot 1
subframe
10 ms
0 1 2 3 4 5 6 7 8 9
slot
RB
RB
subframe
300

FIG. 3

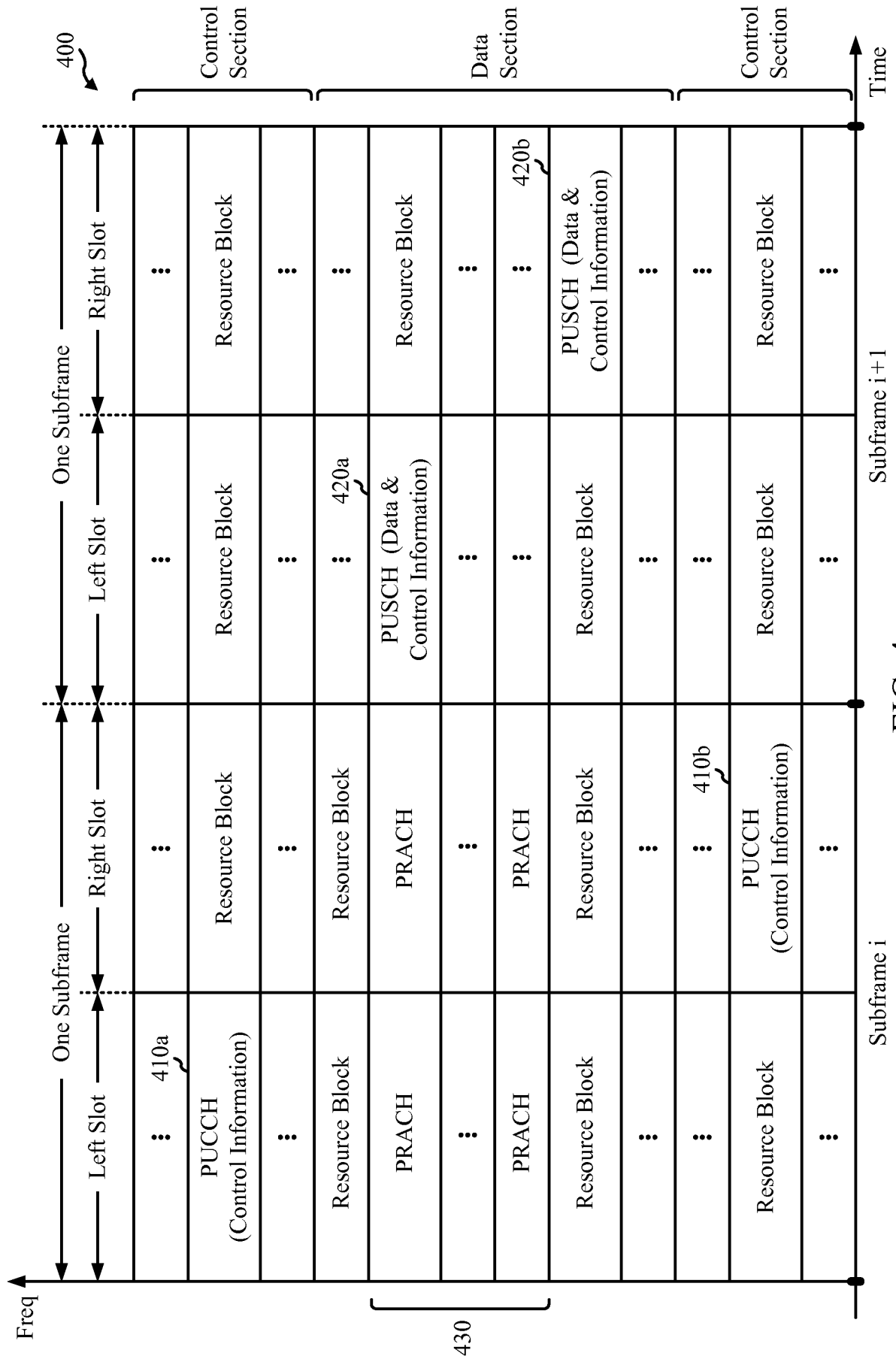
400
Control Section
Data Section
Control Section
One Subframe
Left Slot
Right Slot
Left Slot
Right Slot
Freq
Time
410a
PUCCH (Control Information)
Resource Block
PRACH
420a
PUSCH (Data & Control Information)
420b
410b
PUCCH (Control Information)
430
Subframe i
Subframe i+1

FIG. 4

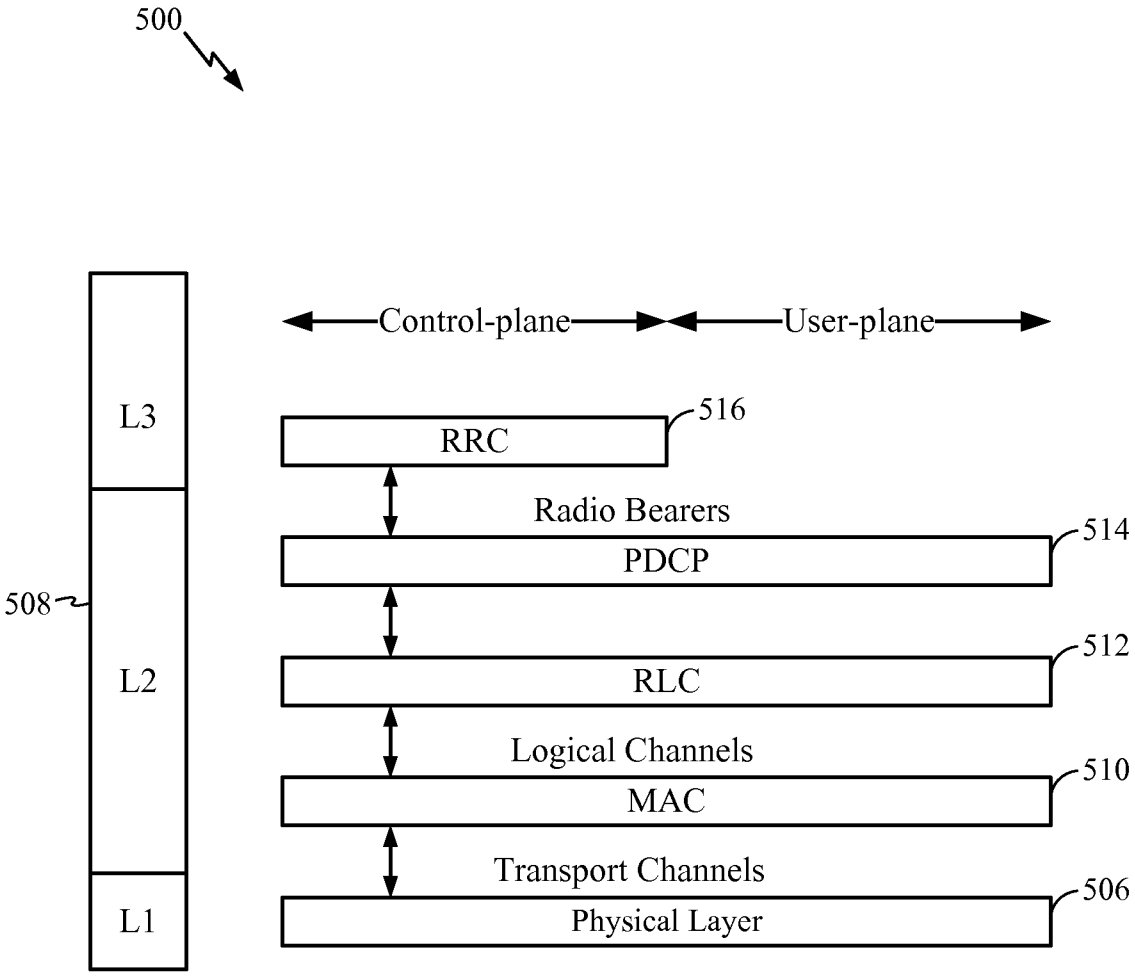
500
Control-plane
User-plane
L3
L2
L1
508
RRC
516
Radio Bearers
PDCP
514
RLC
512
Logical Channels
MAC
510
Transport Channels
Physical Layer
506

FIG. 5

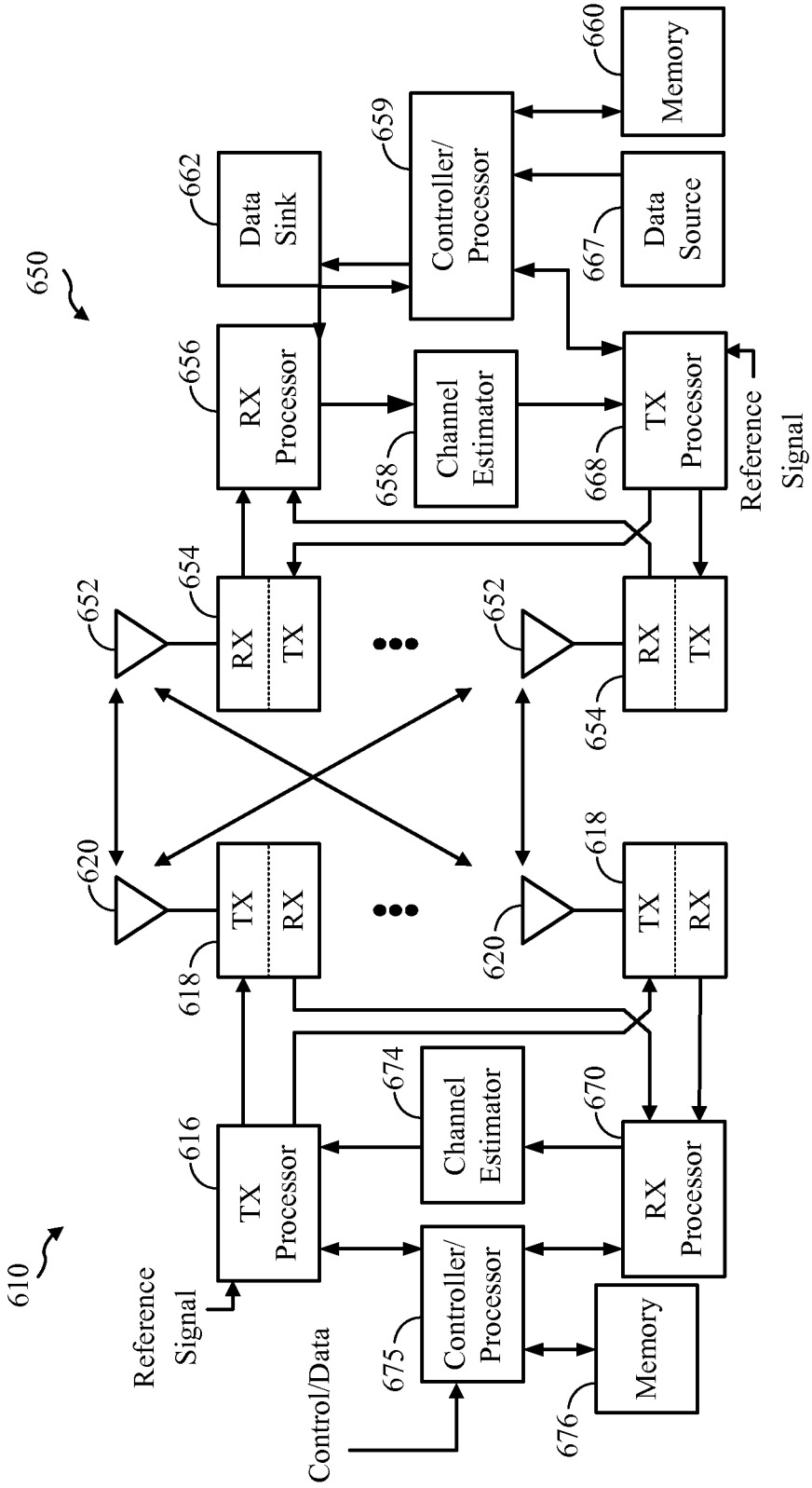
610
650
Reference Signal
Control/Data
675
Controller/ Processor
676
Memory
616
TX Processor
674
Channel Estimator
670
RX Processor
618
TX
RX
620
652
654
RX
TX
656
RX Processor
658
Channel Estimator
668
TX Processor
Reference Signal
662
Data Sink
659
Controller/ Processor
660
Memory
667
Data Source

FIG. 6

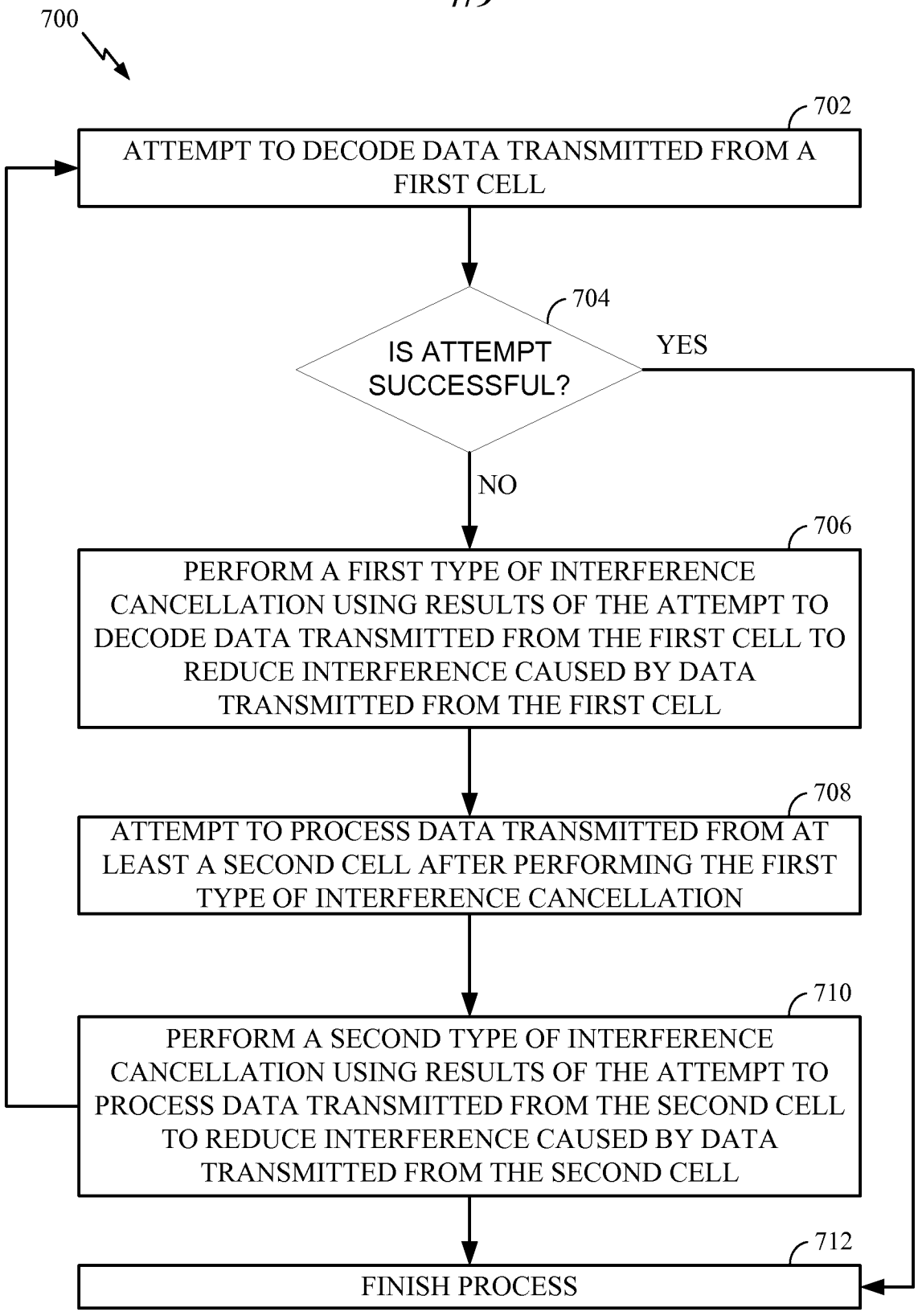
700
702
ATTEMPT TO DECODE DATA TRANSMITTED FROM A FIRST CELL
704
IS ATTEMPT SUCCESSFUL?
YES
NO
706
PERFORM A FIRST TYPE OF INTERFERENCE CANCELLATION USING RESULTS OF THE ATTEMPT TO DECODE DATA TRANSMITTED FROM THE FIRST CELL TO REDUCE INTERFERENCE CAUSED BY DATA TRANSMITTED FROM THE FIRST CELL
708
ATTEMPT TO PROCESS DATA TRANSMITTED FROM AT LEAST A SECOND CELL AFTER PERFORMING THE FIRST TYPE OF INTERFERENCE CANCELLATION
710
PERFORM A SECOND TYPE OF INTERFERENCE CANCELLATION USING RESULTS OF THE ATTEMPT TO PROCESS DATA TRANSMITTED FROM THE SECOND CELL TO REDUCE INTERFERENCE CAUSED BY DATA TRANSMITTED FROM THE SECOND CELL
712
FINISH PROCESS

FIG. 7

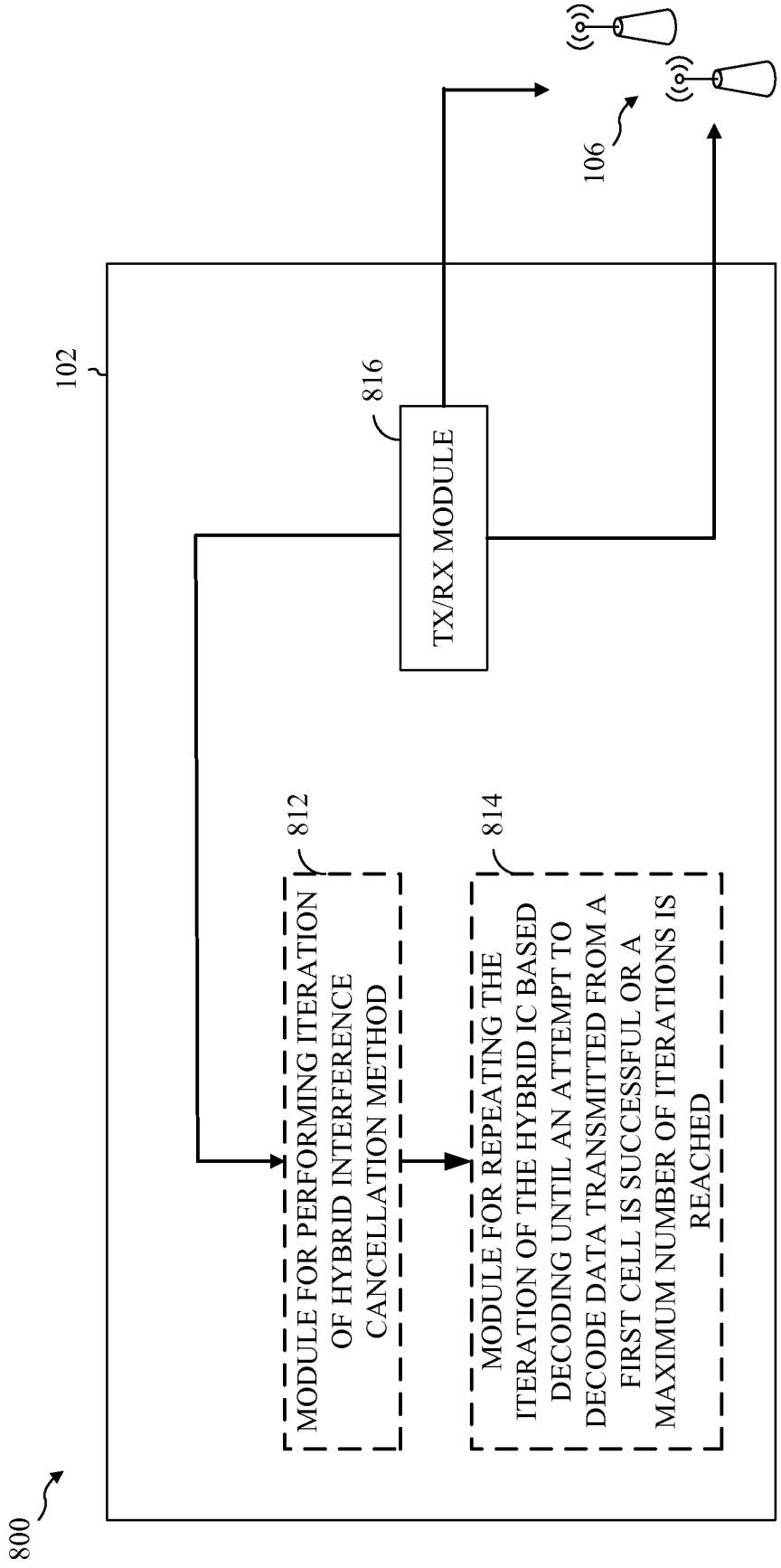
800
102
106
816
TX/RX MODULE
812
MODULE FOR PERFORMING ITERATION OF HYBRID INTERFERENCE CANCELLATION METHOD
814
MODULE FOR REPEATING THE ITERATION OF THE HYBRID IC BASED DECODING UNTIL AN ATTEMPT TO DECODE DATA TRANSMITTED FROM A FIRST CELL IS SUCCESSFUL OR A MAXIMUM NUMBER OF ITERATIONS IS REACHED

FIG. 8

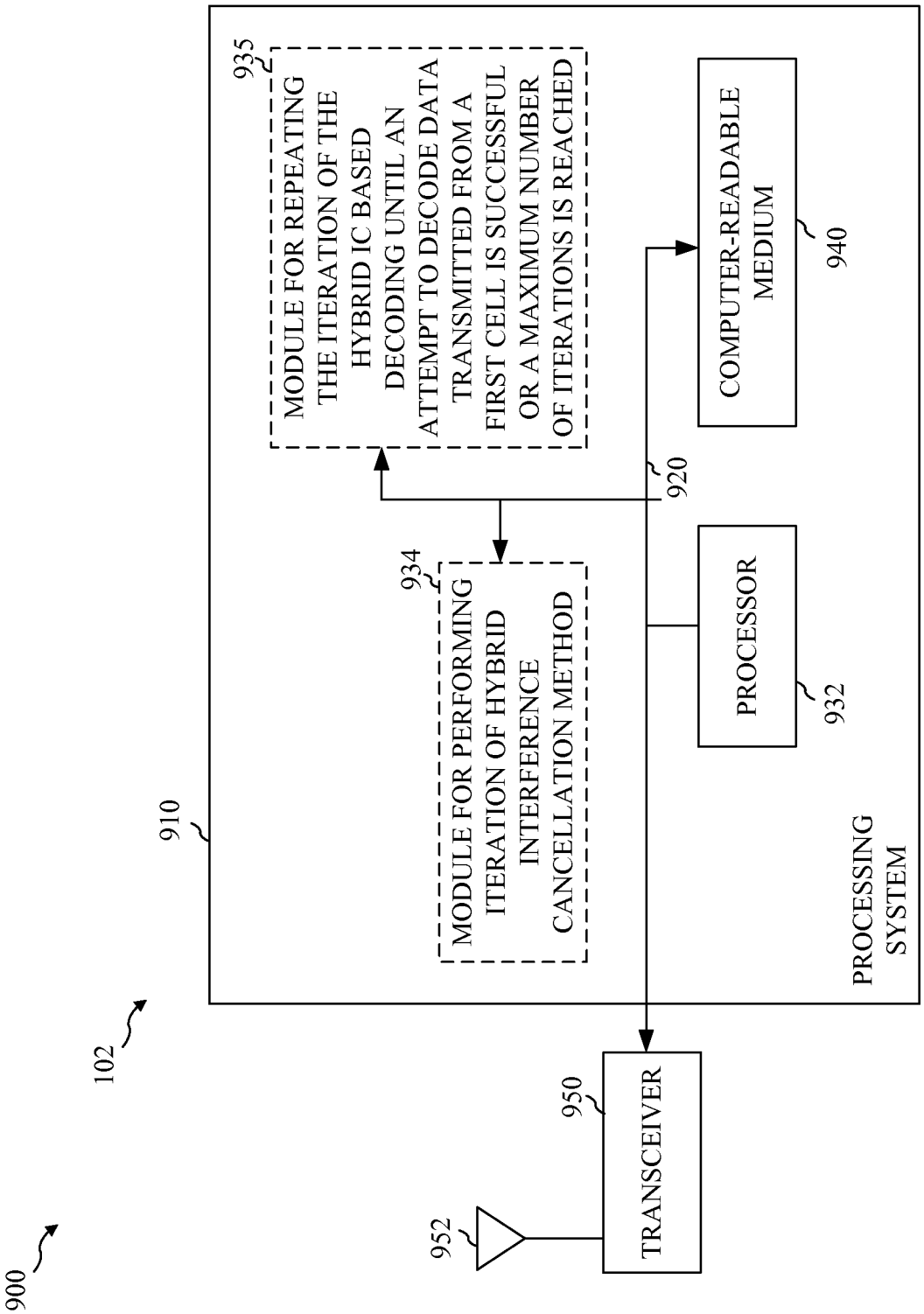
900
102
910
PROCESSING SYSTEM
935
MODULE FOR REPEATING THE ITERATION OF THE HYBRID IC BASED DECODING UNTIL AN ATTEMPT TO DECODE DATA TRANSMITTED FROM A FIRST CELL IS SUCCESSFUL OR A MAXIMUM NUMBER OF ITERATIONS IS REACHED
934
MODULE FOR PERFORMING ITERATION OF HYBRID INTERFERENCE CANCELLATION METHOD
920
PROCESSOR
932
COMPUTER-READABLE MEDIUM
940
950
TRANSCEIVER
952

FIG. 9