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(54) **Title:** SYSTEM AND METHOD FOR AUTOMATIC ELIMINATION OF DESIGN RULE VIOLATIONS DURING CONSTRUCTION OF A MASK LAYOUT BLOCK

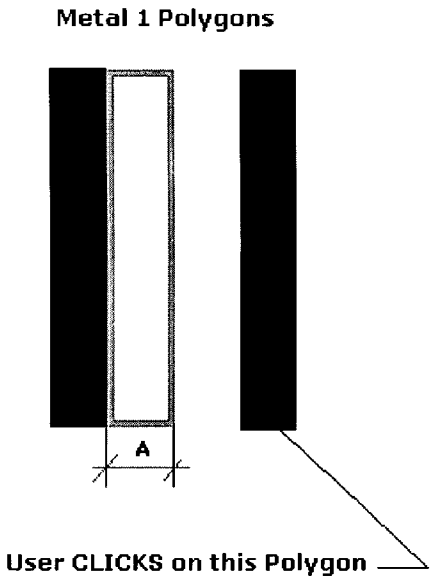

Figure #3

(57) **Abstract:** A system and method for automatic elimination of design rule violations during construction of a mask layout block are disclosed. The method includes analyzing a selected position for a polygon in a mask layout block and obtaining one or more design rules associated with the polygon from a technology file. The method provides an Advise Area associated with the selected position for the polygon that graphically represents space, enclosure, width, notch or any other topological condition in the mask layout block where the selected position complies with the design rule violation. The Advice Area is associated with the selected position to alert the mask designer about any process design rule violation. The method and system also provides an option to automatically correct the identified process design rule, maintaining the process design rules (DRC Clean), layout connectivity (LVS Clean), Circuit Timing constraints and DFM (Design for Manufacturing) correctness.

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System and method for automatic elimination of design rule violations during construction of a mask layout block

BACKGROUND OF INVENTION

TECHNICAL FIELD OF THE INVENTION

The present invention is generally related to the field of integrated circuits, and more particularly to a system and method for automatic elimination of process design rules violations during construction of a mask layout block, maintaining the process design rules (DRC Clean), layout connectivity (LVS Clean), Circuit Timing Constraints and DFM (Design For Manufacturing) correctness, in the integrated circuit mask layout database.

BACKGROUND OF THE INVENTION

Over the past several years, the number of transistors in a semiconductor device has increased dramatically. Due to this increase, the time to design and manufacture semiconductor devices has also increased.

A typical semiconductor design process includes numerous steps. Initially, a circuit designer prepares a schematic diagram that includes logical connections between logic elements that together form an integrated circuit. The schematic diagram is then tested to verify that the logic elements and associated logical connections perform a desired function. Once the circuit is verified, the schematic diagram is converted into a mask layout database that includes a series of polygons. The polygons may

represent the logic elements and the logical connections contained in the schematic diagram. The mask layout database is then converted into multiple photomasks, also known as masks or reticles that may be used to

image different layers of the integrated circuit on to a semiconductor wafer. Typically, the mask layout database is created manually by a layout designer or automatically by a synthesis tool. In a 0.13 micron or below manufacturing process, the layout designer or synthesis tool may have to use thousands of design rules to create the mask layout database. The large number of design rules adds complexity to the layout design process because the layout designer may have to memorize or constantly look up the design rules to place polygons in the mask layout database. Since the process may be completely manual, the layout designer may create design rule violations during the construction of the mask layout database. In order to correct the design rule violations, spacing between polygons on the same layer and dimensions of polygons are compared to the design rules included in a technology file for a desired manufacturing process. This comparison may identify design rule violations if the spacing between the polygons or the dimensions of the polygons in the mask layout database is less than the corresponding minimum allowable design rule in the technology file.

Today, any design rule violations in the mask layout database are corrected manually by a layout designer. The layout designer typically finds each violation and manually corrects the violations by moving polygons associated with the violations. During the correction process, the layout designer may create new design rule violations and, therefore, the correction process may be repeated until the mask layout database does

not include any design rule violations. The process of iteratively correcting the design rule violations may take several hours or even days to complete and can increase the time needed to design the integrated circuit.

SUMMARY OF THE INVENTION

In accordance with the present invention, the disadvantages and problems associated with automatic elimination of design rule violations during construction of a mask layout block have been substantially reduced or eliminated. In a particular embodiment, a method for eliminating design rule violations during construction of a mask layout block includes automatically preventing a polygon from being placed in a selected position in a mask layout block if a design rule violation is identified.

In accordance with one embodiment of the present invention, an automated method for eliminating design rule violations during construction of a mask layout block includes analyzing a selected position for a polygon in a mask layout block and obtaining one or more design rules associated with the polygon from a technology file. The method provides an advice area associated with the selected position for the polygon that graphically represents a space, enclosure, width, notch or any other topological condition in the mask layout block where the selected position complies with the design rules.

In accordance with another embodiment of the present invention, an automated method for eliminating design rule violations during construction of a mask layout block includes analyzing a selected position of a polygon in

a mask layout block and identifying a design rule violation in the mask layout block if the selected position is less than a design rule from a technology file. If the design rule violation is identified, the placement of the polygon at the selected position is automatically prevented.

In accordance with a further embodiment of the present invention, a computer system for eliminating design rule violations during construction of a mask layout block includes a processing resource coupled to a computer readable memory. Processing instructions are encoded in the computer readable memory. When the processing instructions are executed by the processing resource, the instructions analyze a selected position of a polygon in a mask layout block and identify a design rule violation in the mask layout block if the selected position is less than a design rule from a technology file. If the design rule violation is identified, the instructions prevent the polygon from being placed at the selected position in the mask layout block.

Important technical advantages of certain embodiments of the present invention include a Design-Rule-Aware Environment (DRA) tool that prevents design rule violations from being created during the construction of a mask layout block. A layout designer may move a cursor on a display device over a polygon in order to select the polygon. The DRA tool highlights an area that may represent a space, enclosure, width, notch or any other topological condition in the layout block where polygons may be placed, created or edited without violating any of the design rule constraints contained in a technology file. For Example, if the layout designer attempts to move the polygon outside of the highlighted area, the DRA tool prevents the layout

designer from placing the polygon in the desired position and automatically places the polygon in a position located inside the highlighted area. The mask layout block, therefore, may be created free of design rule violations. Another important technical advantage of certain embodiments of the present invention includes DRA tool that reduces the design time for an integrated circuit. In a typical integrated circuit design process, a design rule check (DRC) tool analyzes a mask layout file for design rule violations and identifies any violations in an output file. A layout designer may use the output file to manually eliminate the identified design rule violations. In contrast, the present invention may eliminate design rule violations from a mask layout block before the mask layout block is converted into a mask layout file. The time needed to complete the design process for the integrated circuit, therefore, may be substantially reduced since the steps of checking the layout with a DRC tool and correcting the identified design rule violations may be eliminated.

All, some, or none of these technical advantages may be present in various embodiments of the present invention. Other technical advantages will be readily apparent to one skilled in the art from the following figures, descriptions, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete and thorough understanding of the present embodiments and advantages thereof may be acquired by referring to the following description taken in conjunction with the accompanying drawings, in which like reference numbers indicate like features, and wherein:

FIG. 1 illustrates a mask design view of Metal 1 type polygon as shows in commercial IC layout editor. Distance D represents the existing distance between the two (2) Metal 1 polygons.

FIG. 2 illustrates a mask design view of Metal 1 type polygon as shows in commercial IC layout editor. Distance A is the minimum allowed between two (2) Metal 1 polygons according to the IC process specifications, as determine by the IC fabrication plant.

FIG. 3 illustrates a mask design view of Metal 1 type polygon as shows in commercial IC layout editor. When a user clicks on the right side Metal 1 polygon the system automatically highlights an Advise A. (Green Polygon) to show the minimum distance between Metal 1 polygons, as indicated in the process specifications in accordance with teachings of the present invention;

FIG. 4 illustrates a mask design view of Metal 1 type polygon as shows in commercial IC layout editor. In this layout view of the example integrated circuit of FIG. 3, the right side Metal 1 polygon is moved by the user into the Advise Area, which means that the polygon's distance is in violation

according to the process specifications. (Smaller than the minimum distance allowed according the process specification)

FIG. 5 illustrates a layout view of the example integrated circuit of FIG. 4 after the right side polygon has been placed in the Advise Area formed in accordance with teachings of the present invention; and has been pushed back to the minimum distance A, that is allowed according to the process specifications, creating Auto-Correct Mode.

FIG. 6 illustrates a flow chart for a method for eliminating design rule violations during construction of a mask layout block in accordance with teachings of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Preferred embodiments of the invention and its advantages are best understood by reference to FIGS. 1 through 6 of the drawings, like numerals being used for like and corresponding parts of the various drawings.

As the number of transistors on an integrated circuit continues to increase, the design process for the integrated circuit becomes more complex. For example, an increasing number of transistors may require additional layers to form the integrated circuit on a semiconductor wafer. Each layer of the integrated circuit may have one or more design rules that define how polygons on each layer should be placed in a mask layout block for a desired manufacturing process. The number of design rules for the desired manufacturing process, therefore, increases with the number of layers formed on the semiconductor wafer.

A design rule typically defines the minimum or maximum allowable dimension for a feature fabricated on a specific layer of the integrated circuit. For example, an integrated circuit may include, among other layers, a polysilicon layer that forms transistor gates, a metal layer that forms interconnects between the transistors and a contact or via layer that connects the polysilicon layer to the metal layer. Each layer typically has one or more design rules associated with the features in a mask layout file that are formed on the specific layer. The metal layer may include design rules for a minimum allowable spacing between two adjacent metal

features, a minimum width of a metal feature and a minimum and/or maximum length of a metal feature. The polysilicon and contact layers may include similar design rules where the minimum or maximum allowable dimensions are unique to that layer.

FIG. 1 illustrates a mask design view of Metal 1 type polygon as shows in commercial IC layout editor. Distance D represents the existing distance between the two (2) Metal 1 polygons. During the construction of an integrated circuit (IC) mask layout database many types of polygons have to be drawn. Each polygon type has to meet minimum distance from related layer polygon, as specified in the process specifications. For example, a polygon of layer type called Metal 2 has to meet a certain distance from the same layer type. Another example is a polygon of the layer type of Poly has to meet a certain distance to all same layer type polygons, as specified in the process specifications.

FIG. 2 illustrates a mask design view of Metal 1 type polygon as shows in commercial IC layout editor from FIG. 1. Distance A is the minimum allowed between two (2) Metal 1 polygons according to the IC process specifications, as determine by the IC fabrication plant.

FIG. 3 illustrates a mask design view of Metal 1 type polygon as shows in commercial IC layout editor. When a user clicks on the right side Metal 1 polygon the system automatically highlights an Advise A. (Green Polygon) to show the minimum distance between Metal 1 polygons, as indicated in the process specifications in accordance with teachings of the present invention. If the layout designer chooses to operate in Advise Mode, the layout designer may select a polygon by clicking or moving a cursor over

the desired polygon. The DRA tool uses the design rules to graphically display a space, otherwise known as an Advise Area, within the mask

layout block where the layout designer may move, click and/or place a polygon without creating a design rule violation. In another embodiment, the DRA tool may display an Advise Area that represents position in the mask layout block where the placement of a polygon would cause a design rule violation.

The DRA tool may graphically represent the Advise Area in the mask layout block by highlighting the space with an appropriate color and/or pattern. The Advise Area may have a color and/or pattern that is similar to the color and pattern used to represent the layer (e.g., diffusion, polysilicon, metal, etc.) of the polygon being moved or placed in the mask layout block. The Advise Area may have a color and/or pattern that is different from the color and pattern of the polygon in order to distinguish the Advise Area from the polygon.

The layout designer may also choose where the DRA tool displays the Advise Areas. For example, the DRA tool may only display the Advise Area for polygons immediately surrounding the polygon being move or placed. The DRA tool may display Advise Areas for all polygons within a selected distance from the polygon being placed or moved. In Advise mode, the DRA tool may allow the layout designer to place a polygon in any position within the mask layout block. The layout designer, therefore, may create a design rule violation if the polygon is placed in a position that does not comply with the Advise Area.

FIG. 4 illustrates a mask design view of Metal 1 type polygon as shows in commercial IC layout editor. In this layout view of the example integrated circuit of FIG. 3, the right side Metal 1 polygon is moved by the user into the Advise Area, which means that the polygon's distance is in violation according to the process specifications. (Smaller than the minimum distance allowed according the process specification)

However, if the layout designer chooses to operate in Auto-Correct mode, the DRA tool may prevent the layout designer from placing a polygon in a position within the mask layout block that will cause a design rule violation.

FIG. 5 illustrates a layout view of the example integrated circuit of FIG. 4 after the right side polygon has been placed in the Advise Area formed in accordance with teachings of the present invention; and has been pushed back to the minimum distance A, that is allowed according to the process specifications, creating Auto-Correct Mode.

If the layout designer attempts to place a polygon in a position that does not comply with the Advise Areas, the DRA tool returns the polygon to its original position or size in the mask layout block. The DRA tool moves the polygon to the minimum design rule associated with the design layer for the polygon. For example, if the selected polygon is a metal one interconnect line, the DRA tool reads the design rule for minimum spacing between metal one lines and minimum width of a metal one line and moves the polygon from the position selected by the layout designer to the position that is approximately equal to the design rules. The DRA tool places the polygon at any position in the mask layout block that complies

with the Advise Areas (e.g., the polygon is inside the Advise Area if the Advise Area represents the space where a polygon may be placed without creating a design rule violation or the polygon is outside the Advise Area if the Advise Area represents the space where the placement of a polygon would create a design rule violation. The DRA tool, therefore, prevents the layout designer from accidentally creating a design rule violation in the mask layout block. Furthermore, the DRA tool maintains connectivity of any nodes affected by the moved polygon by adding and/or subtracting polygons as necessary. Furthermore, the DRA tool maintain the circuit connectivity (LVS) correctness and Timing constraints if exists.

In another example, the layout designer may select a position in the mask layout block for the polygon or alter the dimensions of the polygon such that the modification does not create a design rule violation. The DRA tool may detect that the dimensions and/or spacing between adjacent polygons are greater than the corresponding minimum design rules contained in the technology file. The DRA tool may provide a highlighted area (Advise Area) that represents an area of the mask layout block that may be compacted. The layout designer may manually move any polygons associated with the highlighted area to the corresponding minimum design rules indicated within the mask layout block. In another example, the layout designer may choose to allow the DRA tool to automatically move the associated polygons to the minimum design rules.

In some embodiments, the processing instructions for correcting design rule violations in a mask layout file may be encoded in computer-usable media. Such computer-usable media may include, without limitation, storage media such as floppy disks, hard disks, CD-ROMS, DVDs, read-only

memory, and random access memory; as well as communications media such wires, optical fibers, microwaves, radio waves, and other electromagnetic or optical carriers.

In another example, during the construction of layout block, a layout designer may decide to place polygons in different positions within a layout block and/or move edges of the polygons to increase or decrease the dimensions of the polygons. The placement of polygons in certain positions in a layout block may create design rule violations. Since the layout designer may have to memorize over a thousand different design rules, the layout designer may not be able to identify all possible types of design rule violations. The design rule violations, therefore, may be removed by using a design rule check (DRC) tool that compares the dimensions of polygons and the spaces between polygons with design rules included in a technology file for a desired manufacturing process. In order to reduce the time needed to eliminate design rule violations from a layout block, a DRA tool integrated with a layout editor may use the design rules from the technology file to provide Advise areas and prevent the layout designer from placing polygons in positions that may create design rule violations.

In addition to preventing any design rule violations, the DRA tool also maintains the connectivity of electrical connections represented by the polygons in the mask layout file.

In addition to preventing any design rule violations, the DRA tool also maintains the circuit timing constraints of electrical connections represented by the polygons in the mask layout file.

FIGS. 6 illustrate a flow chart of a method for eliminating design rule violations during construction of a mask layout block. Generally, a Design-Rule-Aware (DRA) tool, which is integrated into a commercially available layout editor, operates in two modes: an Advise Mode and an Auto-Correct mode. In the Advise Mode, the DRA tool provides an Advise Area when a layout designer creates a new polygon or selects an existing polygon in the mask layout block. The Advise Area provides a graphical representation of a space in the mask layout block where a polygon may be placed. When the DRA tool is operating in Auto-Correct Mode, the DRA tool may provide Advise areas and prevent the layout designer from creating a design rule violation. If the DRA tool determines that the selected position (e.g., position of the polygon in the mask layout block and/or the size of the polygon based on the position of the edges) will create a design rule violation, the DRA tool automatically returns the polygon to its original position or places the polygon in a position that does not create a design rule violation. The DRA tool also simultaneously maintains connectivity of any electrical connections that are affected by the placement of the polygon. The DRA tool also provides a compaction area in the mask layout block if the selected position for the polygon creates a space between polygons and/or a dimension of the polygon that is greater than the design rules in the technology file.

A layout designer may attempt to place a polygon at a selected position in layout block by creating a new polygon or selecting an existing polygon. If the DRA tool is running in the Advise mode, the DRA tool provides Advise areas associated with the polygon being placed in the layout block. The Advise areas may graphically represent a space in the layout block where the polygon may be placed without creating a design rule violation. The

Advise areas may graphically represent a space in the layout block where the polygon may not be placed because a design rule violation would be created. The Advise areas may have any color and/or pattern that allow a layout designer to identify the Advise areas in the layout block.

The DRA tool determines if the layout designer has selected the Auto-Correct mode. If the DRA tool is operating in the Advise mode but not the Auto-Correct mode, the DRA tool may provide the Advise areas but allow the layout designer ignore the Advise areas and place a polygon at any position in the layout bloc. If the DRA tool is operating in the Auto-Correct mode, the DRA tool determines if the selected position for the polygon in the layout block will create a design rule violation. If the selected position for the polygon does not create a design rule, the DRA tool allows the layout designer to place the polygon in the selected position in the layout.

However, if the selected position violates one or more design rules from the technology file, the DRA tool determines a position in the layout block for the polygon by using the design rules from the technology file. The DRA tool selects a position in the layout block that is approximately equal to the corresponding minimum design rules. The DRA tool selects a position in the layout block that is greater than the corresponding minimum design rules. The DRA tool returns the polygon to its original position in the layout block. The DRA tool places the polygon in the position that will not create a design rule violation. The DRA tool may place the polygon on a layer other than the layer selected by the layout designer in order to avoid creating a design rule violation. For example, the layout designer may want to place a polygon on a specific layer. The DRA tool may analyze the selected position

and determine that the polygon cannot be placed on the selected layer without creating a design rule violation. The DRA tool may determine that

the polygon may be placed on another layer and provide Advise areas for the placement of the polygon on the new layer.

During placement of the polygons, the DRA tool may also maintain connectivity for the electrical connections and compact the features (e.g., spaces between polygons and dimensions of polygons) in the layout block. When the layout designer moves a polygon to a new position in the layout block, the DRA tool determines if polygons should be added or removed in order to maintain the correct connectivity for the node being modified. The addition of new polygons and the increase in distance between certain polygons may cause the size of the layout block to increase. The DRA tool may also reduce the size of the layout block by compacting the layout so that the spacing between the polygons on the same or different layers is approximately equal to the minimum spacing allowed for a specific manufacturing process. Since the compaction process uses design rules from the technology file, no design rule violations are introduced into the mask layout file.

Although the present invention has been described with respect to a specific preferred embodiment thereof, various changes and modifications may be suggested to one skilled in the art and it is intended that the present invention encompass such changes and modifications fall within the scope of the appended claims.

Claims

1. An automated method for eliminating design rule violations during construction of a mask layout block, comprising: analyzing a selected position for a polygon in the mask layout block; obtaining one or more design rules associated with the polygon from a technology file; providing an advice area associated with the selected position for the polygon, the advice area operable to graphically represents a space, enclosure, width, notch or any other topological condition in the mask layout block where the selected position complies with the design rules: and automatically preventing a layout designer from placing, creating or moving the polygon at the selected position based on the advice area if the selected position creates a design rule violation.

2. The method of claim 1, further comprising: identifying the design rule violation if the selected position for the polygon is located inside of the advice area.

3. The method of claim 1, further comprising: identifying the design rule violation if the selected position for the polygon is located outside of the advice area.

4. The method of claim 1, further comprising: determining if the selected position for the polygon creates a feature dimension in the mask layout block greater than at least one of the design rules; and modifying the selected position until the feature dimension is approximately equal to the at least one design rule.

5. The method of claim 1, further comprising providing a compaction area associated with the polygon, the compaction area operable to graphically represent that the selected position creates a feature dimension greater than at least one of the design rules.

6. The method of claim 1, further comprising the design rules selected from a group consisting of an n-well spacing, a p-well spacing, a diffusion spacing, a polysilicon spacing, a metal spacing and a contact spacing.

7. The method of claim 1, further comprising the design rules selected from a group consisting of an n-well width, a p-well width, a diffusion width, a polysilicon width, a metal width and a contact width.

8. The method of claim 1, wherein the selected position for the polygon comprises a location for the polygon in the mask layout block.

9. The method of claim 1, wherein the selected position for the polygon comprises a location for edges of the polygon in the mask layout block.

10. The method of claim 1, wherein the mask layout block is hierarchical.

11. An automated method for eliminating design rule violations during construction of a mask layout block, comprising: analyzing a selected position of a polygon in the mask layout block; providing an advice area associated with the polygon; determining if the selected position produces a design rule violation in the mask layout block based on a design rule from a technology file; and automatically preventing a layout designer from placing the polygon in the mask layout block at the selected position based on the

advice area if the design rule violation exists.

12. The method of claim 11, further comprising automatically placing the polygon in an original position in the mask layout block if the design rule violation exists.

13. The method of claim 11, further comprising automatically adjusting the selected position until the design rule violation is eliminated.

14. The method of claim 11, further comprising: identifying the design rule violation if the selected position for the polygon is located inside of the advice area.

15. The method of claim 11, further comprising: identifying the design rule violation if the selected position for the polygon is located outside of the advice area.

16. The method of claim 11, further comprising: the mask layout block including at least one top-level cell and one or more instances of a subcell located in the top-level cell; and determining if the selected position produces a design rule violation in one or more instances of a subcell in the mask layout block, the subcell located in a top-level cell; and simultaneously preventing the layout designer from placing the polygon in mask layout block at the selected position based on the advice area in each instance of the subcell if the design rule violation exists.

17. The method of claim 11, further comprising generating a mask layout file from the mask layout block that does not include the design rule violation.

18. A computer system for eliminating design rule violations during construction of a mask layout block, comprising: a processing resource; a computer readable memory; and processing instructions encoded in the computer readable memory, the processing instructions, when executed by the processing resource, operable to perform operations comprising: analyzing a selected position of a polygon in the mask layout block; providing an advice area associated with the polygon; determining if the selected position produces a design rule violation in the mask layout block based on a design rule from a technology file; and automatically preventing a layout designer from placing the polygon in the mask layout block at the selected position based on the advice area if the design rule violation exists.

19. The system of claim 18, further comprising the instructions operable to perform operations including automatically placing the polygon in an original position in the mask layout block if the design rule violation exists.

20. The system of claim 18, further comprising the instructions operable to perform operations including automatically adjusting the selected position until the design rule violation is eliminated.

21. The system of claim 18, further comprising the instructions operable to perform operations including: identifying the design rule violation if the selected position for the polygon is located inside of the advice area.

22. The system of claim 18, further comprising the instructions operable to perform operations including: identifying the design rule violation if the selected position for the polygon is located outside of the advice area.

23. The system of claim 18, further comprising the instructions operable to perform operations including: determining if the selected position for the polygon creates a feature dimension in the mask layout block greater than the design rule; and modifying the selected position until the feature dimension is approximately equal to the design rule.

24. Software for eliminating design rule violations during construction of a mask layout block, the software being embodied in computer-readable media and when executed operable to: analyze a selected position of a polygon in the mask layout block; providing an advise area associated with the polygon; and determining if the selected position produces a design rule violation in the mask layout block based on a design rule from a technology file; and automatically prevent a layout designer from placing the polygon in the mask layout block at the selected position based on the advice area if the design rule violation exists.

25. The software of claim 24, further operable to automatically place the polygon in an original position in the mask layout block if the design rule violation exists.

26. The software of claim 24, further operable to automatically adjust the selected position until the design rule violation is eliminated.

27. The software of claim 24, further operable to: identify the design rule violation if the selected position for the polygon is located inside of the advice area.

28. The software of claim 24, further operable to: identify the design rule violation if the selected position for the polygon is located outside of the advice area.

29. The software of claim 24, further operable to provide a compaction area associated with the polygon, the compaction area operable to graphically represent that the selected position creates a feature dimension greater than the design rule.

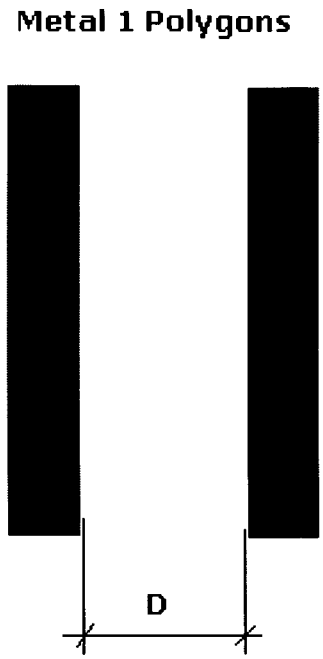

Figure #1

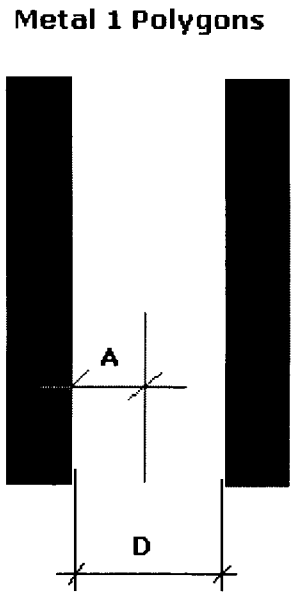

Figure #2

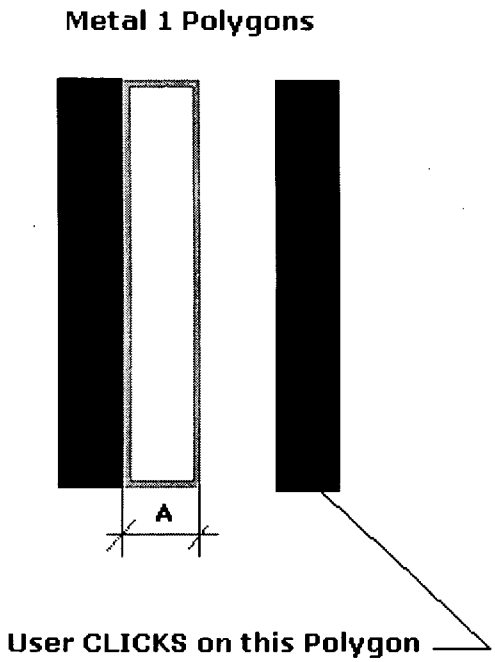

Figure #3

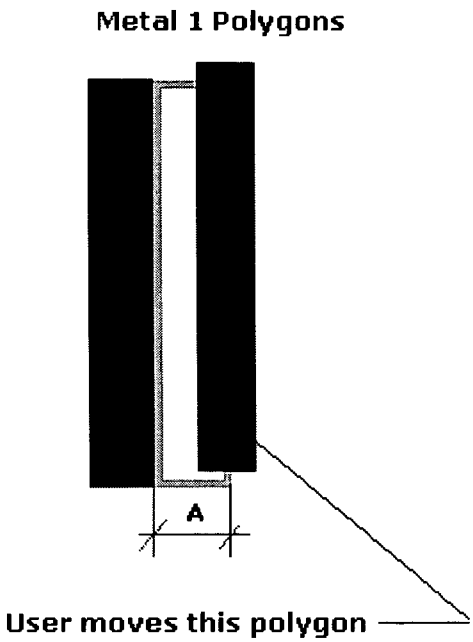

Figure #4

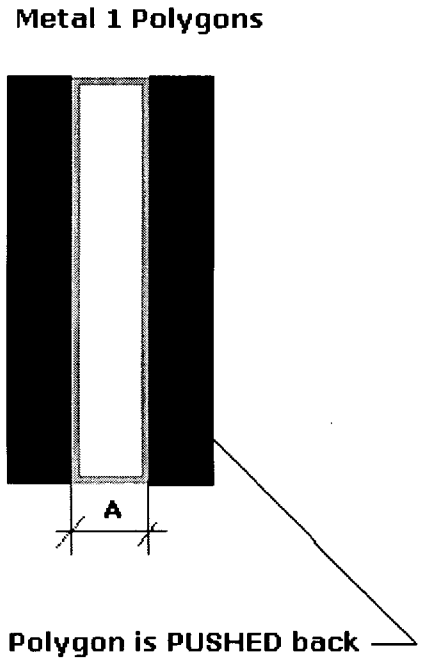

Figure #5

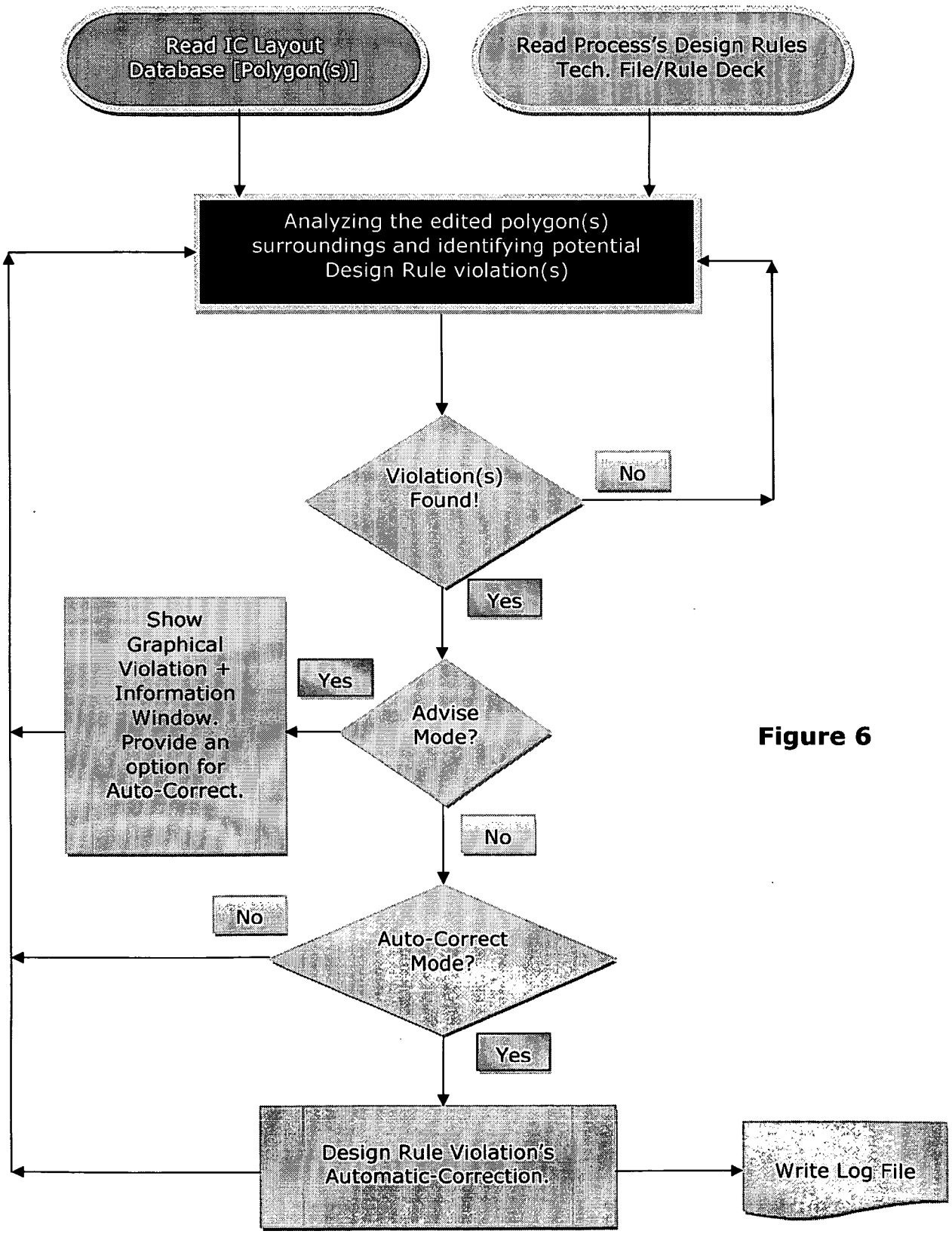
Read IC Layout Database [Polygon(s)]
Read Process's Design Rules Tech. File/Rule Deck
Analyzing the edited polygon(s) surroundings and identifying potential Design Rule violation(s)
Violation(s) Found!
No
Yes
Show Graphical Violation + Information Window. Provide an option for Auto-Correct.
Yes
Advise Mode?
No
No
Auto-Correct Mode?
Yes
Design Rule Violation's Automatic-Correction.
Write Log File

Figure 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 07/23916

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G06F 17/50 (2008.04)
USPC - 716/19
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8): G06F 17/50 (2008.04)
USPC: 716/19

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 716/10; 716/11; 716/1 (text search)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
WEST(USPT,PGPB,EPAB,JPAB,USOCR); DialogWEB(Engineering); Google Search terms: mask layer hierarchy order violation error compliance design layout automation box are boundary placement sizing correction prevent undoing flag alert rule illegal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/0064796 A1 (LI et al.) 01 April 2004 (01.04.2004), fig 8; para [0038]-[0055], [0108]-[0130], [0138], [0139], [0193]-[0198].	1-29
A	US 2007/0213959 A1 (KROPACZEK et al.) 13 September 2007 (13.09.2007), para [0143], [0162], [0175], [0242].	1, 11, 18, 24
A	US 2005/0288913 A1 (SHAH et al.) 29 December 2005 (29.12.2005), abstract; para [0029], [0031], [0035].	1, 11, 18, 24

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 May 2008 (28.05.2008)	05 JUN 2008
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (April 2007)