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A semiconductor memory

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(52) Domestic classification
H1K 11A3 11B4 11C1A 11C4 11D1 11D 1CA 1FE 4C11 4C14 9B1 9C1 9C2 9D1 9E 9N2 9N3 9R2 GAF
H3T 2B7 2T3F MC
U1S 2121 H1K H3T

(56) Documents cited
None

(58) Field of search
H1K
H3T

GB 2117565B

FIG. 1

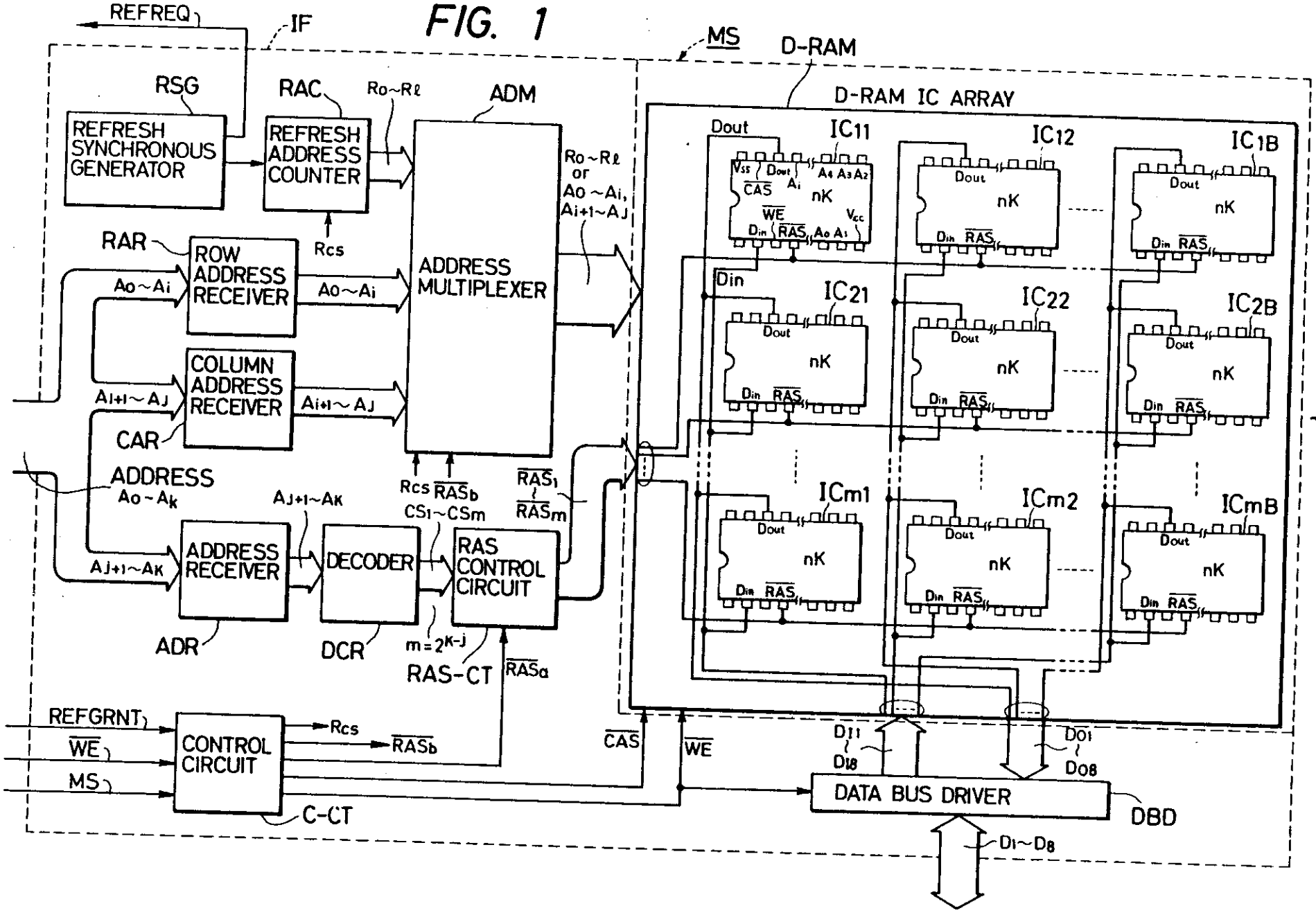

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FIG. 2

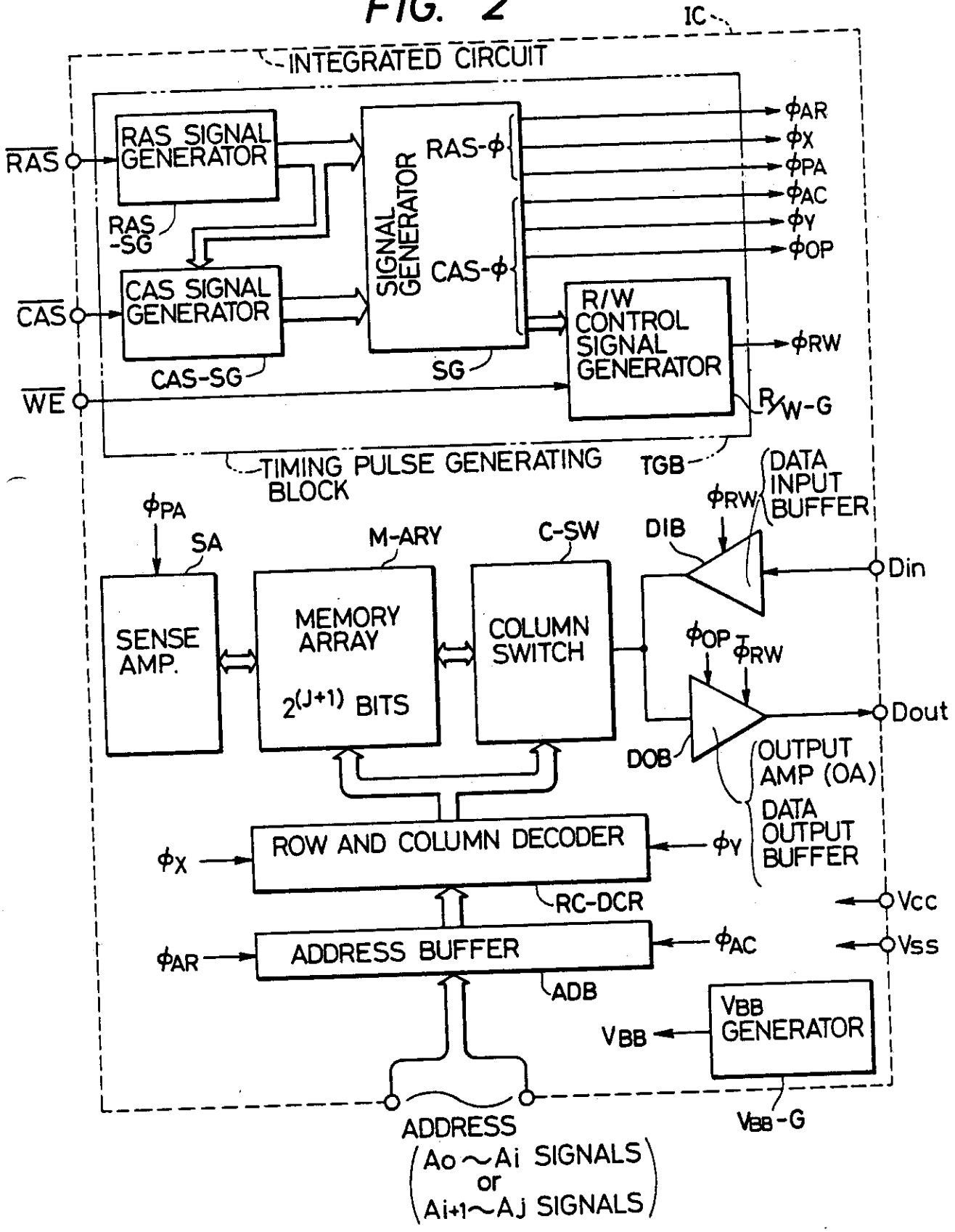
IC
INTEGRATED CIRCUIT
RAS
RAS SIGNAL GENERATOR
RAS -SG
CAS
CAS SIGNAL GENERATOR
CAS-SG
WE
SIGNAL GENERATOR
RAS-φ
CAS-φ
SG
R/W CONTROL SIGNAL GENERATOR
φAR
φX
φPA
φAC
φY
φOP
φRW
RW-G
TGB
TIMING PULSE GENERATING BLOCK
φPA
SA
SENSE AMP.
M-ARY
MEMORY ARRAY
2(J+1) BITS
C-SW
COLUMN SWITCH
DIB
φRW
DATA INPUT BUFFER
Din
φOP
φRW
Dout
DOB
OUTPUT AMP (OA)
DATA OUTPUT BUFFER
φX
ROW AND COLUMN DECODER
φY
RC-DCR
Vcc
φAR
ADDRESS BUFFER
φAC
Vss
ADB
VBB
VBB GENERATOR
VBB-G
ADDRESS
(Ao ~ Ai SIGNALS
or
Ai+1 ~ Aj SIGNALS)

FIG. 3B

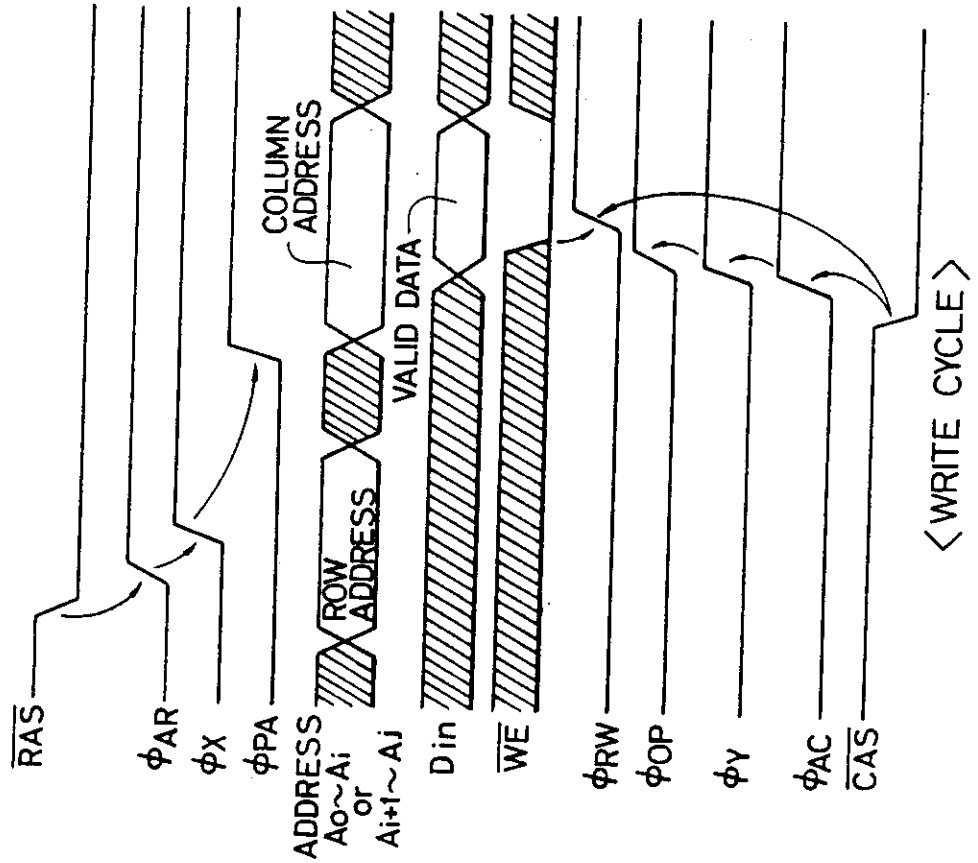
RAS
φAR
φX
φPA
ADDRESS Ao~Ai or Ai+1~Aj
ROW ADDRESS
COLUMN ADDRESS
Din
VALID DATA
WE
φRW
φOP
φY
φAC
CAS
<WRITE CYCLE>

FIG. 3A

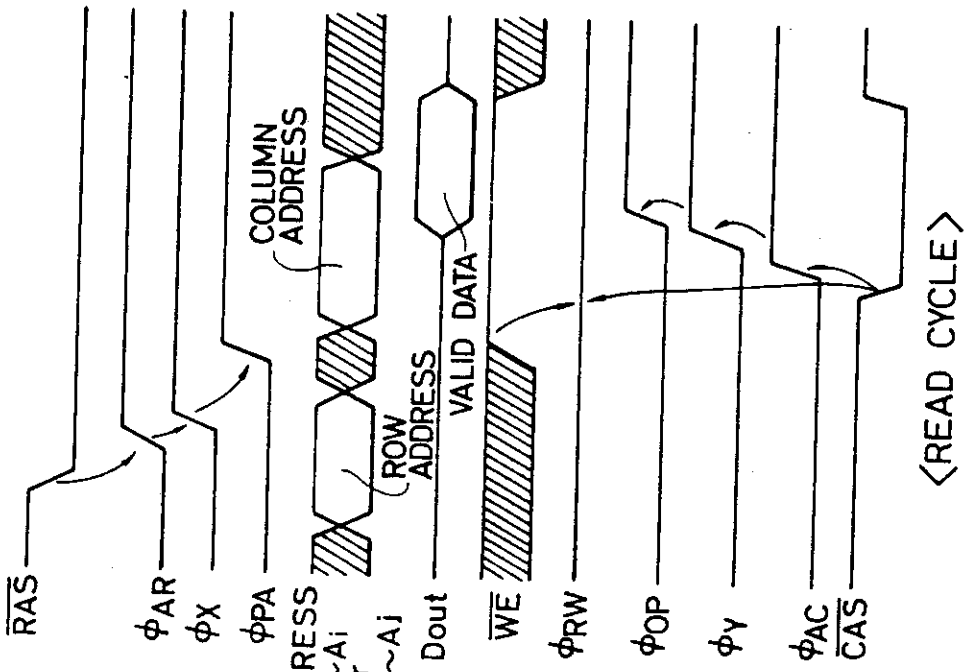
RAS
φAR
φX
φPA
ADDRESS Ao~Ai or Ai+1~Aj
ROW ADDRESS
COLUMN ADDRESS
Dout
VALID DATA
WE
φRW
φOP
φY
φAC
CAS
<READ CYCLE>

FIG. 4A

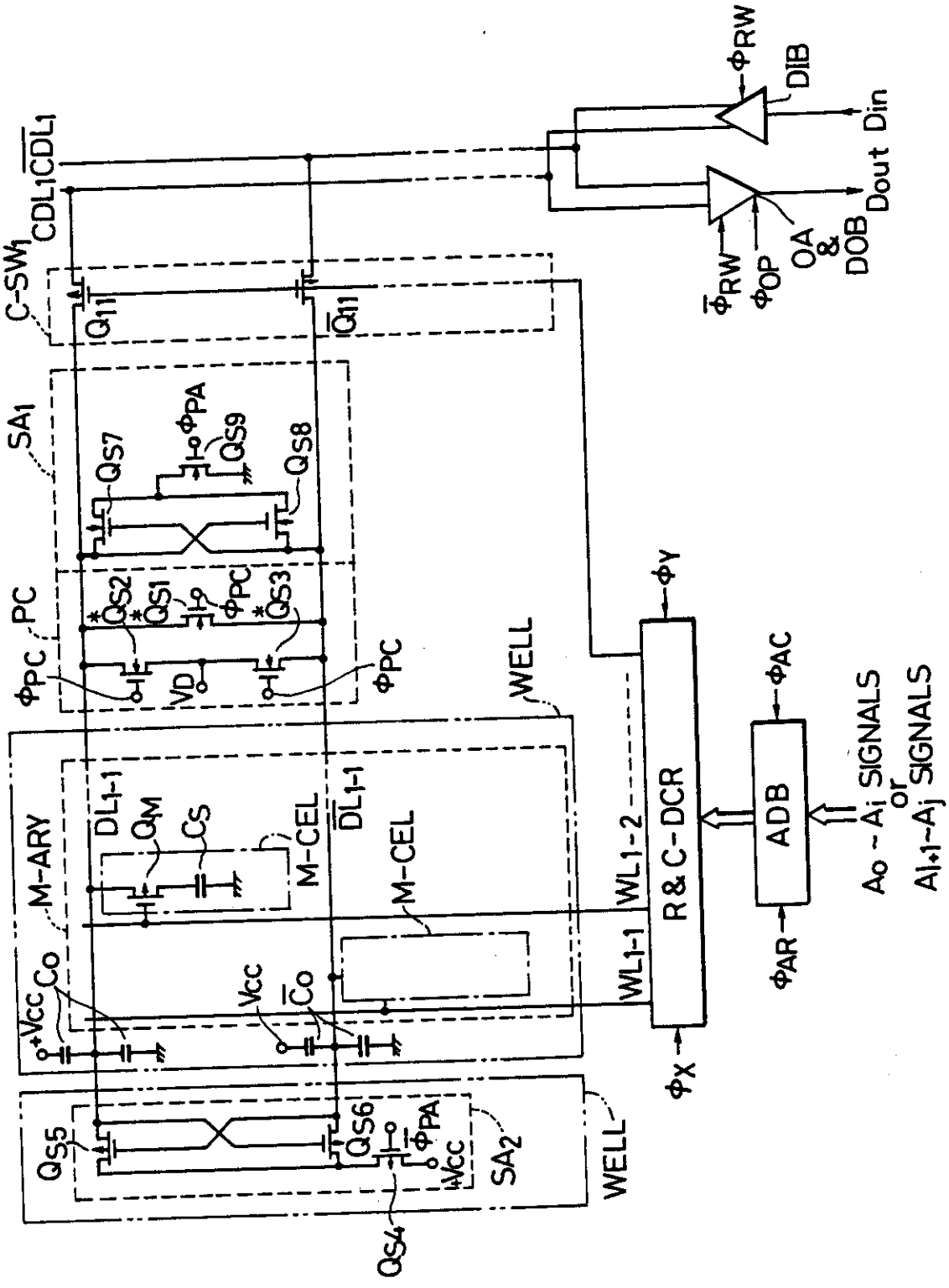
φRW
DIB
Din
Dout
C-SW1
CDL1
CDL1
Q11
Q11
φRW
φOP
OA & DOB
SA1
QS7
QS9
φPA
QS8
QS2
QS1
φPC
QS3
PC
φPC
VD
φPC
WELL
φY
φAC
M-ARY
DL1-1
QM
CS
M-CEL
DL1-1
M-CEL
WL1-2
R&C-DCR
ADB
Ao - Ai SIGNALS or Ai+1 - Aj SIGNALS
Vcc
Co
Vcc
Co
WL1-1
φAR
QS5
QS6
φPA
Vcc
SA2
WELL
φX
QS4

FIG. 4B

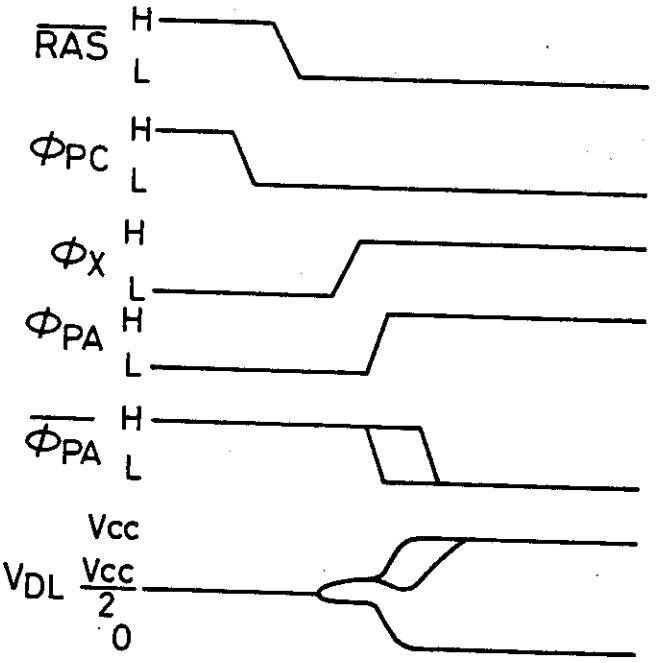
RAS
H
L
ΦPC
H
L
ΦX
H
L
ΦPA
H
L
ΦPA
H
L
Vcc
VDL
Vcc
2
0

FIG. 4D

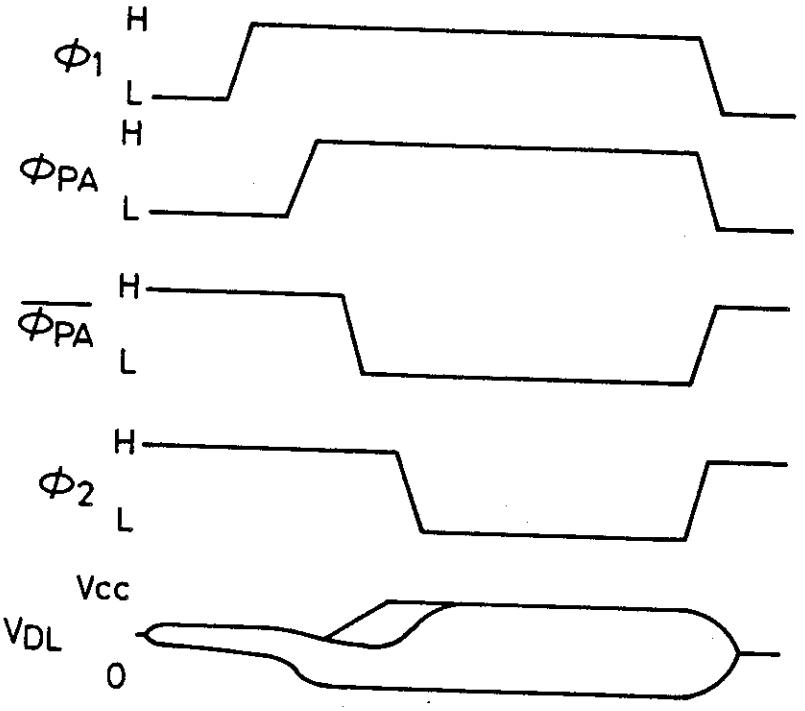
Φ1
H
L
ΦPA
H
L
ΦPA
H
L
Φ2
H
L
Vcc
VDL
0

FIG. 4C

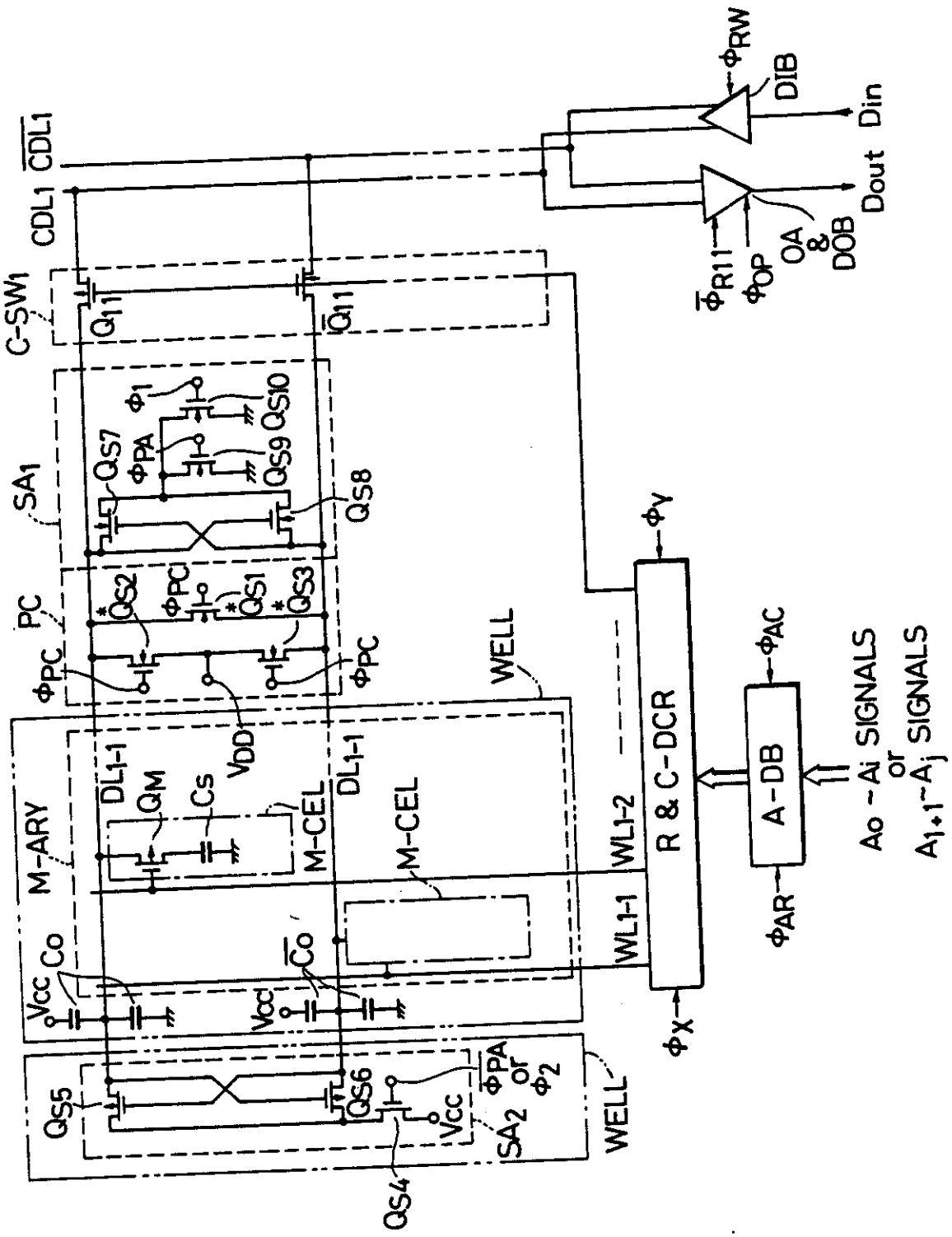
CDL1
$\overline{CDL1}$
C-SW1
Q_{11}
$\overline{Q}_{11}$
SA1
Q_{S7}
ϕ_{PA}
ϕ_1
Q_{S9}
Q_{S10}
Q_{S8}
PC
ϕ_{PC}
Q_{S2}
Q_{S1}
Q_{S3}
V_{DD}
WELL
M-ARY
DL_{1-1}
Q_M
Cs
M-CEL
$\overline{Co}$
Co
Vcc
Q_{S5}
Q_{S6}
Q_{S4}
$\overline{\phi}_{PA}$ or ϕ_2
SA_2
ϕ_X
ϕ_Y
R & C-DCR
WL_{1-1}
WL_{1-2}
A-DB
ϕ_{AR}
ϕ_{AC}
Ao ~ Ai SIGNALS or A_{1+1}~A_j SIGNALS
$\overline{\phi}_{R11}$
ϕ_{OP}
OA & DOB
Dout
Din
DIB
ϕ_{RW}

FIG. 4E

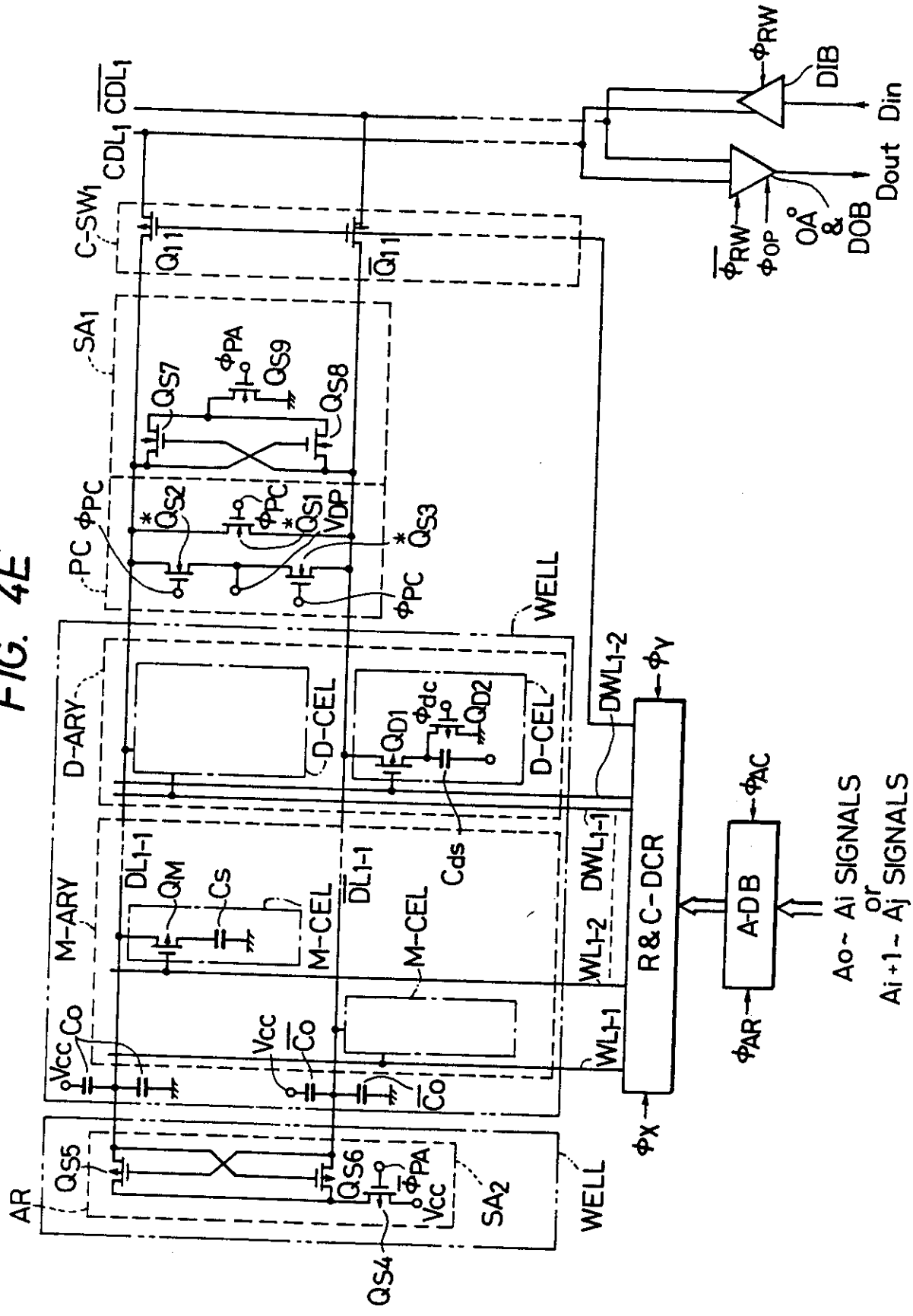
$\overline{CDL_1}$
CDL_1
C-SW1
Q_{11}
$\overline{Q_{11}}$
SA1
ϕ_{PA}
QS7
QS9
QS8
PC
ϕ_{PC}
QS2
QS1
VDP
QS3
WELL
D-ARY
D-CEL
QD1
ϕ_{dc}
QD2
DWL1-2
ϕ_Y
DL1-1
QM
Cs
M-CEL
Cds
DWL1-1
WL1-2
WL1-1
R&C-DCR
A-DB
ϕ_{AC}
ϕ_{AR}
M-ARY
Vcc
Co
$\overline{Co}$
ϕ_X
AR
QS5
QS6
SA2
QS4
ϕ_{RW}
DIB
Din
Dout
$\overline{\phi_{RW}}$
ϕ_{OP}
OA & DOB
Ao~ Ai SIGNALS
or
Ai+1~ Aj SIGNALS

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FIG. 5A

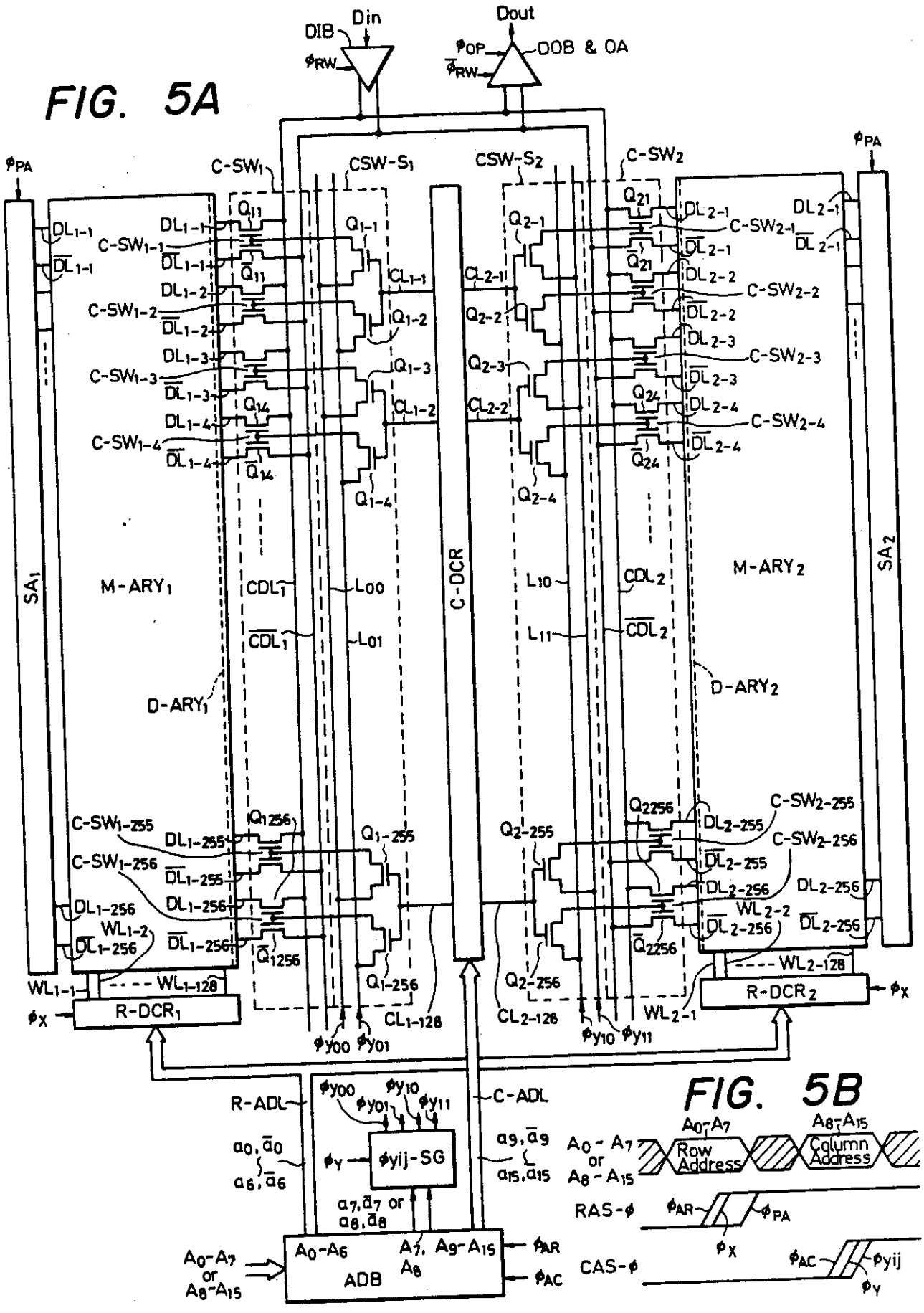

FIG. 5B

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FIG. 6

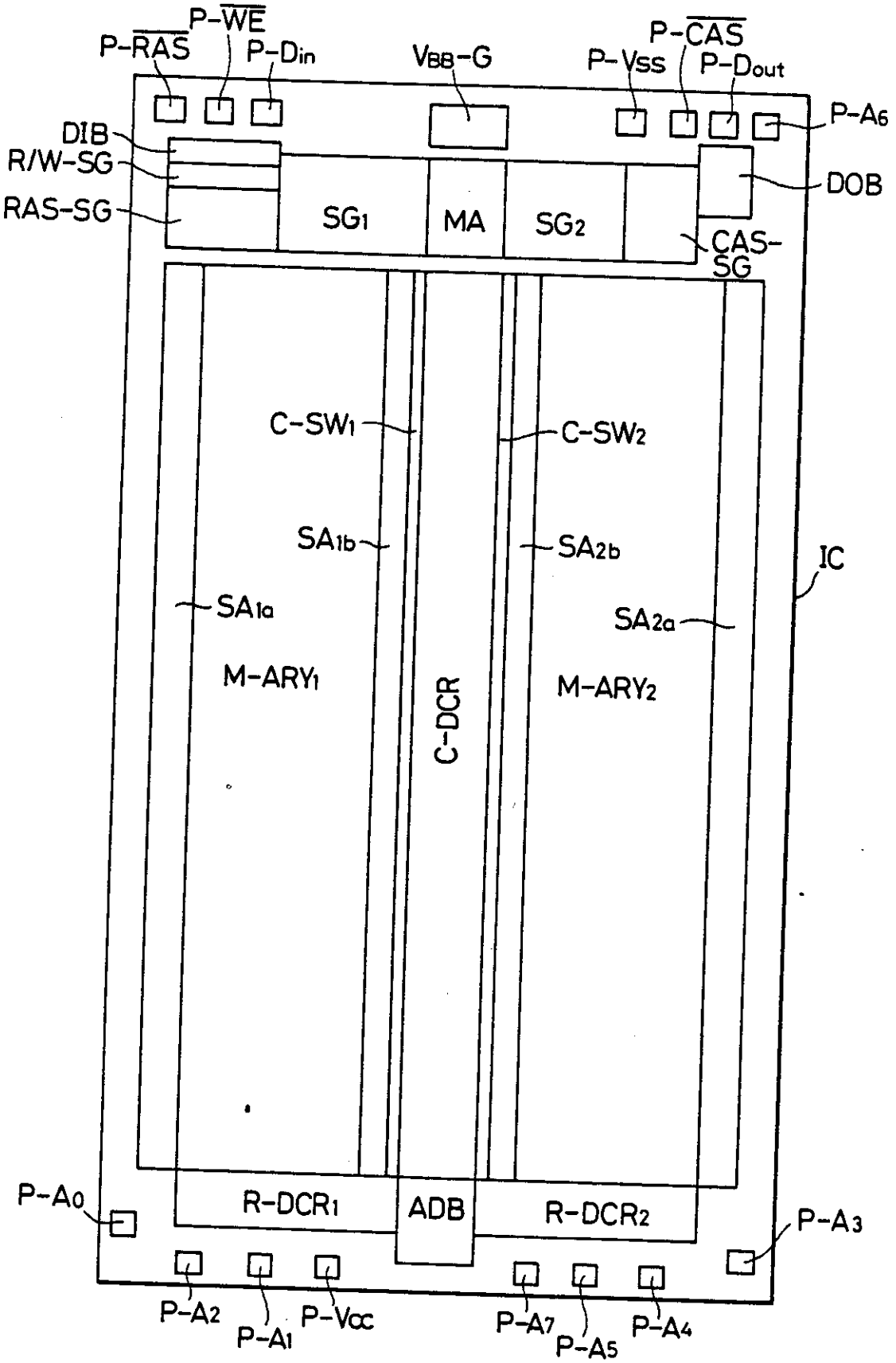

FIG. 7A

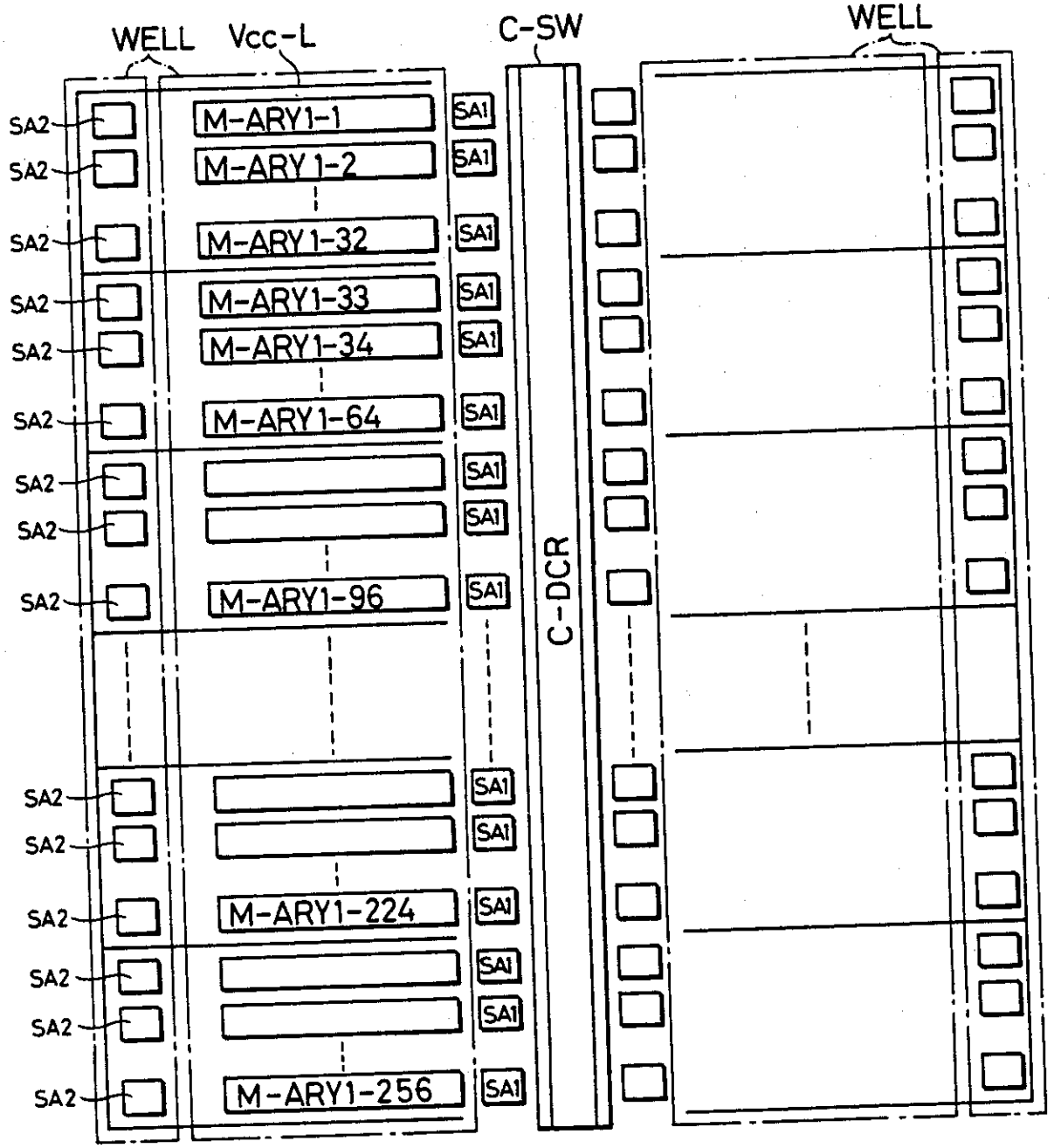
WELL
Vcc-L
C-SW
WELL
C-DCR
M-ARY1-1
M-ARY1-2
M-ARY1-32
M-ARY1-33
M-ARY1-34
M-ARY1-64
M-ARY1-96
M-ARY1-224
M-ARY1-256
SA1
SA2

FIG. 7B

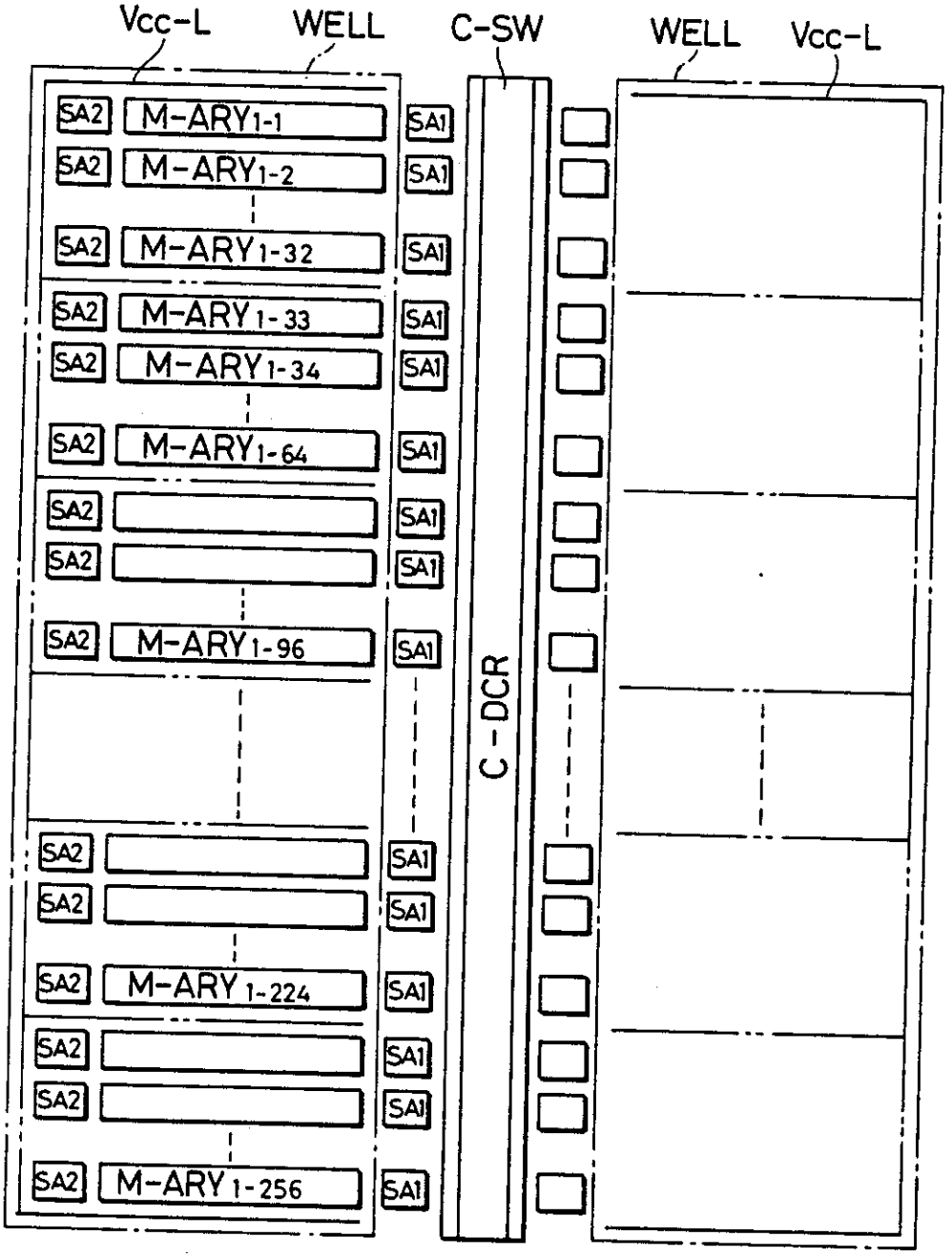
Vcc-L
WELL
C-SW
WELL
Vcc-L
SA2
M-ARY1-1
SA1
M-ARY1-2
M-ARY1-32
M-ARY1-33
M-ARY1-34
M-ARY1-64
M-ARY1-96
M-ARY1-224
M-ARY1-256
C-DCR

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FIG. 8A

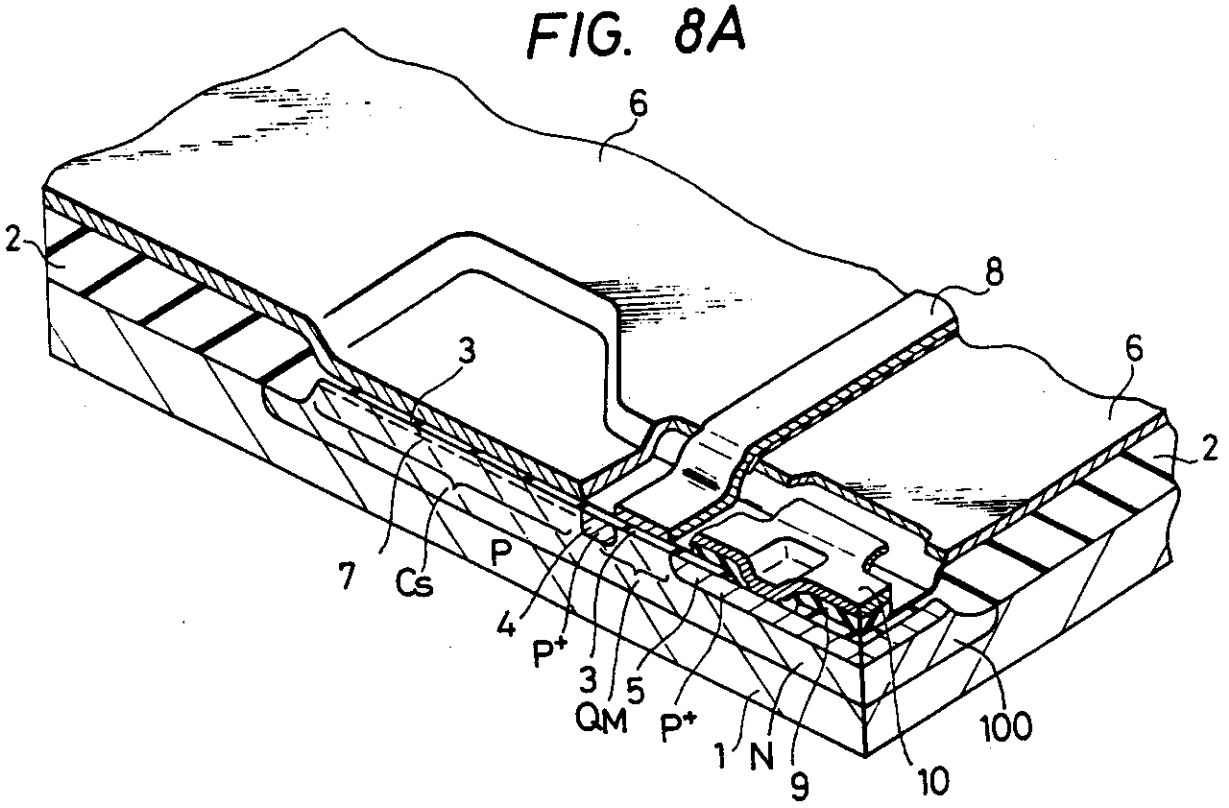


FIG. 8B

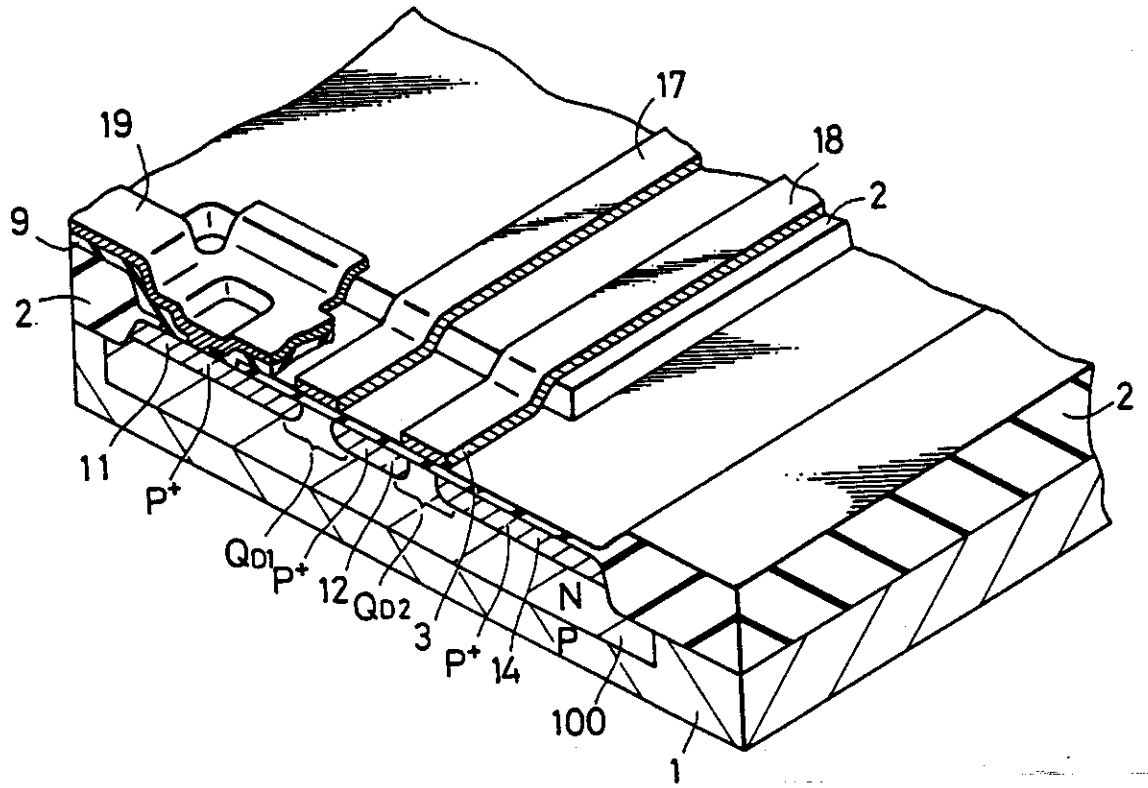


FIG. 9A

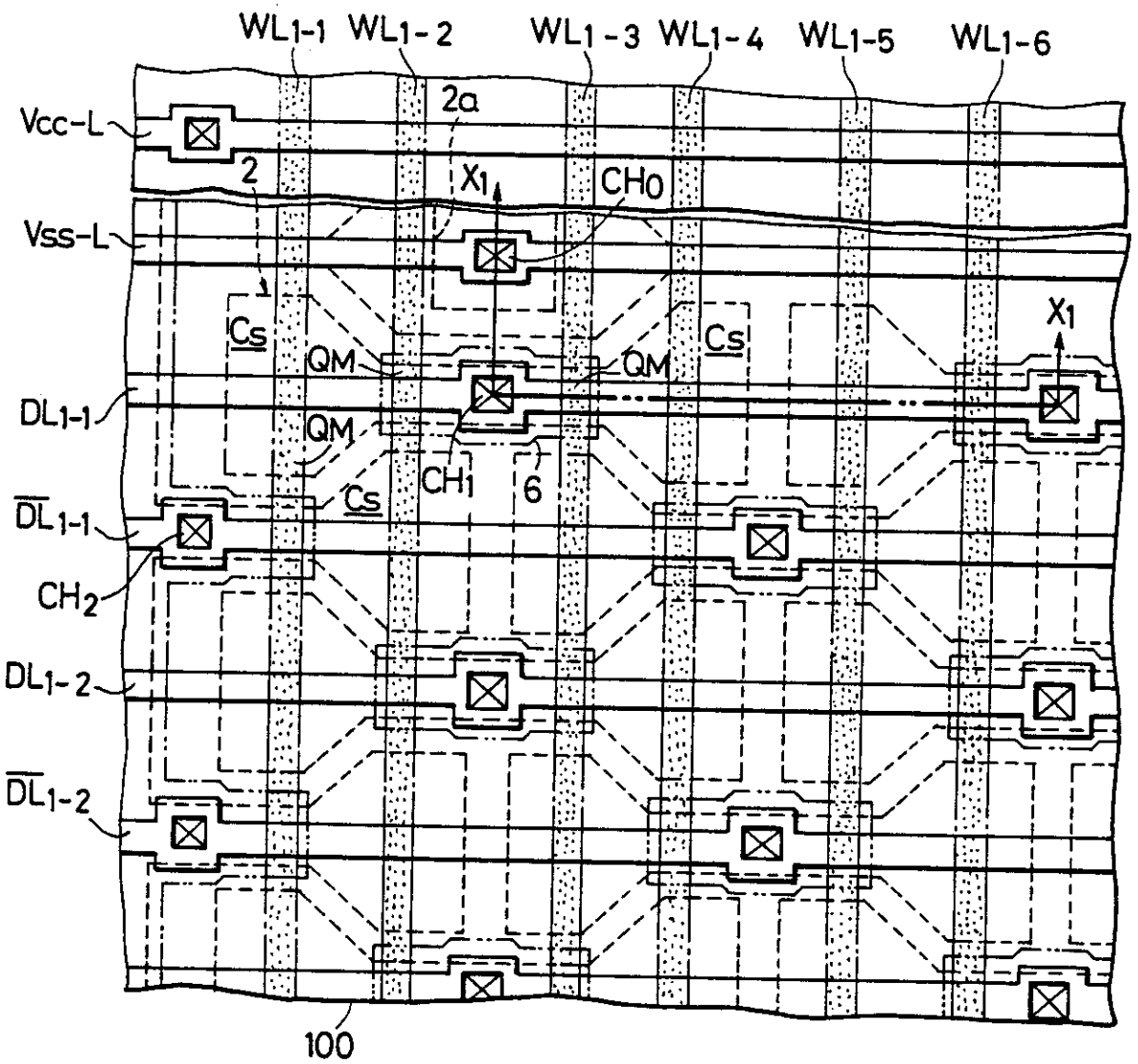

WL1-1
WL1-2
WL1-3
WL1-4
WL1-5
WL1-6
Vcc-L
Vss-L
2
2a
X1
CH0
Cs
QM
DL1-1
CH1
6
DL1-1
CH2
DL1-2
DL1-2
100

FIG. 9B

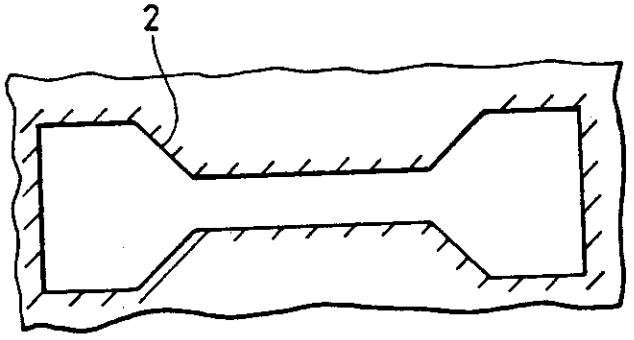


FIG. 9C

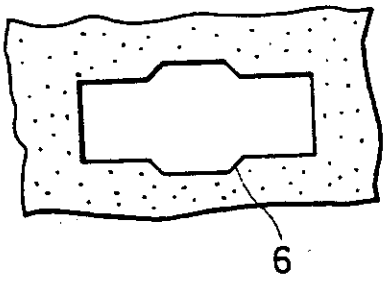


FIG. 9D

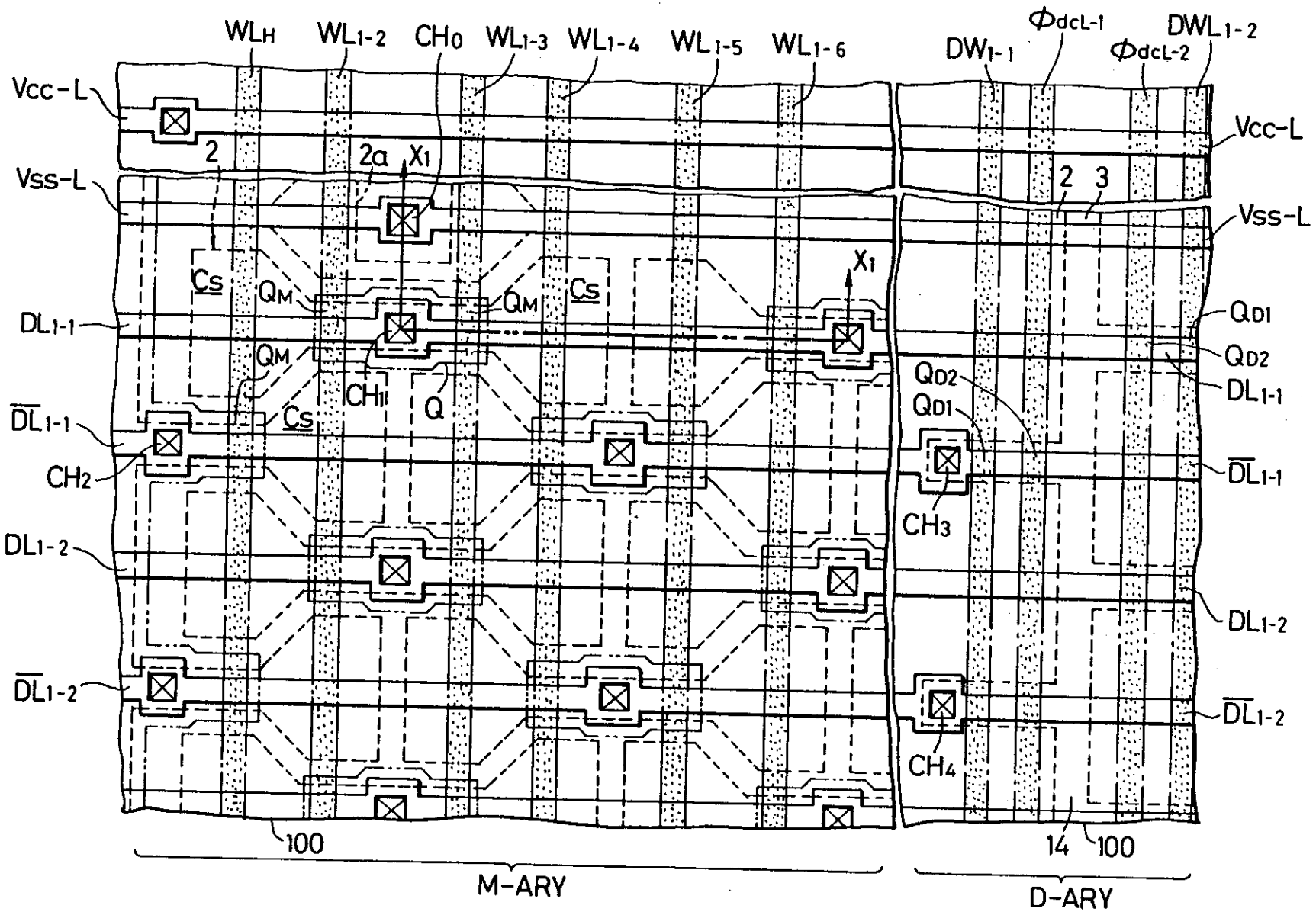

WLH
WL1-2
CH0
WL1-3
WL1-4
WL1-5
WL1-6
DW1-1
ΦdcL-1
ΦdcL-2
DWL1-2
Vcc-L
Vss-L
2
2a
X1
2
3
Cs
QM
QM
Cs
X1
DL1-1
QM
CH1
Q
QD1
QD2
QD2
QD1
DL1-1
DL1-1
Cs
CH2
CH3
DL1-2
DL1-2
DL1-2
DL1-2
CH4
100
14
100
M-ARY
D-ARY

FIG. 10

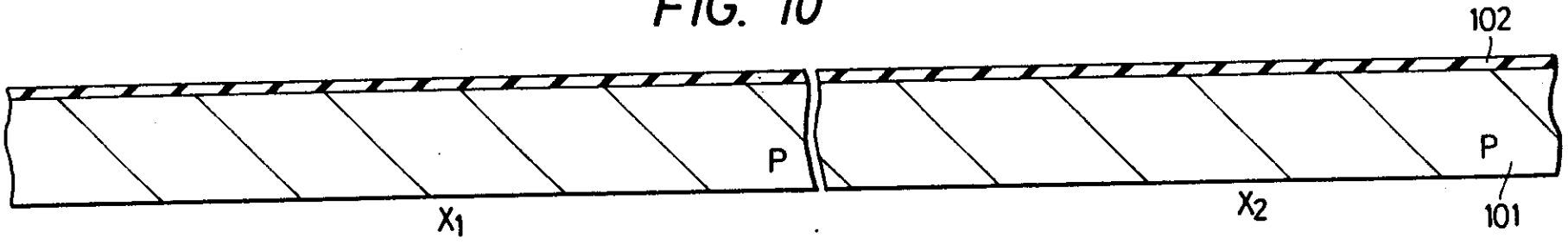


FIG. 11

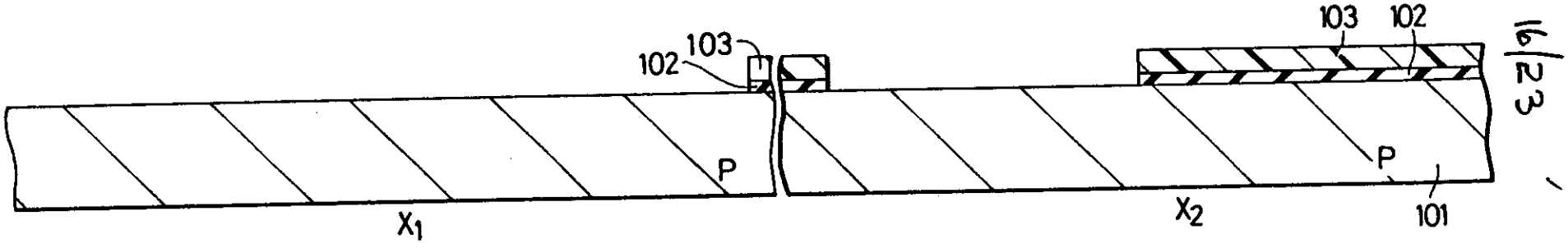
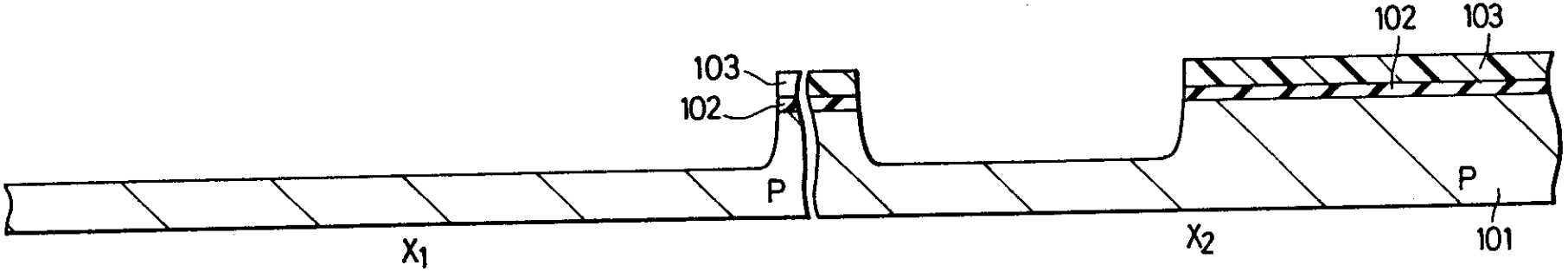


FIG. 12



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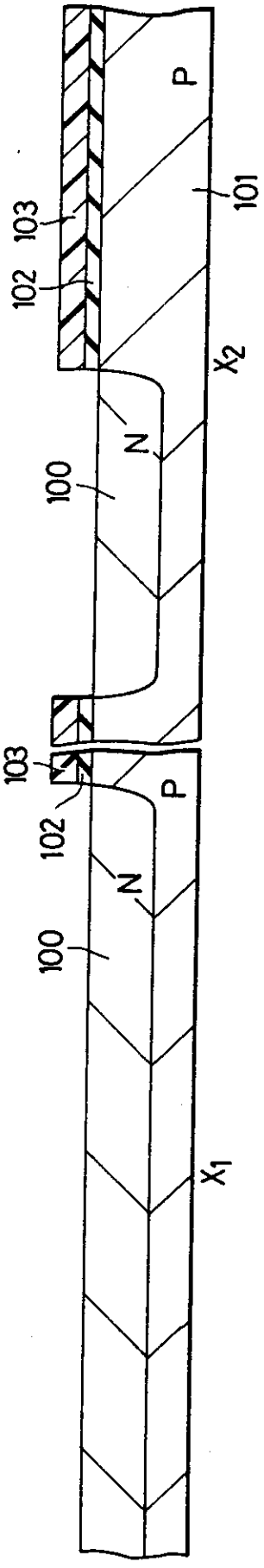

FIG. 13

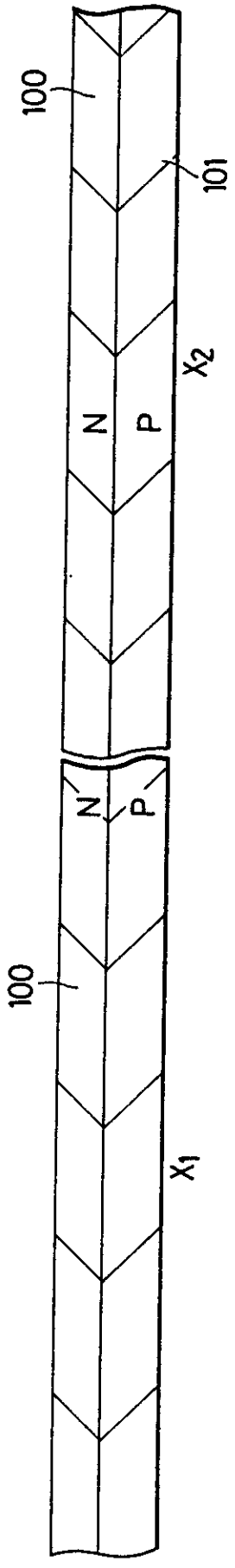

FIG. 14

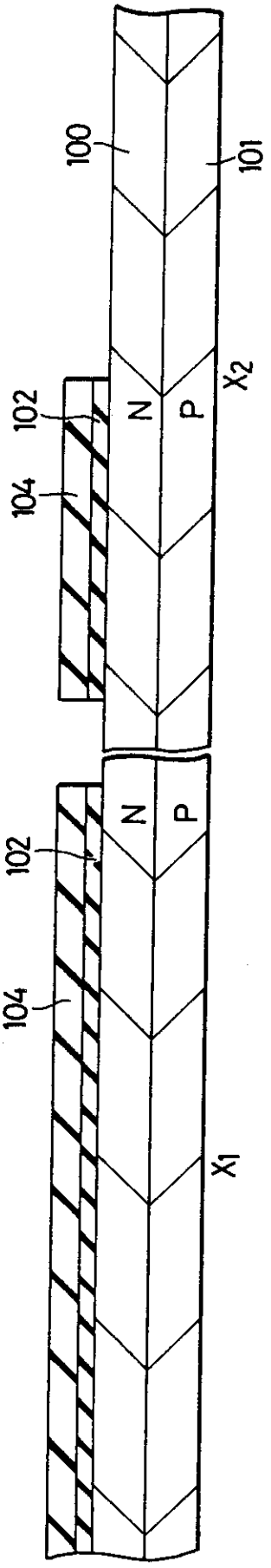

FIG. 15

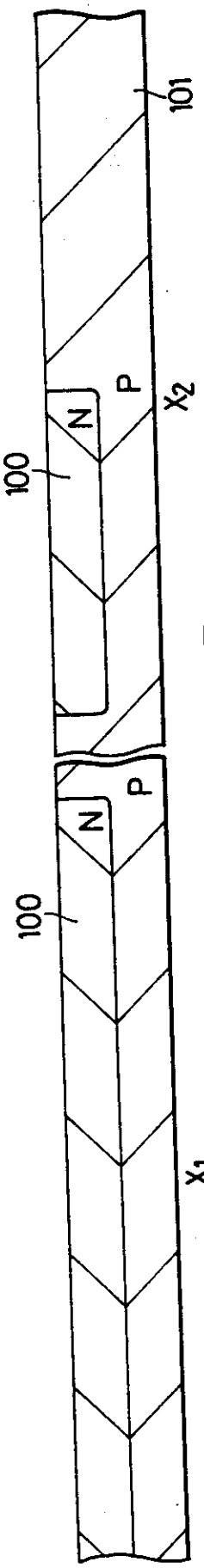

FIG. 16

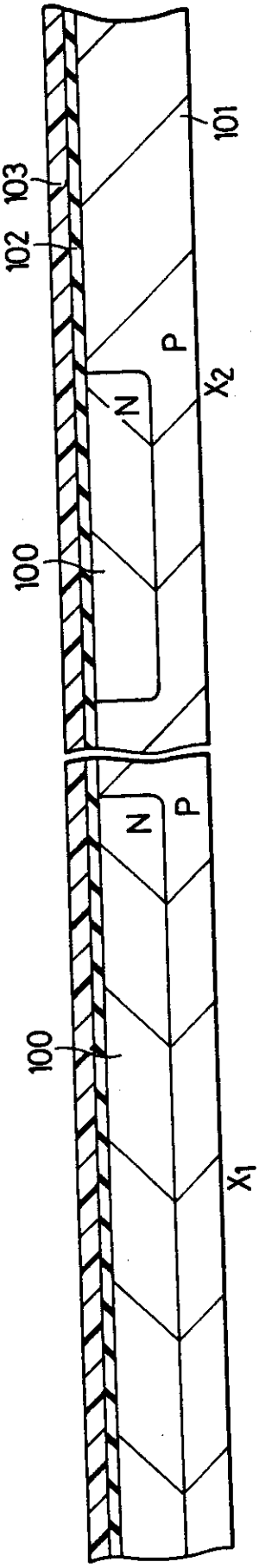

FIG. 17

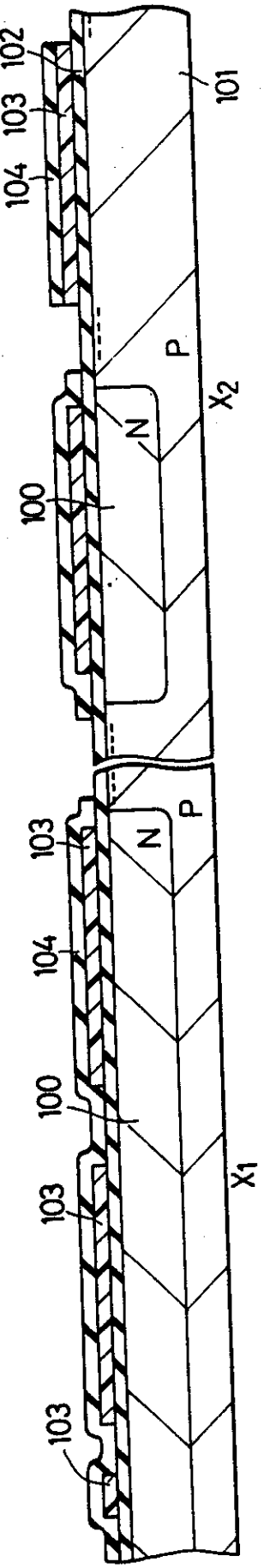

FIG. 18

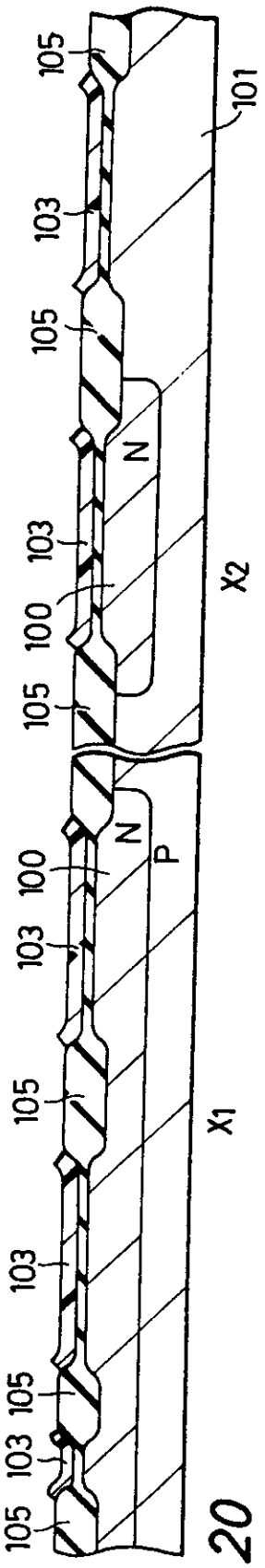

FIG. 19

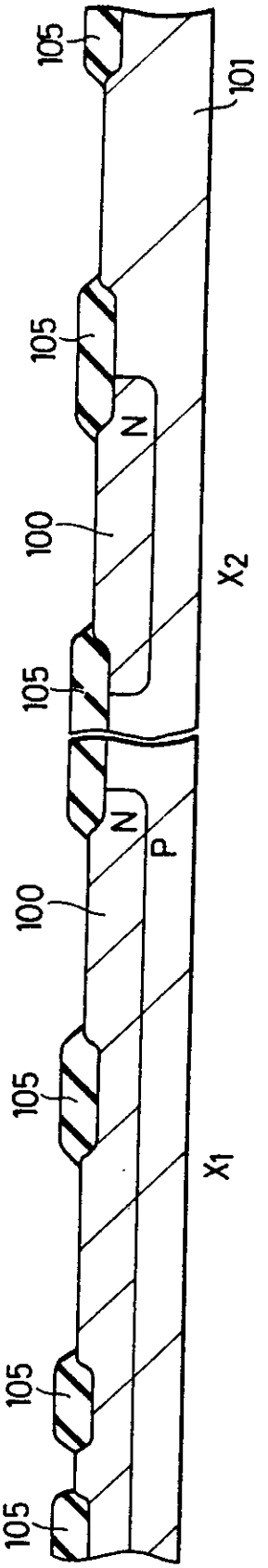

FIG. 20

FIG. 21

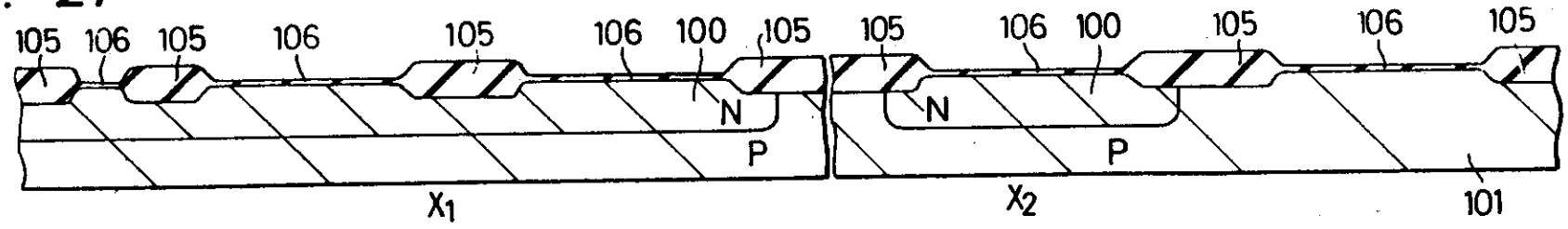

FIG. 22

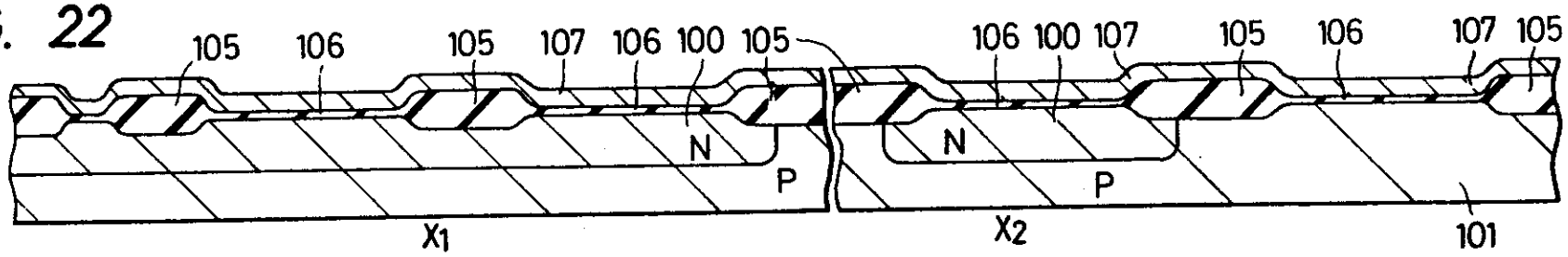

FIG. 23

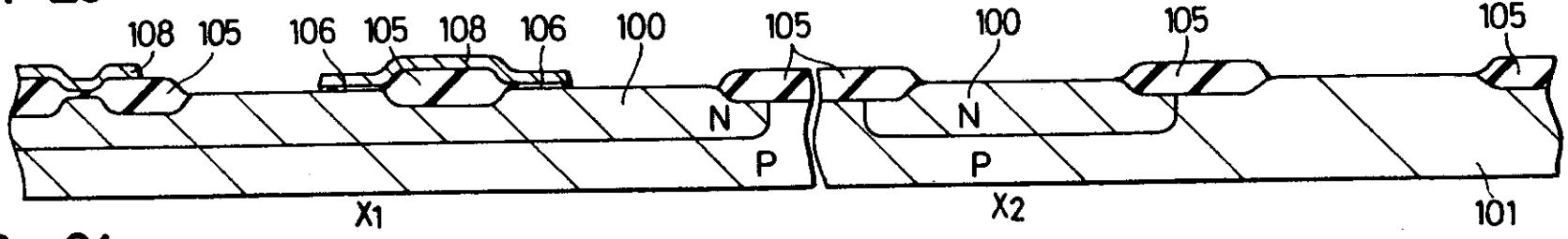

FIG. 24

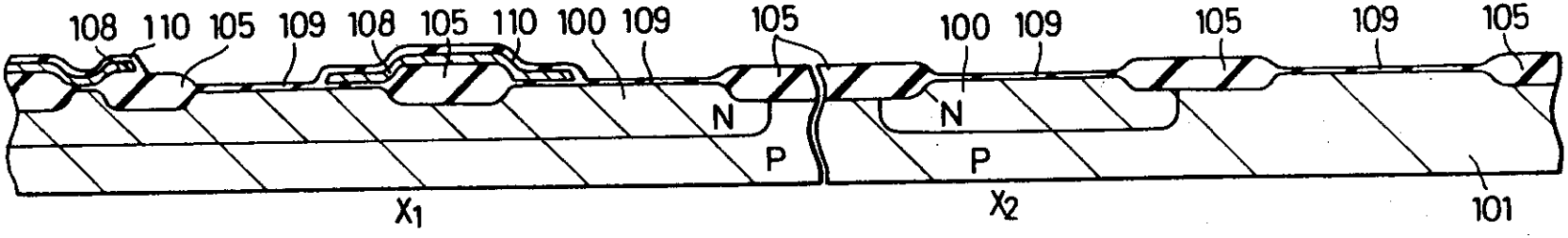

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FIG. 25

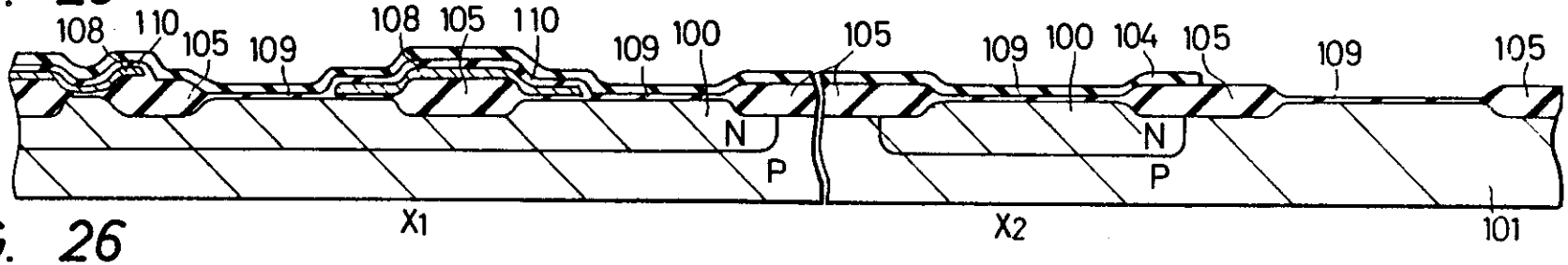

FIG. 26

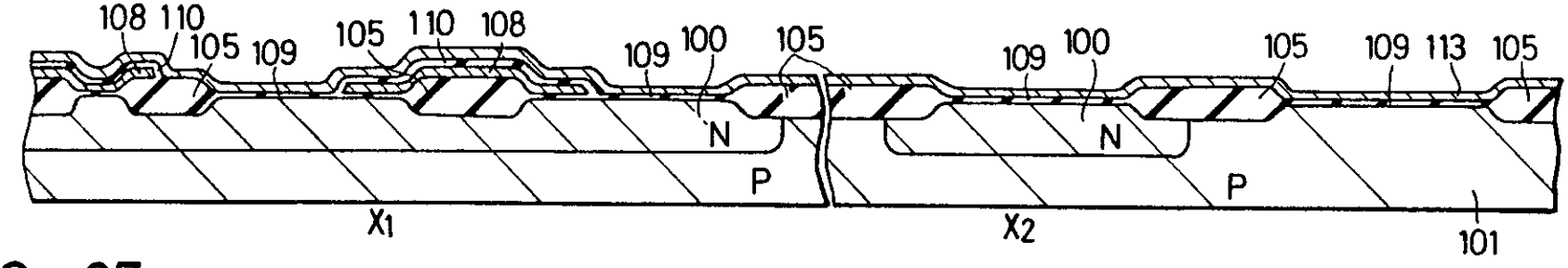

FIG. 27

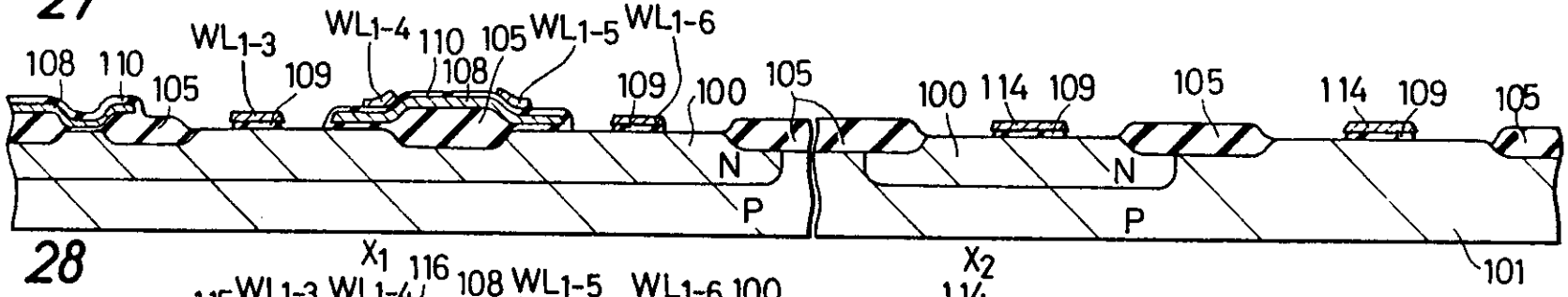

FIG. 28

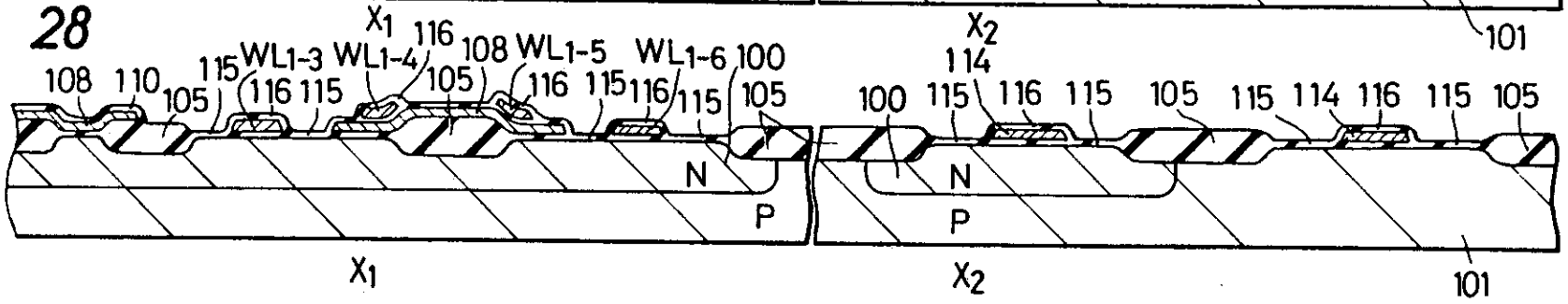

FIG. 29

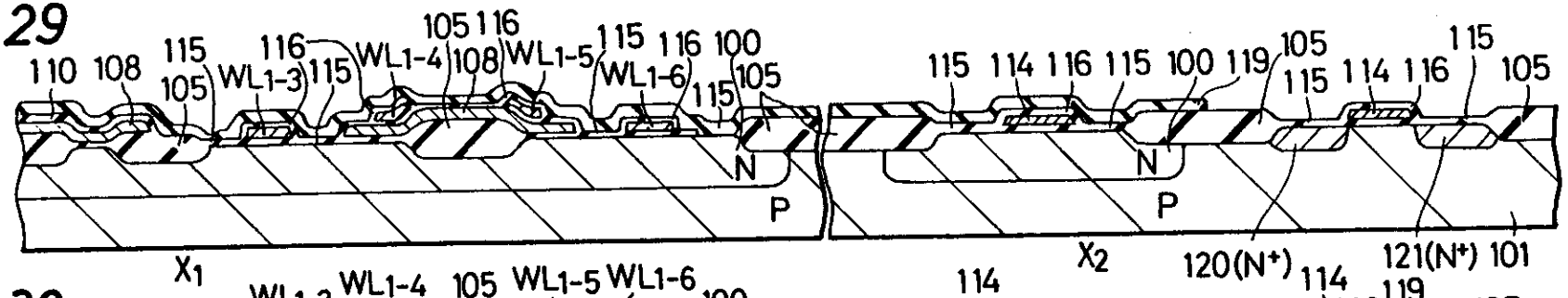

FIG. 30

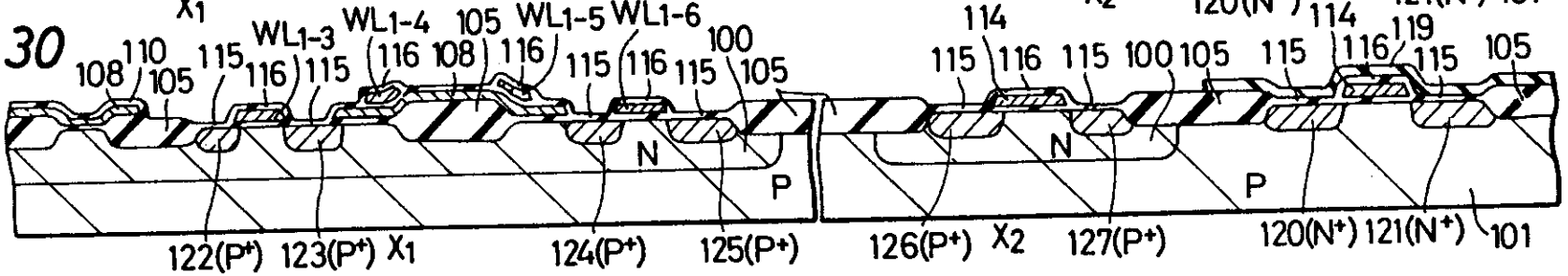

FIG. 31

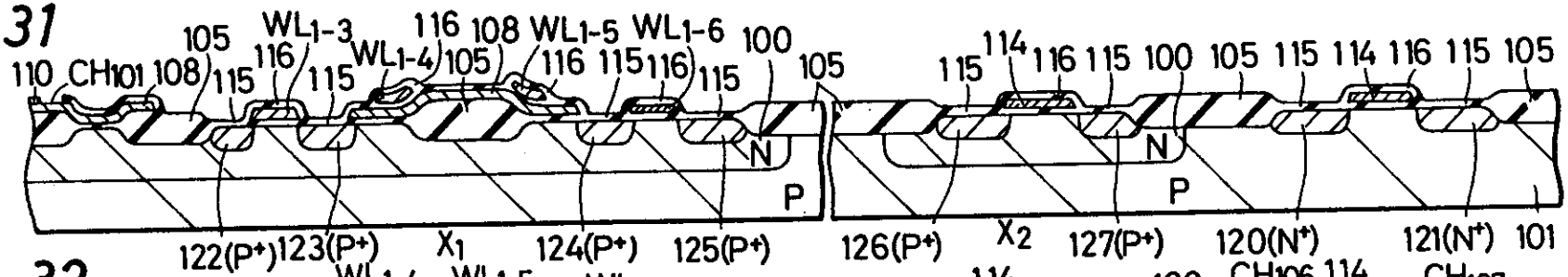

FIG. 32

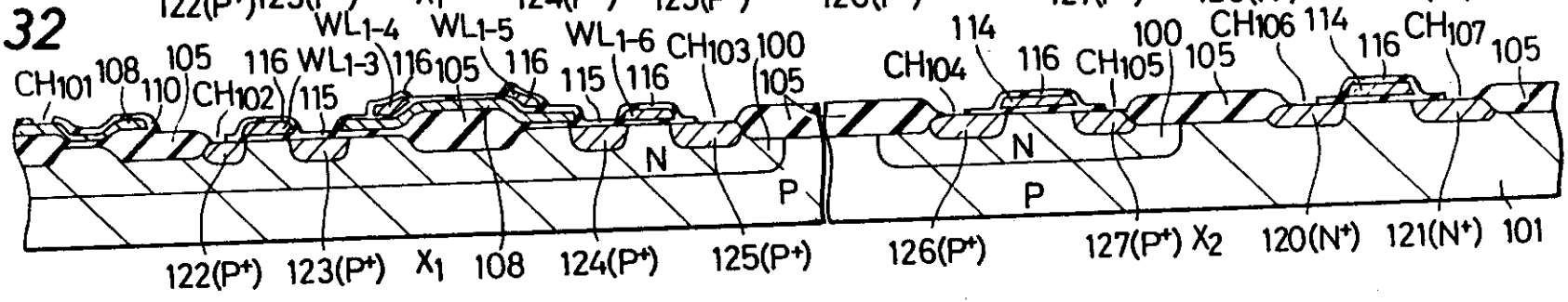

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FIG. 33

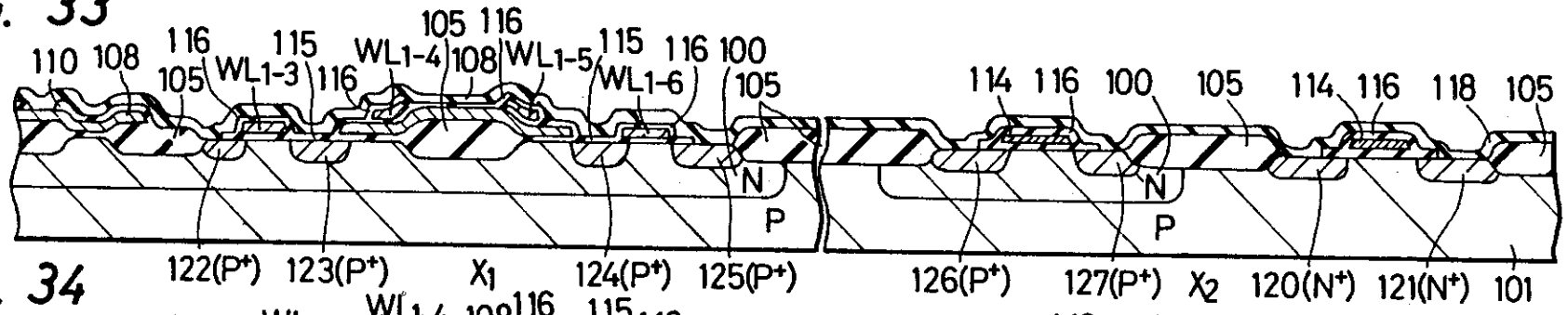


FIG. 34

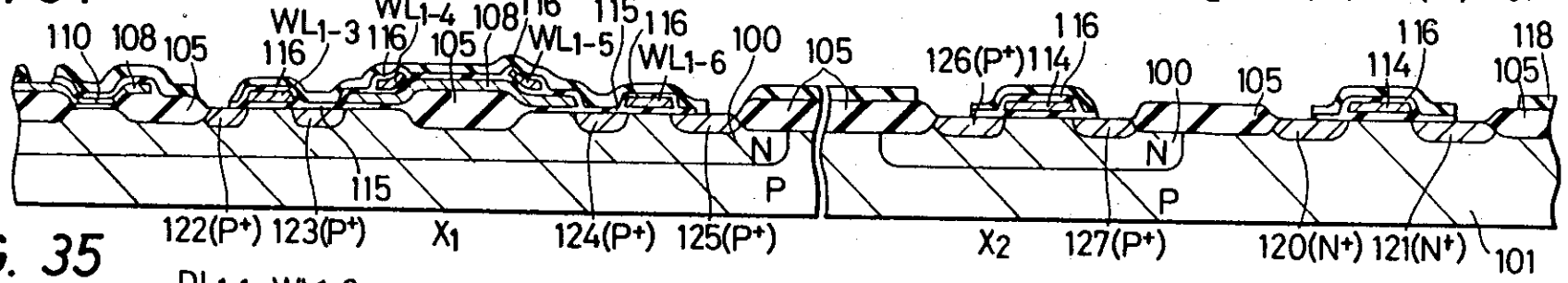
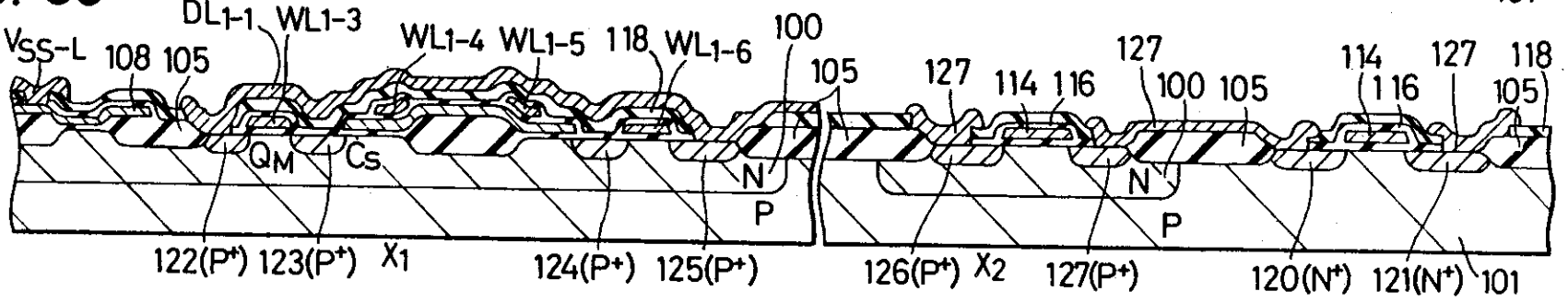


FIG. 35



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"A semiconductor memory".

The present invention relates to a semiconductor memory. More particularly, it relates to a semiconductor memory which is constructed of MISFETs (Metal-Insulator-Semiconductor Field Effect Transistors) represented by MOSFETs (Metal-Oxide-Semiconductor Field Effect Transistors) (hereinafter abbreviated to "MOS").

Hereinafter, a P-channel MOSFET and an N-channel MOSFET shall be respectively called "P-MOS" and "N-MOS", and a complementary MOSFET with both the MOSFETs combined shall be called "CMOS". A pair of data lines connected to a sense amplifier as are formed in parallel with each other shall be named "folded data lines".

The so-called one-element memory cell which is constructed of one MOSFET and one capacitor has few elements and also has few

connections, and therefore has the advantage that the size of the memory cell is small. For this reason, a semiconductor memory employing one-element type memory cells is being put into extensive use as a dynamic RAM having a large memory capacity.

Since the performance of a sense amplifier in the dynamic RAM is greatly influential on the operation margin of the memory, the sense amplifier is the most important in the circuit design as to the one-element type memory cell. In addition, the sense amplifier must be formed in one semiconductor substrate together with the memory cells by the semiconductor integrated circuit technology efficiently so as not to require a large occupying area.

On the other hand, in the dynamic RAM, the structure of the memory cell must be considered so that a soft error attributed to an α-particule (alpha-particle) is preventable. Further, when integrated to be unitary with the sense amplifier, the memory cell is required to be high in the speed of read-out of an information.

It is an object of the present invention to enhance the performance of a dynamic RAM which is constructed of one-element type memory cells, owing to a specific combination between the

structure of a sense amplifier and the structure of the memory cell.

According to the present invention there is provided a dynamic type semiconductor memory including:

(a) a plurality of pairs of data lines to which memory cells are connected;

(b) differential amplifiers each of which amplifies a difference between signal magnitudes appearing on each corresponding pair of data lines; said each differential amplifier including a pair of P-channel MOSFETs which have their drains and gates cross-coupled to each other and which have the drains connected to the corresponding pair of data lines respectively, a pair of N-channel MOSFETs which have their drains and gates cross-coupled to each other and which have the drains connected to the corresponding pair of data lines respectively, and a circuit which controls positive feedback operations of both MOSFET pairs;

(c) a plurality of word lines each of which is arranged in a manner to intersect with both of the pair of data lines; and

(d) a precharging circuit which sets said respective pairs of data lines at a potential intermediate between two potentials representative

of binary signals to be stored in said memory cells, before the positive feedback operations are started.

Preferably the control signals with which the positive feedback operation of the P-channel FET pair and that of the N-channel FET pair are started at different timings, are applied to the positive feedback operation-control circuit.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:

Figure 1 is a diagram of a semiconductor memory system in a dynamic RAM (D-RAM);

Figure 2 is a block diagram of a D-RAM;

Figures 3A and 3B are waveform diagrams of the D-RAM;

Figure 4A is a block diagram of a first embodiment of a D-RAM;

Figure 4B is a waveform diagram of the D-RAM shown in Figure 4A;

Figure 4C is a block diagram of a second embodiment of the D-RAM;

Figure 4D is a waveform diagram of the D-RAM shown in Figure 4C;

Figure 4E is a block diagram of a third embodiment of a D-RAM;

Figure 5A is a circuit diagram of a fourth embodiment being a 2-mat type 64 Kbit D-RAM;

Figure 5B is a waveform diagram of the 2-mat type 64 Kbit D-RAM shown in Figure 5A;

Figure 6 is a diagrammatic arrangement of a fifth embodiment of a 2-mat type D-RAM IC:

Figures 7A and 7B are partial layout pattern diagrams of the 2-mat type D-RAM ICs shown in Figure 6;

Figure 8A is a perspective structural view of a memory cell;

Figure 8B is a perspective structural view of a dummy cell;

Figure 9A is a diagrammatic arrangement of a memory array;

Figure 9B is a diagram of a field insulating film in a memory;

Figure 9C is an electrode diagram of a storing capacitor in a memory cell;

Figure 9D is a diagrammatic arrangement of a memory array and a dummy array; and

Figures 10 to 35 are sectional views of a C-MOS dynamic RAM showing the respective steps in the manufacture thereof.

Embodiments in which this invention is applied to a dynamic RAM employing one-element type memory cells will now be described with reference to the drawings.

The construction of a dynamic memory system will be explained with reference to Figure 1. First, a block diagram MS enclosed with a dotted line indicates a dynamic memory system. This system is constituted by a D-RAM IC ARRAY portion in which a plurality of IC chips IC_{11} - IC_{mB} of a D-RAM are arrayed (hereinafter referred to as a "D-RAM"), a central processing unit portion of a computer (not shown, and hereinafter referred to as a "CPU"), and an interface circuit IF between the CPU and the D-RAM.

Next, input and output signals between the dynamic memory system and the CPU will be explained. Address signals A_0 - A_k are signals for selecting the address of the D-RAM. REFGRNT denotes a refresh grant signal for refreshing the memory information of the D-RAM. $\overline{WE}$ denotes a write enable signal,

which is a read-out and write-down instruction signal for data in the D-RAM. MS denotes a memory start signal for starting the memory operation of the D-RAM. D_1 to D_8 designate input/output data on a data bus which couples the CPU and the D-RAM. REFREQ designates a refresh request signal for the memory information of the D-RAM.

The dynamic memory system will now be explained on the D-RAM and the interface circuit (IF) separately. The D-RAM is made up of an IC array which is formed into a matrix arrangement of (n x m) words x B bits in such a way that n·kbit integrated circuits received in individual IC packages (hereinafter referred to as "nk") are arrayed in a number m in each column and in a number B in each row. It should be noted that 1kbit inidcates 2^{10} = 1024 bits.

The interface circuit IF will be first described. It has the following components:-

(a) a row address receiver RAR which receives the address signals A_0 - A_i among the address signals A_0 - A_k transmitted from the CPU and which converts them into address signals of timings adapted to the operation of the D-RAM.

(b) a column address receiver CAR which receives the address signals A_{i+1} - A_j among the address signals A_0 - A_k and which converts them into address signals of timings adapted to the operation of the D-RAM.

(c) an address receiver ADR which receives

the address signals $A_{j+1} - A_k$ among the address signals $A_0 - A_k$ and which converts them into address signals of timings adapted to the operation of the D-RAM.

(d) a decoder DCR which transmits a chip selection control signal for selecting the chip of the D-RAM (hereinafter referred to as "$CS_1 - CS_m$" where $m = 2^{k-j}$).

(e) a RAS control circuit RAS-CT which transmits a chip selection signal and a row address introducing signal of timings adapted to the operation of the D-RAM.

(f) an address multiplexer ADM which multiplexes the address signals $A_0 - A_i$ and $A_{i+1} - A_j$ in time sequence and then transmits them to the D-RAM.

(g) a refresh synchronous generator RSG which determines a timing for refreshing the memory information of the D-RAM.

(h) a refresh address counter RAC which transmits refresh address signals $R_0 - R_1$ in order to refresh the memory information of the D-RAM.

(i) a data bus driver DED whose data input and output operations between the CPU and the D-RAM are switched by the $\overline{WE}$ signal.

(j) a control circuit C-CT which transmits signals for controlling the above-mentioned RAC, ADM, RAS-CT, DBD and D-RAM.

The actions of the address signals within the dynamic memory system will now be described.

The address signals A_0 - A_k which are transmitted from the CPU are divided into the two functions of the address signals A_0 - A_j and the address signals A_{j+1} - A_k within the dynamic memory system.

More specifically, the address signals A_0 - A_j are used as the address signals of memory matrices within the respective chips of the D-RAM.

On the other hand, the address signals A_{j+1} - A_k become the chip selection signal which, when viewed from the IC chip of the D-RAM, determines whether or not the entire chip is selected.

Here, in conformity with the matrix within the IC chip of the D-RAM, the address signals A_0 - A_j are so designed that the address signals A_0 - A_i are allotted to the selection of the row of the IC chip array, while those A_{i+1} - A_j to the selection of the column of the IC chip array.

Now, circuit operations within the dynamic memory system will be described.

$\overline{RAS}$ signals or $\overline{RAS_1}$ - $\overline{RAS_m}$ signals, a $\overline{RAS_a}$ signal and a $\overline{RAS_b}$ signal are row address strobe signals, while a $\overline{CAS}$ signal is a column address strobe signal.

The address signals A_0 - A_i and those A_{i+1} - A_j are respectively applied to the ADM through the RAR and CAR.

When the $\overline{RAS_b}$ signal has become a certain level, the row address signals $A_0 - A_i$ are transmitted from the ADM and applied to the address terminals of the D-RAM. At this time, the column address signals $A_{i+1} - A_j$ are prevented from being transmitted.

Next, when the $\overline{RAS_b}$ signal has become the opposite level to the above, the column address signals $A_{i+1} - A_j$ are transmitted from the ADM and applied to the address terminals. At this time, the row address signals $A_0 - A_i$ are prevented from being transmitted from the ADM.

In this way, the address signals $A_0 - A_i$ and $A_{i+1} - A_j$ are applied to the address terminals of the D-RAM in time sequence in accordance with the levels of the $\overline{RAS_b}$ signal.

Since a refresh control signal R_{cs} is applied to neither the ADM nor the RAC, the refresh address signals $R_0 - R_\ell$ are not transmitted from the ADM.

The chip selection signals $A_{j+1} - A_k$ are converted through the DCR into the chip selection control signals $CS_1 - CS_m$ ($m = 2^{k-j}$) which principally select the chips within the D-RAM. The converted signals are further converted into the $\overline{RAS_1} - \overline{RAS_m}$ signals whose timings have been controlled by the $\overline{RAS_a}$ signal and which are used as the chip selecting signals and the row address introducing signals.

There will now be explained the operation of setting addresses within the chips in each column of the D-RAM.

First, the row address signals A_0 - A_i are applied to the address terminals of all the IC chips of the D-RAM.

It is assumed that when one of the $\overline{RAS_1}$ - $\overline{RAS_m}$ signals, for example, the $\overline{RAS_1}$ signal has thereafter become a certain level, the ICs numbering B as located in the uppermost stage are selected. At this time, the row address signals A_0 - A_i are introduced into the row addresses of the memory matrix arrays within the IC (IC_{11}, IC_{12}, ····· IC_{1B}) chips. Here, the reason why the row address signals A_0 - A_i are applied to the ICs in advance of the $\overline{RAS_1}$ signal is that, when the $\overline{RAS_1}$ signal is applied before the row address signals A_0 - A_i, signals other than the row address signals might be introduced.

Subsequently, the column address signals A_{i+1} - A_j are applied to the address terminals of all the IC chips of the D-RAM.

Thereafter, when the $\overline{CAS}$ signal delayed with respect to the $\overline{RAS_1}$ signal has become a certain level, the column address signals A_{i+1} - A_j are introduced into the column addresses of the memory matrix arrays within the B IC chips of n·k bits located in the uppermost stage. Here, the reason why the column address signals

A_{i+1} - A_j are applied to the ICs in advance of the $\overline{CAS}$ signal is the same as the aforecited reason.

The action of the $\overline{CAS}$ signal is to distinguish which signals are being sent between the row address signals A_0 - A_i and the column address signals A_{i+1} - A_j.

By the above operation, the addresses within the B nk chips in the uppermost stage of the D-RAM have been set.

The ICs except those in the uppermost stage of the D-RAM are not selected because the $\overline{RAS_2}$ - $\overline{RAS_m}$ signals are at the opposite level to the level of $\overline{RAS_1}$.

The write-down operation and read-out operation of data in the set addresses will now be explained.

The D-RAM is so designed that the write-down operation and read-out operation of data are determined by the high level or low level of the write enable signal $\overline{WE}$.

The write-down operation is executed in such a way that when the $\overline{WE}$ signal is at a certain level, data D_{I1} - D_{IB} from the CPU are applied to the set addresses.

The read-out operation is executed in such a way that when the $\overline{WE}$ signal is at the opposite level to the above, the data D_{01} - D_{0B} of the

respective addresses having been written down are delivered at B bits.

In Figure 1, abbreviations signify the actions of signals. The abbreviation over which an inversion symbol (bar) is attached indicates that when the signal is at "0" (low level), the action signified by the abbreviation is executed, while the abbreviation without the bar symbol indicates that when the signal is at "1" (high level), the action is executed.

The C-CT receives the instruction signals from the CPU, i.e. the REFGRNT signal, $\overline{WE}$ signal and MS signal and delivers the $\overline{CAS}$ signal, $\overline{RAS_a}$ signal, $\overline{RAS_b}$ signal, $\overline{WE}$ signal and R_{cs} signal. The actions of these delivered control signals will be explained.

The $\overline{CAS}$ signal is the signal for distinguishing which of the row address signals A_0 - A_i and the column address signals A_{i+1} - A_j are being transmitted to the respective chips within the D-RAM, and also the signal for introducing the column address signals of the IC chips.

The $\overline{RAS_a}$ signal is the signal for adjusting the timings of the CS_1 - CS_m signals and supplying the adjusted signals to the IC chip array within the D-RAM.

The $\overline{WE}$ signal is the signal for determining the read-out of data from the memory cells within the IC chips of the D-RAM and the write-down of data into the memory cells.

The R_{cs} signal is the signal for starting the refresh operation and for inhibiting the ADM from transmitting the address signals $A_0 - A_i$ and $A_{i+1} - A_j$ and simultaneously permitting it to transmit the refresh address signals $R_0 - R_\ell$ from the RAC.

The $\overline{RAS_b}$ signal is the switching timing signal for converting the row address signals $A_0 - A_i$ and column address signals $A_{i+1} - A_j$ from the ADM into the time-sequential multiplexed signals. In addition, it is made a signal according to which the time of the switching between the row address signals $A_0 - A_i$ and the column address signals $A_{i+1} - A_j$ is delayed with respect to the $\overline{RAS_a}$ signal so that the row address signals $A_0 - A_i$ may have been provided from the ADM when one of the $\overline{RAS}$ ($\overline{RAS_1} - \overline{RAS_m}$) signals is selected.

There will now be described the relationship between the $\overline{WE}$ signal and the data bus driver (DBD).

The $\overline{WE}$ signal transmitted from the C-CT is applied to the D-RAM and the DBD. By way of example, when the $\overline{WE}$ signal is at the high level, the read-out mode is established, and the data of the D-RAM are provided and transmitted to the CPU through the DBD. At this time, input data are controlled by the $\overline{WE}$ signal so as not to be introduced from the DBD into the D-RAM. When the $\overline{WE}$ signal is at the low level, the write-down mode is established, and the input data are applied from the CPU through the DBD to the data input terminals of the D-RAM and are written into the set addresses.

At this time, the data outputs of the D-RAM are controlled by the $\overline{WE}$ signal so as not to be provided from the DBD.

In the memory cell circuit of the D-RAM, an information is retained by accumulating charges in the MOS capacitor of the one-element type memory cell, and the charges disappear with time on account of leakage current. Problematic here is that when the charges of the information "1" (high level) have disappeared to become less than a reference level for discriminating the information "1" and "0", the information "1" is discriminated as "0", resulting in a malfunction. In order to keep the information "1" stored, the charges need to be refreshed before they decrease below the reference level. The refresh operation needs must be carried out within the information storage time of the memory cell. Accordingly, the refresh mode has preference to the read-out mode and the write-down mode.

The refresh operation will now be explained with reference to Figure 1.

The refresh synchronous generator RSG transmits the refresh request signal REFREQ to the CPU every period of (information storage time)/(number of refresh cycles). The number of refresh cycles is equivalent to the number of word lines connected to a column data line.

Upon receiving the REFREQ, the CPU transmits the refresh grant signal REFGRNT. At this time, neither the write enable signal $\overline{WE}$ nor the memory start signal MS is transmitted from the CPU. When the REFGRNT is applied to the control circuit C-CT, the refresh control signal R_{cs} being the output signal thereof is applied to the address multiplexer ADM and the refresh address counter RAC. Then, the ADM responds to the R_{cs} signal to send the address signals exclusive for refresh $R_0 - R_\ell$ to the D-RAM in place of the address signals for random access $A_0 - A_j$.

Refreshing methods in the D-RAM are broadly classified into two. One of them is a method in which the respective rows of the IC chip array (IC_{11}, IC_{12}, ····· and IC_{1B} constitute one row) are refreshed by turns. This method has the advantage that the power dissipation required for the refresh operation may be low, but has the disadvantage that the period of time taken for the refresh operation is long.

The other method is a method in which the whole IC chip array of the D-RAM is simultaneously refreshed. This method performs the refresh in such a manner that, although no illustration is made in Figure 1, the address signals $A_{j+1} - A_k$ from the address receiver ADR are applied to the RAS control circuit RAS-CT without

passing through the decoder DCR, all the output signals $\overline{RAS_1}$ - $\overline{RAS_m}$ of the RAS-CT becoming a certain level, the ICs of all the columns of the D-RAM being selected at the same time.

The advantage of this method is a short period of time taken for the refresh, whereas the disadvantage is a high power dissipation.

The refresh operation in the matrix array within the IC of the D-RAM will now be explained.

The refresh address signals R_0 - R_1 are applied from the ADM to the address terminals of the D-RAM, the $\overline{RAS}$ signal thereafter becomes a certain level, and the 2^{l+1} row addresses of the IC matrix array are successively selected. At this time, the $\overline{CAS}$ signal is held at the opposite level to the above. The refresh is accordingly performed in such a manner that the information of the memory cells connected to the selected row addresses are amplified by a sense amplifier (not shown) so as to expand the level difference between "1" and "0".

Since the $\overline{WE}$ signal is transmitted to neither the D-RAM nor the DBD during the refresh operation, the input or output operation of data from the DBD is not executed.

The actions of RAS-group signals (hereinafter, termed "RAS-ϕ") [and CAS-group signals (hereinafter, termed "CAS-ϕ")] will be explained with reference to Figure 2.

ϕ_{AR} is an address buffer control signal, which is a signal that is applied to an address buffer ADB and that determines whether or not levels a_0, $\overline{a_0}$, ... and a_i, $\overline{a_i}$ corresponding to the row address signals A_0 - A_i as latched in the ADB are to be transmitted to a row and column decoder RC-DCR.

ϕ_X is a word line control signal, which is a signal that is applied to the RC-DCR and that determines whether or not one selected signal is to be transmitted to a memory array M-ARY in order to select the row address of the M-ARY.

ϕ_{PA} is a sense amplifier control signal, which is a signal that is applied to a sense amplifier SA and that drives the SA.

(2) CAS-ϕ

ϕ_{AC} is an address buffer control signal, which is a signal that is applied to the ADB and that determines whether or not levels a_{i+1}, $\overline{a_{i+1}}$, ... and a_j, $\overline{a_j}$ corresponding to the column address signals A_{i+1} - A_j as latched in the ADB are to be transmitted to the RC-DCR.

ϕ_Y is a column switch control signal, which is a signal that is applied to the RC-DCR and that selects a column switch C-SW connected to the column data line of the M-ARY, by means of one selected signal.

ϕ_{OP} is a data output buffer and output amplifier control signal, which is a signal that is applied to a data output buffer DOB and an output amplifier OA and that transmits a read-out data from the M-ARY to an output data terminal D_{out}.

ϕ_{RW} is a data input buffer control signal, which is a signal that is applied to a data input buffer DIB and that transmits a write-down data from an input data terminal D_{in} to the M-ARY.

$\overline{\phi_{RW}}$ is a data output buffer control signal, which is a signal that is applied to the DOB and that prevents any data from being delivered to the data output terminal D_{out} during the write-down operation.

The construction of the D-RAM will be described with reference to Figure 2.

In the IC, a block enclosed with a two-dot chain line is a timing pulse generating block TGB, which comprises circuits for generating the signals to control the operations of the various circuits of the D-RAM.

The operations of the various circuits of the D-RAM will now be described with reference to Figures 3A and 3B.

When the row address signals A_0 - A_i have been introduced into the address buffer ADB and latched therein, the $\overline{RAS}$ signal becomes the low level later than the row address signals A_0 - A_i. The measure of making the $\overline{RAS}$ signal later than the row address signals A_0 - A_i here, is intended to reliably introduce the row address signals A_0 - A_i as the row address in the memory array.

Subsequently, the signal ϕ_{AR} delayed from the $\overline{RAS}$ signal is applied to the ADB, so that the levels a_0, $\overline{a_0}$, ····· and a_i, $\overline{a_i}$ corresponding to the latched row address signals are transmitted to the row and column decoder RC-DCR. When the levels a_0, $\overline{a_0}$, ····· and a_i, $\overline{a_i}$ have been applied to the RC-DCR, this RC-DCR conducts the operation of allowing only selected ones to remain the high level and rendering unselected ones the low level.

The selected signals are transmitted to the M-ARY when the signal ϕ_X delayed from the signal ϕ_{AR} is applied to the RC-DCR. The measure of delaying ϕ_X with respect to ϕ_{AR} here, is intended to operate the RC-DCR after completion of the operation of the ADB. The row address in the M-ARY is thus set in such a manner that, since one of the 2^{i+1} output signals

of the RC-DCR becomes the high level, one row address line within the M-ARY as corresponds thereto is selected.

Next, the information "1" and "0" of the memory cells connected to the selected row address line in the M-ARY are respectively amplified by the sense amplifier SA shown in Figure 2. This operation of the SA starts upon application of the signal ϕ_{PA}.

Thereafter, when the column address signals $A_{i+1} - A_j$ have been introduced into the ADB and latched therein, the $\overline{CAS}$ signal becomes the low level later than the column address signals $A_{i+1} - A_j$. The measure of making the $\overline{CAS}$ signal later than the column address signals $A_{i+1} - A_j$ here, is intended to reliably introduce the column address signals as the column address in the memory array.

When the signal ϕ_{AC} delayed from the $\overline{CAS}$ signal is subsequently applied to the ADB, the levels a_{i+1}, $\overline{a_{i+1}}$ ..... and a_j, $\overline{a_j}$ corresponding to the column address signals are transmitted to the RC-DCR. Then, the RC-DCR conducts an operation similar to the above. The selected signals are transmitted to the column switch C-SW shown in Figure 2 when the signal ϕ_Y delayed from the signal ϕ_{AC} is applied to the RC-DCR. The column address in the M-ARY is thus set in such a manner that, since one of the 2^{j-i} output signals of the

AD-DCR becomes the high level, one C-SW is selected, so a column address line or data line connected to this C-SW is selected.

In this way, one address within the M-ARY is set. The read-out and write-down operations for the address set as described above will now be explained.

In the read-out mode, the $\overline{WE}$ signal becomes the high level. This $\overline{WE}$ signal is designed so as to become the high level before the $\overline{CAS}$ signal becomes the low level. The reason therefor is that, since the low level of the $\overline{CAS}$ signal results in setting one address of the M-ARY, the $\overline{WE}$ signal is brought into the high level beforehand, thereby to make ready for the read-out operation and to shorten a read-out starting time.

When the signal ϕ_{OP} of the CAS-group signal is applied to the output amplifier OA, this output amplifier becomes active, and the information of the set address is amplified and then read out at the data output terminal D_{out} through the data output buffer DOB. The read-out is carried out in this manner, and the read-out operation is completed when the $\overline{CAS}$ signal becomes the high level.

In the next place, in the write-down mode, the $\overline{WE}$ signal becomes the low level. When the signal ϕ_{RW} which is formed by the $\overline{WE}$ signal of the low level and

the $\overline{CAS}$ signal of the low level becomes the high level and is applied to the data input buffer DIB shown in Figure 2, the DIB becomes active and the write-down data from the input data terminal D_{in} is transmitted to the set address of the M-ARY, whereby the write-down operation is carried out.

Meantime, the inverted signal of the signal ϕ_{RW}, that is, the signal $\overline{\phi_{RW}}$ of the low level is applied to the DOB, to control the M-ARY so as to prevent the read-out of any data during the write-down operation.

A first preferred embodiment of the D-RAM is shown in Figure 4A.

An M-CEL of 1 bit consists of a capacitor C_S for storing an information and a P-MOS Q_M for selecting an address. The information of logic "1" or "0" is stored in the form of the existence or nonexistence of charges in the capacitor C_S. The information of the logic "1" is accumulated by a voltage V_{cc}, and that of the logic "0" by the null potential.

The gate of the P-MOS Q_M is connected to the word line WL, and one of the source and drain thereof is connected to the data line DL and the other to the capacitor C_S.

When the gate voltage of the P-MOS Q_M or a word voltage has become lower than the power source voltage $+V_{cc}$ by a threshold voltage V_{thp} (the threshold voltage of the P-MOS Q_M), the P-MOS Q_M turns "on" to permit the selection of the memory cell M-CEL.

In the case where an N-MOS is used for a prior-art memory cell (not shown), when the word voltage has been changed from 0 (zero) V to $(V_{cc} - V_{thn})$ (V_{thn}; the threshold voltage of the N-MOS Q_M), the N-MOS Q_M turns "on" to permit the selection of the memory cell.

The switching speed of the P-MOS Q_M shown in Figure 4A can be made higher than that of the N-MOS in such prior-art memory cell because the information of the logics "1" and "0" can be determined with only the magnitude between V_{cc} and $|V_{thp}|$. The detailed description of the switching operation of the P-MOS Q_M is contained in Japanese Patent Application Laid-open Specification No. 44189/81.

Sense amplifiers SA_1 and SA_2 are sense amplifiers

by which the difference of potential changes developing on folded data lines DL_{1-1} and $\overline{DL_{1-1}}$ during addressing is expanded in a sense period determined by the timing signals ϕ_{PA} and $\overline{\phi_{PA}}$ (sense amplifier control signals), and the input and output nodes of which are coupled to the pair of folded data lines DL_{1-1} and $\overline{DL_{1-1}}$ arranged in parallel.

The sense amplifiers SA_1 and SA_2 are connected in parallel, and it can be considered that both constitute a single sense amplifier. They differ, however, in that the SA_1 is constructed of N-MOS Q_{S7} and Q_{S8}, whereas the SA_2 is constructed of P-MOS Q_{S5} and Q_{S6} of the opposite conductivity type. Each sense amplifier is composed of a pair of cross-connected FETs (Q_{S5} - Q_{S8}) for effecting the positive-feedback differential amplification operation, and a FET (Q_{S4}, Q_{S9}) connected on the source side of the cross-connected FETs and for controlling the positive-feedback differential amplification operation.

The sense amplifiers SA_1 and SA_2 can also be deemed the single complementary sense amplifier as stated previously, and hence, they may well be arranged adjacent to one other. However, they can be arranged separately from one other as in Figure 4A (for example, at both the ends of the M-ARY) for the purpose of efficiently packaging them in consideration

of the arrangement and configuration of connections, the transistors or well regions.

The sense amplifier SA_2 and the memory array M-ARY which consist of the P-MOS, and the sense amplifier SA_1 and a precharging circuit PC which consist of the N-MOS can be arranged in an isolated manner. Therefore, the circuit arrangement within the chip can have the P-MOS portion and the N-MOS portion isolated, and the circuits can be efficiently packaged.

The folded data lines DL_{1-1} amd $\overline{DL_{1-1}}$ are formed of a metal such as Al, Au, Mo, Ta and W. Since the metal is very low in resistivity, voltage drops in the dada lines during the operation are small and no malfunction occurs.

The precharging circuit PC is composed of a pair of N-MOS Q_{S2} and Q_{S3} for precharging the data lines to about half (V_{DP}) of the power source voltage V_{CC}, and an N-MOS Q_{S1} for eliminating the unbalance of precharged voltages between both the data lines. As indicated by marks * in the figure, these N-MOS are designed so as to have threshold voltages lower than those of the other N-MOS.

The numbers of the memory cells to be coupled to the respective folded data lines DL_{1-1} and $\overline{DL_{1-1}}$

arranged geometrically in parallel with each other are made equal in order to raise the detection accuracy. Each memory cell is coupled between one word line WL and one of the folded data lines. Each word line WL crosses the adjoining pair of data lines. Therefore, even when a noise component developing on the word line WL has been put on the data lines by the electrostatic coupling, the induced noise components appear equally on both the data lines and are cancelled by the differential type sense amplifiers SA_1 and SA_2.

The operation of the circuit in Figure 4A will be described with reference to an operating waveform diagram in Figure 4B.

Before reading out the stored signal of the memory cell, when the precharge control signal ϕ_{PC} having a voltage higher than the V_{CC} voltage is at the high level, the N-MOS Q_{S2} and Q_{S3} become conductive, and the stray capacitances C_0 and $\overline{C_0}$ of the folded data lines DL_{1-1} and $\overline{DL_{1-1}}$ with respect to earth are precharged to about $\frac{1}{2} V_{CC}$. At this time, the N-MOS Q_{S1} becomes conductive simultaneously. Therefore, even when the voltages precharged by the N-MOS Q_{S2} and Q_{S3} have become unbalanced, the folded data lines DL_{1-1} and $\overline{DL_{1-1}}$ are short-circuited and are set at

the same potential. The N-MOS Q_{S1} to Q_{S3} have the threshold voltages V_{th} set to be lower than those of the transistors without the marks * lest any voltage loss should arise between the respective sources and drains.

On the other hand, the capacitor C_S in the memory cell holds a potential substantially equal to zero volt when the written information is of logic "0", and it holds a potential substantially equal to V_{CC} when the information is of logic "1". The precharged voltage V_{DP} of the data lines DL and $\overline{DL}$ is set to be intermediate between both the stored potentials.

Accordingly, in the case where the read line control signal ϕ_X becomes the high level so as to address the desired memory cell, the potential V_{DL} of one data line coupled to the memory cell becomes higher than V_{DP} when the information of "1" or the voltage V_{CC} has been read out, and it becomes lower than V_{DP} when the information of "0" or the zero potential has been read out. By comparing the potential of the above data line and the potential of the other data line which maintains the potential of V_{DP}, it can be discriminated whether the information of the addressed memory cell is "1" or "0".

The positive-feedback differential amplification

operations of the sense amplifiers SA_1 and SA_2 are started when the FETs Q_{S9} and Q_{S4} have begun to turn "on" owing to the respective timing signals (sense amplifier control signals) ϕ_{PA} and $\overline{\phi_{PA}}$. On the basis of the potential difference given at the addressing, the higher data-line potential (V_H) and the lower potential (V_L) change toward the voltage V_{CC} and the null potential V_{GND}, respectively, and the difference becomes wider. The sense amplifier SA_1 composed of the N-MOS Q_{S7}, Q_{S8} and Q_{S9} contributes to lower the potential of the data line to the null potential V_{GND}, while the sense amplifier SA_2 composed of the P-MOS Q_{S4}, Q_{S5} and Q_{S6} contributes to raise the potential of the data line to V_{CC}. The respective sense amplifiers SA_1 and SA_2 operate in the **earthed-source mode.**

When, in this way, the potential of $(V_L - V_{GND})$ has become equal to the threshold voltages V_{thn} of the N-MOS Q_{S7} and Q_{S8} of the sense amplifier SA_1, the positive feedback operation of the sense amplifier SA_1 ends. In addition, when the potential of $(V_{CC} - V_H)$ has become equal to the threshold voltages V_{thp} of the P-MOS Q_{S5} and Q_{S6} of the sense amplifier SA_2, the positive feedback operation of the sense amplifier SA_2 ends. Finally, V_L reaches the null potential and V_H reaches V_{CC}, and they become stable in a state

of low impedance.

The sense amplifiers SA_1 and SA_2 may be started to operate at the same time, SA_1 may well be started to operate previously to SA_2, and SA_2 may well be started to operate previously to SA_1. In point of the read-out speed, it is speedier to operate SA_1 and SA_2 at the same time. Since, however, a through current flows, the power dissipation increases. On the other hand, the expedient of making the operation starting times of SA_1 and SA_2 different has the advantage that the through current is avoided and that the power dissipation decreases. However, with regard to the read-out speed, this expedient is somewhat inferior to the above.

Figure 4C shows the circuit arrangement of a second detailed embodiment of the D-RAM. Parts corresponding to thos in Figure 4A bear the same reference symbols. The third embodiment is different from the embodiment of Figure 4A in that the positive feedback operation-control means of the sense amplifier SA_1 is constructed of N-MOS Q_{S9} and Q_{S10} which are connected in parallel.

The operations of the sense amplifiers SA_1 and SA_2 will be described with reference to Figure 4D. It is to be assumed that the folded data lines are charged to about $\frac{1}{2} V_{CC}$ in advance.

The FET Q_{S10} of the positive feedback operation-

control means of the sense amplifier SA_1 is rendered conductive by a sense amplifier control signal ϕ_1, whereby only either the FET Q_{S7} or the FET Q_{S8} is rendered conductive so as to reduce the lower data-line potential (V_L) a little in the direction of the null potential V_{GND}. At this time, the higher data-line potential (V_H) does not change because either the FET Q_{S7} or the FET Q_{S8} is nonconductive. The conductance of the FET Q_{S10} is designed to be smaller than that of the FET Q_{S9}.

Subsequently, when the FET Q_{S9} has begun to turn "on" owing to the sense amplifier control signal ϕ_{PA}, the sense amplifier SA_1 starts the positive feedback operation and changes the potential V_L toward the null potential V_{GND}.

That is, after the difference of the potentials of the folded data lines has been somewhat expanded by the sense amplifier control signal ϕ_1, the sense amplifier control signal ϕ_{PA} is applied so as to execute the positive feedback operation of the sense amplifier SA_1. Thus, even when the potential difference of the folded data lines is small, it is permitted to be amplified by the sense amplifier SA_1. In other words, the sensitivity of the sense amplifier improves.

Subsequently, when the FET Q_{S4} has begun to be turned

"on" by a sense amplifier control signal ϕ_{PA} or ϕ_2, the positive-feedback differential amplification operation of the sense amplifier SA_2 is started, and the higher data-line potential (V_H) rises toward V_{CC}.

Eventually, the potential V_L of the data line reaches the null potential and V_H reaches V_{CC}, and they become stable in a state of low impedance.

Figure 4E shows the circuit arrangement of a third detailed embodiment of a D-RAM. Parts corresponding to those in Figure 4A bear the same reference symbols. The fourth embodiment is different from the embodiment of Figure 4A is that dummy cells D-CEL are connected to the folded data lines.

The dummy cell D-CEL is constructed of a series connection circuit consisting of a P-MOS Q_{D1} and a P-MOS Q_{D2}. The gate of the P-MOS Q_{D1} is connected to a dummy word line, and one of the source and drain thereof is connected to the data line and the other to one of the source and drain of the P-MOS Q_{D2}, the other of which is earthed.

The dummy cell D-CEL does not require a capacitance C_{ds} for storing the reference potential. The reason is that the reference potential is precharged in the data lines. The dummy cells D-CEL are fabricated under the same manufacturing conditions and with the same

design constants as those of the memory cells M-CEL.

The dummy cells D-CEL function to cancel various noises which develop on the folded data lines during, for example, the write-down and read-out operations of memory information.

The time-sequential operations of the D-RAM transistor circuit will be described with reference to Figure 4A.

The read-out of an information is carried out in such a way that the P-MOS Q_M is turned ON to couple the capacitor C_S to the common column data line DL and that how the potential of the data line DL changes in accordance with the quantity of charges stored in the capacitor C_S is sensed. It is supposed that the potential charged in the stray capacitance C_0 of the data line DL beforehand is half of the power source voltage, i. e., $\frac{1}{2} V_{CC}$. Then, in the case where the information accumulated in the capacitor C_S is "1" (the potential V_{CC}), the potential $(V_{DL})_{"1"}$ of the data line DL becomes $V_{CC} \cdot (C_0 + 2 C_S)/2 (C_0 + C_S)$ when the corresponding memory cell is addressed, and in the case where the information is "0" (zero V), the potential $(V_{DL})_{"0"}$ of the data line DL becomes $V_{CC} \cdot C_0/2 (C_0 + C_S)$. Here, the difference between the logic "1" and the logic "0", that is, a

signal quantity to be detected ΔV_S becomes:

$$\Delta V_S = (V_{DL})_{"1"} - (V_{DL})_{"0"}$$
$$= V_{CC} \cdot C_S / (C_O + C_S)$$
$$= (C_S/C_O) \cdot V_{CC} / \{1 + (C_S/C_O)\}$$

Owing to the memory matrix of high integration density which has no capacitance even when the memory cells are made small and a large number of such memory cells are connected to the common data lines, $C_S \ll C_O$ holds, that is, (C_S/C_O) has a value almost negligible relative to 1 (one). Accordingly, the above equation is expressed by $\Delta V_S \simeq V_{CC} \cdot (C_S/C_O)$, and ΔV_S is a very small signal.

The read-out operation will now be described. The precharging operation is the same as previously stated.

The row address signals A_0 to A_j which have been supplied from the address buffer ADB at the timing of the timing signal (address buffer control signal) ϕ_{AR} (refer to Figures 3A and 3B) are decoded by the row and column decoder RC-DCR, and the addressing of the memory cell M-CEL is started simultaneously with the rise of the word line control signal ϕ_X.

As a result, the voltage difference substantially equal to ΔV_S arises between the folded data lines DL_{1-1} and $\overline{DL_{1-1}}$ on the basis of the stored content of the memory cell as stated before.

At the same time that the N-MOS Q_{S9} has begun to be rendered conductive by the timing signal (sense amplifier control signal) ϕ_{PA}, the sense amplifier SA_1 starts the positive feedback operation and amplifies the detection signal of ΔV_S having developed at the addressing. Simultaneously with the amplifying operation or after the starting of the amplifying operation, the sense amplifier SA_2 starts the positive feedback operation owing to the timing signal $\overline{\phi_{PA}}$ and recovers the level of logic "1" to V_{CC}.

The column address signals A_{i+1} to A_j which have been sent from the address buffer ADB in synchronism with the timing signal (address buffer control signal) ϕ_{AC} are decoded by the row and column decoder RC-DCR. Subsequently, the stored information of the memory cell M-CEL at the column address which has been selected by the timing signal (column switch control signal) ϕ_Y is transmitted to the common input/output lines CDL_1 and $\overline{CDL_1}$ through the column switch $C\text{-}SW_1$.

Subsequently, the output amplifier/data output buffer OA & DOB is operated by the timing signal (data output buffer and output amplifier-control signal) ϕ_{OP}, and the stored information having been read is transmitted to the output terminal D_{out} of the chip. During write-down, the OA & DOB is held inoperative by the timing signal (data output buffer-control signal) $\overline{\varphi_{RW}}$.

The precharging, addressing and sensing operations are the same as in the foregoing read-out operation. Accordingly, irrespective of the logic value of an input write-down information D_{in}, the stored information of the memory cell into which the information ought to be written is read out between the folded data lines DL_{1-1} and $\overline{DL_{1-1}}$. This information read out is ignored by a writing operation to be stated below. Therefore, the operations up to this point of time may substantially be considered as selecting a row address.

As in the read-out operation, the folded data lines DL_{1-1} and $\overline{DL_{1-1}}$ which lie at the column selected in synchronism with the timing signal (column switch-control signal) ϕ_Y are coupled to the common input/output lines CDL_1 and $\overline{CDL_1}$ through the column switch $C\text{-}SW_1$.

Subsequently, complementary writing input signals d_{in} and $\overline{d_{in}}$ supplied from the data input buffer DIB in synchronism with the timing signal (data input buffer-control signal) ϕ_{RW} are written into the memory cell M-CEL through the column switch C-SW_1. Meantime, the sense amplifier SA is operating. Since, however, the output impedance of the data input buffer DIB is low, information to appear on the folded data lines DL_{1-1} and $\overline{DL_{1-1}}$ are determined by the information of the input D_{in}.

Refresh is carried out in such a way that an information stored in the memory cell M-CEL as is being lost is once read out onto the column common data line DL, and that the information read out is brought into the restored level by the sense amplifiers SA_1 and SA_2 and then written into the memory cell M-CEL again. Accordingly, the refresh operation is similar to the operation of the row addressing or sensing period as has been explained in the read-out operation. In this case, however, the column switch C-SW_1 is made inoperative, and all the columns are simultaneously refreshed row by row.

Figure 5A shows a diagram of a D-RAM circuit arrangement

and in which memory cells of about 64 Kbits are divided and arrayed into two memory cell matrices (memory arrays M-ARY$_1$ and M-ARY$_2$) each having a memory capacity of 128 rows x 256 columns = 32,768 bits (32 Kbits). Principal blocks in this figure are depicted in conformity with the actual geometrical arrangement. The respective blocks have the same constructions as described above, and bear the same reference symbols. As the circuit arrangement of the memory array, any of the systems shown in Figures 4A, 4C and 4E can be adopted.

The row-series address selection lines (word lines WL) of the respective memory arrays M-ARY$_1$ and M-ARY$_2$ are supplied from row decoders (serving also as word drivers) R-DCR$_1$ and R-DCR$_2$ with 2^7 = 128 sorts of decode output signals which are obtained on the basis of row address signals A_0 - A_6.

A column decoder C-DCR provides 128 sorts of decode output signals on the basis of column address signals A_9 - A_{15}. The column selecting decode output signals are common to the right and left memory arrays and upper and lower adjoining columns within each memory array, totaling four columns.

In order to select any one of the four columns, address signals A_7 and A_8 are allotted. By way of

example, the signal A_7 is allotted to the selection of the right or left array, and the signal A_8 to the selection of the upper or lower column.

It is a ϕ_{yij} signal generator circuit ϕ_{yij}-SG that encodes the address signals A_7 and A_8 into four combinations, and it is column switch selectors CSW-S_1 and CSW-S_2 that switch the columns on the basis of the output signals ϕ_{y00}, ϕ_{y01}, ϕ_{y10} and ϕ_{y11} of the generator circuit.

In this manner, the decoder for selecting the columns of the memory arrays is divided into the two stages of the column decoder C-DCR and the column switch selector CSW-S_1 as well as CSW-S_2. The first aim of the division of the decoder into the two stages is to prevent any useless blank part from occurring within the IC chip. That is, it is aimed at that the vertical arrayal pitch of NOR gates which take charge of a pair of right and left output signal lines of the column decoder C-DCR and which have comparatively large areas is made equal to the column arrayal pitch of the memory cells. Owing to the division of the decoder into the two stages, the NOR gate has the number of its constituent transistors reduced and can occupy an area of relatively small size.

The second aim of the division of the decoder

into the two stages consists in that the number of the NOR gates to be connected to one address signal line is reduced, thereby to lighten the load on one address signal line and to enhance the switching speed.

The address buffer ADB processes the eight multiplexed external address signals A_0 - A_7; and A_8 - A_{15} into eight complementary pairs of address signals (a_0, $\overline{a_0}$) - (a_7, $\overline{a_7}$); and (a_8, $\overline{a_8}$) - (a_{15}, $\overline{a_{15}}$), respectively. It transmits them to the decoder circuits at the timings ϕ_{AR} and ϕ_{AC} adjusted to the operations within the IC chip.

The circuit operation of an address setting process in the 2-mat type 64-K-D-RAM will be described with reference to Figures 5A and 5B.

First, the address buffer control signal ϕ_{AR} of the row series rises to the high level, whereby the seven complementary pairs of row address signals (a_0, $\overline{a_0}$) - (a_6, $\overline{a_6}$) corresponding to the row address signals A_0 - A_6 are applied from the address buffer ADB to the row decoders R-DCR$_1$ and R-DCR$_2$ through a row address line R-ADL.

Next, the word line control signal ϕ_X rises to the high level, whereby the row decoders R-DCR$_1$ and R-DCR$_2$ become active, and one of the word lines WL of each of the memory arrays M-ARY$_1$ and M-ARY$_2$ is selected

and is made the high level.

Subsequently, the address buffer control signal ϕ_{AC} of the column series rises to the high level, whereby the seven complementary pairs of column address signals $(a_9, \overline{a_9})$ - $(a_{15}, \overline{a_{15}})$ corresponding to the column address signals A_9 - A_{15} are applied from the address buffer ADB to the column decoder C-DCR through a column address line C-ADL.

As a result, one pair of output signal lines among the 128 pairs of output signal lines of the column decoder C-DCR become the high level, and the high level signals are applied to the column switch selectors CSW-S_1 and CSW-S_2.

Subsequently, when the column switch control signal ϕ_Y rises to the high level, the ϕ_{yij} signal generator circuit ϕ_{yij}-SG becomes operable.

On the other hand, the complementary pair of signals $(a_7, \overline{a_7})$ corresponding to the address signal A_7 and the complementary pair of signals $(a_8, \overline{a_8})$ corresponding to the address signal A_8 have already been applied to the ϕ_{yij} signal generator circuit ϕ_{yij}-SG respectively when the address buffer control signal ϕ_{AR} has become the high level and when the address buffer control signal ϕ_{AC} has become the high level. Accordingly, when the column switch control signal ϕ_Y has become

the high level, the ϕ_{yij} signal generator circuit ϕ_{yij}-SG transmits the signals to the column switch selectors CSW-S_1 and CSW-S_2 substantially concurrently therewith.

In this way, one pair among a total of 512 transistor pairs in the column switches C-SW_1 and C-SW_2 is selected, and one pair of data lines DL within the memory array are connected to the common data line CDL.

The D-RAM IC layout pattern of the so-called 2-mat type in which the single IC chip includes the two divided memory arrays will be described with reference to Figure 6.

The two memory arrays M-ARY_1 and M-ARY_2 each of which is constructed of a plurality of memory cells are arranged in the IC chip in a manner to be spaced from each other.

In the central part of the IC chip between the M-ARY_1 and the M-ARY_2, the common column decoder C-DCR is arranged.

The column switch C-SW_1 for the M-ARY_1 is arranged between the M-ARY_1 and the C-DCR.

On the other hand, the column switch C-SW_2 for the M-ARY_2 is arranged between the M-ARY_2 and the C-DCR.

The sense amplifiers SA_1 and SA_2 are respectively arranged in the left end part and right end part of the IC chip in order to prevent them from operating erroneously due to noise, for example, signals applied to the C-DCR and also to facilitate the layout of connections.

On the left side of the upper part of the IC chip, there are arranged the data input buffer DIB, a read/write signal generator circuit R/W-SG, a RAS signal generator circuit RAS-SG, and a RAS-group signal generator circuit SG_1. In proximity to these circuits, there are arranged a $\overline{RAS}$ signal applying pad P-$\overline{RAS}$, a $\overline{WE}$ signal applying pad P-$\overline{WE}$, and a data signal applying pad P-D_{in}.

On the other hand, on the right side of the upper part of the IC chip, there are arranged the data output buffer DOB, a CAS signal generator circuit CAS-SG, and a CAS-group signal generator circuit SG_2. In proximity to these circuits, there are arranged a V_{SS} voltage feeding pad P-V_{SS}, a $\overline{CAS}$ signal applying pad P-$\overline{CAS}$, a data signal deriving pad P-D_{out}, and an address signal A_6 feeding pad P-A_6.

A main amplifier MA is arranged between the RAS-group signal generator circuit SG_1 and the CAS-group signal generator circuit SG_2.

A V_{BB} generator circuit V_{BB}-G is arranged above such circuit of large occupying area as the RAS-group signal generator circuit SG_1, the CAS-group signal generator circuit SG_2 or the main amplifier MA. The reason is as stated below. The V_{BB}-G produces minority carriers, and there is the danger that the memory cells constituting the M-ARY_1 and M-ARY_2 will suffer from undesired information inversion due to the minority carriers. In order to prevent the danger, therefore, the V_{BB} generator circuit V_{BB}-G is disposed at the position distant from the M-ARY_1 and M-ARY_2 to the utmost as described above.

On the left side of the lower part of the IC chip, the row decoder R-DCR_1 for the M-ARY_1 is arranged. In proximity to the R-DCR_1, there are arranged address signal feeding pads P-A_0, P-A_1 and P-A_2 and a V_{CC} voltage feeding pad P-V_{CC}.

On the other hand, on the right side of the lower part of the IC chip, the row decoder R-DCR_2 for the M-ARY_2 is arranged. In proximity to the row decoder R-DCR_2, there are arranged address signal applying pads P-A_3, P-A_4, P-A_5 and P-A_7.

The address buffer ADB is arranged between the R-DCR_1 and R-DCR_2.

A partial layout pattern diagram centering on the memory arrays M-ARY and the sense amplifiers SA_1 and SA_2 in the 64 Kbit D-RAM will be described with reference to Figure 7A. The memory arrays M-ARY and the sense amplifiers SA_2 are formed in individual N-channel type well regions enclosed with dot-and-dash lines. Since the memory arrays M-ARY, the sense amplifiers SA_2, etc. are laid out in line symmetry with respect to the column decoder C-DCR, the memory arrays M-ARY and the sense amplifiers SA_1 and SA_2 within well regions on the right side are omitted or illustrated only schematically.

Since the N-channel type wells are supplied with the power source voltage V_{CC}, power supply lines V_{CC}-L are formed as shown in Figure 7A.

In Figure 7A, supposing the memory array $M\text{-}ARY_{1-1}$ to be the first row, the power supply line is formed every 32nd row of the memory arrays M-ARY.

As the intervals of the power supply lines become larger, the well voltage becomes ununiform more. In order to prevent this drawback, the power supply line may be formed every row of the M-ARY, but the chip area increases in this case. It is therefore favorable to form the power supply lines at equal intervals among the memory arrays M-ARY, for example, at intervals of 8 rows, 16 rows, 32 rows or 64 rows.

To the end of making the well voltage uniform, the power supply lines are formed of a metal exhibiting almost no voltage loss, such as Al, Au, Mo and Ta. In the case where the power supply lines formed of the metal are arranged in the wells, they should preferably be arranged in parallel with the data lines so as not to short-circuit to the data lines formed of Al.

The N-channel type well region for the memory arrays M-ARY and that for the sense amplifiers SA_2 are isolated for the following reason.

A voltage drop develops between the power supply line within the well region for the sense amplifier SA_2 and the positive feedback operation-control means (Figure 4A) within the sense amplifier SA_2. The voltage drop becomes greater in the sense amplifier SA_2 being more distant from the power supply line, and it forms a noise. If the memory arrays M-ARY and the sense amplifiers SA_2 are formed within a single N-type well region, the aforecited voltage drop will lower the well potential, resulting in lowering the threshold voltage V_{TH} of the P-MOS Q_M (Figure 4A) of the memory cell. Then, the P-MOS Q_M will become easier to turn "on", which forms the cause of a malfunction.

The N-channel type well regions for forming the memory arrays M-ARY and the sense amplifiers SA_2

are formed to be independent of each other, whereby the noise developing in the sense amplifiers SA_2 is prevented from influencing memory operations.

Figure 7B illustrates a modification of the layout shown in Figure 7A, and is a partial layout pattern diagram centering on the memory arrays M-ARY and the sense amplifiers SA_1 and SA_2 in the 64 Kbit D-RAM.

Parts corresponding to those in Figure 7A bear the same reference symbols. Different from the layout of Figure 7A is that the memory arrays M-ARY and the sense amplifiers SA_2 are formed within an identical well region.

The modification has the advantage that the chip area becomes smaller than in the layout of Figure 7A. It is disadvantageous, however, in that the noise developing in the sense amplifiers SA_2 is prone to affect the memory operations as described above.

Figure 8A is a perspective sectional view showing the element structure of one memory cell M-CEL described above. The memory cell M-CEL comprises a P-type silicon semiconductor substrate 1, a comparatively thick insulating film 2 such as silicon oxide film (hereinafter referred to as a "field insulating film") a comparatively thin insulating film 3 such as silicon oxide film (hereinafter referred to as a

"gate insulating film"), P^+-type semiconductor regions 4 and 5, a first polycrystalline silicon layer 6, a P-type surface inversion layer 7, a second polycrystalline silicon layer 8, a PSG (phosphosilicate glass) layer 9, an aluminium layer 10, and an N-type well region 100.

The MOS Q_M in one memory cell M-CEL has its substrate, well region, drain region, source region, gate insulating film and gate electrode made of the above-mentioned P-type semiconductor substrate 1, N-type well region 100, P^+-type semiconductor region 4, P^+-type semiconductor region 5, gate insulating folm 3 and second polycrystalline silicon layer 8, respectively. The second polycrystalline silicon layer 8 is used as, for example, the word line WL_{1-2} shown in Figure 4A. The aluminium layer 10 connected to the P^+-type semiconductor region 5 is used as, for example, the data line DL_{1-1} shown in Figure 4A.

On the other hand, the storing capacitor C_S in the memory cell M-CEL has one electrode, a dielectric layer and the other electrode thereof made of the first polycrystalline silicon layer 6, the gate insulating film 3 and the P-type surface inversion layer 7, respectively. Earth potential V_{SS} is applied to the first polycrystalline silicon layer 6, and it induces the P-type surface inversion layer 7 in the surface of the N-type well region 100 owing to the field effect caused through the gate

insulating film 3.

Although the MOS Q_M in the memory cell M-CEL has been exemplified as the P-channel type, an N-channel type MOS Q_M can be formed by changing all the aforecited conductivity types into the opposite conductivity types.

Figure 8B is a perspective sectional view showing the element sttucture of one dummy cell D-CEL. The dummy cell D-CEL comprises P^+-type semiconductor 11, 12 and 14, second polycrystalline silicon layers 17 and 18, and an aluminium layer 19.

The MOS Q_{D1} in one dummy cell D-CEL has its substrate, well region, source region, drain region, gate insulating film and gate electrode made of the P-type semiconductor substrate 1, N-type well region 100, P^+-type semiconductor region 11, P^+-type semiconductor region 12, gate insulating film 3 and second polycrystalline silicon layer 17, respectively. The second polycrystalline silicon layer 17 extends over the N-type well region 100 as, for example, the dummy word line DWL_{1-2} shown in Figure 4E. The aluminium layer 19 connected to the P^+-type semiconductor

region 11 extends over the P-type semiconductor substrate 1 as, for example, the dummy data line DL_{1-1} shown in Figure 4E.

The MOS Q_{D2} in the dummy cell D-CEL has its substrate, well region, source region, drain region, gate insulating film and gate electrode made of the P-type semiconductor region 1, N-type well region 100, P^+-type semiconductor region 12, P^+-type semiconductor region 14, gate insulating film 3 and second polycrystalline silicon layer 18, respectively. The polycrystalline silicon layer 18 is supplied with a discharge signal ϕ_{dc} illustrated in the dummy cell D-CEL of Figure 4E by way of example.

Although the MOS Q_{D1} and Q_{D2} in the dummy cell D-CEL have been exemplified as the P-channel type, N-channel type MOS Q_{D1} and Q_{D2} can be formed by changing all the aforecited conductivity types into the opposite conductivity types.

The layout pattern of the memory array M-ARY will be described with reference to Figure 9A.

The memory array M-ARY shown in Figure 9A is such that a plurality of memory cells M-CEL as shown in Figure 8 are arrayed in the N-type well region 100.

First, the memory array M-ARY is constructed as stated below.

In order to isolate from one another the plurality of memory cells M-CEL each of which is constructed of the MOS Q_M and the storing capacitor C_S in the surface of the N-type well region 100, the field insulating film 2 is formed in a basic pattern shown in Figure 9B.

A field insulating film 2a is exceptionally arranged under a contact hole CH_0 for applying earth potential V_{SS} to the first polycrystalline silicon layer 6. It is accordingly possible to prevent the fault in which an aluminium - silicon alloy formed in the vicinity of the contact hole CH_0 on the basis of the interaction between the aluminium layer and the polycrystalline silicon layer penetrates through the insulating film located directly below the contact hole CH_0 and undesirably reaches the surface of the N-type well region 100.

On the field insulating film 2 and the gate insulating film 3, the first polycrystalline silicon layer 6 which is used as one electrode of the storing capacitor C_S in the memory cell M-CEL is formed in a basic pattern shown in Figure 9C.

Further, on the first polycrystalline silicon layer 6, the word lines WL_{1-1} - WL_{1-6} each of which is formed by the second polycrystalline silicon layer 8 in Figure 8A extend in the vertical direction in Figure 9A.

Further, on the polycrystalline silicon layer 6 as one electrode of the storing capacitor C_S, the power supply line V_{SS}-L for feeding earth potential V_{SS} through the contact hole CH_0 extends in the lateral direction in Figure 9A.

On the other hand, the data lines DL_{1-1} and $\overline{DL_{1-1}}$ each of which is formed by the aluminium layer 10 in Figure 8A extend substantially in parallel with the power supply line V_{SS}-L as shown in Figure 9A. The data line DL_{1-1} is connected to the source region of the MOS Q_M in one memory cell M-CEL through a contact hole CH_1, while the data line $\overline{DL_{1-1}}$ is connected to the source region of the MOS Q_M in another memory cell M-CEL through a contact hole CH_2. In addition, the data lines DL_{1-2} and $\overline{DL_{1-2}}$ extend in the lateral direction in Figure 9A likewise to the data lines DL_{1-1} and $\overline{DL_{1-1}}$, and they are connected to the source regions of the MOS Q_M in memory cells M-CEL through contact holes in predetermined parts.

In order to bias the N-type well region 100 to the power source voltage V_{CC}, the power supply line V_{CC}-L extends at an end of the memory array M-ARY in the lateral direction in Figure 9A and substantially in parallel with the data lines.

The layout pattern of the memory array shown in Figure 4E as includes the memory array M-ARY and the dummy array D-ARY is illustrated in Figure 9D. Parts corresponding to those in Figure 9A bear the same reference symbols. The layout pattern is different from Figure 9A in that the dummy array D-ARY is added.

A dummy cell D-CEL shown in Figure 9D is constructed as stated below.

A part of the surface of the N-type well region 100 is formed with the field insulating film 2, while another part of the surface of the N-type well region 100 is formed with the gate insulating film 3.

The P^+-type semiconductor region 14 is used as the common earth line of a plurality of dummy cells D-CEL.

On the field insulating film 2, the dummy word line DWL_{1-1} extends which is formed by the second polycrystalline silicon layer 17 in Figure 8B.

The dummy word line DWL_{1-1} constructs the gate electrode of the MOS Q_{D1} in the dummy cell D-CEL. On the other hand, a control signal line ϕ_{dc}-L1 which is formed by the second polycrystalline silicon layer 18 in Figure 8B in order to apply the discharge control signal ϕ_{dc} illustrated in Figure 4E is kept apart from the dummy word line DWL_{1-1} and is extended in

parallel therewith. The control signal line ϕ_{dc}-L1 constructs the gate electrode of the MOS Q_{D2} in the dummy cell D-CEL. Likewise, the dummy word line DWL_{1-2} and a control signal line ϕ_{dc}-L2 extend in parallel with the dummy word line DWL_{1-1} and the control signal line ϕ_{dc}-L1.

The data lines DL_{1-1}, $\overline{DL_{1-1}}$, DL_{1-2} and $\overline{DL_{1-2}}$ extend from the memory array M-ARY as shown in Figure 9D. The $\overline{DL_{1-1}}$ is connected to the source region of the MOS Q_{D1} in one dummy cell D-CEL through a contact hole CH_3, and the $\overline{DL_{1-2}}$ is similarly connected to the source region of the MOS Q_{D1} in another D-CEL through a contact hole CH_4.

The manufacture of the dynamic RAM of complementary type having the N-MOS and the P-MOS (hereinafter referred to as "C-MOS") will be described with reference to Figures 10 to 35. In each of the figures, X_1 is a sectional process diagram of section $X_1 - X_1$ in the memory array M-ARY shown in Figure 9A, while X_2 is a sectional process diagram of the C-MOS circuit portion of the sense amplifier SA_2 shown in Figure 4A.

As shown in Figure 10, an oxide film 102 is formed

on the surface of a semiconductor substrate 101. As favorable materials for the semiconductor substrate 101 and the oxide film 102, a P-type single-crystal silicon (Si) substrate having the (100) crystal face and a silicon dioxide (SiO_2) film are respectively used.

As shown in Figure 11, in order to form well regions of the conductivity type opposite to that of the semiconductor substrate, those parts of the SiO_2 film 102 on the semiconductor substrate 101 which correspond to the well forming regions are removed. To this end, a silicon nitride (Si_3N_4) film 103 is first formed on selected areas of the surface of the SiO_2 film 102 as an etching mask. In this state, the SiO_2 film not covered with the Si_3N_4 film 103 is removed with an etchant.

As shown in Figure 12, in order to form the well regions of the conductivity type opposite to that of the semiconductor substrate 101 within this semiconductor substrate, the semiconductor substrate 101 is etched down to a desired depth by the wet etching process or the dry etching process by employing the Si_3N_4 film 103 as an etching mask.

As shown in Figure 13, the single crystal of Si is epitaxially grown in each of the etched regions within the semiconductor substrate 101. Simultaneously, the Si crystal is doped with arsenic.

In this way, the N-type well regions 100 having an impurity concentration of about 10^{15} cm^{-3} are formed on the semiconductor substrate 101. Thereafter, the SiO_2 film 102 and the Si_3N_4 film 103 on the semiconductor substrate 101 are removed.

By forming the N-type well regions, the following advantage is achieved:

When the memory cell is constructed within the N-type well region in order to prevent a stored information from being inverted by the absorption of α-particles into the capacitor C_S of the memory cell, holes generated in and below the N-type well by the α-particles are reflected by the barrier of a P-N junction, and the influence of the holes on the capacitor C_S is avoided.

By epitaxially forming the well region, the following advantages are achieved over the case of forming it by diffusion:

(a) Since the impurity concentration of the well can be readily controlled, it can be made uniform.

(b) The junction capacitance in the well surface can

be made low, and the speed of the memory operation becomes high.

(c) Since the impurity concentration in the well surface can be made low, the breakdown voltage increases.

(d) The control of the threshold voltage is facilitated.

(e) The depth of the well can be precisely adjusted.

The steps of forming N-type well regions by another method will now be described with reference to Figures 14 to 16.

As shown in Figure 14, the single crystal of Si is epitaxially grown on the whole surface of a semiconductor substrate 101 whilst doping it with arsenic. The impurity concentration of arsenic is 10^{15} cm^{-3}. Thus, an N-type well region approximately 3 μm deep is formed uniformly on the semiconductor substrate 101.

As shown in Figure 15, in order to form desired N-type well regions, an SiO_2 film 102 and a photoresist film 104 are formed on the N-type well forming regions. Thereafter, using the SiO_2 film 102 and the photoresist film 104 as a mask, boron at an impurity concentration of 2×10^{15} cm^{-3} is ion-implanted into the surface of the N-type well, whereupon thermal diffusion is executed to diffuse the boron and to form the same P-type regions as the semiconductor substrate 101.

As shown in Figure 16, the SiO_2 film 102 and the photoresist film 104 are removed to form the desired N-type well regions within the semiconductor substrate 101.

It is a matter of course that the process for forming the N-type well regions is not restricted to the two sorts of methods mentioned above, but that another method may well be resorted to. Needless to say, the well regions may well be formed by diffusion.

As shown in Figure 17, an SiO_2 film 102 and an insulating film which does not let oxygen pass therethrough, that is, an oxidation-resisting film 103 are formed on the surfaces of the semiconductor substrate 101 and the N-type wells 100.

As a favorable material for the oxidation-resisting film 103, a silicon nitride (Si_3N_4) film is used.

The SiO_2 film 102 is formed to a thickness of approximately 500 Å by the surface oxidation of the Si substrate for the following reason. In the case where the Si_3N_4 film 103 is formed directly on the surface of the Si substrate 101, a thermal strain is afforded to the surface of the Si substrate 101 by the difference between the coefficients of thermal expansion of the Si substrate 101 and the Si_3N_4 film 103. In consequence,

crystal defects are caused in the surface of the Si substrate 101. In order to prevent this drawback, the SiO_2 film 102 is formed on the surface of the Si substrate 101 before the formation of the Si_3N_4 film 103. On the other hand, the Si_3N_4 film 103 is used as a mask for the selective oxidation of the Si substrate 101 as will be described in detail later, and it is therefore formed to a thickness of approximately 1,400 Å by, for example, the CVD (Chemical Vapour Deposition) process.

In order to selectively remove the Si_3N_4 film 103 on those parts of the surface of the Si substrate 101 in which a comparatively thick insulating film, that is, field insulating film is to be formed, a photoresist film 104 is first formed on selected areas of the surface of the Si_3N_4 film 103 as an etching mask. Under this state, the exposed parts of the Si_3N_4 film 103 are removed by, for example, the plasma etching process capable of precise etching.

Subsequently, in order to prevent layers of the conductivity type opposite to that of the substrate or the so-called inversion layers from being formed in the surface parts of the Si substrate 101 in which

the field insulating film is formed, an impurity of the same conductivity type as that of the substrate or a P-type impurity is introduced into the Si substrate 101 through the SiO_2 film 102 exposed in the state in which the photoresist film 104 is left as shown in Figure 18. As a process for the introduction of the P-type impurity, the ion implantation is favorable. By way of example, the ions of boron being the P-type impurity are implanted into the Si substrate 101 at an implantation energy of 75 keV. The dose of the ions at this time is 3×10^{12} atoms/cm^2.

A field insulator 105 is formed on the selected areas of the surface of the Si substrate 101. More specifically, as shown in Figure 19, after removing the photoresist film 104, the surface of the Si substrate 101 is selectively oxidized by thermal oxidation by employing the Si_3N_4 film 103 as a mask, and the SiO_2 film 105 being approximately 9,500 Å thick (hereinafter, termed "field SiO_2 film") is formed. During the formation of the field SiO_2 film 105, the ion-implanted boron is brought into the Si substrate 101 by outdiffusion, so that P-type inversion-preventive layers (not shown) having a predetermined depth are formed directly below the field SiO_2 film 105.

In order to expose those parts of the surface of the Si substrate 101 which are not formed with the field SiO_2 film 105, the Si_3N_4 film 103 is removed with, for example, a hot phosphoric acid (H_3PO_4) liquid. The SiO_2 film 102 is subsequently removed with, for example, a hydrofluoric acid (HF) liquid, to expose the selected areas of the surface of the Si substrate 101 as shown in Figure 20.

In order to obtain the dielectric layers of the capacitors C_S in the memory cells M-CEL, the exposed surfaces of the Si substrate 101 and the N-type wells 100 are formed with a first gate insulating film 106 as shown in Figure 21. That is, the exposed surfaces of the Si substrate 101 and the N-type wells are thermally oxidized, whereby the first gate insulating film 106 being approximately 430 Å thick is formed in the surfaces. Accordingly, the first gate insulating film 106 is made of SiO_2.

A first conductor layer 107 for use as one electrode of the capacitor C_S in each memory cell is formed on the whole surface of the resultant Si substrate 101

as shown in Figure 22. A polycrystalline silicon layer is formed on the whole surface of the Si substrate 101 as the first conductor layer 107 by the CVD process. The thickness of the polycrystalline silicon layer is approximately 4,000 Å. Subsequently, in order to lower the resistance of the polycrystalline silicon layer 107, an N-type impurity, e.g., phosphorus is introduced into the polycrystalline silicon layer 107 by the diffusion process. As a result, the sheet resistance of the polycrystalline silicon layer 107 becomes approximately 16Ω per square.

In order to put the first conductor layer or first polycrystalline silicon layer 107 into a predetermined electrode shape, the first polycrystalline silicon layer 107 is selectively removed by the photoetching process so as to form electrodes 108 as shown in Figure 23. The plasma etching capable of precise etching is suitable as a process for selectively removing the first polycrystalline silicon layer 107. Subsequently, the exposed parts of the first gate SiO_2 film 106 are also etched to partially expose the surfaces of the N-type wells 100.

In order to obtain the gate insulating films of the MOSFETs in the memory array M-CEL, the dummy

array D-CEL and the peripheral circuit portion, the exposed surfaces of the Si substrate 101 and the N-type wells 100 are formed with a second gate insulating film 109 as shown in Figure 24. That is, the exposed surfaces of the Si substrate 101 and the N-type wells 100 are thermally oxidized, whereby the second gate insulating film 109 being approximately 530 Å thick is formed in the surfaces. Accordingly, the second gate insulating film 109 is made of SiO_2. Simultaneously with the formation of the second gate insulating film or second gate SiO_2 film 109, the surfaces of the electrodes 108 made of the first polycrystalline silicon are oxidized and are formed with SiO_2 films 110 being approximately 2,200 Å thick. The SiO_2 film 110 serves for the inter-layer insulation between the electrode 108 and an electrode made of second polycrystalline silicon to be described later.

As shown in Figure 25, in order to control the threshold voltage of the N-MOS, a P-type impurity is introduced into that part of the surface of the Si substrate 101 in which the N-MOS is to be formed, by the ion implantation process and by employing a photoresist film 104 over the surfaces of the N-type wells as a mask for the ion implantation. Boron, for example,

is used as the P-type impurity. It is preferable that the implantation energy is 30 keV and that the dose of ions is 4.5×10^{11} atoms/cm^2.

A second conductor layer 113 is formed on the whole surface of the resultant Si substrate 101 in order to use it as the gate electrodes of all the MOSFETs and the wiring layers.
As shown in Figure 26, a polycrystalline silicon layer is formed on the entire surface of the Si substrate 101 as the second conductor layer 113 by the CVD process. The thickness of the polycrystalline silicon layer 113 is approximately 3,500 Å. Subsequently, in order to lower the resistance of the polycrystalline silicon layer 113, an N-type impurity, e. g., phosphorus is introduced into this polycrystalline silicon layer by the diffusion process. As a result, the sheet resistance of the polycrystalline silicon layer 113 becomes approximately 10Ω per square.

The second conductor layer or second polycrystalline silicon layer 113 is selectively removed by the photoetching process in order to put it into a predetermined electrode or wiring shape. That is, as shown in Figure 27, the photoetched silicon layer 113 forms the word lines

WL_{1-1} - WL_{1-6}, dummy word lines DWL_{1-1} and DWL_{1-2}, and control signal lines ϕ_{dc}-L1 and ϕ_{dc}-L2 shown in Figure 9D. Further, the exposed second gate SiO_2 film 109 is removed to expose the surfaces of the Si substrate 101 and the N-type wells 100.

In order to prevent the contamination of surface parts in which the source regions and drain regions of the MOSFETs are to be formed, the exposed surfaces of the Si substrate 101 and the N-type wells 100 are formed with an SiO_2 film 115 being 100 Å thick by the thermal oxidation thereof as illustrated in Figure 28. Simultaneously with the formation of the SiO_2 film 115, the surfaces of the word lines WL_{1-1} - WL_{1-6}, dummy word lines DWL_{1-1} and DWL_{1-2}, control signal lines ϕ_{dc}-L1 and ϕ_{dc}-L2, and the gate electrodes of the complementary MOSFETs as are made of the second polycrystalline silicon are oxidized, with the result that the surfaces are formed with an SiO_2 film 116 being about 300 Å thick as shown in Figure 28.

In order to form the source and drain regions of the N-MOS in the selected parts of the Si substrate 101, as illustrated in Figure 29, a mask for ion implantation, e. g., CVD SiO_2 film 119 is formed on the N-type wells 100,

whereupon an N-type impurity, e. g., arsenic is introduced into the Si substrate 101 through those areas of the SiO_2 film 115 which are not covered with the CVD SiO_2 film 119. As a process for introducing the N-type impurity, the ion implantation is favorable. By way of example, arsenic ions are implanted into the Si substrate 101 at an implantation energy of 80 keV. The dose of the ions at this time is 1×10^{16} atoms/cm^2. By subsequently performing a heat treatment, the ion-implanted arsenic impurity is subjected to outdiffusion, and N^+-type semiconductor regions 120 and 121 having a predetermined depth are formed. These N^+-type semiconductor regions 120 and 121 form the source and drain regions.

Next, in order to form the source and drain regions of the P-MOS in the selected parts of the N-type wells 100, as illustrated in Figure 30, a mask for ion implantation, e. g., CVD SiO_2 film 119 is formed on the surface of the resultant Si substrate 101 except the N-type wells 100, whereupon a P-type impurity, e. g., boron is introduced into the N-type wells through the SiO_2 film 115 overlying the N-type wells 100 by the ion implantation process. By way of example, boron ions are implanted into the N-type wells at an implantation energy of 80 keV. The dose of the ions at this time is 3×10^{15} atoms/cm^2.

By subsequently performing a heat treatment, the ion-implanted boron impurity is subjected to outdiffusion, and P^+-type semiconductor regions 122 - 127 having a predetermined depth are formed.

These P^+-type semiconductor regions 122 - 127 form the source and drain regions.

The reason why the sources and drains of the P-MOS are formed after the sources and drains of the N-type MISFETs is that the heat treatment step is carried out only once so as to prevent the boron from diffusing more than is necessary.

A contact hole for the connection between the first conductor layer or first polycrystalline silicon layer 108 and a third conductor layer to be stated later is formed in the SiO_2 film 110. That is, as shown in Figure 31, a contact hole CH_{101} is formed in the selected part of the SiO_2 film 110 by employing a photoresist film (not shown) as a mask. This contact hole CH_{101} corresponds to the contact hole CH_0 shown in Figure 9A.

The reason why only the contact hole CH_{101} for the connection between the first polycrystalline silicon layer 108 and the third conductor layer is formed is as follows. As stated before, the thickness of

the SiO_2 film 110 formed in the surface of the first polycrystalline silicon layer 108 is 300 Å. On the other hand, the thickness of the SiO_2 film 115 formed in the surfaces of the Si substrate 101 and the N-type wells 100 is 100 Å. Accordingly, when these SiO_2 films 110 and 115 are etched at the same time, there is the fear that the SiO_2 film 115 will be overetched before the first polycrystalline silicon film 108 is completely exposed.

In order to prevent this drawback, the contact hole CH_{101} is formed independently as stated above.

Contact holes for the connections between the source and drain regions and the third conductor layer are formed in the SiO_2 film 115. That is, using a predetermined mask, contact holes CH_{102} - CH_{107} are formed as shown in Figure 32 by the selective etching of the SiO_2 film 115.

Although the mask has an opening also in its part corresponding to the contact hole CH_{101}, the overetch of the SiO_2 film 110 in the contact hole CH_{101} is not problematic in actuality.

The contact hole CH_{102} corresponds to the contact hole CH_1 in Figure 9A.

An inter-layer insulating film is formed on the whole surface of the resultant Si substrate 101. That is, as illustrated in Figure 33, an inter-layer insulating film 118, for example, phosphosilicate glass (PSG) film being approximately 8,000 Å thick is formed on the entire surface of the Si substrate 101. This PSG film 118 serves also as a getter for sodium ions which affect the characteristics of the MOS.

Contact holes are formed in the PSG film 118 for the connections between the second polycrystalline silicon layer and the third conductor layer and between the source and drain regions and the third conductor layer.

As shown in Figure 34, the PSG film 118 is selectively etched to form contact holes CH_{101} - CH_{107}. A mask which is used in forming these contact holes CH_{101} - CH_{107} is the same as the mask used for forming the contact holes CH_{101} - CH_{107} in the contact hole forming step (2). Subsequently, the PSG film 118 is heat-treated at a temperature of about 1,000 °C in order to flatten it.

It is also possible that the formation of the contact holes into the SiO_2 film 115 explained in the contact hole forming step (2) is achieved simultaneously with the formation of the contact holes into the PSG

film 118. However, while the contact holes in the SiO_2 film 115 are being formed, the PSG film 118 is also etched. In other words, the overetch of the PSG film 118 occurs. In order to prevent the overetch, accordingly, it is favorable that the formation of the contact holes into the PSG film 118 and the formation of the contact holes into the SiO_2 film 115 are separately executed as described above.

In order to form the power supply line V_{SS}-L and the data lines DL_{1-1}, $\overline{DL_{1-1}}$, DL_{1-2} and $\overline{DL_{1-2}}$ shown in Figure 9A, the third conductor layer, e. g., aluminium layer being 12,000 Å thick is first formed on the whole surface of the resultant Si substrate 101. Subsequently, this aluminiumlayer is selectively etched to form a power supply line V_{SS}-L, a data line DL_{1-1} and a wiring layer 127 as illustrated in Figure 35.

The D-RAM as described and constructed above has the following effects:

(a) Since a plurality of N-type well regions formed by an identical process are disposed in a P-type semiconductor substrate and P-channel MISFETs serving as memory cells and a pair of P-channel FETs of a complementary sense amplifier are formed in the surfaces of the respective well regions, the memory cells which are immune against

α-particles and the sense amplifier which is of high speed and stable are simultaneously obtained.

Merely by constructing the memory cell of the P-MOS and varying a word voltage within a range between a power source voltage V_{cc} and $(V_{cc} - |V_{thp}|)$, the selection of information "1" or "0" is permitted, so that a memory capable of operating at high speed is obtained.

(b) Since a complementary sense amplifier is connected to folded data lines, an areal margin in layout as is approximately double that in the prior art appears, and hence, a high packaging density becomes possible.

(c) Since means for precharging folded data lines to a potential intermediate between the logics "1" and "0" of a memory cell is comprised, the change of the potential of a data line equal to half of the potential difference between the logics "1" and "0" determines a read-out time, and hence, a memory of high speed and low power dissipation is obtained.

In addition, the coupling noise of a word line and the data line arecancelled because plus and minus noise develop in the folded data lines respectively.

Further, since the data line is precharged as its reference potential to the potential intermediate between the logics "1" and "0" of the memory cell,

a dummy cell can be dispensed with and a memory of small chip area is obtained.

(d) Since the starting times of the positive feedback operation of the P-channel FET pair of a sense amplifier and the positive feedback operation of the N-channel FET pair thereof are made different, any through current does not flow and a memory of low power dissipation is obtained.

(e) Since the P-channel FET pair and N-channel FET pair of a complementary sense amplifier are arranged at both the ends of a memory array, the layout within a chip can be separated into the group of P-channel FETs and the group of N-channel FETs, and hence, an efficient packaging is permitted.

(f) Since folded data lines are formed of Al, the wiring resistance is very low and an operation of high reliability is permitted.

(g) Since an N-type well region for forming memory cells therein is made of an epitaxial layer, a uniform well of desired impurity concentration can be obtained. Therefore, a threshold voltage can be controlled and a junction capacitance can be made lower than in case of diffusion, so that a memory of high speed is obtained. In addition, the surface impurity concentration of the well can be made lower than in the case of diffusion,

so that a memory of great breakdown voltage is obtained.

(h) since a plurality of N-type well regions are formed with well biasing wirings in parallel with data lines, well voltages become substantially uniform and well resistances can be made low, so that a memory which is little influenced by noise is obtained.

(i) when the D-RAM is laid out so as to isolate a well region for forming memory cells therein and a wel region for forming a sense amplifier therein, noise having developed in the sense amplifier have no influence on the memory cells, and hence, an operation of high reliability becomes possible.

Attention is drawn to Application No. 82.10824 (Serial No. 2,098,396) from which the present Application has been divided, in which there is claimed in claim 1 a semiconductor memory formed in a semiconductor integrated circuit including:

(a) a semiconductor substrate of a first conductivity type which has at least one well region of a second conductivity type;

(b) an array of memory cells which are formed in said well region, said each cell of said array including a MOS transistor of the first conductivity type and a capacitor;

(c) a plurality of data lines which extend over said well region, and each of which is electrically connected to selected ones of said memory cells of said array;

(d) a plurality of word lines which extend over said well region, and each of which is electrically connected to gates of the MOS transistors of selected ones of said memory cells of said array;

and

(e) a plurality of sense amplifiers each of which is coupled to a pair of adjacent ones of said data lines; said each sense amplifier including a pair of first MOS transistors of the first conductivity type which are formed in one well region of the second conductivity type formed in said semiconductor substrate, and a pair of second MOS transistors of the second conductivity type which are formed in said semiconductor substrate; said pair of first MOS transistors having their respective gates and drains cross-coupled to each other and having said respective drains electrically connected to said pair of data lines; said pair of second MOS transistors having their respective gates and drains cross-coupled to each other and having said respective drains electrically connected to said pair of data lines.

CLAIMS.

1. A dynamic type semiconductor memory including:

(a) a plurality of pairs of data lines to which memory cells are connected;

(b) differential amplifiers each of which amplifies a difference between signal magnitudes appearing on each corresponding pair of data lines; said each differential amplifier including a pair of P-channel MOSFETs which have their drains and gates cross-coupled to each other and which have the drains connected to the corresponding pair of data lines respectively, a pair of N-channel MOSFETs which have their drains and gates cross-coupled to each other and which have the drains connected to the corresponding pair of data lines respectively, and a circuit which controls positive feedback operations of both MOSFET pairs;

(c) a plurality of word lines each of which is arranged in a manner to intersect with both of the pair of data lines; and

(d) a precharging circuit which sets said respective pairs of data lines at a potential intermediate between two potentials representative of binary signals to be stored in said memory cells, before the positive feedback operations are started.

2. A dynamic type semiconductor memory according to claim 1, wherein control signals with which the positive feedback operation of the P-channel FET pair and that of the N-channel FET pair are started at different timings are applied to the positive feedback operation-control circuit.

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