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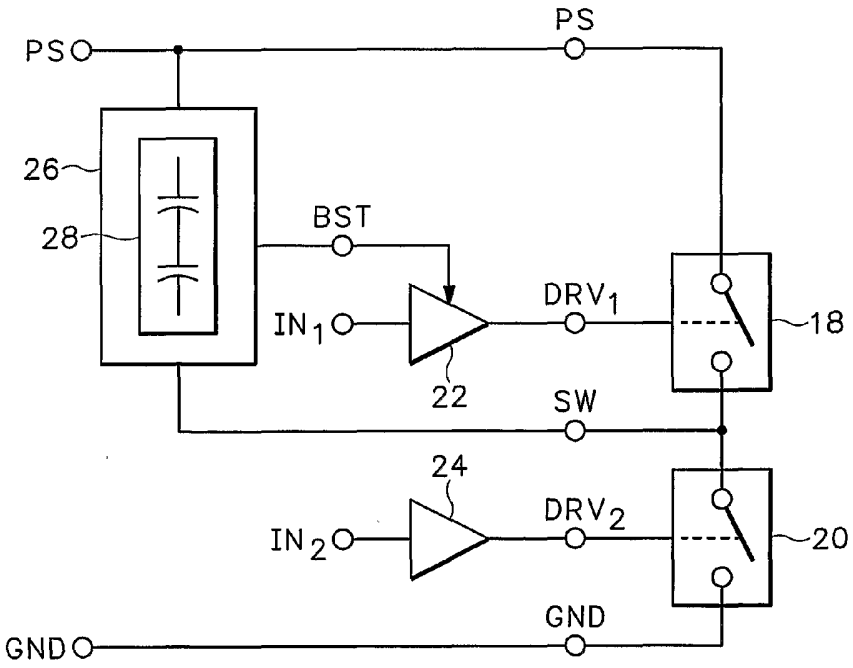
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(54) Title: BOOSTED SWITCH DRIVE WITH CHARGE TRANSFER



(57) Abstract: A switch drive circuit utilizes charge transfer within and/or between boost circuit and/or snubber circuits for boosted switch drives. A boost circuit may include a divider to limit a boosted signal for driving a switch. A snubber circuit may transfer charge to a boost circuit.

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BOOSTED SWITCH DRIVE WITH CHARGE TRANSFER

This application claims priority from U.S. Provisional Application Serial No. 60/598,666 entitled Gate Drive and Snubber for Switching Power Supply filed August 2, 2004, and U.S. Patent Application Serial No. 10/976,196 filed October 26, 2004 entitled Boosted Switch Drive With Charge Transfer, which are incorporated by reference.

BACKGROUND

Fig. 1 illustrates a prior art gate drive circuit for a switching power supply. The circuit of Fig. 1 includes two transistors Q1 and Q2 connected to a switch node SW and arranged to alternately switch an inductor between two different power supply terminals PS and GND. This type of switch arrangement is commonly used in switching power supplies such as a synchronous buck converter. Transistors Q1 and Q2 are controlled by input signals IN_1 and IN_2 which drive the gates of Q1 and Q2 through drive circuits 10 and 12, respectively.

Drive circuit 12 can receive its power from the positive power supply terminal PS because the source of Q2 is referenced to the power supply ground terminal GND. However, the source of Q1 is referenced to the switch terminal SW which is at nearly the same voltage as PS when the gate of Q1 must be driven with a significantly higher voltage than PS. Therefore, the circuit of Fig. 1 includes a boost circuit 14 to generate a boosted power supply BST which is used to operate the drive circuit 10 for Q1. Boost circuit 14 includes a diode D_B and capacitor C_B connected in a charge pump arrangement.

The circuit of Fig. 1 also includes an RC snubber circuit 16 which dampens voltage spikes at the switch SW caused by parasitic inductances in the transistors, the PC board on which they may be mounted, as well as the main inductor for the switching power supply.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates a prior art gate drive circuit for a switching power supply.

Fig. 2 illustrates an embodiment of a circuit according to some of the inventive principles of this patent disclosure.

Fig. 3 illustrates another embodiment of a circuit according to some of the inventive principles of this patent disclosure.

Fig. 4 illustrates an embodiment of a circuit showing some additional implementation details according to some of the inventive principles of this patent disclosure.

DETAILED DESCRIPTION

Referring to the circuit of Fig. 1, as an operational example, the power supply PS is assumed to be at a positive voltage V_{PS}, and the power supply terminal GND is assumed to be at ground potential. Capacitor C_B in the boost circuit is charged to V_{PS}-V_D when the low-side transistor Q2 is turned on, that is, when the switch node SW is grounded through Q2 (except for any resistive drop through Q2). This capacitor voltage is driven onto the gate of high-side transistor Q1 through driver 10 when input IN_1 is activated. The capacitor voltage added to the voltage at the switch node SW when Q1 is on creates the boost voltage V_{BST} at the boost terminal BST. This places almost the full supply voltage V_{CC} (minus diode drop) across the gate-source input of Q1 and requires C_B to store enough charge to charge up the gate capacitance of Q1 to almost the full supply voltage. This can cause high switching losses due to the large amount of charge involved.

One possible technique for reducing the switching losses is to provide a lower supply voltage to the boost circuit 14, i.e., not connect it directly to PS. The reduced supply voltage would need to be high enough to generate a boost voltage V_{BST} that turns the high-side transistor Q1 completely on so as to minimize conduction losses through Q1, but low enough to minimize switching losses. There would typically be an optimum reduced supply voltage that would result in an optimum boost voltage, but the reduced supply voltage would usually have to be generated by a special circuit that adds cost and complexity to the system.

Another potentially problematic aspect of the circuit of Fig. 1 is the power loss in the snubber circuit 16. In many situations, a snubber circuit may be essential to prevent voltage spikes from damaging transistors Q1 and Q2. However, a substantial amount of charge is shunted to ground through the snubber, thereby wasting power and reducing efficiency.

Some of the inventive principles of this patent disclosure relate to transferring charge within and/or between boost circuits and/or snubber circuits. Fig. 2 illustrates an embodiment of a circuit that transfers charge according to some of the inventive principles of this patent disclosure. The circuit of Fig. 2 includes a first switch 18 arranged between a power supply terminal PS and a switch node SW and controlled by a drive signal at drive node DRV_1. A second switch 20 is arranged between SW and a second power supply terminal GND and controlled by a second drive signal at a second drive node DRV_2. The drive signals DRV_1 and DRV_2 are generated by drive circuits 22 and 24 in response to switch input signals IN_1 and IN_2, respectively.

A boost circuit 26 generates a boosted signal V_{BST} at boost node BST to operate the drive circuit 22. The boost circuit includes a divider circuit 28, shown conceptually in this

example as a capacitive divider that transfers charge between components to limit the boosted signal.

Fig. 3 illustrates another embodiment of a circuit that transfers charge according to some of the inventive principles of this patent disclosure. The circuit of Fig. 3 includes switches 18 and 20 and drive circuits 22 and 24 arranged in the same manner as the circuit of Fig. 2. The circuit of Fig. 3, however includes a snubber circuit 30 arranged to transfer charge to a boost circuit 32 which generates a boosted signal V_{BST} for providing power to drive the switch 18.

Fig. 4 illustrates an embodiment of a circuit showing some example implementation details according to some of the inventive principles of this patent disclosure. Switches 18 and 20 are implemented as metal oxide semiconductor field effect transistors (MOSFETs), but any other type of suitable switches may be used. Drive circuits 22 and 24 may be any suitable gate drivers. A boot-strap diode D_1 is connected between a power source node PS and a boost node BST. A capacitor C_1 is connected between the switch node SW and the boost node BST, preferably through a resistor R_1. A second capacitor C_2 is connected between BST and power supply GND. Capacitors C1 and C2 form a capacitive voltage divider that reduces the boost voltage V_{BST} at boost node BST. The arrangement of components shown in Fig. 4 also provides snubbing at switch node SW which may transfer charge from the switch node SW to the boost circuit.

Depending on the details of implementation, the circuit of Fig. 4 may reduce switching losses because of the reduced voltage level of the boost signal V_{BST} due to the voltage dividing effect of C_1 and C_2. It may also provide optimized slew-rate control when switch 18 is turned on because of the feedback from switch node SW to the boost node BST through R_1/C_1 and C_2. That is, the voltage at the gate of transistor 18 may ramp up quickly to turn the transistor on quickly, then final slew-rate control may reduce voltage spikes at the switch node SW. The snubbing of the SW node through the interaction of R_1 in series with the C_1/C_2 combination may provide better snubbing response than prior art methods because the snubbing is in the feedback of the driver. The arrangement of Fig. 4 may reduce stresses on some or all of the components, for example, the voltage stresses on the switches and the boot strap diode. The overall efficiencies that may be obtained from the circuit of Fig. 4 may, in turn, enable the use of fewer and/or lower cost switches and other components to be used. Yet another potential benefit of the circuit of Fig. 4 is that resistor R_1 may reduce stress by limiting current surges through the boot-strap diode. Because the boosting and snubbing functions are integrated into the same components, these potential benefits may be realized

without additional components and their associated costs. A further potential benefit is that efficiency may be improved because charge that may have been wasted by shunting to ground may be preserved by transferring it to the boost node.

Although not necessary to an understanding of the inventive principles of this patent disclosure, some helpful equations relating to component values in Fig. 4 are provided as follows. The value of the capacitors may be determined from:

$$C_1 = 10 \times \frac{Q_{GATE}}{V_{CC} - V_D}$$

and

$$C_2 = 10 \times \frac{Q_{GATE}}{V_{GATE}} - C_1$$

where Q_{GATE} is the total charge required on the gate of switch 18 at the desired gate voltage V_{GATE}, V_{CC} is the power supply voltage, and V_D is the voltage drop across D_1. The peak surge current $I_{F(PEAK)}$ rating for the boot-strap diode may be determined from:

$$I_{F(PEAK)} = \frac{V_{CC} - V_D}{R_1}$$

The inventive principles of this patent disclosure have been described above with reference to some specific example embodiments, but these embodiments can be modified in arrangement and detail without departing from the inventive concepts. For example, switches have been shown in some embodiments as MOSFETS, but any other suitable switches may be used in accordance with the inventive principles of this patent disclosure. As a further example, the power supply and boosted signals are not limited to any particular polarity, voltage or switching power supply topology. As yet another example, resistor R_1 may be rearranged or omitted from the circuit of Fig. 4 while still maintaining beneficial results. And as yet another example, the arrangement of C2 may be between BST and other nodes besides GND. Thus, such changes and modifications are considered to fall within the scope of the following claims.

CLAIMS

1. A circuit comprising:

a switch node;

a drive node;

a power source node; and

a boost circuit coupled to the switch node and the power source node to generate a boosted signal for driving a switch coupled to the switch node and the drive node, wherein the boost circuit comprises a divider to limit the boosted signal.

2. The circuit of claim 1 wherein the divider comprises a capacitor coupled between a boost node and a power supply node.

3. The circuit of claim 1 wherein the divider comprises a capacitor coupled between a boost node and the switch node.

4. The circuit of claim 1 wherein the divider comprises:

a first capacitor coupled between a boost node and a power supply node; and

a second capacitor coupled between the boost node and the switch node.

5. The circuit of claim 4 wherein the divider further comprises a resistor coupled in series with one of the capacitors.

6. The circuit of claim 1 wherein the divider is integral with a snubber circuit.

7. A circuit comprising:

a snubber circuit coupled to a switch node; and

a boost circuit coupled to the switch node to generate a boosted signal for driving a switch coupled to the switch node and a drive node;

wherein the snubber circuit is arranged to transfer charge from the switch node to the boost circuit.

8. The circuit of claim 7 wherein the snubber circuit comprises a capacitor and a resistor coupled between the switch node and the boost circuit.

9. The circuit of claim 8 wherein the capacitor and resistor are coupled to a boost node in the boost circuit.

10. The circuit of claim 9 wherein the capacitor and resistor are coupled in series.

11. The circuit of claim 9 wherein the boost circuit comprises a second capacitor coupled between the boost node and a power supply terminal.

12. A method comprising:

generating a boosted signal for driving a switch coupled to a switch node and a drive node; and

transferring charge to reduce the voltage of the boosted signal.

13. The method of claim 12 wherein transferring charge comprises transferring charge between two capacitors.

14. The method of claim 12 wherein transferring charge comprises dividing a voltage.

15. The method of claim 12 further comprising transferring charge from the switch node to the drive node.

16. The method of claim 15 wherein transferring charge from the switch node to the drive node comprises transferring charge through a capacitor.

17. The method of claim 16 wherein transferring charge from the switch node to the drive node further comprises transferring charge through a resistor.

18. A circuit comprising:

a switch node;

a drive node;

a power source node;

means for generating a boosted signal for driving a switch coupled to the switch node and the drive node; and

means for limiting the boosted signal.

19. The circuit of claim 18 further comprising means for snubbing the switch node.

20. The circuit of claim 19 wherein the means for snubbing the switch node is integral with the means for limiting the boosted signal.

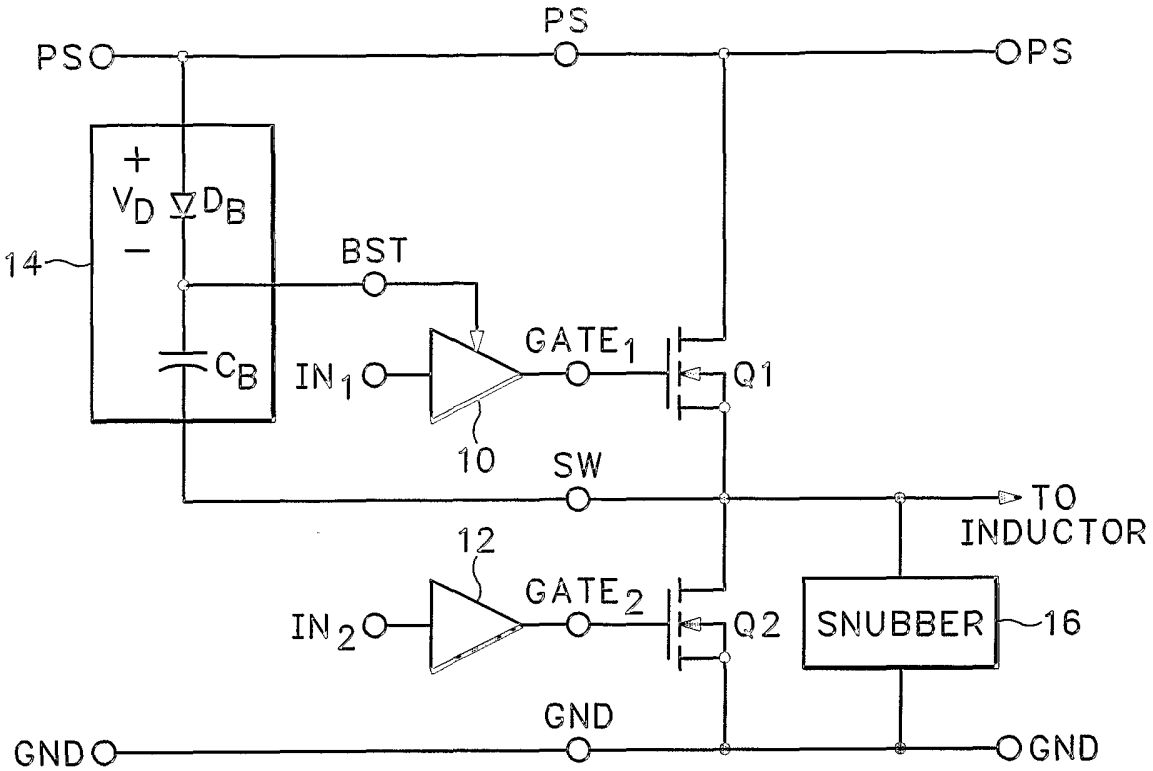


FIG.1
(PRIOR ART)

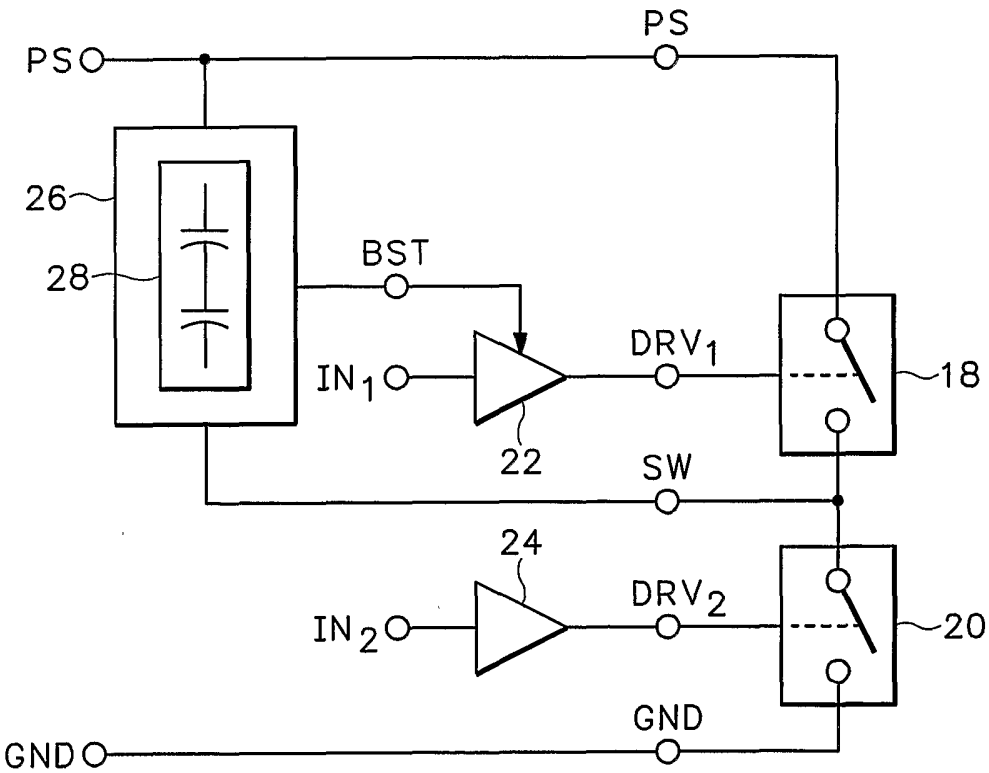


FIG.2

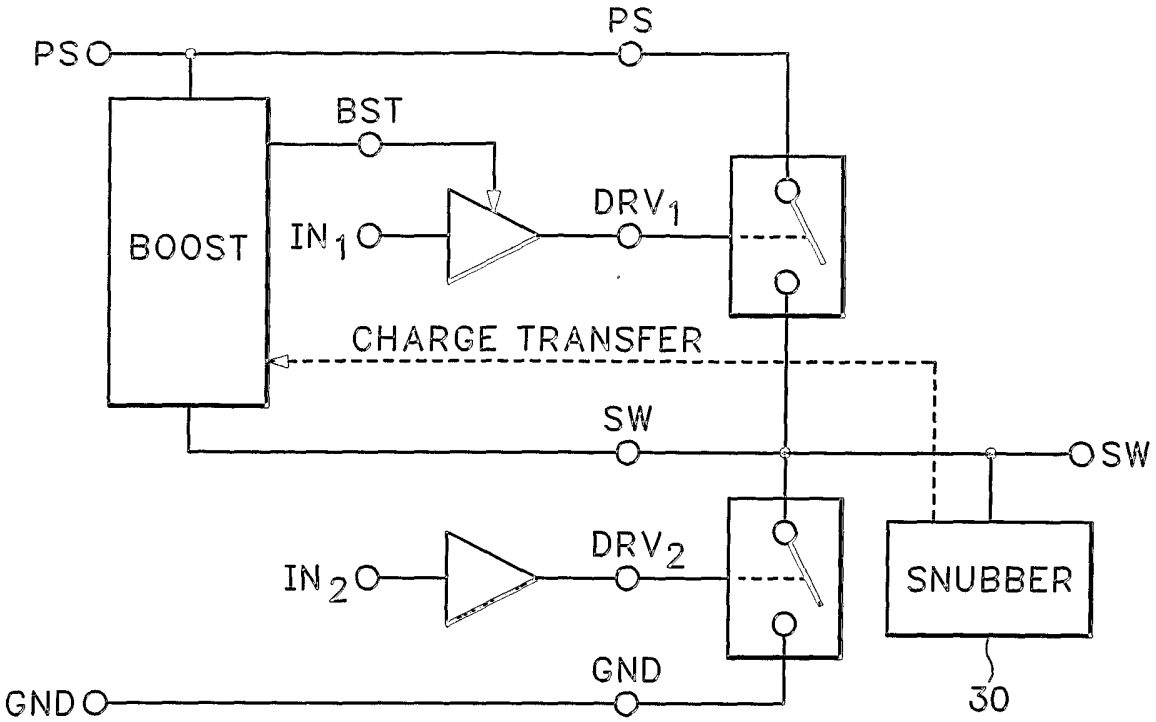

PS
PS
BST
BOOST
IN1
DRV1
CHARGE TRANSFER
SW
SW
IN2
DRV2
SNUBBER
GND
GND
30

FIG.3

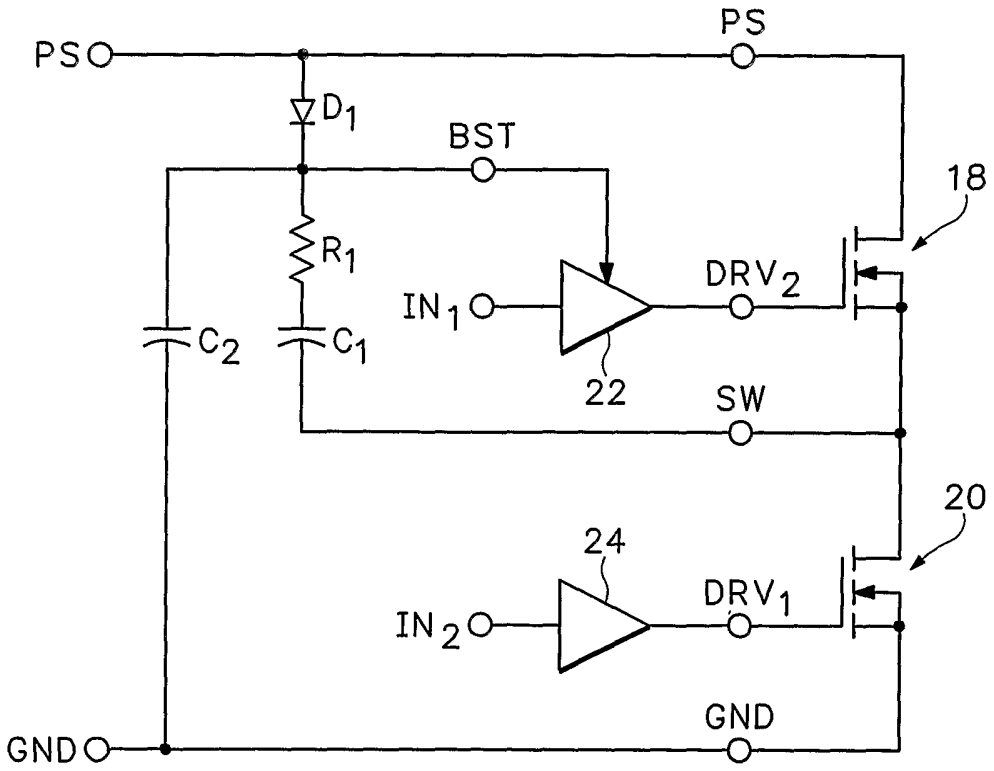

PS
PS
D1
BST
18
R1
IN1
DRV2
C2
C1
22
SW
20
24
IN2
DRV1
GND
GND

FIG.4