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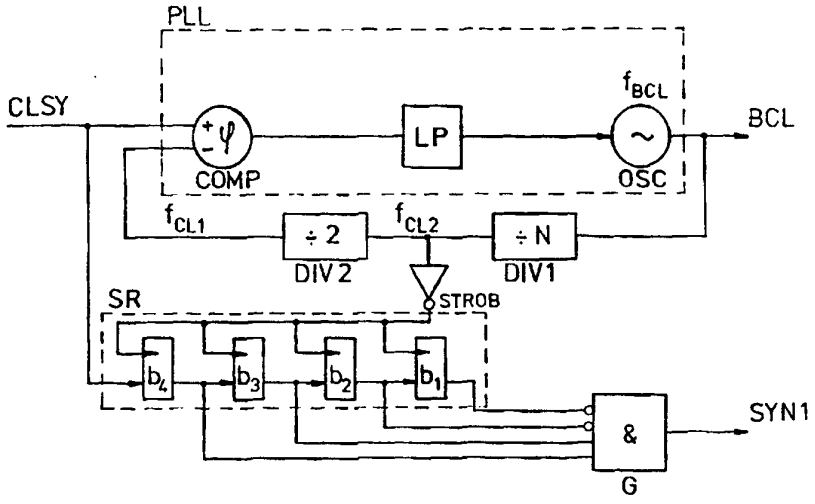

(57) Abstract

The present invention provides a composite clock signal, CLSY, which with one single signal distributes both clock signal and synchronizing signal, wherein the detection of this synchronizing signal in a subsequent bit clocking generator for a high bit clocking frequency (f_{BCL}) means that any time jitter that may exist on the edges of the clock signal (CLSY) will not influence the definition of the locally obtained synchronizing signal (SYN1), wherein each data bit frame defined by the synchronizing signal (SYN1) will always include the exact number of data bits at the bit clocking frequency (f_{BCL}). The bit clocking generator includes basically a PLL-circuit, a dividing circuit and a shift register and a logic gate for generating from the CLSY-signal the bit clocking signal with its frame reference, wherein there is obtained from the bit clocking generator in addition to the bit clocking frequency a synchronizing pulse which has high precision in relation to both the high frequency system clock and also in relation to an external time domain transferred through the composite reference signal (CLSY).

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COMPOSITE CLOCK SIGNAL

TECHNICAL FIELD

The present invention relates to the field of clock control signals, and more particularly to timing with the aid of distributed clock signals and synchronizing signals in, for instance, a telecommunications system and with the aid of a composite clock signal, CLSY (Clock and Synch).

BACKGROUND ART

In telephony and telecommunications contexts, there is normally a general need for some form of clock and/or synchronizing signal distribution. This need is particularly extensive in large connected systems (the word large having a physical meaning), for instance switches which include various multiplexing stages.

In the case of large switches which comprise circuits mounted on circuit boards that are stored in magazines and cabinets, there is a need to distribute a relatively high frequency clock and a timing or synchronization pulse of lower frequency as a reference to framing, etc.

To this end, telecommunications equipment stored in a magazine or cabinet includes a considerable number of transmission means in the form of cables, connector pins in back planes and electric contacts, conductors in back planes, etc. The space required by all of these signal transmission devices is both large and expensive. The number of connector pins in the connectors is normally a resource which limits the size of a switch, for instance.

In earlier systems in which clock signal and synchronizing signal are intended to be distributed to all magazines and cabinets, there is, as a rule, used two coaxial cables or twisted-pair cables for all receivers. In other words, one coaxial cable for the high frequency clock and another coaxial

cable for the synchronizing clock.

In a clock distribution in which the high frequency clock is distributed together with synchronizing pulses, this means that precision must be very high in order for the synchronizing signal not to arrive at the wrong place or to be interpreted on the wrong clocking flank or edge. Among other things, this places high demands on the mutual exactness of the lengths of the cables (clock and synchronizing signal supply) and the relationship of these cables to other cable pairs that have other destinations in the system.

Furthermore, the distribution of the actual high frequency clock signal with which the circuits actually operate also places high demands on screening of cables and devices together with good earthing of the cables and devices, etc., so that EMC-interference can be avoided and continued functioning can be managed and maintained.

A typical method of generating an accurate clock frequency is to depart from a high frequency oscillator and to divide the frequency down to the desired clock frequency, which is therewith obtained with good stability and a resolution accuracy which has been improved by the division factor.

A typical method of distributing clock signals is also to transmit a clock signal of lower frequency which, in turn, then controls some type of oscillator having a higher frequency from which the desired clock frequency is generated. Swedish Publication SE 406,655 discloses a particular solution for such technique. U.S. Publication US-A 5,077,734 discloses a small private branch exchange in a digital network which applies this technique to generate a slightly higher clock frequency from a lower reference frequency.

French Publication EP-A1 0,190,731 discloses an arrangement comprising a receiver unit which delivers a clock signal and a

synchronizing signal, wherein the receiver unit obtains from the transmitter, via repeaters, a clock signal which is followed by a synchronizing signal.

Finally, British Publication GB-A 2,216,366 discloses a timing generator in which a composite bit data stream is tapped-off and caused to generate a data bit clocking signal of 64 Khz and an 8 Khz signal for clocking bytes synchronously with this bit stream; wherein the clocking signals thus generated continue to provide correct clocking even should the bit data stream cease. In this case, the composite signal is based on bipolar or alternating inversion of the pulse for a binary "one".

None of the aforedescribed arrangements fully solves the basic problems of needing to be able to distribute a clock signal in, for instance, telecommunications equipment that may contain many planes while simultaneously working with clock frequencies in the order of hundreds of megahertz.

SUMMARY OF THE INVENTION

When practicing the present invention, there is obtained a composite reference signal, CLSY, which through one single signal readily distributes both external clock signals and synchronizing signals through simple modulation of this CLSY-signal, wherein detection of the synchronizing signal in a subsequent bit clocking frequency generator for generating a high bit clocking frequency f_{BCL} has the result that any time jitter that may be present on the flanks or edges of the reference signal CLSY will not influence the definition of the secondary obtained local synchronizing signal, and wherein each data bit frame defined by the local synchronizing signal will always include precisely the intended number of data bits at the bit clocking frequency f_{BCL}.

According to the present invention, a bit clocking frequency generator comprising a PLL-circuit, a dividing circuit, a

shift register and a logic circuit will interpret the synchronizing information stored on the reference signal and create a bit clocking frequency which is much higher than the clocking frequency of the CLSY-signal, there being obtained from the bit clocking frequency generator a synchronizing pulse which has high precision both in relation to its high frequency system clock and in relation to an external time domain transferred through the synchronizing signal in the composite reference signal CLSY.

In accordance with the present invention, CLSY includes a clock frequency which preferably lies solely in the range of 5-10 megahertz, whereas the bit clocking frequency, i.e. the system frequency, is in the order of hundreds of megahertz, while, at the same time, the synchronizing frequency may only be in the order of some tens of kilohertz or lower.

The present invention affords the following advantages:

- Clock signals are distributed more easily from an EMC-aspect. The distribution medium need not have the same precision as when system clock and synchronizing are distributed separately. This enables, for instance, a single low quality optocable to be used.

- Pins and space are saved in devices and back planes, etc., because the same physical signal paths are used for both clock signals and synchronizing signals.

- Very good precision can be achieved, because the phase locked loop, the PLL-device, is allowed to generate both the local system clock and the synchronizing signal on one and the same chip.

In the illustrated case, the frequency f of the reference signal is, for instance, 5.12 Mhz and the external synchronizing signal SYNO corresponds to a frequency f_{SYNO} of 1/640 of the clock frequency for instance, i.e.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will now be described with reference to a preferred exemplifying embodiment thereof and with reference to the accompanying drawings, in which

Figure 1 illustrates generally and in block form a generator for producing a synchronizing signal and a high frequency bit clocking signal from a composite reference signal;

Figure 2 illustrates in somewhat more detail an exemplifying embodiment of the invention, comprising a generator for obtaining from the clock signal contained in a composite reference signal a high frequency bit clocking signal and also to obtain a frame synchronizing signal from the synchronizing signal in the composite reference signal;

Figure 3 illustrates the time relationship between a bit clocking signal, a first clock signal, a second clock signal, and a strobing signal in the generator according to Figure 1; and

Figure 4 illustrates the time relationship between a composite reference signal and the first clock signal, the second clock signal and the strobing signal when the reference signal presents a synchronizing pattern which defines a synchronizing signal.

BEST MODES OF CARRYING OUT THE INVENTION

Figure 1 illustrates generally a block which represents a generator GEN that operates to produce a synchronizing signal SYN1 and a high frequency bit clocking signal BCL from a composite reference signal CLSY which is comprised basically of an external clocking signal CL0. In the illustrated case, the frequency f_{CL0} of the reference signal is, for instance,

5.12 Mhz and the external synchronizing signal SYNO corresponds to a frequency f_{SYNO} of 1/640 of the clock frequency for instance, i.e. a frequency of 8 Khz. Expressed by the formula $f_{CLO} = M \cdot f_{SYNO}$, M will equal 640 in the case of the illustrated embodiment. There is generated in the generator GEN an internal bit clocking signal BCL which has a frequency f_{BCL} = 184.32 Mhz and in the case of the illustrative embodiment 2N will equal 36 in the formula $f_{BCL} = 2N \cdot f_{CLO}$, with N thus equalling 18. There is also delivered from the generator GEN a local synchronizing signal SYN1 having the frequency f_{SYN1} = 8 Khz, which is also related to the bit clocking signal BCL in its time domain and, at the same time, is related to the external synchronizing signal SYNO through the inventive method of detecting the synchronizing signal SYNO stored in the composite reference signal CLSY.

Figure 2 illustrates an exemplifying embodiment of the present invention which comprises the generator GEN shown in Figure 1, the main components of which include a frequency and phase locking loop PLL for generating the bit clocking frequency f_{BCL}, a frequency divider which includes two part-counters for generating from the frequency f_{BCL} two frequencies f_{CL1} and f_{CL2}, a circuit for generating a strobing signal STROB, a shift register SR including the four bits b_1 - b_4 and a logic circuit in the form of a simple AND-gate for generating the synchronizing signal SYN1. The frequency and phase locking loop or circuit PLL also includes a multiplying comparator COMP, a lowpass filter LP and a voltage controlled oscillator OSC. The frequency and phase locking loop PLL which generates the bit clocking frequency f_{BCL} may incorporate any standard circuit solution whatsoever known to the art. The bit clocking signal BCL delivered by the voltage controlled oscillator is divided by the factor N in a part-counter DIV1, this factor being equal to the integer 18 in the illustrated embodiment, to a frequency f_{CL2}, whereafter the frequency f_{CL2} is divided down in a second part-counter DIV2 by a further factor of 2, to obtain a frequency f_{CL1} which shall be equal to the clock frequency f_{CLO} in the composite reference signal CLSY. Thus, in the illustra-

tive embodiment, f_{BCL} = 184.32 Mhz, f_{CL2} = 10.24 Mhz and f_{CL1} = 5.12 Mhz. The clock frequency f_{CL0} for the composite reference signal CLSY is compared in the comparator with the frequency f_{CL1} from the other part-counter. The comparator delivers a signal voltage which is proportional to the phase deviation and which, via the lowpass filter LP, endeavours to control the voltage controlled oscillator so that $f_{CL1} = f_{CL0}$ and so that the phase difference between the signals will be close to zero. The lowpass filter functions to make the regulating loop slow, which means that temporary deviations in the frequency f_{CL0} will not immediately affect the voltage controlled oscillator. This means that when the phase controlled loop PLL has obtained a state of equilibrium, the frequency f_{BCL} will be held stable even in the event of minor interferences, such as a temporary absence of the signal CLSY, and also that a stable bit clocking frequency will actually be obtained even though time jitter should occur in the incoming clock signal CL0.

Starting from the signal that has the frequency f_{CL1}, in the illustrated case a frequency of 10.24 Mhz, there is generated a strobing signal STROB which, together with the reference signal CLSY, is fed into, for instance, a shift register SR which, in the case of the illustrated preferred embodiment, has four bits b_1 - b_4. The strobing signal STROB strobes the four bits b_1 - b_4 in the shift register SR and the resultant signal on the output of the shift register is delivered to an AND-gate G, wherein in the case of the illustrated embodiment the last two outputs are inverted prior to delivering the signal to the gate G, i.e. the signals from the outputs b_1 and b_2. Consequently, this gives the condition that if the bit combination 0011 on the four outputs from the shift register are delivered simultaneously to the gate G, the gate will deliver, according to a known pattern, a signal during the time in which all of its inputs have a high logic level. Thus, in the preferred embodiment, the CLSY-signal has a binary configuration ...0101<u>0011</u>0101... in association with a synchronizing signal. According to a basic exemplifying embodi-

ment, in principle the shift register SR requires only two bits in order to detect a bit combination 11 or 00 capable of defining a synchronizing signal. In other words, in the synchronizing signal, CLSY can have respectively a configuration ...1010-110101... and ...0101001010... in order to retain the phase in CLSY as seen totally, and it is beneficial in such an embodiment to construct the logic gate G to detect the bit combination 11 and 00 respectively, suitably alternately, delivered by the shift register SR, by arranging the logic circuit to function, for instance, alternately as an AND-gate having two inputs and alternately as a NOR-gate having two inputs. By increasing the number of bits that define the synchronizing signal, for instance to four bits as in the case of the preferred embodiment, the certainty that temporary inference will not generate a signal which is taken to be a synchronizing signal is further improved.

With the intention of further illustrating the signal sequence, Figure 3 illustrates a time slice which includes the signals BCL, CL1, CL2 and STROB for an imaginary case in which 2N = 16, i.e. in which the frequency of the generated signal BCL is sixteen times higher than the frequency of the clock signal in the composite reference signal CLSY. It will be seen from Figure 3 that a strobing signal STROB is generated conventionally with the aid of the signal CL2, and that the strobing signal will be centred or generally centred with the centre point of each half-period of the clock signal CL1, and therewith also with the clock signal CL0 in the composite reference signal CLSY, since these signals coincide as a result of the action of the frequency and phase locking circuit or loop PLL. The strobing signal pulses may, for instance, have a pulse length which conveniently corresponds to the pulse length of the bit clocking signal BCL and are generated in a known manner.

Figure 4 illustrates a time slice of the composite reference signal CLSY, and shows the signal to include a synchronizing

signal SYNO. The Figure also shows in the same time scale the signals CL1, CL2 and STROB obtained in accordance with what has already been described above with reference to Figures 2 and 3. The binary result of the strobe effected with the strobing signal STROB against the signal CLSY is shown at the bottom of Figure 4. When the signal CLSY has been shifted in the shift register SR in Figure 2 so that the section referenced SYNO, and which in the illustrated embodiment has a length of four bits, b_1 - b_4, is located in the shift register SR and is strobed by the strobing signal STROB, the binary values $b_1 = 0$, $b_2 = 0$, $b_3 = 1$ and $b_4 = 1$ are delivered in parallel to the inputs of the gate G in Figure 2. Since the two inputs of the gate corresponding to b_1 and b_2 have been inverted, the gate G will obtain signals which have a high logic level on all of its four inputs and will therewith deliver a corresponding signal on its output SYN1. The signals obtained by strobing the shift register SR are suitably obtained with the same pulse lengths as the strobing signal STROB and the gate G will therewith also produce a pulse of the same order of magnitude as a one half-period of the bit clocking signal BCL. It will be obvious to one skilled in this art that it is equally as effective to, for instance, invert the two inputs corresponding to b_3 and b_4 instead and to use, for instance, a NOR-type gate instead of the AND-gate G. Correspondingly, an AND-gate whose inputs corresponding to the two bits b_3 and b_4 from the shift register are inverted instead would produce an output pulse for the bit combination 1100, i.e. in the case of the illustrative embodiment, the incorporated synchronizing signal would be comprised of a signal having two time intervals in the signal CLSY with high logic level followed by two time intervals with low logic level, where one time interval t corresponds to one half-period of the frequency f_{CL0} or f_{CL1}.

By placing the strobing signal STROB centrally between two expected level changes in the signal CLSY with a high degree of accuracy, it is ensured that the synchronizing signal SYNO will be sensed or strobed even should the clock signal CL0 in

the composite reference signal have strong time jitter and a poorly defined transition between high and low logic levels. The inventive method ensures detection of the synchronizing signal SYNO and, because the strobing signal STROB is located in the time domain of the bit clocking signal BCL, the synchronizing signal SYN1 is automatically related to the bit clocking signal and it is therewith guaranteed that there will be obtained from the bit clocking signal BCL precisely $2N \cdot M$ clock pulses for a data bit frame that is defined by the synchronizing signal SYNO, i.e. through the frequency f_{SYN1}. The frequency f_{SYN1} is thus simultaneously fully locked to the frequency f_{BCL} of the bit clocking signal with maximum time resolution when the signal STROB which generates SYN1 has been obtained by dividing down the bit clocking signal BCL. In the illustrative embodiment, 2N is thus equal to 36 and M is equal to 640, which provides 23 040 clock pulses at the bit clocking frequency of 184.32 Mhz for each data bit frame having the synchronizing frequency of 8 Khz and which is obtained stably but with a transferred reference clock which runs solely at a frequency of 5.12 Mhz, which affords much better conditions for clock distribution than if it were effected at the higher frequency of 184.24 Mhz.

In an inventive system, each plane may have its own CLSY-signal. When generating the signals, CLSYn, n = 1, 2, 3..., it is ensured that their mutual phase relationship will not deviate by more than one-half time interval t, where t corresponds to one half-period of the clock frequency f_{CLO} in the CLSY-signal. In other words, CLSYn must be located within a window which is suitable
$\frac{1}{2}t$ = 44 ns wide at a clocking frequency f_{CLO} = 5.12 Mhz, in accordance with the illustrated embodiment. By suitable selection of a time constant through the lowpass filter LP in the phase locking loop PLL it is then possible for any plane whatsoever in the system to take over the composite reference signal CLSYn from any plane in the system whatsoever and at any time whatsoever, which provides an important safety redun-

dancy in such a system.

CLAIMS

1. A method for distributing a common frame reference for a high frequency bit clocking generator through the medium of a composite clock and synchronizing signal, **characterized** in that the clock and synchronizing signal is formed as a composite reference signal (CLSY) which, at the same time, includes an external clock signal (CLO) which with high frequency alternates between two logic levels, and an external synchronizing signal (SYNO) having a low frequency and stored in the signal of high frequency forming the external clock signal, wherein the frequency (f_{CLO}) of the external clock signal is an integer M times the frequency (f_{SYN}) of the synchronizing signal; and

in that the external synchronizing signal (SYNO) in the composite reference signal (CLSY) will be decoded with high precision irrespective of any phase jitter that may occur on the edges of the reference clock signal by virtue of the fact that it includes within the time frame of the primary clock signal at least two mutually sequential intervals of the same logic level, preferably followed by a corresponding number of intervals having the opposite logic level, wherein one such interval (t) corresponds to one half-period of the primary clock signal frequency (f_{CLO}); and in that each such interval (t) is sensed in the centre of the interval between two expected signal edges.

2. A method according to Claim 1, **characterized** in that when detecting the composite reference signal from the clock signal in the composite reference signal, there is first created a bit clocking signal frequency (f_{BCL}) which is a multiple of the external clock signal frequency (f_{CLO}) in the composite reference signal (CLSY) by a factor equal to twice an integer N; in that there is created at the same time a first clock signal frequency (f_{CL1}) by dividing the bit clocking frequency (f_{BCL}) by 2N; in that the first clock signal frequency is compared with the external clock signal frequency (f_{CLO}) in a frequency and phase locking circuit; and in that there is created a second

signal frequency (f_{CL2}) by dividing the bit clocking frequency (f_{BCL}) by N, wherein the second clock signal frequency (f_{CL2}) is intended for use to create a strobing signal (STROB) for detection of the synchronizing signal (SYNO) in the composite reference signal (CLSY).

3. A method according to Claim 2, **characterized** by aligning the strobing signal (STROB) by displacement through one-half of a time interval in relation to the first clock frequency (f_{CL1}) and therewith at the same time in relation to the external clock frequency (f_{CL0}) for reading the external clock signal (CL0) in the interval centrally between the positive and the negative edges or the transitions between the two logic levels which form the external clock signal (CL0) in the composite reference signal (CLSY) and whose signal edges can generally jitter.

4. A method according to Claim 3, **characterized** in that the external synchronizing signal (SYNO) is considered to exist close to the strobing signal (STROB) in the composite reference signal and is detected during several mutually sequential intervals having the same logic level followed preferably by a corresponding number of intervals having the opposite logic level.

5. A method according to Claim 3, **characterized** in that the external synchronizing signal (SYNO) is considered to lie close to the strobing signal (STROB) in the composite reference signal and is detected during two mutually sequential intervals having the same logic level, followed by two intervals having the opposite logic level.

6. A method according to Claim 4 or 5, **characterized** in that by virtue of the bit clocking signal (BCL) creating a factor 2N which is twice the primary clock signal (CL), there is obtained a data bit frame against the synchronizing signal which constantly contains exactly 2N x M data bits, and in

that the bit clocking signal (BCL) and the frame synchronizing signal (SYN) are totally referred to the composite reference signal (CLSY) with sufficient precision.

7. A method according to Claim 6, **characterized** by using a selective composite reference signal (CLSYn, n = 1, 2, 3...) representing a selective plane in the system to create the bit clocking signal (BCL) and the frame synchronizing signal (SYN1) in the system when the selective composite reference signals (CLSYn) have a mutual time difference which is below one-half time interval (t).

8. An arrangement for using a composite reference signal (CLSY) to create a high frequency bit clocking signal (BCL) having a frequency (f_{BCL}), said arrangement including a phase locking circuit (PLL) including generally a comparator, a lowpass filter, an oscillator and a frequency divider, **characterized** in that the frequency divider is divided into a first divider (DIV1) which divides with an integer N, to obtain a second clock frequency (f_{CL2}) which is used to create a strobing signal (STROB); and in that the frequency divider also includes a further second divider (DIV2) which divides by the factor 2, to obtain a first clock frequency (f_{CL1}) which is equal to the reference frequency in the composite reference signal (CLSY) for use in the phase locking circuit.

9. An arrangement according to Claim 8, **characterized** in that the arrangement further includes a shift register (SR) having a number of steps corresponding to the number of bits in a signal which defines a synchronizing signal (SYNO) in the composite reference signal (CLSY), wherein the composite reference signal (CLSY) is fed into the shift register and the shift register strobes with the strobing signal (STROB) to create an input to a logic circuit (G) for detecting and generating the synchronizing signal with a locked relationship to the created bit clocking frequency (f_{BCL}).

10. An arrangement according to Claim 9, **characterized** in that the logic gate circuit has a number of inputs which correspond to the number of steps in the shift register (SR), wherein preferably a first half or a second half of the gate circuit inputs are provided with an inverting device so as to obtain from the composite reference signal a synchronizing condition in the composite reference signal (CLSY) with the aid of the logic gate circuit.

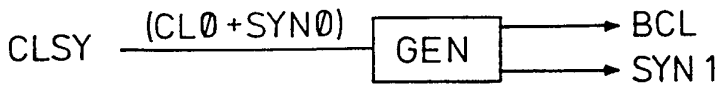
11. An arrangement according to Claim 10, **characterized** in that the synchronizing condition in the composite reference signal (CLSY) is defined by the presence of several mutually sequential intervals having the same logic level, preferably followed by a corresponding number of intervals having the opposite logic level, wherein one such interval (t) is equal to one half-period of the primary clock signal frequency (f_{CL0}).

12. An arrangement according to Claim 10, **characterized** in that the synchronizing condition in the composite reference signal (CLSY) is defined by the presence of two mutually sequential intervals having the same logic level followed by two intervals having the opposite logic level, wherein one such interval (t) is equal to one half-period of the primary clock signal frequency (f_{CL0}).

13. A reference signal (CLSY) composed of a clock signal (CL0) having a clock frequency (f_{CL0}) and a synchronizing signal (SYN0) for creating an internal high frequency bit clocking signal (BCL) having a high frequency (f_{BCL}) and an internal synchronizing signal (SYN1) in a system, **characterized** in that the external synchronizing signal (SYN0) is defined by the presence of several mutually sequential intervals (t) having the same logic level, preferably followed by a corresponding number of intervals having the opposite logic level, wherein one such interval (t) is equal to one half-period of the primary clock signal frequency (f_{CL0}).

14. A reference signal according to Claim 13, characterized in that there is included in the time frame for the clock frequency (f_{CLO}) of the clock signal (CLO) a binary bit information 0011 as a characteristic of the synchronizing signal (SYNO) in the composite reference signal (CLSY).

15. A reference signal according to Claim 13, characterized in that there is included in the time frame for the clock frequency (f_{CLO}) of the clock signal (CLO) a binary bit information 1100 as a characteristic of the synchronizing signal (SYNO) in the composite reference signal (CLSY).



$f_{CL\emptyset} = M \cdot f_{SYN}$ $f_{BCL} = 2Nf_{CL\emptyset}$

Fig. 1

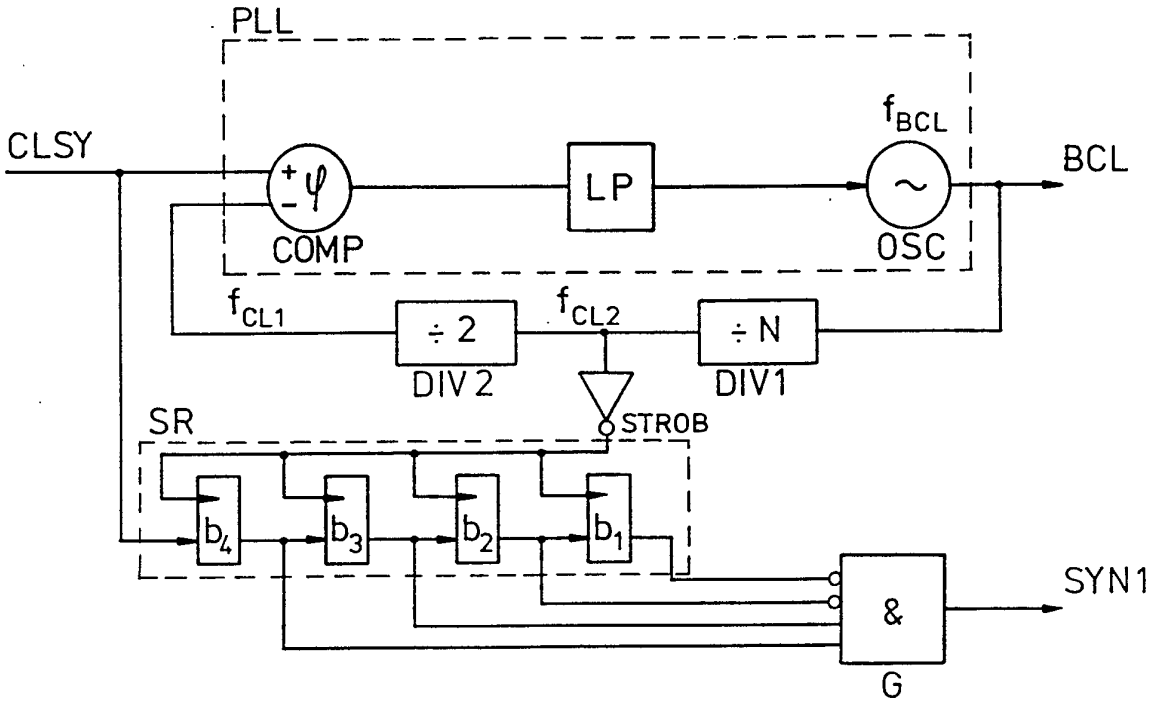
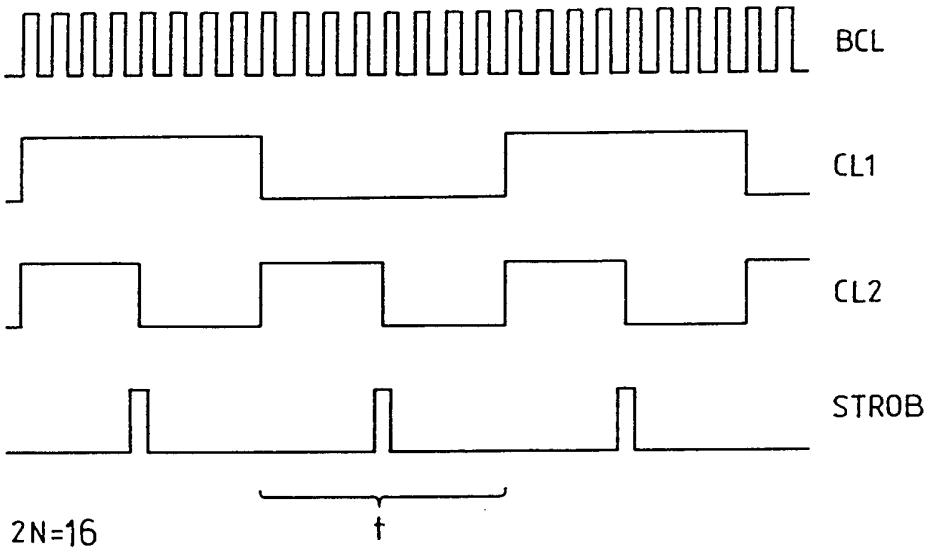


Fig. 2

Fig. 3


BCL
CL1
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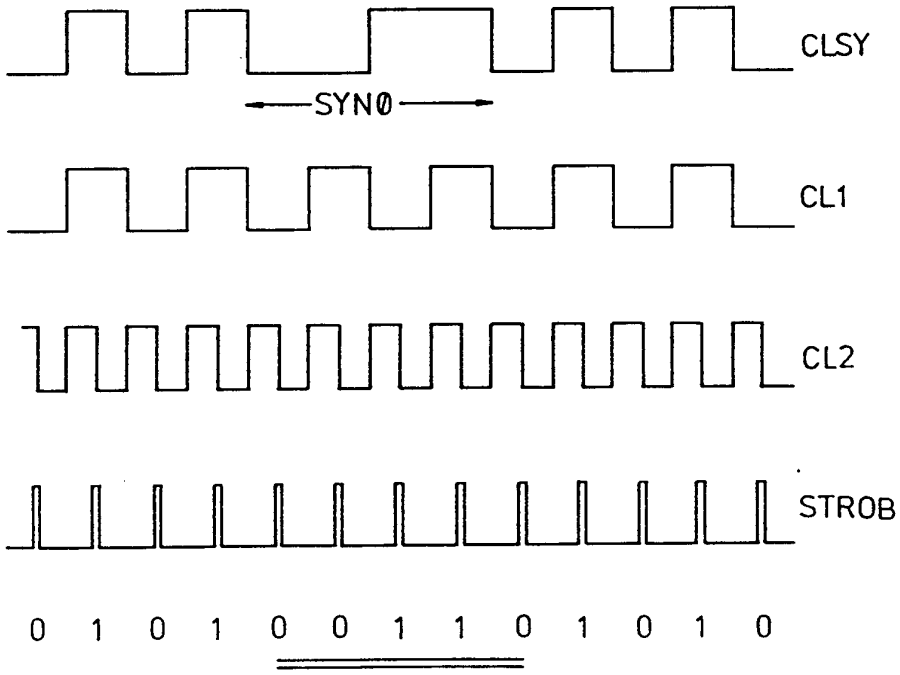
CLSY
SYNØ
CL1
CL2
STROB
0 1 0 1 0 0 1 1 0 1 0 1 0

Fig. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 94/00321

A. CLASSIFICATION OF SUBJECT MATTER

IPC5: H04L 7/04, H04J 3/06
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC5: H04L, H04J, G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	DK, B, 149279 (MINNESOTA MINING AND MANUFACTURING COMPANY), 3 May 1979 (03.05.79), see the whole document --	1-14
A	EP, A1, 0491054 (FUJITSU LIMITED), 24 June 1992 (24.06.92), see the whole document --	1-14
A	US, A, 4759041 (S.C. ANDERSON ET AL.), 19 July 1988 (19.07.88), see the whole document -- --------	1-14

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
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Date of the actual completion of the international search	Date of mailing of the international search report
26 July 1994	29 -07- 1994
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Göran Magnusson Telephone No. +46 8 782 25 00

INTERNATIONAL SEARCH REPORT

Information on patent family members

02/07/94

International application No.
PCT/SE 94/00321

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DK-B- 149279	03/05/79	NONE	
EP-A1- 0491054	24/06/92	AU-B- 636050	08/04/93
		AU-A- 8189191	04/02/92
		JP-A- 4068625	04/03/92
		WO-A- 9201343	23/01/92
US-SA- 4759041	19/07/88	NONE	