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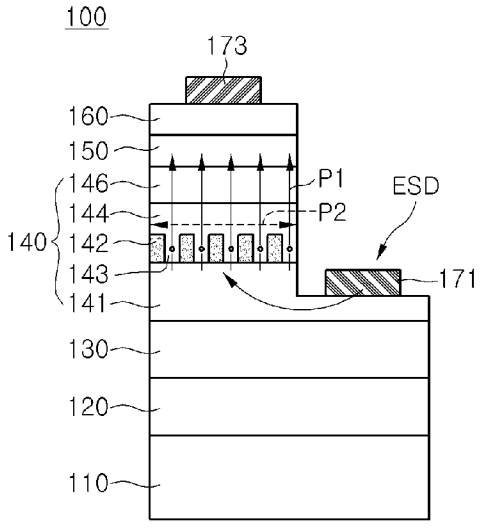
(54) **Title:** SEMICONDUCTOR LIGHT EMITTING DEVICE AND METHOD OF FABRICATING THE SAME

[Fig. 2]



(57) **Abstract:** Provided are a semiconductor light emitting device and a method of fabricating the same. The semiconductor light emitting device comprises a first conductive type semiconductor layer, an active layer, and a second conductive type semiconductor layer. The first conductive type semiconductor layer comprises an insulation layers comprising a predetermined interval and a voids between the insulation layers. The active layer is disposed on the first conductive type semiconductor layer. The second conductive type semiconductor layer is disposed on the active layer.

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Description

SEMICONDUCTOR LIGHT EMITTING DEVICE AND METHOD OF FABRICATING THE SAME

Technical Field

[1] Embodiments relate to a semiconductor light emitting device and a method of fabricating the same.

Background Art

[2] A III-V group nitride semiconductor has been variously used for an optical device such as blue/green light emitting diodes (LEDs), a high speed switching device such as a metal semiconductor field effect transistor (MOSFET) and a hetero junction filed effect transistor (HEMT), a light source of an illumination or a display apparatus, and the like. In particular, a light emitting device using an III group nitride semiconductor has a direct transition-type bandgap corresponding to the range of visible rays to ultraviolet rays, and can perform high efficient light emission.

[3] The nitride semiconductor has been mainly utilized as a LED or a laser diode (LD), and research for improving the manufacturing process or light efficiency has been conducted.

Disclosure of Invention

Technical Problem

[4] Embodiments provide a semiconductor light emitting device comprising a conductive type semiconductor layer comprising an insulation layers or voids, and a method of fabricating the same.

[5] Embodiments provide a semiconductor light emitting device comprising a first conductive type semiconductor layer comprising an insulation layers and a voids, and a method of fabricating the same.

Technical Solution

[6] An embodiment provides a semiconductor light emitting device comprising: a first conductive type semiconductor layer comprising an insulation layers comprising a predetermined interval and a voids between the insulation layers; an active layer on the first conductive type semiconductor layer; and a second conductive type semiconductor layer on the active layer.

[7] An embodiment provides a semiconductor light emitting device comprising: a first conductive type semiconductor layer comprising a first nitride layer formed with a first electrode layer and a second nitride layer comprising a voids; an active layer on the second nitride layer; and a second conductive type semiconductor layer on the active layer.

[8] An embodiment provides a method of fabricating a semiconductor light emitting device comprising: forming a first conductive type semiconductor layer comprising an insulation layers and a voids between the insulation layers therein; forming an active layer on the first conductive type semiconductor layer; and forming a second conductive type semiconductor layer on the active layer.

Advantageous Effects

[9] Embodiments can improve electrostatic discharge (ESD) characteristics.

[10] Embodiments can reduce dislocation density due to insulation layers and voids of a first conductive type semiconductor layer.

[11] Embodiments can minimize damage of an active layer.

[12] Embodiments can improve internal quantum efficiency because a first conductive type semiconductor layer uniformly distributes a current injected into an active layer.

[13] Embodiments can improve reliability of a semiconductor light emitting device.

Brief Description of the Drawings

[14] Fig. 1 is a side cross-sectional view of a semiconductor light emitting device according to a first embodiment.

[15] Fig. 2 is a view of current distribution when an electrostatic discharge (ESD) voltage is applied to the semiconductor light emitting device of Fig. 1.

[16] Figs. 3 to 7 are side cross-sectional views illustrating a process of fabricating the semiconductor light emitting device according to a first embodiment.

[17] Fig. 8 is a side cross-sectional view of a semiconductor light emitting device according to a second embodiment.

Mode for the Invention

[18] Hereinafter, a semiconductor light emitting device and a method of fabricating the same according to embodiments will be described in detail with reference to the accompanying drawings. In the following description, when a layer (or film) is referred to as being on or under another layer, its description will be made with reference to the accompanying drawings. The thickness of each layer may be described as one example, and is not limited to the thicknesses of the accompanying drawings.

[19] Fig. 1 is a side cross-sectional view of a semiconductor light emitting device according to a first embodiment.

[20] Referring to Fig. 1, a semiconductor light emitting device 100 comprises a substrate 110, a buffer layer 120, an undoped semiconductor layer 130, a first conductive type semiconductor layer 140 comprising an insulation layers 142 and a voids 143, an active layer 150, a second conductive type semiconductor layer 160, a first electrode layer 171, and a second electrode layer 173.

[21] The substrate 110 may be formed of at least one of sapphire (Al_2O_3), SiC, Si, GaAs,

GaN, ZnO, GaP, InP, and Ge. Also, the substrate 110 may be formed of a material having conductive characteristics. Uneven patterns may be disposed on and/or under the substrate 110. Each of the uneven patterns may have one of stripe, lens, cylindrical, and cone shapes, but are not limited thereto.

[22] A nitride semiconductor is grown on the substrate 110. An E-beam evaporator, a physical vapor deposition (PVD) apparatus, a chemical vapor deposition (CVD) apparatus, a plasma laser deposition (PLD) apparatus, a dual-type thermal evaporator, a sputtering apparatus, and a metal organic chemical vapor deposition (MOCVD) apparatus may be used as growth equipment, but not limited to the apparatuses.

[23] The buffer layer 120 is disposed on the substrate 110. The undoped semiconductor layer 130 is disposed on the buffer layer 120. The buffer layer 120 acts as a layer decreasing a lattice constant difference between the substrate 110 and GaN material. The undoped semiconductor layer 130 comprises an undoped GaN layer and acts as a substrates on which the nitride semiconductor is grown. Only one of the buffer layer 120 and the undoped semiconductor layer 130 may be disposed on the substrate 110, or all two layers of the buffer layer 120 and the undoped semiconductor layer 130 may not be disposed on the substrate 110.

[24] The first conductive type semiconductor layer 140 is disposed on the undoped semiconductor layer 130. For example, the first conductive type semiconductor layer 140 may be realized with an n-type semiconductor layer doped with n-type dopants. The n-type semiconductor layer may be formed of one of semiconductor materials having a composition formula expressed by $In_yAl_xGa_{1-x-y}N$ ($0\leq x\leq 1$, $0\leq y\leq 1$, $0\leq x+y\leq 1$), e.g., InAlGaN, GaN, AlGaN, InGaN, AlN, and InN. The n-type dopants may comprise Si, Ge, Sn, Se, and Te.

[25] The first conductive type semiconductor layer 140 comprises a first nitride layer 141, the insulation layers 142, the voids 143, a second nitride layer 144, and a third nitride layer 146.

[26] The first to third nitride layers 141, 144, and 146 may be realized with the n-type semiconductor layer doped with the n-type dopants.

[27] The first nitride layer 141 is disposed on the undoped semiconductor layer 130, and the first electrode layer 171 is disposed on one side thereof. The first nitride layer 141 may be formed of one of InAlGaN, GaN, AlGaN, InGaN, AlN, and InN, and defined as a first electrode contact layer.

[28] The insulation layers 142 are disposed on the first nitride layer 141. Each of the insulation layers 142 may have a protrusion shape having insulation characteristics. The insulation layers 142 may be realized with MgN layers. The MgN layers may have a random size and shape and irregular intervals.

[29] Also, the insulation layers 142 may comprise a nitride semiconductor having the

insulation characteristics. The nitride semiconductor having the insulation characteristics may be realized with a nitride semiconductor doped with p-type dopants and the n-type dopants, for example, may be formed of one of GaN, AlGaN, InGaN, and InAlGaN. The p-type dopants comprise Mg, Zn, Ca, Sr, and Ba, and the n-type dopants comprise Si, Ge, Sn, Se, and Te.

[30] Each of the insulation layers 142 has a predetermined thickness, e.g., a thickness ranging from about 0.0001μm to about 1μm on a surface of the first nitride layer 141. A pitch between a protrusion and an adjacent protrusion of the insulation layers 142 may be in the range of about 10Å to 3μm.

[31] Since the insulation layers 142 are spaced a predetermined distance from each other on the first nitride layer 141, the insulation layers 142 partially block an electrostatic discharge (ESD) voltage applied through the first nitride layer 141.

[32] The second nitride layer 144 is disposed on the insulation layers 142. The second nitride layer 144 may comprise a semiconductor layer formed of GaN, for example, may be formed of one of InAlGaN, GaN, AlGaN, and InGaN. Preferably, the second nitride layer 144 may be formed of GaN.

[33] The second nitride layer 144 comprises voids 143 disposed between the insulation layers 142. The voids 143 may be disposed between the insulation layers 142, within the second nitride layer 144, or between the first nitride layer 141 and the second nitride layer 144. Here, the voids 143 may be disposed between some or all protrusions of the insulation layers 142.

[34] The second nitride layer 144 acts as a bridge layer receiving a voltage of the first nitride layer 141. The second nitride layer 144 may act as a low defect layer having a dislocation lower than that of the first nitride layer 141. The low defect layer diffuses current into a whole layer.

[35] Since the insulation layers 142 are disposed on the first nitride layer 141, regions (comprising void regions) between the insulation layers 142 may act as a seed layer of the second nitride layer 144.

[36] Since the insulation layers 142 and the voids 143 block the dislocation existing within the first nitride layer 141, dislocation density of the second nitride layer 144 may be less than that of the first nitride layer 141. Since the dislocation density of the second nitride layer 144 is reduced, ESD resistance may be improved.

[37] The insulation layers 142 and the voids 143 may be disposed between the layer 141 on which the first electrode layer 171 is disposed and the active layer 150.

[38] The third nitride layer 146 is disposed on the second nitride layer 144. The third nitride layer 146 may be formed of one of InAlGaN, GaN, AlGaN, InGaN, AlN, and InN.

[39] The active layer 150 is disposed on the third nitride layer 146. The active layer 150

may comprise a single quantum well structure or a multi quantum well structure. A conductive type clad layer (not shown) may be disposed on and/or under the active layer 150. The conductive type clad layer may be realized with an AlGaN layer.

[40] The second conductive type semiconductor layer 160 is disposed on the active layer 150. The second conductive type semiconductor layer 160 may be realized with a p-type semiconductor layer doped with the p-type dopants. The p-type semiconductor layer may be formed of one of semiconductor materials having a composition formula expressed by $In_yAl_xGa_{1-x-y}N$ ($0 \le x \le 1$, $0 \le y \le 1$, $0 \le x+y \le 1$), e.g., InAlGaN, GaN, AlGaN, InGaN, AlN, and InN. The p-type dopants may comprise Mg, Zn, Ca, Sr, and Ba.

[41] The second electrode layer 173 is disposed on the second conductive type semiconductor layer 160. A third conductive type semiconductor layer (not shown) and/or a transparent electrode layer (not shown) may be disposed between the second conductive type semiconductor layer 160 and the second electrode layer 173. The third conductive type semiconductor layer may be realized with the n-type semiconductor layer or the p-type semiconductor layer according to an n-p-n junction structure or a p-n-p junction structure.

[42] Fig. 2 is a view of current distribution when an ESD voltage is applied to the semiconductor light emitting device of Fig. 1.

[43] Referring to Fig. 2, an ESD voltage may be applied to the first electrode layer 171 of the semiconductor light emitting device 100. The ESD voltage applied to the first electrode layer 171 is voltage-dropped and dispersed by the first conductive type semiconductor layer 140 to transmit the voltage-dropped and dispersed voltage into the active layer 150.

[44] The insulation layers 142 of the first conductive type semiconductor layer 140 block the ESD voltage. The blocked ESD voltage moves into a position at which the insulation layers 142 are not disposed, i.e., a position at which the voids are disposed. That is, the ESD voltage dispersedly moves into the position at which the voids are disposed by the insulation layers 142 within the first nitride layer 141.

[45] The ESD voltage is transmitted to the second nitride layer 144 through the voids 143 disposed between the insulation layers 142. Here, the ESD voltage passes through the voids 143 using a tunneling effect. The ESD voltage passing through the voids 143 is voltage-dropped. That is, the ESD voltage transmitted to the second nitride layer 144 is lower than an initial applied voltage. The tunneling effect is in inverse proportion to a depth (i.e., height) of each of the voids 143 and in proportion to a width of each of the voids 143.

[46] The insulation layers 142 partially block an ESD voltage of the first nitride layer 141 to horizontally disperse the ESD voltage. The voids 143 transmit the ESD voltage to the second nitride layer 144 through a vertical channel P1. Here, the ESD voltage is

primarily dropped by the tunneling effect of the voids 143.

[47] Since the second nitride layer 144 acts as the low defect layer, the second nitride layer 144 can horizontally disperse the ESD voltage transmitted through the voids 143.

[48] The first conductive type semiconductor layer 140 partially blocks, voltage-drops, and disperses the ESD voltage applied to the first electrode layer 171 to transmit the ESC voltage to the active layer 150. The semiconductor light emitting device 100 has resistance against a high-voltage such as the ESD voltage applied to the first electrode layer 171. Also, damage of the active layer 150 due to the ESD voltage can be minimized.

[49] Since the first conductive type semiconductor layer 140 disperses a forward current to transmit the dispersed current to the active layer 150, internal quantum efficiency can be improved.

[50] Figs. 3 to 7 are side cross-sectional views illustrating a process of fabricating the semiconductor light emitting device according to a first embodiment.

[51] Referring to Fig. 3, a buffer layer 120, an undoped semiconductor layer 130 and a first nitride layer 141 of a first conductive type semiconductor layer 141 are sequentially formed on a substrate 110.

[52] The substrate 110 may be formed of at least one of sapphire (Al_2O_3), SiC, Si, GaAs, GaN, ZnO, GaP, InP, and Ge.

[53] The buffer layer 120 acts as a layer decreasing a lattice constant difference between the substrate 110 and the undoped semiconductor layer 130, and may be formed of one of GaN, AlN, AlGaN, and InGaN.

[54] The undoped semiconductor layer 130 may be realized with an undoped GaN layer on the buffer layer 120 or the substrate 110. Only one of the buffer layer 120 and the undoped semiconductor layer 130 may be formed on the substrate 110, or none of them may be formed on the substrate 110.

[55] The first nitride layer 141 of the first conductive type semiconductor layer is formed on the undoped semiconductor layer 130. For example, in a growth method of the first nitride layer 141, a silane gas comprising an n-type dopants such as NH_2, TMGa (or TEGa), and Si is supplied to form a GaN layer having a predetermined thickness. Here, the first nitride layer 141 may be formed of one of InAlGaN, AlGaN, InGaN, AlN, and InN instead of GaN.

[56] Referring to Fig. 4, the insulation layers 142 are formed on the first nitride layer 141. Each of the insulation layers 142 are formed with a random protrusion shape and have irregular intervals relative to each other.

[57] Recesses 143A are formed between the insulation layers 142. The insulation layers 142 act as a voltage blocking layer, and may be formed of a material having insulation characteristics, e.g., MgN. In a growth method of the MgN insulation layers 142, for

example, H_2 atmosphere gas and NH_3 source gas are supplied with a predetermined amount (e.g., H_2:100 slpm, NH_3:30 slpm), and then, Cp2Mg source gas flows for a predetermined time interval (e.g., about five minutes) and with a predetermined amount (e.g., about 1-2 μmol) in a state where the H_2 atmosphere gas is not supplied to form the MgN layers having the random protrusion shape on the first nitride layer 141.

[58] The insulation layers 142 may comprise a nitride semiconductor doped with the n-type dopants and p-type dopants. For example, the insulation layers 142 may comprise a GaN layer co-doped with Mg-Si.

[59] Referring to Fig. 5, the second nitride layer 144 is formed on the insulation layers 141. The second nitride layer 144 is formed on the insulation layers 141 and the first nitride layer 141, and voids 143 are formed between the insulation layers 142. A surface of the second nitride layer 144 may have an uneven shape or a flat shape.

[60] For example, in a growth method of the second nitride layer 144, the silane gas comprising the n-type dopants such as NH_2, TMGa (or TEGa), and Si is supplied to form a GaN layer having a predetermined thickness. Here, the amount of TMGa gas supplied to the second nitride layer 144 is more than the amount of TMGa gas supplied to the first nitride layer 141. Thus, the second nitride layer 144 grows actively in a vertical direction such that the recesses (reference numeral 143A of Fig. 4) between the insulation layers 142 exist in a state of voids 143 having a predetermined size. That is, when the second nitride layer 144 is grown, a size of each of the voids 143 between the insulation layers 142 can be adjusted by adjusting the Ga source gas (i.e., TMGa).

[61] Since the second nitride layer 144 has a growth condition different from that of the first nitride layer 141, a dislocation existing on a bounday between the two layers 141 and 144 is not propagated, but horizontally progressed. As a result, the dislocation is reduced or eliminated. Thus, threading dislocation of the second nitride layer 144 is bended or removed, and thus, grown as a low defect layer, thereby increasing resistance against the voltage.

[62] A doping density of the n-type dopants of the second nitride layer 144 is $(1\sim9.9)\times10^{17}/cm^3$, and hole mobility is greater than about $500cm^2/Vs$.

[63] Here, the insulation layers 142 partially block a voltage transmitted from the first nitride layer 141 to the second nitride layer 144. The second nitride layer 144 disperses a voltage applied to the first nitride layer 141, and then, transmits the dispersed voltage to the third nitride layer 146.

[64] The voids 143 drop high-voltage such as an EDS voltage applied to the first nitride layer 141 using a tunneling effect to transmit the dropped voltage to the second nitride layer 144. The tunneling effect is in inverse proportion to a depth of each of the voids 143 and in proportion to a width of each of the voids 143.

[65] The second nitride layer 144 may have the growth condition different from those/that

of the first nitride layer 141 and/or the third nitride layer 146. The insulation layers 142 and the voids 143 are formed on the first nitride layer 141, i.e., an electrode contact layer.

[66] Referring to Fig. 6, the third nitride layer 146 is formed on the second nitride layer 144. For example, in a growth method of the third nitride layer 146, the silane gas comprising the n-type dopants such as NH_2, TMGa (or TEGa), and Si is supplied to form a GaN layer having a predetermined thickness.

[67] The first conductive type semiconductor layer 140 comprises the first nitride layer 141, the insulation layers 142, the second nitride layer 144 and the third nitride layer 146. Also, the first conductive type semiconductor layer 140 blocks, voltage-drops, and disperses the ESD voltage. That is, resistance against an ESD reverse voltage of the semiconductor light emitting device can be improved.

[68] An active layer 150 is formed on the third nitride layer 146 of the first conductive type semiconductor layer 140. A second conductive type semiconductor layer 160 is formed on the active layer 150. A third conductive type semiconductor layer (not shown) and/or a transparent electrode layer (not shown) may be formed on the second conductive type semiconductor layer 160. The third conductive type semiconductor layer may be realized with the n-type semiconductor layer.

[69] The active layer 150 may comprise a single quantum well structure or a multi quantum well structure. A conductive type clad layer (not shown) may be formed on and/or under the active layer 150. The conductive type clad layer may be realized with an AlGaN layer.

[70] The second conductive type semiconductor layer 160 may be realized with a p-type semiconductor layer doped with the p-type dopants. The p-type semiconductor layer may be formed of one of semiconductor materials having a composition formula expressed by $In_yAl_xGa_{1-x-y}N$ ($0\leq x\leq 1$, $0\leq y\leq 1$, $0\leq x+y\leq 1$), e.g., InAlGaN, GaN, AlGaN, InGaN, AlN, and InN. The p-type dopants may comprise Mg, Zn, Ca, Sr, and Ba.

[71] Referring to Fig. 7, a mesa etching process is performed on a portion of the second conductive type semiconductor layer 160 to expose the first nitride layer 141 of the first conductive type semiconductor layer 140. A first electrode layer 171 is formed on the first nitride layer 141, and a second electrode layer 173 is formed on the second conductive type semiconductor layer 160.

[72] Fig. 8 is a side cross-sectional view of a semiconductor light emitting device according to a second embodiment. In the following description of the second embodiment, duplicate description for elements which are the same as those of the first embodiment will be omitted.

[73] Referring to Fig. 8, a semiconductor light emitting device 100A comprises a first conductive type semiconductor layer 140 comprising an insulation layers 142 and a

voids 143, an active layer 150, a second conductive type semiconductor layer 160, a reflective electrode layer 180, and a conductive support substrate 190.

[74] The reflective electrode layer 180 is disposed on the second conductive type semiconductor layer 160, and the conductive support substrate 190 is disposed on the reflective electrode layer 180.

[75] Here, the reflective electrode layer 180 serves as a p-type electrode, and the p-type electrode becomes an ohmic contact in order to stably supply current to the second conductive type semiconductor layer 160. Here, the reflective electrode layer 180 may be formed of a single layer or a multilayer having one of Ag, Ni, Al, Rh, Pd, Ir, Ru, Mg, Zn, Pt, Au, Hf, and a combination thereof. The conductive support substrate 190 may be formed of copper or gold. Materials of the reflective electrode layer 180 and the conductive support substrate 190 may vary and are not limited to the above materials.

[76] A first electrode 171 is disposed under the first conductive type semiconductor layer 140. Since the conductive support substrate 190 and the reflective electrode layer 180 serve as a second electrode, a vertical type semiconductor light emitting device can be realized.

[77] Referring to Fig. 6, the substrate 110 disposed under the first conductive type semiconductor layer 140, the buffer layer 120, and the undoped semiconductor layer 130 are removed using a physical and/or chemical removing method. For example, the removing method of the substrate 110 may be performed through a laser lift off (LLO) method. That is, when a laser of a predetermined wavelength is projected on the substrate 110, heat energy is concentrated on the boundary between the substrate 110 and the first conductive type semiconductor layer 140, and the substrate 110 separates from the first conductive type semiconductor layer 140.

[78] Here, the buffer layer 120 or/and the undoped semiconductor layer 130 disposed between the substrate 110 and the first conductive type semiconductor layer 140 can be separated from the substrate 110 by injecting a wet etchant.

[79] A polishing process may be performed using an Inductively coupled Plasma/Reactive Ion Etching (ICP/RCE) method on the bottom of the first conductive type semiconductor layer 140 in which the substrate 110 is removed.

[80] The first electrode layer 171 is disposed under the first conductive type semiconductor layer 140. When the ESD voltage is applied to the first electrode layer 171, the ESD voltage is partially blocked by the insulation layers 142 in the first nitride layer 141 of the first conductive type semiconductor layer 140, tunneled through the voids 143, and dispersed by the second nitride layer 144. Therefore, the first conductive type semiconductor layer 140 can disperse and drop the ESD voltage to transmit the ESD voltage to the active layer 150, thereby minimizing damage of the

active layer 150.

[81] The embodiments of the present invention can be realized with one of a p-n structure, an n-p structure, an n-p-n structure, and a p-n-p structure. In the description of embodiments, it will be understood that when a layer (or film), region, pattern or structure is referred to as being 'on' or 'under' another layer (or film), region, pad or pattern, the terminology of 'on' and 'under' comprises both the meanings of 'directly on/under' and 'indirectly on/under'. Further, the reference about 'on' and 'under' each layer will be made on the basis of drawings. Also, the thickness of each layer in the drawings is an example, and is not limited thereto.

[82] Although embodiments have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this disclosure.

[83] More particularly, various variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

Industrial Applicability

[84] Embodiment can provide a semiconductor light emitting device.

[85] Embodiment can provide a semiconductor light emitting device variously applicable to a high speed switching device, a lighting, or a light source of a display device.

[86] Embodiment can improve reliability of a semiconductor light emitting device.

Claims

[1] A semiconductor light emitting device, comprising:
a first conductive type semiconductor layer comprising an insulation layers and a voids between the insulation layers, the insulation layers being spaced by a pre-determined interval;
an active layer on the first conductive type semiconductor layer; and
a second conductive type semiconductor layer on the active layer.

[2] The semiconductor light emitting device according to claim 1, wherein the insulation layers comprise protrusions having a random size and irregular intervals, and the voids are disposed between some protrusions of the insulation layers.

[3] The semiconductor light emitting device according to claim 1, wherein the insulation layers comprise MgN layers.

[4] The semiconductor light emitting device according to claim 1, wherein the insulation layers comprise a nitride semiconductor doped with n-type dopants and p-type dopants.

[5] The semiconductor light emitting device according to claim 1, wherein the first conductive type semiconductor layer comprises:
a first nitride layer under the insulation layer;
a second nitride layer comprising the voids on the insulation layers and the first nitride layer; and
a third nitride layer between the second nitride layer and the active layer.

[6] The semiconductor light emitting device according to claim 1, comprising a first electrode layer on the first nitride layer.

[7] The semiconductor light emitting device according to claim 1, wherein dislocation density of the second nitride layer is less than that of the first nitride layer.

[8] A semiconductor light emitting device, comprising:
a first conductive type semiconductor layer comprising a first nitride layer formed with a first electrode layer and a second nitride layer comprising a voids;
an active layer on the second nitride layer; and
a second conductive type semiconductor layer on the active layer.

[9] The semiconductor light emitting device according to claim 8, comprising an insulation layers having a predetermined interval on the first nitride layer, wherein the voids are disposed between the insulation layers.

[10] The semiconductor light emitting device according to claim 8, comprising a third nitride layer between the second nitride layer and the active layer,

wherein the first to third nitride layers comprise an n-type semiconductor layer.

[11] The semiconductor light emitting device according to claim 9, wherein the insulation layers block a voltage applied to the first nitride layer, and the second nitride layer receives the voltage of the first nitride layer through a tunneling effect of the voids.

[12] The semiconductor light emitting device according to claim 9, wherein the insulation layers comprise MgN layers having a protrusion shape, and each of the protrusions of the MgN layers has a thickness ranging from about 0.0001μm to about 1μm and a pitch ranging from about 10Å to about 3μm.

[13] A method of fabricating a semiconductor light emitting device, the method comprising:

forming a first conductive type semiconductor layer comprising an insulation layers and a voids between the insulation layers;

forming an active layer on the first conductive type semiconductor layer; and

forming a second conductive type semiconductor layer on the active layer.

[14] The method according to claim 13, wherein the forming of the first conductive type semiconductor layer comprises:

forming a first nitride layer in contact with a first electrode layer;

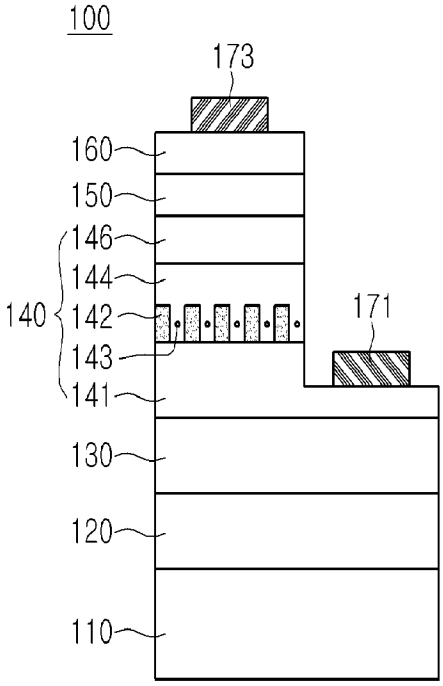
forming the insulation layers spaced by a predetermined interval on the first nitride layer;

forming the voids between the insulation layers while a second nitride layer is formed on the insulation layers and the first nitride layer; and

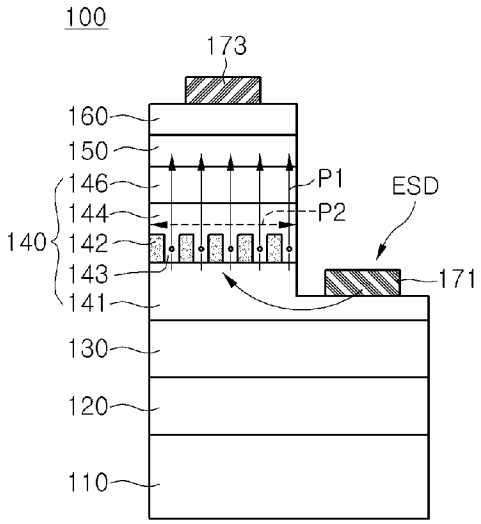
forming a third nitride layer on the second nitride layer.

[15] The method according to claim 13, wherein the insulation layers comprise MgN layers or a nitride semiconductor doped with n-type dopants and p-type dopants.

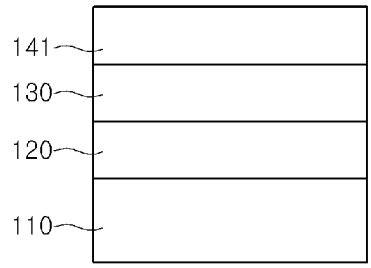
[Fig. 1]



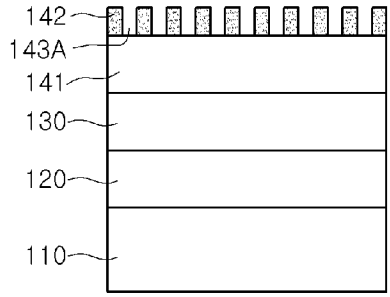
[Fig. 2]



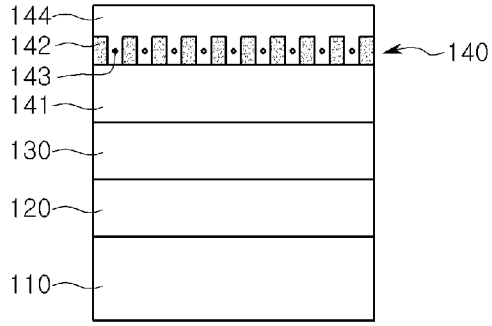
[Fig. 3]



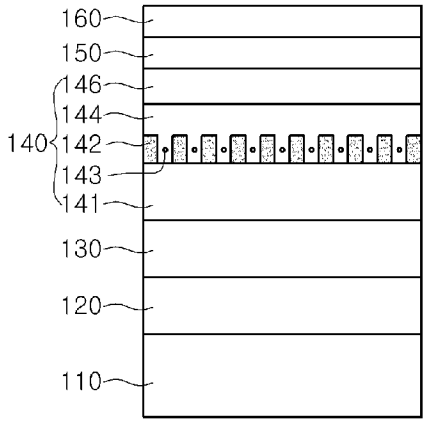
[Fig. 4]



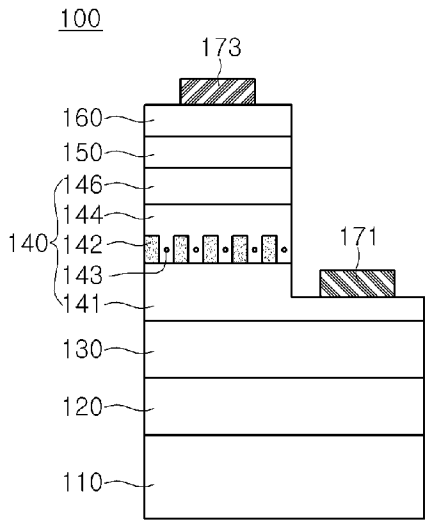
[Fig. 5]



[Fig. 6]



[Fig. 7]



[Fig. 8]