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(71) Applicant: **HUAWEI TECHNOLOGIES CO., LTD.**
[CN/CN]; Huawei Administration Building, Bantian, Long-
gang District, Shenzhen, Guangdong 518129 (CN).

(72) Inventor: **ZHOU, Libing**; Huawei Base, Bantian, Long-
gang, Shenzhen, Guangdong 518129 (CN).

(74) Agent: **LEADER PATENT & TRADEMARK FIRM**;
8F-6, Bldg. A, Winland International Center, NO. 32 Xizhi-
men North Street, Haidian District, Beijing 100082 (CN).

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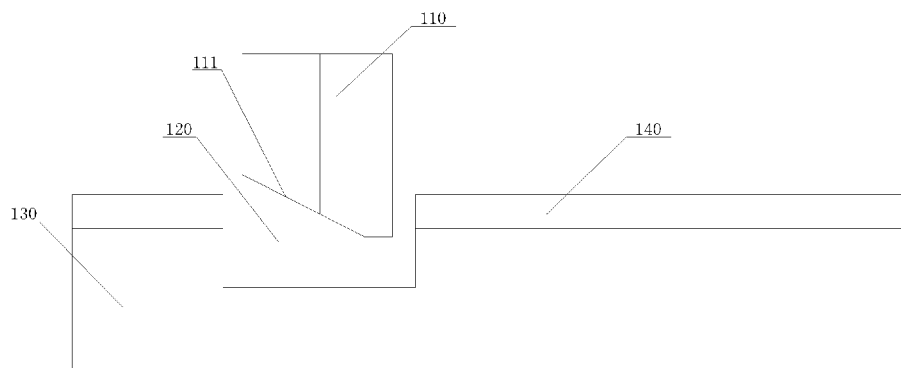


FIG. 1(a)

(57) Abstract: A system for testing a photonic integration circuit is provided in the disclosure. The system for testing the photonic integration circuit includes a first optical fiber (110) with a first end face (111), a first trench structure (120) on a wafer (130) and an edge coupler structure (140) on the photonic integration circuit. Where a first angle between an inclined section of the first end face (111) and an axial direction of the first optical fiber (110) is an acute angle. The edge coupler structure (140) is configured to receiving or transmitting an optical signal through the first optical fiber (110), and the first optical fiber (110) is located at one end of the edge coupler structure (140). Further, a normal line of the first end face (111) inclines to the edge coupler structure (140) when the first optical fiber (110) being inserted into the first trench structure (120). The technical solution of this embodiment can achieve a wafer-level test without dicing the wafer into chips or chip-bars, which further improving test efficiency and lower cost of chip. Further, a method for testing a photonic integration circuit corresponded to the system is also provided in this disclosure.



METHOD AND SYSTEM FOR TESTING PHOTONIC INTEGRATION CIRCUIT

TECHNICAL FIELD

The present disclosure relates to the optical test technology, and in particular, to a
5 method and a system for testing a photonic integration circuit.

BACKGROUND

Silicon photonics realizes optoelectronic integration and fabrication compatible with
(Complementary Metal Oxide Semiconductor) CMOS process, resulting in the unique
advantage of performance, cost, size, power consumption and mass manufacture, etc. It is the
10 development direction of optical interconnection technology, and has broad application
prospects in wide fields, such as optical network, data center, and high-performance computer.

Wafer-level testing is the foundation of the (Application Specific Integrated Circuit)
ASIC chip and CMOS industry and has a plurality of advantages. The optical chip has the
same requirements for wafer-level test to realize chip process monitoring and wafer shipment
15 and incoming material inspection.

The existing wafer-level optical chip testing technology requires that the input light and
the output light be in vertical direction of the wafer surface, which can only be realized by the
grating vertical coupling structure (Grating Coupler). However, the wafer-level optical testing
using grating vertical coupling structure has large optical coupling loss and narrow optical
20 wavelength range, and is not suitable for a plurality of silicon optical chip applications.

For silicon optical chips that require small coupling loss and wide optical operating
bandwidth, an edge coupled structure (Edge Coupler) is required, but the light of the edge
coupled structure is inside the wafer, so the optical test using edge coupled structure can only
be performed on chip level after dicing the wafer into chips or chip-bars. However, the optical

testing performed on single chip or chip-bar has low test efficiency and high cost, and cannot screen the chip before wafer dicing.

Therefore, a wafer-level optical test using edge coupled structure cannot be achieved in prior art, which has become a bottleneck in the industrialization of silicon photonics, affecting cost of chip and delivery efficiency.

SUMMARY

In view of the above, in order to overcome the problem that a wafer-level optical test using edge coupled structure cannot be achieved; the present disclosure provides a method and a system for testing photonic integration circuit.

The foregoing and other objects are achieved by the subject matter of the independent claims. Further implementation forms are apparent from the dependent claims, the description and the figures.

According to a first aspect the present disclosure relates to a method for testing a photonic integration circuit. The method includes: inserting a first optical fiber, at a first end face, into a first trench structure on a wafer; aligning a first intersection of the core of the first optical fiber and the first end face with the edge coupler structure; and performing at least one of an optical test and a photoelectric test for the photonic integration circuit using the first optic fiber. Where a first angle between an inclined section of the first end face and an axial direction of the first optical fiber is an acute angle, and after the first optical fiber is inserted into the first trench structure, a normal line of the first end face inclines to an edge coupler structure on the photonic integration circuit.

With the method for testing photonic integration circuit provided in the present disclosure, a wafer-level test using edge coupled structure might be achieved without dicing the wafer into chips or chip-bars, which further improving test efficiency and lower cost of chip.

In a first possible implementation form of the method according to the first aspect as such, the method further includes: inserting a second optical fiber, at a second end face, into the second trench structure on the wafer; aligning a second intersection of a core of the second

optical fiber and the second end face with the edge coupler structure; and performing at least one of the optical test and the photoelectric test for the photonic integration circuit using the first optic fiber in combination with the second optical fiber. Where a second angle between an inclined section of the second end face and an axial direction of the second optical fiber is an acute angle, and after the second optical fiber is inserted into the second trench structure, a normal line of the second end face inclines to the edge coupler structure.

At least one of the optical test and photoelectric test for the photonic integration circuit is performed using the first optic fiber in combination with the second optical fiber, a wafer-level test might be achieved without dicing the wafer into chips or chip-bars, which further improving test efficiency and lower cost of chip.

In a second possible implementation form of the method according to the first aspect as such or the first possible implementation form of the method, a depth of the first trench structure is 10um-100um, and the first angle ranges from 40 degrees to 50 degrees.

In a third possible implementation form of the method according to the first possible implementation form of the method, a depth of the second trench structure is 10um-100um, and the second angle ranges from 40 degrees to 50 degrees.

In a fourth possible implementation form of the method according to the first aspect as such or any one of the first to third possible implementation form of the method, where a surface of the first end face is coated with a total reflection film.

In a fifth possible implementation form of the method according to the first possible implementation form or the third possible implementation form of the method, where a surface of the second end face is coated with a total reflection film.

The total reflection film coted on the surface of the first end face and/or the total reflection film coted on the surface of the second end face increases the reflection efficiency of the first end face and/or the second end face, which further increases the intensity of the optical signal transmitted to/received from the edge coupler structure.

In a sixth possible implementation form of the method according to the first aspect as such or any one of the first to fifth possible implementation form of the method, where a cross section of the first optical fiber is an ellipse. Where the inserting a first optical fiber, at a first end face, into the first trench structure includes: inserting the first optical fiber, at the first end

face, into the first trench structure with a direction of a major axis of the ellipse is along a direction of the edge coupler structure.

In a seventh possible implementation form of the method according to the first possible implementation form or the third possible implementation form or the fifth possible implementation form of the method. Where a cross section of the second optical fiber is an ellipse; where the inserting a second optical fiber, at a second end face, into the second trench structure includes: inserting the second optical fiber, at the second end face, into the second trench structure with a direction of a major axis of the ellipse is along a direction of the edge coupler structure.

The sixth possible implementation form and the seventh possible implementation form, a light collecting ability of a surface of the first optical fiber that coupling light into the edge coupler structure is higher, and a light collecting ability of a surface of the second optical fiber that coupling light from the edge coupler structure is also higher, which thereby improves the coupling efficiency.

In an eighth possible implementation form of the method according to the first aspect as such or any one of the first to seventh possible implementation form of the method, where the method further includes forming the first trench structure on the wafer.

In a ninth possible implementation form of the method according to the first possible implementation form or the third possible implementation form or the fifth possible implementation form or the seventh possible implementation form of the method, where the method further includes forming the second trench structure on the wafer.

In a tenth possible implementation form of the method according to the first aspect as such or any one of the first to ninth possible implementation form of the method, where the aligning a first intersection of the core of the first optical fiber and the first end face with the edge coupler structure, includes: aligning the first intersection with the edge coupler structure in a horizontal direction; calculating a first relative height value of the first optical fiber according to a value of the first angle, a value of the depth of the first trench structure, and a relative height value of the edge coupler structure; and aligning the first intersection with the edge coupler structure in a vertical direction by tuning the first optical fiber according to the first relative height value.

In a eleventh possible implementation form of the method according to the first possible implementation form or the third possible implementation form or the fifth possible implementation form or the seventh possible implementation form or the ninth possible implementation form of the method, where the aligning a second intersection of a core of the second optical fiber and the second end face with the edge coupler structure includes: aligning the second intersection with the edge coupler structure in a horizontal direction; calculating a second relative height value of the second optical fiber according to a value of the second angle, a value of the depth of the second trench structure, and a relative height value of the edge coupler structure; and aligning the second intersection with the edge coupler structure in a vertical direction by tuning the second optical fiber according to the second relative height value.

According to the tenth possible implementation form and the eleventh possible implementation form, the coarse alignment of the first intersection with the edge coupler structure and the coarse alignment of the second intersection with the edge coupler structure can be achieved.

In a twelfth possible implementation form of the method according to the first aspect as such or any one of the first to eleventh possible implementation form of the method, where the method further includes aligning the first intersection with the edge coupler structure according to a value of a coupling efficiency between an inputting light and an outputting light by using an automatic search algorithm.

In a thirteenth possible implementation form of the method according to the first possible implementation form or the third possible implementation form or the fifth possible implementation form or the seventh possible implementation form or the ninth possible implementation form or the eleventh possible implementation form of the method, where the method further includes aligning the second intersection with the edge coupler structure according to a value of a coupling efficiency between an inputting light and an outputting light by using an automatic search algorithm.

According to the twelfth possible implementation form and the thirteenth possible implementation form, the fine alignment of the first intersection with the edge coupler structure and the fine alignment of the second intersection with the edge coupler structure can

be achieved.

According to a second aspect the present disclosure relates to system for testing a photonic integration circuit. The system includes a first optical fiber with a first end face, a first trench structure on a wafer and an edge coupler structure on the photonic integration circuit. Where a first angle between inclined section of the first end face and an axial direction of the first optical fiber is an acute angle, and a normal line of the first end face inclines to the edge coupler structure when the first optical fiber being inserted into the first trench structure. The edge coupler structure is configured to receiving or transmitting an optical signal through the first optical fiber, and the first optical fiber is located at one end of the edge coupler structure.

With the system for testing photonic integration circuit provided in the present disclosure, a wafer-level test might be achieved without dicing the wafer into chips or chip-bars, which further improving test efficiency and lower cost of chip.

In a first possible implementation form of the system according to the second aspect as such, the system further includes a second optical fiber with a second end face and a second trench structure on the wafer. A second angle between an inclined section of the second end face and an axial direction of the second optical fiber is an acute angle. The second trench structure is located at the other end of the edge coupler structure, and the edge coupler structure is further configured to transmitting or receiving the optical signal through the second optical fiber. A normal line of the second end face inclines to the edge coupler structure when the second optical fiber being inserted into the second trench structure.

In a second possible implementation form of the system according to the second aspect as such or first possible implementation form of the system, where a depth of the first trench structure is 10um-100um, and the first angle ranges from 40 degrees to 50 degrees.

In a third possible implementation form of the system according to first possible implementation form of the system, where a depth of the second trench structure is 10um-100um, and the second angle ranges from 40 degrees to 50 degrees.

In a fourth possible implementation form of the system according to the second aspect as such or any one of first to third possible implementation form of the system, where a surface of the first end face is coated with a total reflection film.'

In a fifth possible implementation form of the system according to first possible implementation form or third possible implementation form of the system, where a surface of the second end face is coated with a total reflection film.

5 In a sixth possible implementation form of the system according to the second aspect as such or any one of first to fifth possible implementation form of the system, where a cross section of the first optical fiber is an ellipse, and a direction of a major axis of the ellipse is along a direction of the edge coupler structure when the first optical fiber being inserted into the first trench structure.

10 In a seventh possible implementation form of the system according to first possible implementation form or third possible implementation form or fifth possible implementation form of the system, where a cross section of the second optical fiber is an ellipse, and a direction of a major axis of the ellipse is along a direction of the edge coupler structure when the second optical fiber being inserted into the second trench structure.

15 With the method or system for testing photonic integration circuit, a wafer-level test might be achieved without dicing the wafer into chips or chip-bars, which further improving test efficiency and lower cost of chip.

BRIEF DESCRIPTION OF DRAWINGS

In the drawings,

20 FIG. 1(a) is a sectional view of an example system for testing a photonic integration circuit according to an embodiment of the present disclosure;

FIG. 1(b) is a top view of an example system for testing a photonic integration circuit according to an embodiment of the present disclosure;

FIG. 2(a) is a sectional view of another example system for testing a photonic integration circuit according to an embodiment of the present disclosure;

25 FIG. 2(b) is a top view of another example system for testing a photonic integration circuit according to an embodiment of the present disclosure;

FIG. 3 is a schematic flowchart of a method for testing a photonic integration circuit according to an embodiment of the present disclosure;

FIG. 4 is a schematic flowchart of a method for testing a photonic integration circuit according to another embodiment of the present disclosure; and

FIG. 5 is a schematic flowchart of a method for testing a photonic integration circuit according to yet another embodiment of the present disclosure.

5

DESCRIPTION OF EMBODIMENTS

For the sake of clarity, several terms involved in the present disclosure will be explained in the first place.

As used herein, the term “photonic integration circuit” in the present disclosure may refer to chips on the wafer, and is the object to-be tested on the wafer, which is not limited in
10 any one of the embodiments of the present disclosure unless otherwise specified.

The term “edge coupler structure” is a structure deposited on the to-be tested photonic integration circuit, used for guiding lights in or out the photonic integration circuit, which is not limited in any one of the embodiments of the present disclosure unless otherwise specified.

15 FIG. 1(a) is a sectional view of an example system for testing a photonic integration circuit according to an embodiment of the present disclosure. FIG. 1(b) is a top view of an example system for testing a photonic integration circuit according to an embodiment of the present disclosure. As shown in FIG. 1(a) and FIG. 1(b), the system for testing a photonic integration circuit includes a first optical fiber 110 with a first end face 111, a first trench
20 structure 120 on a wafer 130 and an edge coupler structure 140 on a photonic integration circuit. Where a first angle between an inclined section of the first end face 111 and an axial direction of the first optical fiber 110 is an acute angle. The edge coupler structure 140 is configured to receiving or transmitting an optical signal through the first optical fiber 110, and the first optical fiber 110 is located at one end of the edge coupler structure 140. Further, a
25 normal line of the first end face 111 inclines to the edge coupler structure 140 when the first optical fiber 110 being inserted into the first trench structure 120.

In the embodiment illustrated in FIG. 1(a) and FIG. 1(b), at least one of the optical test and the photoelectric test for the photonic integration circuit is performed by transmitting or

receiving an optical signal through the first optical fiber 110, and by receiving or transmitting the optical signal in reverse through another optical fiber or through other existing testing probe, which is not limited in this embodiment. Since the first angle between the inclined section of the first end face 111 and the axial direction of the first optical fiber 110 is an acute angle, the edge coupler structure 140 is configured to receiving or transmitting an optical signal through the first optical fiber 110, and the first optical fiber 110 is located at one end of the edge coupler structure 140, and further the normal line of the first end face 111 inclines to the edge coupler structure 140 when the first optical fiber 110 being inserted into the first trench structure 120, the optical signal is transmitted through the first optical fiber 110 along the core of the first optical fiber 110, and being reflected by the first end face 111 into the edge coupler structure 140 when the first optical fiber 110 is an input fiber; the optical signal is received through the first optical fiber 110 along edge coupler structure 140, and being reflected by the first end face 111 into the core of the first optical fiber 110 when the first optical fiber 110 is an output optical fiber. Thereby, a wafer-level test might be achieved without dicing the wafer into chips or chip-bars, which further improving test efficiency and lower cost of chip.

FIG. 2(a) is a sectional view of another example system for testing a photonic integration circuit according to an embodiment of the present disclosure. FIG. 2(b) is a top view of another example system for testing a photonic integration circuit according to an embodiment of the present disclosure. As shown in FIG. 2(a) and FIG. 2(b), based on the system for testing photonic integration circuit shown in FIG. 1(a) and FIG. 1(b), the system for testing a photonic integration circuit further includes a second optical fiber 150 with a second end face 151, a second trench structure 160 on the wafer 130. Where a second angle between an inclined section of the second end face 151 and an axial direction of the second optical fiber 150 is an acute angle. The second trench structure 160 is located at the other end of the edge coupler structure 140, and the edge coupler structure 140 is further configured to transmitting or receiving the optical signal through the second optical fiber 150. Further, a normal line of the second end face 151 inclines to the edge coupler structure 140 when the second optical fiber 150 being inserted into the second trench structure 160. In this embodiment, at least one of the optical test and the photoelectric test for the photonic integration circuit using the first

optic fiber 110 in combination with the second optical fiber 150. The optical signal transmitted in the first optical fiber 110, the edge coupler structure 140, and the second optical fiber 150 along the direction of the arrows shown in FIG. 2(a) and FIG. 2(b). The application principle of the second optical fiber 150 is similar to that of the first optical fiber 110, which will not discuss again. Thereby, a wafer-level test might be achieved without dicing the wafer into chips or chip-bars, which further improving test efficiency and lower cost of chip.

In an embodiment, a depth of the first trench structure 120 is 10um-100um, and the first angle ranges from 40 degrees to 50 degrees; a depth of the second trench structure 160 is 10um-100um, and the second angle ranges from 40 degrees to 50 degrees. It should be understood that the depths of the first trench structure 120 and the second trench structure 160 might be the same or different, and the degrees of the first angle and the second angle might be the same or different, which is not limited in this embodiment.

It should be understood that the first trench structure 120 and/or the second trench structure 160 might be formed specifically for the wafer-level test. In another implementation, the first trench structure 120 and/or the second trench structure 160 is the trench structure already formed for other purpose, such as for dicing the chips. For example, the size of the trench structure is 500um long, 200um wide and 70um high.

In an embodiment, a surface of the first end face 111 is coated with a total reflection film, and a depth of the second trench structure is 10um-100um, and/or a surface of the second end face 151 is coated with a total reflection film. The total reflection film coted on the surface of the first end face 111 and/or the total reflection film coted on the surface of the second end face 151 increases the reflection efficiency of the first end face 111 and/or the second end face 151, which further increases the intensity of the optical signal transmitted to/received from the edge coupler structure 140.

In an embodiment, where a cross section of the first optical fiber 110 is ellipse, and a direction of a major axis of the ellipse is along a direction of the edge coupler structure 140 when the first optical fiber 110 being inserted into the first trench structure 120.

In an embodiment, where a cross section of the second optical fiber 150 is ellipse, and a direction of a major axis of the ellipse is along a direction of the edge coupler structure 140 when the second optical fiber 150 being inserted into the second trench structure 160.

It should be understood that a cross section of an optical fiber might be a circle or an ellipse, when a cross section of the first optical fiber 110 or a cross section of the second optical fiber 150 is ellipse, and the first optical fiber 110 or second optical fiber 150 is positioned with a direction of a major axis of the ellipse is along a direction of the edge coupler structure 140 when the first optical fiber 110 or the second optical fiber 150 being inserted into the second trench structure 160. In this way, a light collecting ability of a surface of the first optical fiber 110 that coupling light into the edge coupler structure 140 is higher, and a light collecting ability of a surface of the second optical fiber 150 that coupling light from the edge coupler structure 140 is also higher, which thereby improves the coupling efficiency.

FIG. 3 is a schematic flowchart of a method for testing a photonic integration circuit according to an embodiment of the present disclosure. As shown in FIG. 3, the method includes the following steps:

S301: inserting a first optical fiber, at a first end face, into a first trench structure on a wafer, where a first angle between an inclined section of the first end face and an axial direction of the first optical fiber is an acute angle, and after the first optical fiber is inserted into the first trench structure, a normal line of the first end face inclines to an edge coupler structure on the photonic integration circuit.

S302: aligning a first intersection of a core of the first optical fiber and the first end face with the edge coupler structure.

S303: performing at least one of an optical test and a photoelectric test for the photonic integration circuit using the first optic fiber.

In conjunction with FIG. 1(a) and FIG. 1(b), the first optical fiber 110 is inserted, at a first end face 111 of the first optical fiber 110, into the first trench structure 120 on a wafer 130, since the first angle between the inclined section of the first end face 111 and the axial direction of the first optical fiber 110 is an acute angle, and after the second optical fiber is inserted into the second trench structure, the normal line of the first end face 111 inclines to the edge coupler structure 140. Once the first intersection of the core of the first optical fiber 110 and the first end face 111 is aligned with the edge coupler structure 140, light inputted in the first optical fiber 110 might be coupled into the edge coupler structure 140 when the first

optical fiber 110 is an input optical fiber, or, light outputted from the first optical fiber 110 might be coupled from the edge coupler structure 140 when the first optical fiber 110 is an output optical fiber. Thereby, a wafer-level test might be achieved without dicing the wafer into chips or chip-bars, which further improving test efficiency and lower cost of chip.

5 The optical test in this embodiment involved wafer-level optical test based on automatic finding of position coordinates correspond to the first optical fiber 110 and the edge coupler structure 140, and predefined variations correspond to height of wafer. The photoelectric Test is performed in combination with an existing wafer-level electrical test system to achieve wafer-level optoelectronic testing.

10 FIG. 4 is a schematic flowchart of a method for testing a photonic integration circuit according to another embodiment of the present disclosure. As shown in FIG. 4, the method includes the following steps:

 S301: inserting a first optical fiber, at a first end face, into a first trench structure on a wafer, where a first angle between an inclined section of the first end face and the axial
15 direction of the first optical fiber is an acute angle, and after the first optical fiber is inserted into the first trench structure, a normal line of the first end face inclines to an edge coupler structure on the photonic integration circuit.

 S302: aligning a first intersection of the core of the first optical fiber and the first end face with the edge coupler structure.

20 S304: inserting a second optical fiber, at a second end face, into the second trench structure on the wafer, where a second angle between an inclined section of the second end face and an axial direction of the second optical fiber is an acute angle, and after the second optical fiber is inserted into the second trench structure, a normal line of the second end face inclines to the edge coupler structure.

25 S305: aligning a second intersection of a core of the second optical fiber and the second end face with the edge coupler structure.

 S306: performing at least one of the optical test and the photoelectric test for the photonic integration circuit using the first optic fiber in combination with the second optical fiber.

In conjunction with FIG. 2(a) and FIG. 2(b), the first optical fiber 110 is inserted, at a first end face 111 of the first optical fiber 110, into the first trench structure 120 on a wafer 130. Where the first angle between the inclined section of the first end face 111 and the axial direction of the first optical fiber 110 is an acute angle. The edge coupler structure 140 is configured to receiving or transmitting an optical signal through the first optical fiber 110, and the first optical fiber 110 is located at one end of the edge coupler structure 140. Further, the normal line of the first end face 111 inclines to the edge coupler structure 140 when the first optical fiber 110 being inserted into the first trench structure 120. Then, the second optical fiber 150 is inserted, at a second end face of the second optical fiber 150, into the second trench structure 160 on the wafer 130. Where a second angle between an inclined section of the second end face 151 and an axial direction of the second optical fiber 150 is an acute angle. The second trench structure 160 is located at the other end of the edge coupler structure 140, and the edge coupler structure 140 is further configured to transmitting or receiving the optical signal through the second optical fiber 150. Further, a normal line of the second end face 151 inclines to the edge coupler structure 140 when the second optical fiber 150 being inserted into the second trench structure 160. Once the first intersection of the core of the first optical fiber 110 and the first end face 111 is aligned with the edge coupler structure 140, and the second intersection of a core of the second optical fiber 150 and the second end face 151 is aligned with the edge coupler structure 140, at least one of the optical test and the photoelectric test for the photonic integration circuit might be performed using the first optical fiber 110 in combination with the second optical fiber 150.

It should be noted that the sequential order of the S301-S302 and the S304-S305 is not limited in this embodiment, and the S301-S302 and the S304-S305 can occur simultaneously.

In an embodiment, a depth of the first trench structure 120 is 10um-100um, and the first angle ranges from 40 degrees to 50 degrees; a depth of the second trench structure 160 is 10um-100um, and the second angle ranges from 40 degrees to 50 degrees. It should be understood that the depths of the first trench structure 120 and the second trench structure 160 might be the same or different, and the degrees of the first angle and the second angle might be the same or different, which is not limited in this embodiment.

It should be understood that the first trench structure 120 and/or the second trench structure 160 might be formed specifically for the wafer-level test. In another implementation, the first trench structure 120 and/or the second trench structure 160 is the trench structure already formed for other purpose, such as for dicing the chips. For example, the size of the trench structure is 500um long, 200um wide and 70um high.

In an embodiment, a surface of the first end face 111 is coated with a total reflection film, and a depth of the second trench structure is 10um-100um, and/or a surface of the second end face 151 is coated with a total reflection film. The total reflection film coted on the surface of the first end face 111 and/or the total reflection film coted on the surface of the second end face 151 increases the reflection efficiency of the first end face 111 and/or the second end face 151, which further increases the intensity of the optical signal transmitted to/received from the edge coupler structure 140.

In an embodiment, where a cross section of the first optical fiber 110 is ellipse, S302 includes: inserting the first optical fiber, at the first end face, into the first trench structure with a direction of a major axis of the ellipse is along a direction of the edge coupler structure.

In an embodiment, where a cross section of the second optical fiber 150 is ellipse, S305 includes: inserting the second optical fiber, at the second end face, into the second trench structure with a direction of a major axis of the ellipse is along a direction of the edge coupler structure.

It should be understood that a cross section of an optical fiber might be a circle or an ellipse, when a cross section of the first optical fiber 110 or a cross section of the second optical fiber 150 is ellipse, and if the first optical fiber 110 or second optical fiber 150 is positioned with a direction a major axis of the ellipse is along a direction of the edge coupler structure 140 when the first optical fiber 110 or the second optical fiber 150 being inserted into the second trench structure 160. In this way, a light collecting ability of a surface of the first optical fiber 110 that coupling light into the edge coupler structure 140 is higher, and a light collecting ability of a surface of the second optical fiber 150 that coupling light from the edge coupler structure 140 is also higher, which thereby improving the coupling efficiency.

In an embodiment, the method for testing photonic integration circuit further includes: forming the first trench structure on the wafer; and/or, forming the second trench structure on the wafer.

FIG. 5 is a schematic flowchart of a method for testing a photonic integration circuit according to yet another embodiment of the present disclosure. As shown in FIG. 5, the method includes the following steps:

S301: inserting a first optical fiber, at a first end face, into a first trench structure on a wafer, where a first angle between an inclined section of the first end face and the axial direction of the first optical fiber is an acute angle, and after the first optical fiber is inserted into the first trench structure, a normal line of the first end face inclines to an edge coupler structure on the photonic integration circuit.

S501: aligning the first intersection with the edge coupler structure in a horizontal direction.

S502: calculating a first relative height value of the first optical fiber according to a value of the first angle, a value of the depth of the first trench structure, and a relative height value of the edge coupler structure.

S503: aligning the first intersection with the edge coupler structure in a vertical direction by tuning the first optical fiber according to the first relative height value.

During alignment process, the first optical is fixed on the automatic fine-tuning frame firstly, the horizontal position is imaged by (Charge-coupled Device) CCD imaging or under optical microscope inspection, then the first intersection is coarsely aligned with the edge coupler structure in horizontal direction. Further, a first relative height value of the first optical fiber is calculated according to value of the first angle, value of the depth of the first trench structure, and relative height value of the edge coupler structure, the first intersection is aligned with the edge coupler structure in vertical direction by tuning the first optical fiber according to the first relative height value. In conjunction of FIG. 2(a) and FIG. 2(b), the coarse alignment of the first intersection with the edge coupler structure 140 realizes the light inputted in the first optical fiber 110 might be coupled into the edge coupler structure 140.

S504: aligning the first intersection with the edge coupler structure according to a value of a coupling efficiency result between an inputting light and an outputting light by using an automatic search algorithm.

Following coarse alignment of the first intersection with the edge coupler structure 140, a fine alignment of the first intersection with the edge coupler structure 140 is performed according to value of coupling efficiency by using an automatic search algorithm, where the coupling efficiency result includes the light loss of coupling. That is, after completion of coarse alignment, the first optical fiber 110 is tuned according to the value of coupling efficiency, which reduces the light loss of coupling.

S304: inserting a second optical fiber, at a second end face, into the second trench structure on the wafer, where a second angle between an inclined section of the second end face and the axial direction of the second optical fiber is an acute angle, and after the second optical fiber is inserted into the second trench structure, a normal line of the second end face inclines to the edge coupler structure.

S505: aligning the second intersection with the edge coupler structure in a horizontal direction.

S506: calculating a second relative height value of the second optical fiber according to a value of the second angle, a value of the depth of the second trench structure, and a relative height value of the edge coupler structure.

S507: aligning the second intersection with the edge coupler structure in a vertical direction by tuning the second optical fiber according to the second relative height value.

S508: aligning the second intersection with the edge coupler structure according to a value of a coupling efficiency between an inputting light and an outputting light by using an automatic search algorithm.

The process of S505-S508 is similar to that of S501-S504, and the coarse alignment of the second intersection with the edge coupler structure 140 realizes the light outputted in the second optical fiber 110 might be coupled from the edge coupler structure 140. After completion of coarse alignment, the second optical fiber 150 is tuned according to the value of coupling efficiency, which reduces the light loss of coupling.

S306: performing at least one of the optical test and the photoelectric test for the photonic integration circuit using the first optic fiber in combination with the second optical fiber.

It is to be understood that the disclosed systems and methods might be used for testing more than one photonic integration circuits, one method is to test the multiple photonic integration circuits at the same time using optical fiber array that consisted of more than one optical fiber disclosed in this application, another method is to move the optical fiber disclosed in this application for testing different photonic integration circuit distributed in different positions in the wafer.

It is to be understood that the singular forms “a”, “an” and “the” include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to “a device” includes reference to one or more of such devices, i.e. that there is at least one device. The terms “comprising”, “having”, “including”, “entailing” and “containing”, or verb tense variants thereof, are to be construed as open-ended terms (i.e., meaning “including, but not limited to,”) unless otherwise noted. All methods described herein might be performed in any suitable order unless otherwise indicated herein or otherwise clearly contradicted by context. The use of examples or exemplary language (e.g. “such as”) is intended merely to better illustrate or describe embodiments of the disclosure and is not intended to limit the scope of the disclosure unless otherwise claimed.

While several embodiments have been provided in the present disclosure, it should be understood that the disclosed systems and methods might be embodied in many other specific forms without departing from the scope of the present disclosure. The present examples are to be considered as illustrative and not restrictive, and the intention is not to be limited to the details given herein. For example, the various elements or components may be combined or integrated in another system or certain features may be omitted, or not implemented.

In addition, techniques, systems, subsystems, and methods described and illustrated in the various embodiments as discrete or separate may be combined or integrated with other systems, modules, techniques, or methods without departing from the scope of the present disclosure. Other items shown or discussed as coupled or directly coupled or communicating with each other may be indirectly coupled or communicating through some interface, device,

or intermediate component whether electrically, mechanically, or otherwise. Other examples of changes, substitutions, and alterations are ascertainable by one skilled in the art and could be made without departing from the inventive concept(s) disclosed herein.

CLAIMS

1. A method for testing a photonic integration circuit, comprising:

inserting a first optical fiber, at a first end face, into a first trench structure on a wafer, wherein a first angle between an inclined section of the first end face and an axial direction of the first optical fiber is an acute angle, and after the first optical fiber is inserted into the first trench structure, a normal line of the first end face inclines to an edge coupler structure on the photonic integration circuit;

aligning a first intersection of a core of the first optical fiber and the first end face with the edge coupler structure; and

performing at least one of an optical test and a photoelectric test for the photonic integration circuit using the first optic fiber.

2. The method according to claim 1, further comprising:

inserting a second optical fiber, at a second end face, into the second trench structure on the wafer, wherein a second angle between an inclined section of the second end face and an axial direction of the second optical fiber is an acute angle, and after the second optical fiber is inserted into the second trench structure, a normal line of the second end face inclines to the edge coupler structure;

aligning a second intersection of a core of the second optical fiber and the second end face with the edge coupler structure; and

performing at least one of the optical test and the photoelectric test for the photonic integration circuit using the first optic fiber in combination with the second optical fiber.

3. The method according to claim 1 or 2, wherein a depth of the first trench structure is 10um-100um, and the first angle ranges from 40 degrees to 50 degrees.

4. The method according to claim 2, wherein a depth of the second trench structure is 10um-100um, and the second angle ranges from 40 degrees to 50 degrees.

5. The method according to any one of claims 1-4, wherein a surface of the first end face is coated with a total reflection film.

6. The method according to claim 2 or 4, wherein a surface of the second end face is

coated with a total reflection film.

7. The method according to any one of claims 1-6, wherein a cross section of the first optical fiber is an ellipse;

5 wherein the inserting a first optical fiber, at a first end face, into the first trench structure comprises:

inserting the first optical fiber, at the first end face, into the first trench structure with a direction of a major axis of the ellipse is along a direction of the edge coupler structure.

8. The method according to claim 2 or 4 or 6, wherein a cross section of the second optical fiber is an ellipse;

10 wherein the inserting a second optical fiber, at a second end face, into the second trench structure comprises:

inserting the second optical fiber, at the second end face, into the second trench structure with a direction of a major axis of the ellipse is along a direction of the edge coupler structure.

9. The method according to any one of claims 1-8, further comprising:

15 forming the first trench structure on the wafer.

10. The method according to claim 2 or 4 or 6 or 8, further comprising:

forming the second trench structure on the wafer.

11. The method according to claims 1-10, wherein the aligning a first intersection of the core of the first optical fiber and the first end face with the edge coupler structure, comprises:

20 aligning the first intersection with the edge coupler structure in a horizontal direction;

calculating a first relative height value of the first optical fiber according to a value of the first angle, a value of the depth of the first trench structure, and a relative height value of the edge coupler structure; and

25 aligning the first intersection with the edge coupler structure in a vertical direction by tuning the first optical fiber according to the first relative height value.

12. The method according to claim 2 or 4 or 6 or 8 or 10, wherein the aligning a second intersection of a core of the second optical fiber and the second end face with the edge coupler structure comprises:

aligning the second intersection with the edge coupler structure in a horizontal direction;

30 calculating a second relative height value of the second optical fiber according to a value

of the second angle, a value of the depth of the second trench structure, and a relative height value of the edge coupler structure; and

aligning the second intersection with the edge coupler structure in a vertical direction by tuning the second optical fiber according to the second relative height value.

5 13. The method according to claims 1-12, further comprising:

aligning the first intersection with the edge coupler structure according to a value of a coupling efficiency between an inputting light and an outputting light by using an automatic search algorithm.

14. The method according to claim 2 or 4 or 6 or 8 or 10 or 12, further comprising:

10 aligning the second intersection with the edge coupler structure according to a value of a coupling efficiency between an inputting light and an outputting light by using an automatic search algorithm.

15. A system for testing a photonic integration circuit, comprising:

15 a first optical fiber (110) with a first end face (111), wherein a first angle between an inclined section of the first end face (111) and an axial direction of the first optical fiber (110) is an acute angle;

a first trench structure (120) on a wafer (130); and

20 an edge coupler structure (140) on the photonic integration circuit, configured to receiving or transmitting an optical signal through the first optical fiber (110), and the first optical fiber (110) is located at one end of the edge coupler structure (140), wherein a normal line of the first end face (111) inclines to the edge coupler structure (140) when the first optical fiber (110) being inserted into the first trench structure (120).

16. The system according to claim 15, further comprising:

25 a second optical fiber (150) with a second end face (151), wherein a second angle between an inclined section of the second end face (151) and an axial direction of the second optical fiber (150) is an acute angle;

a second trench structure (160) on the wafer (130), located at the other end of the edge coupler structure (140), and the edge coupler structure (140) is further configured to transmitting or receiving the optical signal through the second optical fiber (150), wherein a

normal line of the second end face (151) inclines to the edge coupler structure (140) when the second optical fiber (150) being inserted into the second trench structure (160).

17. The system according to claim 15 or 16, wherein a depth of the first trench structure (120) is 10um-100um, and the first angle ranges from 40 degrees to 50 degrees.

5 18. The system according to claim 16, wherein a depth of the second trench structure (160) is 10um-100um, and the second angle ranges from 40 degrees to 50 degrees.

19. The system according to any one of claims 5-18, wherein a surface of the first end face (111) is coated with a total reflection film.

10 20. The system according to claim 16 or 18, wherein a surface of the second end face (151) is coated with a total reflection film.

21. The system according to any one of claims 15-20, wherein a cross section of the first optical fiber (110) is an ellipse, and a direction of a major axis of the ellipse is along a direction of the edge coupler structure (140) when the first optical fiber (110) being inserted into the first trench structure (120).

15 22. The system according to claim 16 or 18 or 20, wherein a cross section of the second optical fiber (150) is an ellipse, and a direction of a major axis of the ellipse is along a direction of the edge coupler structure (140) when the second optical fiber (150) being inserted into the second trench structure (160).

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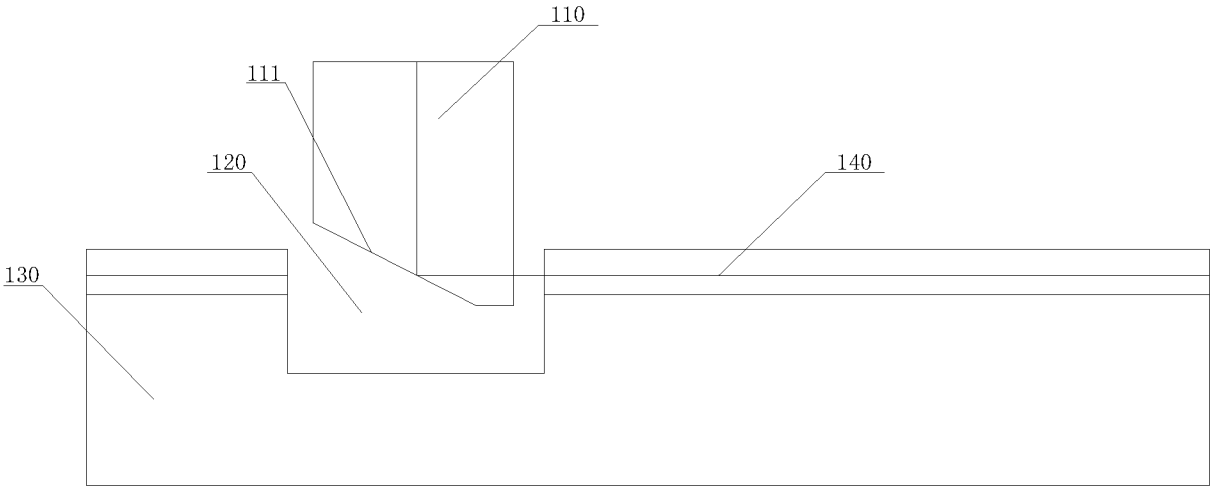


FIG. 1(a)

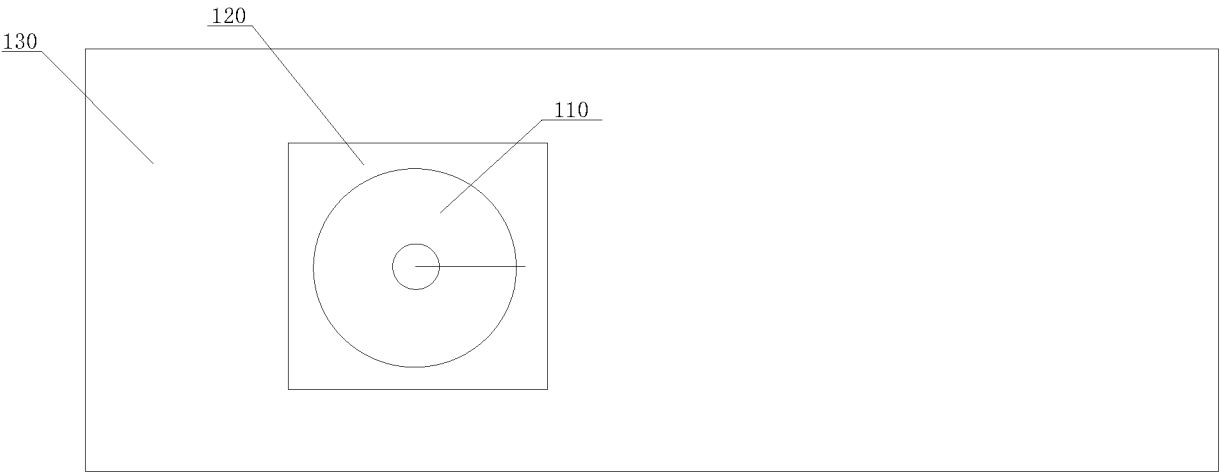


FIG. 1(b)

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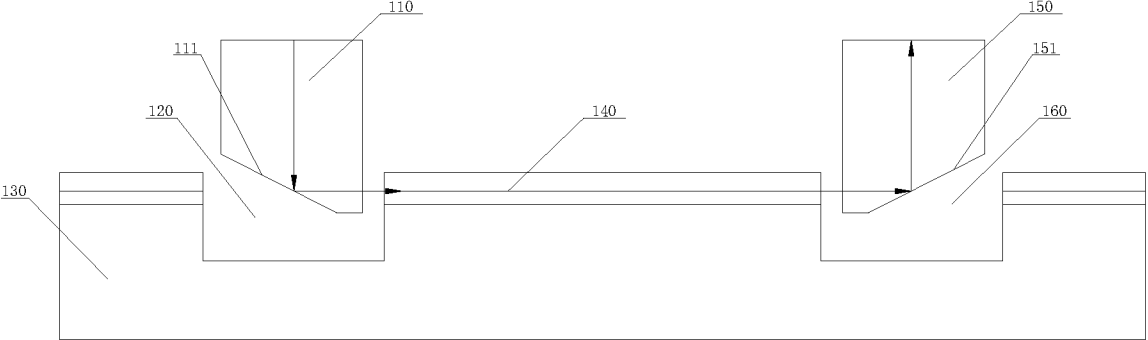


FIG. 2(a)

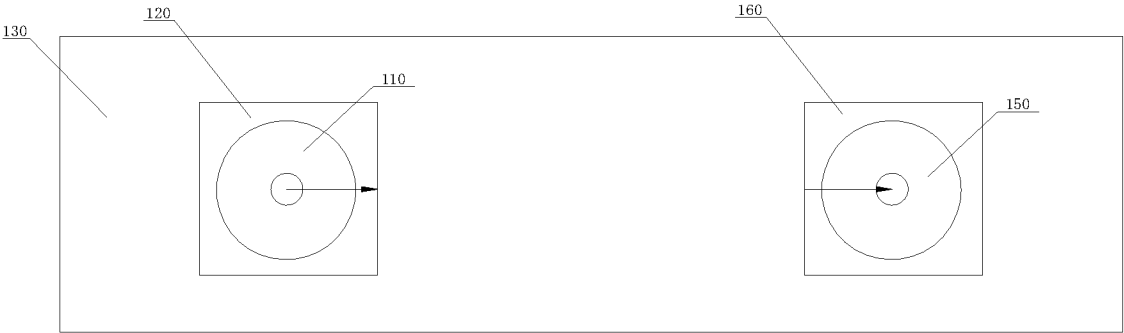


FIG. 2(b)

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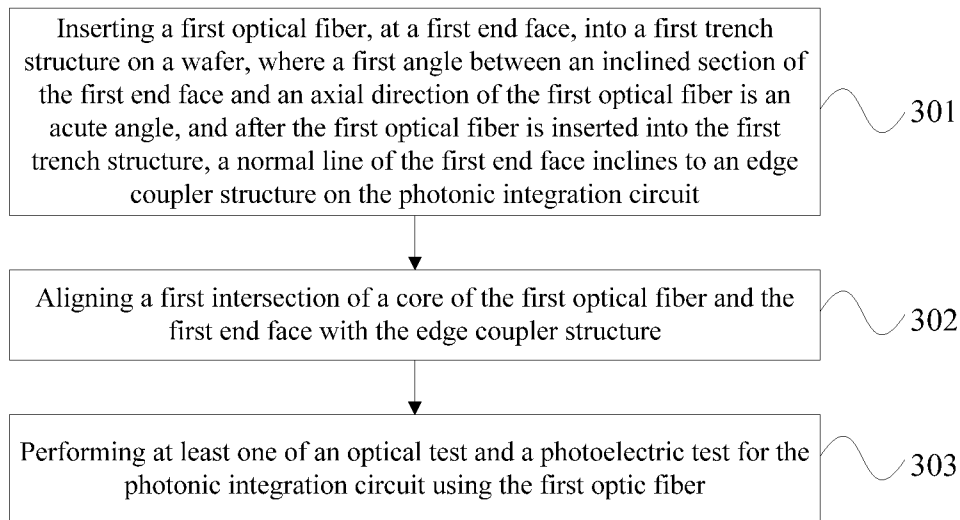


FIG. 3

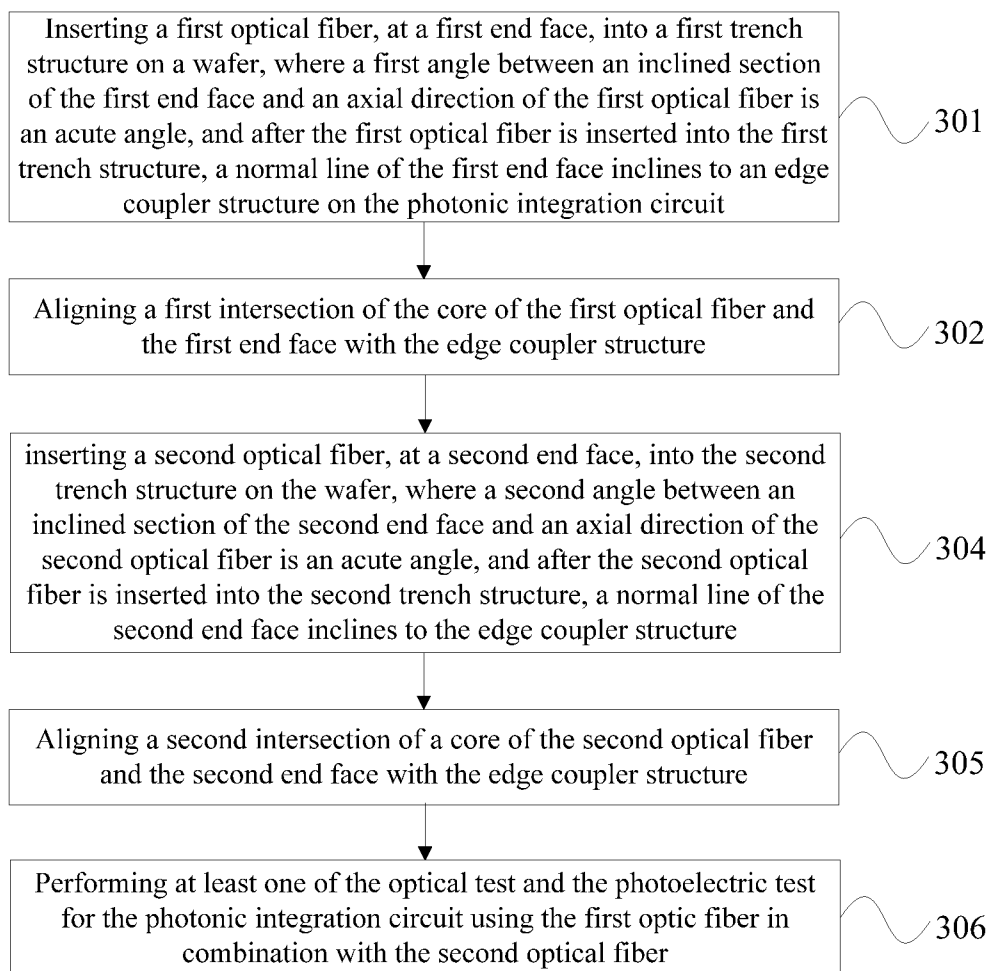


FIG. 4

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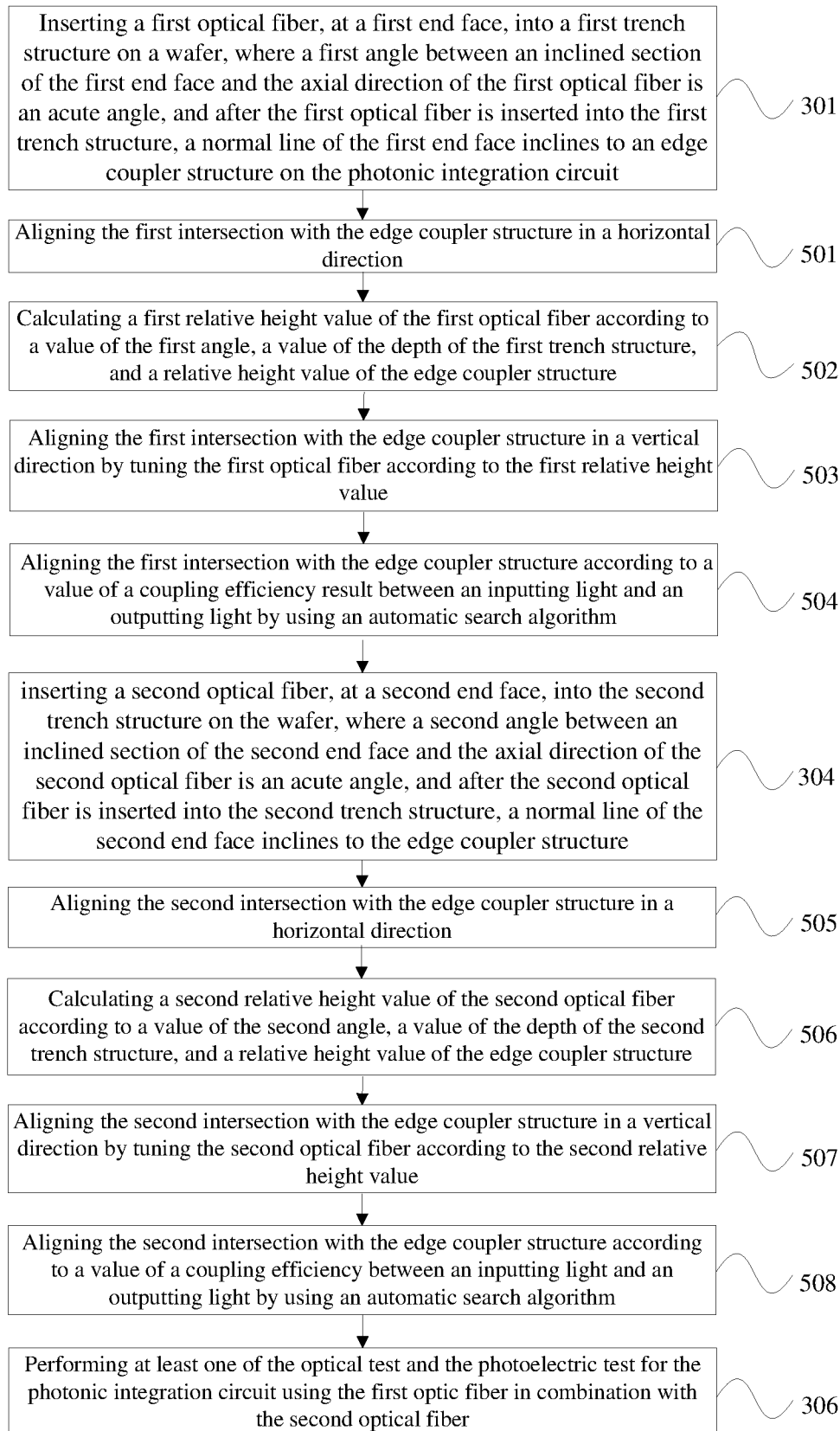


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2018/123998

A. CLASSIFICATION OF SUBJECT MATTER

G02B 6/38(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G02B, H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

VEN;CNTXT:wafer, level, test, trench, angle, reflect+, align+, fiber, coupl+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 9459177 B1 (ALCATEL-LUCENT USA INC ET AL.) 04 October 2016 (2016-10-04) description, columns 5-8, figures 1A-2A	1-22
Y	CN 106662706 A (INTELCORPORATION) 10 May 2017 (2017-05-10) description paragraphs [0051]-[0055], figure 8	1-22
A	CN 107003478 A (HUAWEI TECHNOLOGIES CO., LTD.) 017)8.1. (017)-81) The whole document	1-22

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

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“E” earlier application or patent but published on or after the international filing date

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“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

03 September 2019

Date of mailing of the international search report

18 September 2019

Name and mailing address of the ISA/CN

National Intellectual Property Administration, PRC
6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing
100088
China

Authorized officer

CUI,Xianli

Facsimile No. (86-10)62019451

Telephone No. 86- (010) -62412117

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2018/123998

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				EP	3170041	A4	30 May 2018
				EP	3170041	A1	24 May 2017
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				KR	20170009912	A	25 January 2017
				US	9709734	B2	18 July 2017
				US	9348099	B2	24 May 2016
				US	2016209589	A1	21 July 2016
				SG	11201610604R	A	27 January 2017
				WO	2016010612	A1	21 January 2016
				US	2016018610	A1	21 January 2016
				DE	112015003335	T5	04 May 2017
CN	107003478	A	01 August 2017	US	2017343734	A1	30 November 2017
				US	10215919	B2	26 February 2019
				EP	3091380	A1	09 November 2016
				WO	2016176982	A1	10 November 2016