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THIN FILM RESISTOR INTEGRATED INTO LOCAL INTERCONNECT PRODUCTION

Technical Field

[0001] Embodiments of the invention are in the field of semiconductor devices and, in particular, thin film resistors.

Background

[0002] As discussed more fully in U.S. Patent Application Publication No. 2007/0218685 (assigned to Intel Corp. of Santa Clara, California, USA), Metal-oxide-semiconductor (MOS) transistors, such as MOS field effect transistors (MOSFET), are commonly used in the manufacture of integrated circuits. A conventional MOS transistor includes a gate stack formed atop a semiconductor substrate. The gate stack generally consists of a conductive metal or polysilicon layer formed on an insulating oxide layer. The gate stack is flanked by two diffusion regions, also known as a source region and a drain region. The diffusion regions are regions within the semiconductor substrate (possibly located in a fin formed from the substrate) that have been implanted with dopants such as boron, aluminum, phosphorous, arsenic, or antimony. Between the source and drain regions, directly subjacent to the gate stack, is a channel region. Typically, three electrical contacts are made to the MOS transistor. Two contacts are made to the two diffusion regions (i.e., one to the source region and one to the drain region) and one contact is made to the gate stack.

[0003] As discussed more fully in U.S. Patent Application Publication No. 2006/0176145 (assigned to Intel Corp. of Santa Clara, California, USA), transistors such as those described above are included in electronic devices that are continuously scaled smaller and smaller. This typically means that the electronic components that make up these devices, such as microelectronic packages (which include the aforementioned transistors), must also become smaller in terms of vertical thickness and horizontal area. These microelectronic packages commonly include a die that is coupled to a supporting substrate. One approach to making such packages smaller is to embed passive components such as resistors into metallization (M) layers of the “backend” of a device. One such embedded resistor is the thin-film resistor (TFR), which may be thin and have a thickness of less than or

equal to about 1 μm . As used herein, a TFR is formed using a thin film deposition process, which may include a vacuum based process such as sputtering, chemical vapor deposition (CVD), or atomic layer deposition (ALD). In addition to freeing up surface space, these TFRs may have the added advantage of better stability and electrical performance (less overshooting, ringing, and crosstalk). Also, a TFR has a benefit of good thickness control as well as better resistance variation compared to other resistor structures that require a recess etch (e.g., polysilicon resistors).

[0004] Including the above mentioned transistors and TFRs in aggressively scaled, reliable, cost effective electronic systems is a continuing challenge for electronic system designers.

Brief Description of the Drawings

[0005] Features and advantages of embodiments of the present invention will become apparent from the appended claims, the following detailed description of one or more example embodiments, and the corresponding figures. Where considered appropriate, reference labels have been repeated among the figures to indicate corresponding or analogous elements.

[0006] Figure 1 includes a conventional thin film resistor located in a backend of a device.

[0007] Figure 2 includes a thin film resistor (TFR) located in a frontend of a device in an embodiment.

[0008] Figure 3 includes a top view of a TFR and fins in an embodiment.

[0009] Figures 4(a)-(d) include a process for forming a TFR in a frontend of a device in an embodiment.

[0010] Figure 5 includes a process in an embodiment.

[0011] Figures 6, 7, and 8 depict systems that include embodiments of TFRs described herein.

Detailed Description

[0012] Reference will now be made to the drawings wherein like structures may be provided with like suffix reference designations. In order to show the structures of various embodiments more clearly, the drawings included herein are diagrammatic

representations of semiconductor/circuit structures. Thus, the actual appearance of the fabricated integrated circuit structures, for example in a photomicrograph, may appear different while still incorporating the claimed structures of the illustrated embodiments. Moreover, the drawings may only show the structures useful to understand the illustrated embodiments. Additional structures known in the art may not have been included to maintain the clarity of the drawings. For example, not every layer of a semiconductor device is necessarily shown. “An embodiment”, “various embodiments” and the like indicate embodiment(s) so described may include particular features, structures, or characteristics, but not every embodiment necessarily includes the particular features, structures, or characteristics. Some embodiments may have some, all, or none of the features described for other embodiments. “First”, “second”, “third” and the like describe a common object and indicate different instances of like objects are being referred to. Such adjectives do not imply objects so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner. “Connected” may indicate elements are in direct physical or electrical contact with each other and “coupled” may indicate elements co-operate or interact with each other, but they may or may not be in direct physical or electrical contact.

[0013] As mentioned above, thin film resistors may be included in M layers of the “backend” of the device. Such film resistors may couple to the above mentioned contacts that couple to the gate, source, and/or drain nodes of transistors.

[0014] Regarding the “backend”, once semiconductor wafers are prepared, a large number of process steps are still necessary to produce desired semiconductor integrated circuits. In general the steps can be grouped into four areas: Frontend Processing, Backend Processing, Test, and Packaging. Frontend and backend processing are pertinent to embodiments and are therefore described below.

[0015] Frontend processing refers to the initial steps in device fabrication. In this stage the actual semiconductor devices (e.g., transistors) are created. A typical front end (also referred to herein as “frontend”) process includes: preparation of the wafer surface (e.g., fin formation), patterning and subsequent implantation of dopants to

obtain desired electrical properties, growth or deposition of a gate dielectric, and growth or deposition of insulating materials to isolate neighboring devices.

[0016] Once the semiconductor devices have been created they must be interconnected to form the desired electrical circuits. This "Back End Processing" (BEOL) of the back end (also referred to herein as "backend") involves depositing various layers of metal (sometimes referred to herein as M layers used to form traces, bit lines, word lines, and the like) and insulating material (sometimes referred to herein as V layers because such layers often include vias) in the desired pattern. Typically the metal layers consist of aluminum, copper, and the like. The insulating material may include SiO₂, low-K materials, and the like. The various metal layers are interconnected by etching holes, called "vias", in the insulating material and depositing metal (e.g., Tungsten) in them. Thus, a backend portion may include, for example, 12 metal layers: a bottom metal layer (M0), a top metal layer (M11), and a plurality of metal layers (M1, M2, M3, M4, M5, M6, M7, M8, M9, and/or M10) between the bottom and top metal layers. The "bottom metal layer" is so named because the backend portion includes no metal layer between the bottom metal layer and a top of the frontend portion. The "top metal layer" is so named because the backend portion includes no metal layer between the top metal layer and the top of the backend portion. Having 12 metal layers is just an example and backend portions may include more (e.g., 14, 16, 18, 20 or more) or less (e.g., 4, 6, 8) metal layers.

[0017] Figure 1 depicts a conventional TFR in a backend M layer. As mentioned above, a typical location to place a TFR is in between routing layers (i.e., M layers). The contact to the TFR is made with a via.

[0018] In Figure 1, substrate 101 includes fins 102, 103, 104, 105 for polygate FinFET devices. A FinFET is a transistor built around a thin strip of semiconductor material (referred to as the "fin"). The transistor includes the standard field effect transistor (FET) nodes/components: a gate, a gate dielectric, a source region, and a drain region. The conductive channel of the device resides on the outer sides of the fin beneath the gate dielectric. Specifically, current runs along both "sidewalls" of the fin as well as along the top side of the fin. Because the conductive channel

essentially resides along the three different outer, planar regions of the fin, such a FinFET is typically referred to as a “tri-gate” FinFET. Other types of FinFETs exist (such as “double-gate” FinFETs in which the conductive channel principally resides only along both sidewalls of the fin and not along the top side of the fin).

[0019] Trench-shaped electrical contacts (TCN) 107, 108 include, for example, electrical connections to diffusion regions (e.g., a source region and a drain region). Contacts 109, 110 are also TCNs. Therefore, unlike contacts 107, 108, contacts 109, 110 illustrate that not all TCNs comprise diffusion contacts. If there is no diffusion contact (e.g., contacts 109, 110), the TCN may be considered a “dummy TCN”. A contact for a gate may be referred to as a GCN (not shown in Figure 1). TCNs maximize the surface area in contact with, for example, the diffusion regions and therefore reduce electrical resistance relative to conventional round contacts. Interlayer dielectric (ILD) 113 and etchstop 106 are also shown in frontend 121.

[0020] In some cases, the frontend may include a local interconnect. Unlike global interconnects that connect separate devices to one another in backend 122 (possibly across several metal layers), local interconnects connect diffusions or gates. For example, a gate or source/drain of a single transistor may be connected to other gates or source/drains by a local interconnect in front end 121. As another example, a gate or TCN of a first transistor may connect to a transistor node of a second transistor by a local interconnect in front end 121. TFR 114, in contrast to local interconnects, is not located in the frontend 121 of conventional device 100. Instead, TFR 114 is included in backend 122 along with ILD 111. Additional ILD 111' is included in metal layer 112, which includes interconnects 115, 116. Via 117 connects to TFR 114. Via 117 is included in additional ILD 111". Vias 118, 119 couple interconnects (e.g., interconnect lines 115, 116) from layer 112 to frontend 121.

[0021] In contrast to the conventional device of Figure 1, Figure 2 includes an embodiment of the invention that comprises a TFR in the frontend of a device, instead of or in addition to TFRs included in the backend of the device.

[0022] Specifically, Figure 2 depicts TFR 214 in frontend 221. Substrate 201 includes fins 202, 203, 204, 205 for FinFET devices. TCNs 207, 208 include electrical connections to the diffusion regions (e.g., a source region and a drain region) of MOS transistors. Other contacts 209, 210, ILD 213, and etchstop 206, 225 are also shown in frontend 221. Contacts 209, 210 may couple to planar transistors and the like not specifically illustrated. Vias 218, 219, 220 couple interconnects (e.g., interconnect lines) from an above M layer (not shown), through ILD 211 of backend 222, to frontend 221. TFR 214 is directly between and in direct contact with etchstop 225 and ILD 213 in an embodiment but may only be in direct contact with one or neither of etchstop 225 and ILD 213 in other embodiments.

[0023] Figure 3 includes a top view of a TFR and fins in an embodiment. Figure 3 depicts TFR 314 and fins 302, 303, 304, 305 for FinFET devices. TCNs 307, 308 include electrical connections to diffusion regions (e.g., source or drain regions). Gate contacts 391 are also shown while other TCNs for source and drain nodes are not shown for purposes of clarity. Other contacts 309, 310, 392 are also shown. A vertical plane coming “out of the page” along horizontal axis 380 intersects TCNs 307, 308 as well as TFR 413.

[0024] Figures 4(a)-(d) include a process for forming a TFR in a frontend of a device in an embodiment. These figures are viewed along a cross-section taken along axis 380 of Figure 3 (where axis 380 cuts along TCNs 307, 308). In Figure 4(A) the TCN region and other contact regions are defined by patterning and are covered with etch stop material 406 over fins 402, 403, 404, 405. Also shown is ILD 413 and substrate 401. In Figure 4(b) the TCN end-to-end region and TFR region are opened and oxide is exposed where etch stop 406 is not shown. A dry etch recesses the oxide 413 in the non-TCN regions and the etch stop is removed afterwards. A TFR material (e.g., polysilicon or a metal) is deposited and patterned, such that TFR 414 only remains at the selected recess region. In Figure 4(C) etch stop material 425 is deposited and planarized. The etch stop material 425 only remains in the recessed regions. In Figure 4(D) an oxide dry etch removes the oxide in the TCN and contact regions and the vacated areas are backfilled with contact metal to form TCNs 407, 408, and contacts 409, 410 (contacts 409, 410 may be

TCNs for transistors not illustrated in Figure 4D). After TCN planarization and recess, a hardmask etchstop 406 is formed on top of the TCNs 407, 408 and contacts 409, 410. The TCN hardmask material is selected to prevent the gate contact from shorting to TCNs. The TCN hardmask material (material 406) can be the same material as the etch stop material (material 425) used in Figure 4(C). Afterwards, the device of Figure 2 is produced whereby the vias 218, 219, 220 to the TCNs 207, 208 and TFR 214 are formed.

[0025] Since the TCN hardmask 406 and the etch stop 425 are the same material (in an embodiment), vias to TCNs 207, 208 and TFR 214 can be formed in the same step. In other words, the TFR is integrated into local interconnect production because interconnects (e.g., vias 218, 219, 220) for both the TCNs 207, 208 and the TFR 214 are all made at the same time and using the same material in an embodiment. This simultaneous processing (in an embodiment) of these vias has process advantages regarding time savings for device manufacture.

[0026] Further, integrating the TFR production with local interconnect production allows for using the same material for vias for both the TFR and TCNs. In other words, locating the TFR in the frontend allows for using a certain material for a TFR via (e.g., cobalt) that is also being used for connecting to a local interconnect (e.g., TCN). Routing metal (e.g., interconnect line in a trench) and via metal for the local interconnect and lower layers usually use materials with lower electron migration properties because of their aggressive scaling (i.e., to maintain adequate current density when scaled smaller electron migration needs to be limited) compared to global interconnects. In a typical TFR application (e.g., a TFR operatively coupled to an input/output (I/O) node), a high DC current may be needed for circuit functionality. Contacting such a TFR with via materials having good electron migration properties would be beneficial for device reliability (i.e., as current levels increase the need to maintain adequate current density becomes more difficult). Thus, a TFR that is accessed with a via (e.g., which has low electron migration needs due to high current requirements of an I/O node) that uses the same low electron migration material as other vias (which also have low electron migration needs) is a benefit produced by integrated TFR via formation with local interconnect via formation. Such a TFR

would have superior reliability properties compared to typical TFRs placed in between routing layers in the backend.

[0027] Dielectric layer 213 may be formed from materials such as silicon dioxide or carbon doped oxide. In some implementations, the dielectric layer 213 may be formed from materials such as silicon nitride, organic polymers such as perfluorocyclobutane and polytetrafluoroethylene, organosilicate glass, fluorosilicate glass (FSG), organosilicates such as silsesquioxane, and siloxane.

[0028] When the trench openings are exposed to form TCNs 207, 208 and/or local interconnects 209, 210, a metallization process may be carried out to fill the trench openings with a suitable metal to form electrical contacts to the diffusion regions and gate stacks. Metallization processes such as CVD, plasma enhanced chemical vapor deposition (PECVD), PVD, sputter deposition, ALD, electroplating, electroless plating, or a combination of any of these processes, may be used to deposit one or more layers of metal in the trench openings.

[0029] Metals that may be used for the metallization of TCNs 207, 208, contacts 209, 210, and/or vias 218, 219, 220 include, but are not limited to, copper, ruthenium, palladium, platinum, cobalt, nickel, ruthenium oxide, tungsten, aluminum, titanium, tantalum, titanium nitride, tantalum nitride, hafnium, zirconium, a metal carbide, a conductive metal oxide, or combinations of the above.

[0030] The metal layer that forms TCNs 207, 208 and/or contacts 209, 210 may consist of multiple layers of metals. For instance, in one implementation, a first metal layer may consist of a seed layer, such as a copper seed layer or a noble metal catalyst layer, and a second metal layer may consist of a bulk metal layer such as copper. In further implementations, the various metal layers may provide various functionality, such as barrier layers, adhesion layers, and capping layers.

[0031] Figure 5 includes a method 500 comprising: forming a fin on a substrate and forming source and drain nodes in the fin (block 505); forming an insulative layer on the fin on the substrate (block 510); removing a portion of the insulative layer to form a recess (block 515); forming a TFR in the recess (block 520); forming a contact coupled to one of the source and drain nodes (block 525);

and forming a first via coupled to the contact and a second via coupled to the TFR (block 530); forming a bottom metallization (M) layer over the first and second vias (block 535); and forming additional M layers above the bottom M layer (block 540).

[0032] Various embodiments include a semiconductive substrate. Such a substrate may be a bulk semiconductive material this is part of a wafer. In an embodiment, the semiconductive substrate is a bulk semiconductive material as part of a chip that has been singulated from a wafer. In an embodiment, the semiconductive substrate is a semiconductive material that is formed above an insulator such as a semiconductor on insulator (SOI) substrate. In an embodiment, the semiconductive substrate is a prominent structure such as a fin that extends above a bulk semiconductive material.

[0033] Referring now to Figure 6, shown is a block diagram of an example system with which embodiments can be used. As seen, system 900 may be a smartphone or other wireless communicator or any other internet of things (IoT) device. A baseband processor 905 is configured to perform various signal processing with regard to communication signals to be transmitted from or received by the system. In turn, baseband processor 905 is coupled to an application processor 910, which may be a main CPU of the system to execute an OS and other system software, in addition to user applications such as many well-known social media and multimedia apps. Application processor 910 may further be configured to perform a variety of other computing operations for the device.

[0034] In turn, application processor 910 can couple to a user interface/display 920 (e.g., touch screen display). In addition, application processor 910 may couple to a memory system including a non-volatile memory, namely a flash memory 930 and a system memory, namely a DRAM 935. In some embodiments, flash memory 930 may include a secure portion 932 in which secrets and other sensitive information may be stored. As further seen, application processor 910 also couples to a capture device 945 such as one or more image capture devices that can record video and/or still images.

[0035] A universal integrated circuit card (UICC) 940 comprises a subscriber identity module, which in some embodiments includes a secure storage 942 to store

secure user information. System 900 may further include a security processor 950 (e.g., Trusted Platform Module (TPM)) that may couple to application processor 910. A plurality of sensors 925, including one or more multi-axis accelerometers may couple to application processor 910 to enable input of a variety of sensed information such as motion and other environmental information. In addition, one or more authentication devices 995 may be used to receive, for example, user biometric input for use in authentication operations. Such an input device may use a TFR embodiment described herein.

[0036] As further illustrated, a near field communication (NFC) contactless interface 960 is provided that communicates in a NFC near field via an NFC antenna 965. While separate antennae are shown, understand that in some implementations one antenna or a different set of antennae may be provided to enable various wireless functionalities.

[0037] A power management integrated circuit (PMIC) 915 couples to application processor 910 to perform platform level power management. To this end, PMIC 915 may issue power management requests to application processor 910 to enter certain low power states as desired. Furthermore, based on platform constraints, PMIC 915 may also control the power level of other components of system 900.

[0038] To enable communications to be transmitted and received such as in one or more IoT networks, various circuitry may be coupled between baseband processor 905 and an antenna 990. Specifically, a radio frequency (RF) transceiver 970 (which may also use TFRs described herein) and a wireless local area network (WLAN) transceiver 975 may be present. In general, RF transceiver 970 may be used to receive and transmit wireless data and calls according to a given wireless communication protocol such as 3G or 4G wireless communication protocol such as in accordance with a code division multiple access (CDMA), global system for mobile communication (GSM), long term evolution (LTE) or other protocol. In addition a GPS sensor 980 may be present, with location information being provided to security processor 950 for use as described herein when context information is to be used in a pairing process. Other wireless communications such as receipt or transmission of radio signals (e.g., AM/FM) and other signals may also be provided. In addition, via

WLAN transceiver 975, local wireless communications, such as according to a Bluetooth™ or IEEE 802.11 standard can also be realized.

[0039] Referring now to Figure 7, shown is a block diagram of a system in accordance with another embodiment of the present invention. Multiprocessor system 1000 is a point-to-point interconnect system such as a server system, and includes a first processor 1070 and a second processor 1080 coupled via a point-to-point interconnect 1050. Each of processors 1070 and 1080 may be multicore processors such as SoCs, including first and second processor cores (i.e., processor cores 1074a and 1074b and processor cores 1084a and 1084b), although potentially many more cores may be present in the processors. In addition, processors 1070 and 1080 each may include a secure engine 1075 and 1085 to perform security operations such as attestations, IoT network onboarding or so forth.

[0040] First processor 1070 further includes a memory controller hub (MCH) 1072 and point-to-point (P-P) interfaces 1076 and 1078. Similarly, second processor 1080 includes a MCH 1082 and P-P interfaces 1086 and 1088. MCH's 1072 and 1082 couple the processors to respective memories, namely a memory 1032 and a memory 1034, which may be portions of main memory (e.g., a DRAM) locally attached to the respective processors. First processor 1070 and second processor 1080 may be coupled to a chipset 1090 via P-P interconnects 1052 and 1054, respectively. Chipset 1090 includes P-P interfaces 1094 and 1098.

[0041] Furthermore, chipset 1090 includes an interface 1092 to couple chipset 1090 with a high performance graphics engine 1038, by a P-P interconnect 1039. In turn, chipset 1090 may be coupled to a first bus 1016 via an interface 1096. Various input/output (I/O) devices 1014 (which may use a TFR embodiment described herein) may be coupled to first bus 1016, along with a bus bridge 1018 which couples first bus 1016 to a second bus 1020. Various devices may be coupled to second bus 1020 including, for example, a keyboard/mouse 1022, communication devices 1026 and a data storage unit 1028 such as a non-volatile storage or other mass storage device. As seen, data storage unit 1028 may include code 1030, in one embodiment. As further seen, data storage unit 1028 also includes a trusted

storage 1029 to store sensitive information to be protected. Further, an audio I/O 1024 may be coupled to second bus 1020.

[0042] Embodiments may be used in environments where IoT devices may include wearable devices or other small form factor IoT devices. Referring now to Figure 8, shown is a block diagram of a wearable module 1300 in accordance with another embodiment. In one particular implementation, module 1300 may be an Intel® Curie™ module that includes multiple components adapted within a single small module that can be implemented as all or part of a wearable device. As seen, module 1300 includes a core 1310 (of course in other embodiments more than one core may be present). Such core may be a relatively low complexity in-order core, such as based on an Intel Architecture® Quark™ design. In some embodiments, core 1310 may implement a TEE as described herein. Core 1310 couples to various components including a sensor hub 1320, which may be configured to interact with a plurality of sensors 1380, such as one or more biometric, motion environmental or other sensors. A power delivery circuit 1330 is present, along with a non-volatile storage 1340. In an embodiment, this circuit may include a rechargeable battery and a recharging circuit, which may in one embodiment receive charging power wirelessly. One or more input/output (IO) interfaces 1350, such as one or more interfaces compatible with one or more of USB/SPI/I2C/GPIO protocols, may be present. In addition, a wireless transceiver 1390, which may be a Bluetooth™ low energy or other short-range wireless transceiver is present to enable wireless communications as described herein. Understand that in different implementations a wearable module can take many other forms. Wearable and/or IoT devices have, in comparison with a typical general purpose CPU or a GPU, a small form factor, low power requirements, limited instruction sets, relatively slow computation throughput, or any of the above.

[0043] The following examples pertain to further embodiments.

[0044] Example 1 includes an apparatus comprising: a fin based field effect transistor (FinFET) comprising a source, a drain, and a gate; a contact coupled to at least one of the source, the drain, and the gate; a thin film resistor (TFR); a first via coupled to the contact and a second via coupled to the TFR; and a bottom

metallization (M) layer and additional M layers above the bottom M layer; wherein the TFR and the first and second vias are all below the bottom M layer.

[0045] For instance, contact 207 may couple to a source or drain in or on fin 205. The source or drain may be doped within the fin and/or located in an epitaxial formation on the fin. Also, bottom M layer may include layer 222. The first and second vias may extend from the bottom M layer to below the bottom M layer and into the front end 221. Thus, vias being below an M layer indicate they extend (fully or partially) below the M layer.

[0046] Example 2 includes the apparatus of example 1 wherein: there are no other M layers between the TFR and the bottom M layer; and a horizontal plane intersects the first and second vias.

[0047] For instance, axis 280 may define a plane going into the page that intersects vias 218 and 220.

[0048] Example 3 includes the apparatus of example 2 wherein the first and second vias each include cobalt.

[0049] Example 4 includes the apparatus of example 3 comprising an interlayer dielectric that directly contacts the contact and directly contacts the TFR.

[0050] For example, ILD 213 contacts the bottom of the TFR and a side of contact 207.

[0051] Example 5 includes the apparatus of example 3, wherein the first via directly contacts the contact, the second via directly contacts the TFR, and the contact is a trench contact (TCN).

[0052] A via may “directly contact” the contact despite the presence of a barrier layer, seed layer, and the like between the plug of the via and the contact.

[0053] Example 6 includes an apparatus comprising: a frontend comprising: (a)(i) a fin based field effect transistor (FinFET) comprising a source, a drain, and a gate; (a)(ii) a contact coupled to at least one of the source, drain, and gate; (a)(iii) a first via coupled to the contact; (a)(iv) a thin film resistor (TFR), and (a)(v) a second via

coupled to the TFR; and a backend comprising a bottom metallization (M) layer and additional M layers; wherein (b)(i) there are no other M layers between the frontend and the bottom M layer, and (b)(ii) the TFR and the first and second vias are all below the bottom M layer.

[0054] Example 7 includes the apparatus of example 6 wherein a horizontal plane, which is parallel to a long axis of the substrate, intersects the first and second vias.

[0055] Example 8 includes the apparatus of example 7 wherein the first via includes a metal and the second via also includes the metal.

[0056] Example 9 includes the apparatus of example 7 wherein the first and second vias each include cobalt.

[0057] Example 10 includes the apparatus of example 6 comprising an interlayer dielectric that directly contacts the contact and directly contacts the TFR.

[0058] Example 11 includes the apparatus of example 10 wherein the TFR directly contacts etchstop material.

[0059] Example 12 includes the apparatus of example 10 comprising an input/output (I/O) node that includes the TFR.

[0060] Example 13 includes the apparatus of example 11 wherein the TFR includes a bottom plane that is generally parallel to a long axis of the substrate and at least one sidewall that is generally orthogonal to the long axis of the substrate.

[0061] For instance, see area 281.

[0062] Example 14 includes the apparatus of example 11 wherein the contact couples to at least one of the source and the drain.

[0063] Example 15 includes the apparatus of example 11 wherein the contact is a trench contact and the TFR is less than 1 μm thick vertically.

[0064] Example 16 includes a method comprising: forming a fin on a substrate and forming source and drain nodes in the fin; forming an insulative layer on the fin and on the substrate; removing a portion of the insulative layer to form a recess; forming

a thin film resistor (TFR) in the recess; forming a contact coupled to one of the source and drain nodes; and forming a first via coupled to the contact and a second via coupled to the TFR; forming a bottom metallization (M) layer over the first and second vias; and forming additional M layers above the bottom M layer; wherein the TFR and the first and second vias are all below the bottom M layer.

[0065] Example 17 includes the method of example 16, wherein: there are no other M layers between the TFR and the bottom M layer; and a horizontal plane intersects the first and second vias.

[0066] Example 18 includes the method of example 17 wherein the first and second vias each include cobalt.

[0067] Example 19 includes the method of example 18 wherein the insulative layer directly contacts the contact and directly contacts the TFR.

[0068] Example 20 includes the method of example 19, wherein the first via directly contacts the contact and the second via directly contacts the TFR.

[0069] Example 1a includes an apparatus comprising: a substrate; a fin-based field effect transistor (FinFET), on the substrate, comprising a source, a drain, and a gate; a contact coupled to at least one of the source, the drain, and the gate; a thin film resistor (TFR); a first via coupled to the contact and a second via coupled to the TFR; and a bottom metallization (M) layer, including an interconnect line located in a trench, and additional M layers above the bottom M layer; wherein the TFR and the first and second vias are all between the bottom M layer and the substrate.

[0070] For instance, the bottom layer including a trench having an interconnect line would not include a layer simply having a via or a contact for a transistor node. In an embodiment, the interconnect line is formed using damascene or dual damascene techniques.

[0071] Example 2a includes the apparatus of example 1a wherein: there are no other M layers, including another interconnect line located in another trench, between the TFR and the bottom M layer; and a horizontal plane intersects the first and second vias.

[0072] Example 3a includes the apparatus of example 2a wherein the first and second vias each include cobalt.

[0073] Example 4a includes the apparatus of example 3a comprising an interlayer dielectric (ILD) that directly contacts the contact and directly contacts the TFR.

[0074] Example 5a includes the apparatus of example 3a, wherein the first via directly contacts the contact, the second via directly contacts the TFR, and the contact is a trench contact (TCN) on one of the source and the drain.

[0075] Example 6a includes the apparatus of example 1a, wherein portions of the first and second contacts are included in an interlayer dielectric (ILD) and lateral portions of the TFR, but not a middle portion of the TFR, directly contact the ILD.

[0076] Example 7a includes an apparatus comprising: a frontend portion comprising: (a)(i) a fin-based field effect transistor (FinFET), on a substrate, comprising a source, a drain, and a gate; (a)(ii) a contact coupled to at least one of the source, drain, and gate; (a)(iii) a first via coupled to the contact; (a)(iv) a thin film resistor (TFR), and (a)(v) a second via coupled to the TFR; and a backend portion comprising a bottom metallization (M) layer, including an interconnect line located in a trench, and additional M layers; wherein (b)(i) there are no other M layers, including another interconnect line located in another trench, between the frontend and the bottom M layer, and (b)(ii) portions of the TFR and the first and second vias are all between the bottom M layer and the substrate.

[0077] Example 8a includes the apparatus of example 7a wherein a horizontal plane, which is parallel to a long axis of the substrate, intersects the first and second vias.

[0078] Example 9a includes the apparatus of example 8a wherein the first via includes a metal and the second via also includes the metal.

[0079] Example 10a includes the apparatus of example 8a wherein the first and second vias each include cobalt.

[0080] Example 11a includes the apparatus of example 7a comprising an interlayer dielectric (ILD) that directly contacts the contact and directly contacts the TFR.

[0081] Example 12a includes the apparatus of example 11a wherein the TFR directly contacts etchstop material.

[0082] Example 13a includes the apparatus of example 11a comprising an input/output (I/O) node that includes the TFR.

[0083] Example 14a includes the apparatus of example 12a wherein the TFR includes a bottom plane that is generally parallel to a long axis of the substrate and at least one sidewall that is generally orthogonal to the long axis of the substrate.

[0084] Example 15a includes the apparatus of example 12a wherein the contact couples to at least one of the source and the drain.

[0085] Example 16a includes the apparatus of example 12a wherein the contact is a trench contact (TCN) and the TFR is less than 1 μm thick vertically.

[0086] Example 17a includes the apparatus of example 7a comprising an etchstop layer, wherein lateral portions of the TFR contact sidewalls of the etchstop layer.

[0087] Example 18a includes a method comprising: forming a fin on a substrate and forming source and drain nodes for the fin; forming an insulative layer on the fin and on the substrate; removing a portion of the insulative layer to form a recess; forming a thin film resistor (TFR) in the recess; forming a contact coupled to one of the source and drain nodes; and forming a first via coupled to the contact and a second via coupled to the TFR; forming a bottom metallization (M) layer, including an interconnect line located in a trench, over the first and second vias; and forming additional M layers above the bottom M layer; wherein the TFR and the first and second vias are all between the bottom M layer and the substrate.

[0088] Example 19a includes the method of example 18a, wherein: there are no other M layers, including another interconnect line located in another trench, between the TFR and the bottom M layer; and a horizontal plane intersects the first and second vias.

[0089] Example 20a includes the method of example 19a wherein the first and second vias each include cobalt.

[0090] Example 21a includes the method of example 20a wherein the insulative layer directly contacts the contact and directly contacts the TFR.

[0091] Example 22a includes the method of example 21a, wherein the first via directly contacts the contact and the second via directly contacts the TFR.

[0092] Example 23a includes the method of example 18a comprising forming an etchstop layer, wherein a bottom surface of the TFR directly contacts a top surface of the insulative layer and lateral portions of the TFR directly contact sidewalls of the etch stop layer.

[0093] Example 24a includes a system comprising: a memory; and a processor coupled to the memory, wherein at least one of the processor and the memory include a TFR according to any one of examples 1a to 17a.

[0094] The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. This description and the claims following include terms, such as left, right, top, bottom, over, under, upper, lower, first, second, etc. that are used for descriptive purposes only and are not to be construed as limiting. For example, terms designating relative vertical position refer to a situation where a device side (or active surface) of a substrate or integrated circuit is the "top" surface of that substrate; the substrate may actually be in any orientation so that a "top" side of a substrate may be lower than the "bottom" side in a standard terrestrial frame of reference and still fall within the meaning of the term "top." The term "on" as used herein (including in the claims) does not indicate that a first layer "on" a second layer is directly on and in immediate contact with the second layer unless such is specifically stated; there may be a third layer or other structure between the first layer and the second layer on the first layer. The embodiments of a device or article described herein can be manufactured, used, or shipped in a number of positions and orientations. Persons skilled in the relevant art can appreciate that many modifications and variations are possible in light of the above teaching. Persons skilled in the art will recognize various equivalent combinations and substitutions for various components shown in the Figures. It is

therefore intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

What is claimed is:

- 1 1. An apparatus comprising:
2 a substrate;
3 a fin-based field effect transistor (FinFET), on the substrate, comprising a
4 source, a drain, and a gate;
5 a contact coupled to at least one of the source, the drain, and the gate;
6 a thin film resistor (TFR);
7 a first via coupled to the contact and a second via coupled to the TFR; and
8 a bottom metallization (M) layer, including an interconnect line located in a
9 trench, and additional M layers above the bottom M layer;
10 wherein the TFR and the first and second vias are all between the bottom M
11 layer and the substrate.
- 1 2. The apparatus of claim 1 wherein:
2 there are no other M layers, including another interconnect line located in
3 another trench, between the TFR and the bottom M layer; and
4 a horizontal plane intersects the first and second vias.
- 1 3. The apparatus of claim 2 wherein the first and second vias each include
2 cobalt.
- 1 4. The apparatus of claim 3 comprising an interlayer dielectric (ILD) that directly
2 contacts the contact and directly contacts the TFR.
- 1 5. The apparatus of claim 3, wherein the first via directly contacts the contact,
2 the second via directly contacts the TFR, and the contact is a trench contact (TCN)
3 on one of the source and the drain.
- 1 6. The apparatus of claim 1, wherein portions of the first and second contacts
2 are included in an interlayer dielectric (ILD) and lateral portions of the TFR, but not a
3 middle portion of the TFR, directly contact the ILD.

- 1 7. An apparatus comprising:
2 a frontend portion comprising: (a)(i) a fin-based field effect transistor (FinFET),
3 on a substrate, comprising a source, a drain, and a gate; (a)(ii) a contact coupled to
4 at least one of the source, drain, and gate; (a)(iii) a first via coupled to the contact;
5 (a)(iv) a thin film resistor (TFR), and (a)(v) a second via coupled to the TFR; and
6 a backend portion comprising a bottom metallization (M) layer, including an
7 interconnect line located in a trench, and additional M layers;
8 wherein (b)(i) there are no other M layers, including another interconnect line
9 located in another trench, between the frontend and the bottom M layer, and (b)(ii)
10 portions of the TFR and the first and second vias are all between the bottom M layer
11 and the substrate.
- 1 8. The apparatus of claim 7 wherein a horizontal plane, which is parallel to a
2 long axis of the substrate, intersects the first and second vias.
- 1 9. The apparatus of claim 8 wherein the first via includes a metal and the second
2 via also includes the metal.
- 1 10. The apparatus of claim 8 wherein the first and second vias each include
2 cobalt.
- 1 11. The apparatus of claim 7 comprising an interlayer dielectric (ILD) that directly
2 contacts the contact and directly contacts the TFR.
- 1 12. The apparatus of claim 11 wherein the TFR directly contacts etchstop
2 material.
- 1 13. The apparatus of claim 11 comprising an input/output (I/O) node that includes
2 the TFR.

1 14. The apparatus of claim 12 wherein the TFR includes a bottom plane that is
2 generally parallel to a long axis of the substrate and at least one sidewall that is
3 generally orthogonal to the long axis of the substrate.

1 15. The apparatus of claim 12 wherein the contact couples to at least one of the
2 source and the drain.

1 16. The apparatus of claim 12 wherein the contact is a trench contact (TCN) and
2 the TFR is less than 1 μm thick vertically.

1 17. The apparatus of claim 7 comprising an etchstop layer, wherein lateral
2 portions of the TFR contact sidewalls of the etchstop layer.

1 18. A method comprising:
2 forming a fin on a substrate and forming source and drain nodes for the fin;
3 forming an insulative layer on the fin and on the substrate;
4 removing a portion of the insulative layer to form a recess;
5 forming a thin film resistor (TFR) in the recess;
6 forming a contact coupled to one of the source and drain nodes; and
7 forming a first via coupled to the contact and a second via coupled to the TFR;
8 forming a bottom metallization (M) layer, including an interconnect line located
9 in a trench, over the first and second vias; and
10 forming additional M layers above the bottom M layer;
11 wherein the TFR and the first and second vias are all between the bottom M
12 layer and the substrate.

1 19. The method of claim 18, wherein:
2 there are no other M layers, including another interconnect line located in
3 another trench, between the TFR and the bottom M layer; and
4 a horizontal plane intersects the first and second vias.

1 20. The method of claim 19 wherein the first and second vias each include cobalt.

1 21. The method of claim 20 wherein the insulative layer directly contacts the
2 contact and directly contacts the TFR.

1 22. The method of claim 21, wherein the first via directly contacts the contact and
2 the second via directly contacts the TFR.

1 23. The method of claim 18 comprising forming an etchstop layer, wherein a
2 bottom surface of the TFR directly contacts a top surface of the insulative layer and
3 lateral portions of the TFR directly contact sidewalls of the etch stop layer.

1 24. A system comprising:
2 a memory; and
3 a processor coupled to the memory,
4 wherein at least one of the processor and the memory include a TFR
5 according to any one of claims 1 to 17.

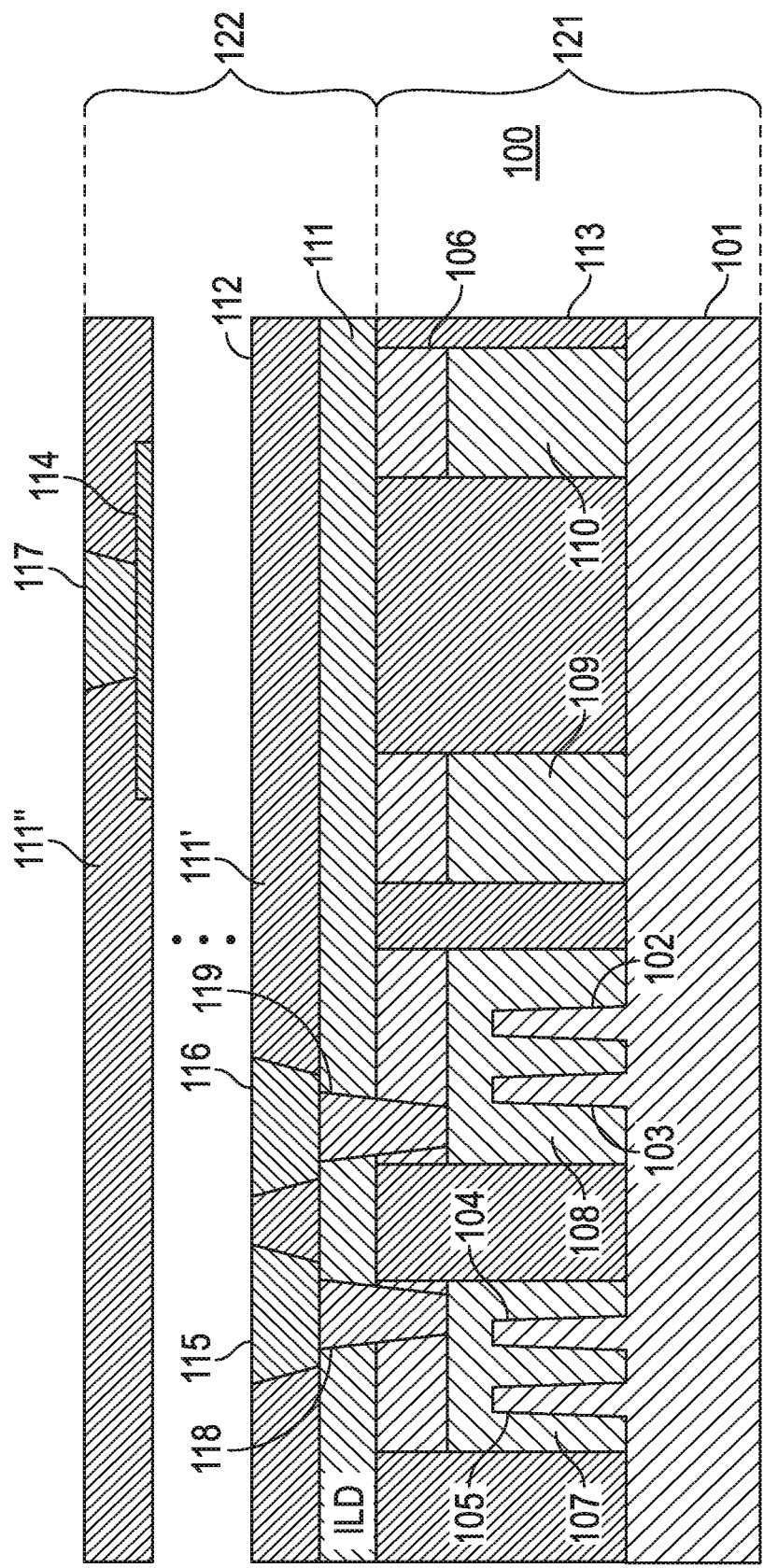


FIG. 1
(Prior Art)

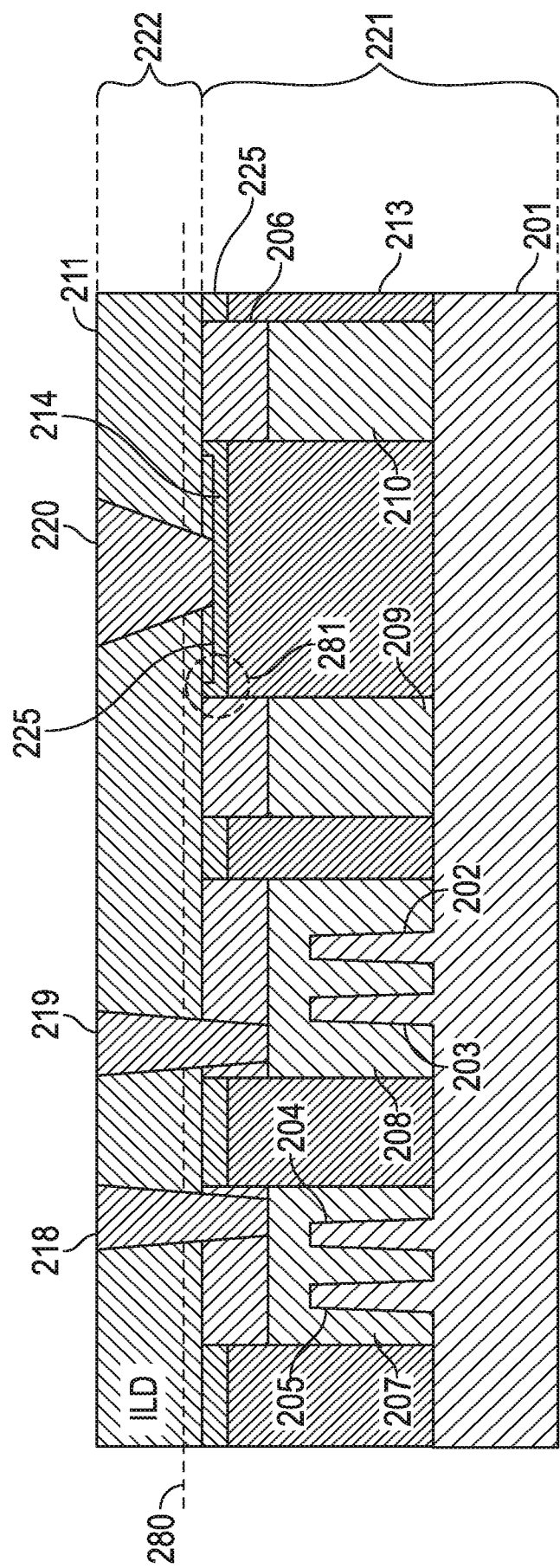


FIG. 2

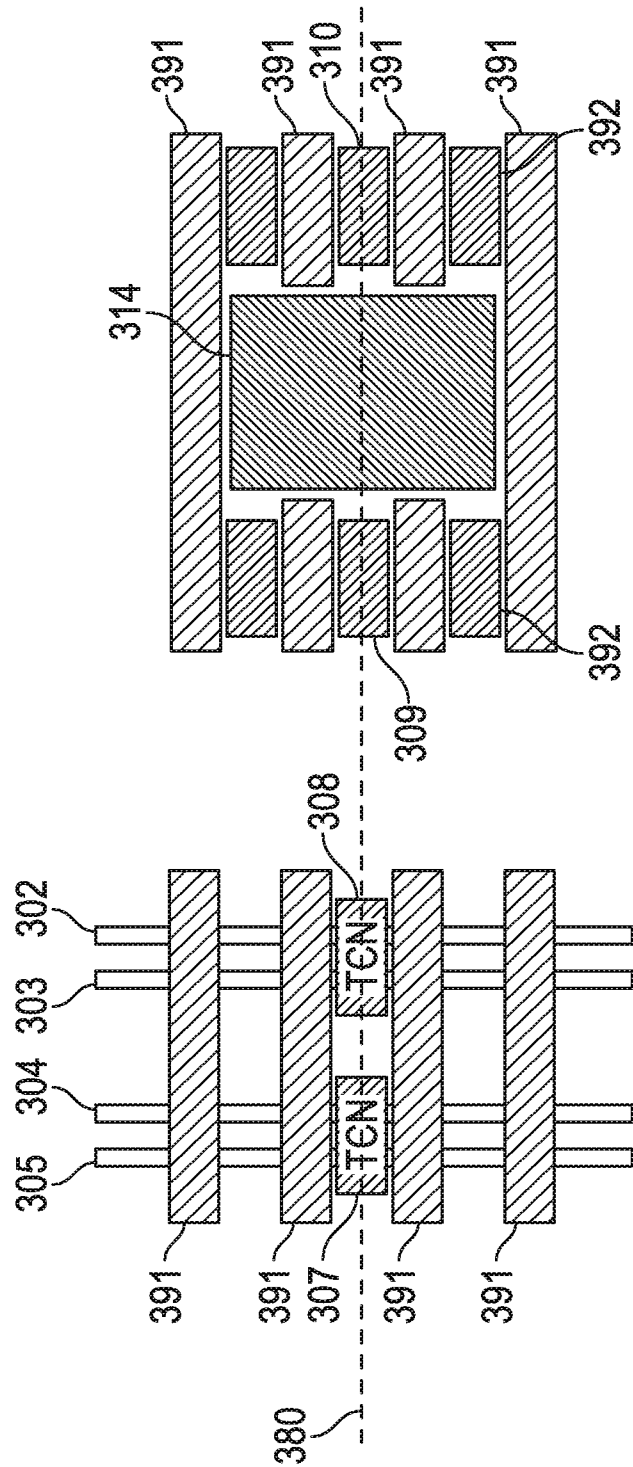


FIG. 3

4/9

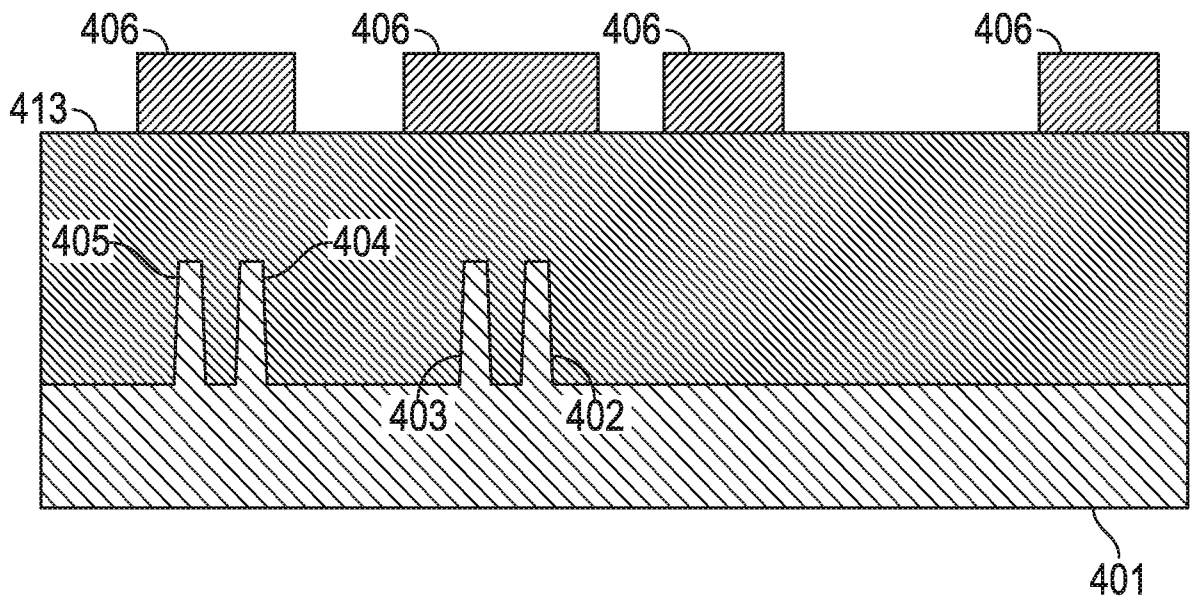


FIG. 4A

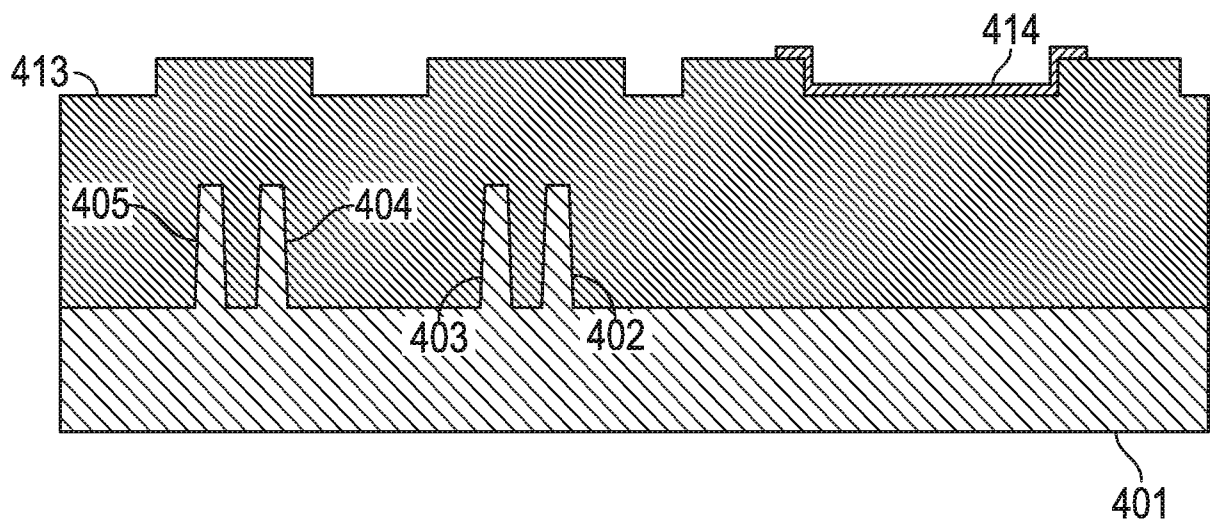


FIG. 4B

5/9

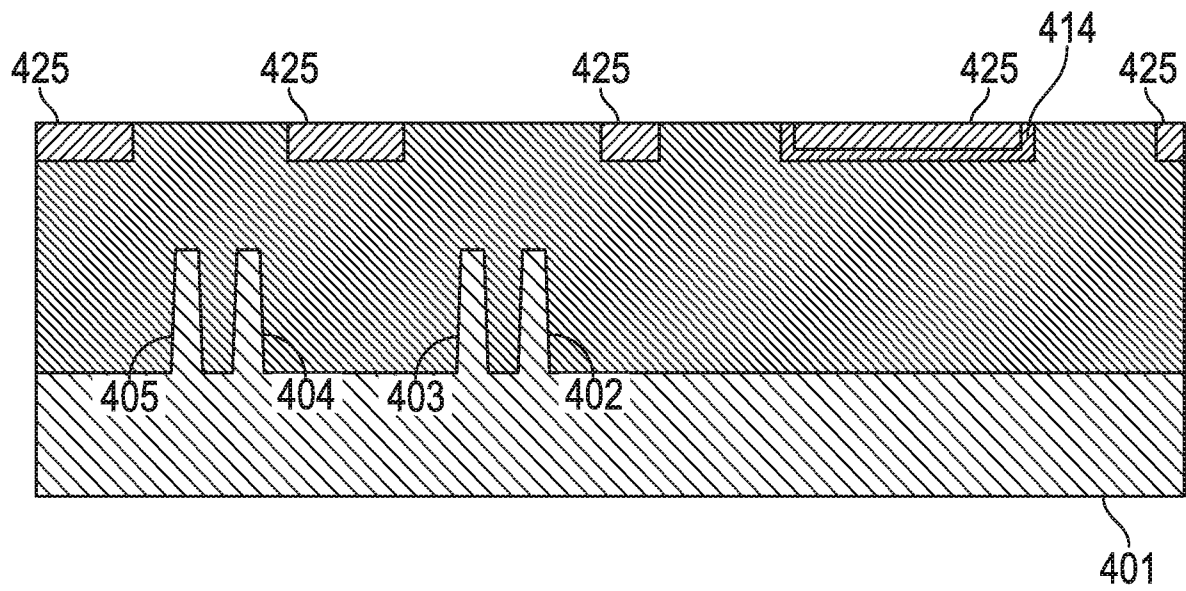


FIG. 4C

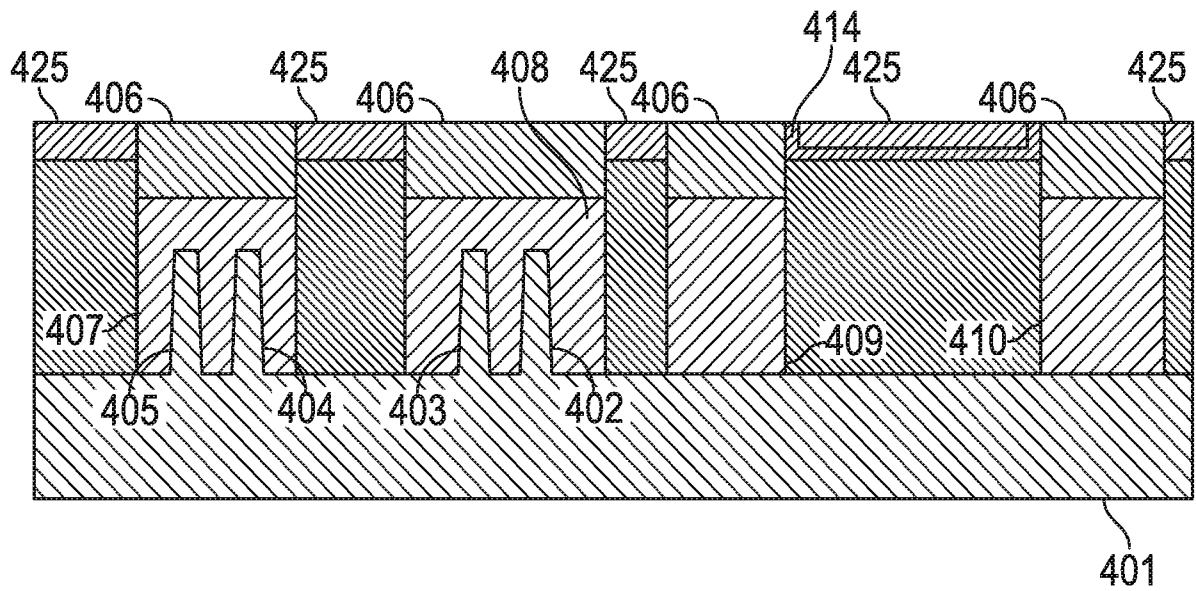


FIG. 4D

6/9

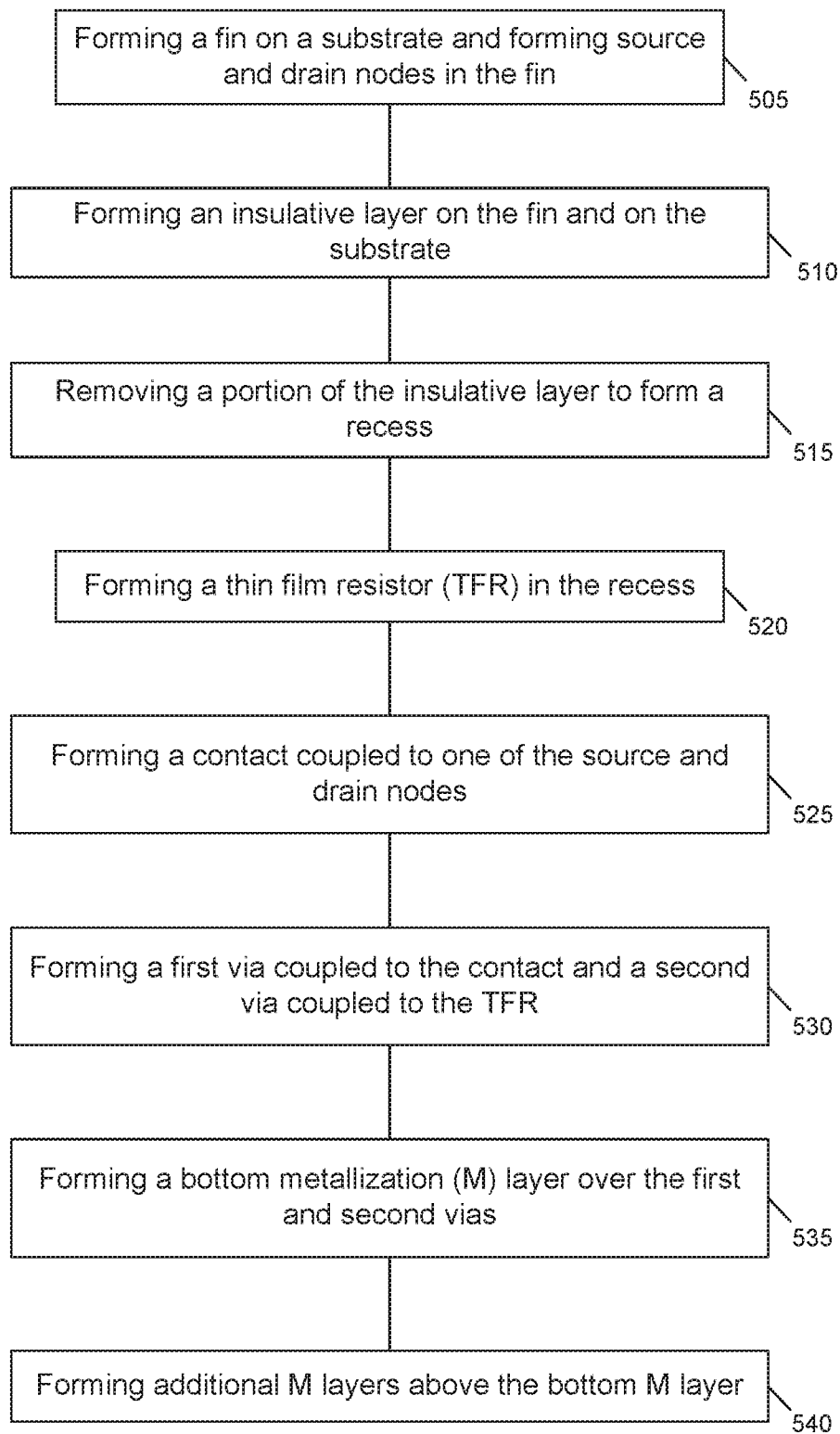
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Figure 5

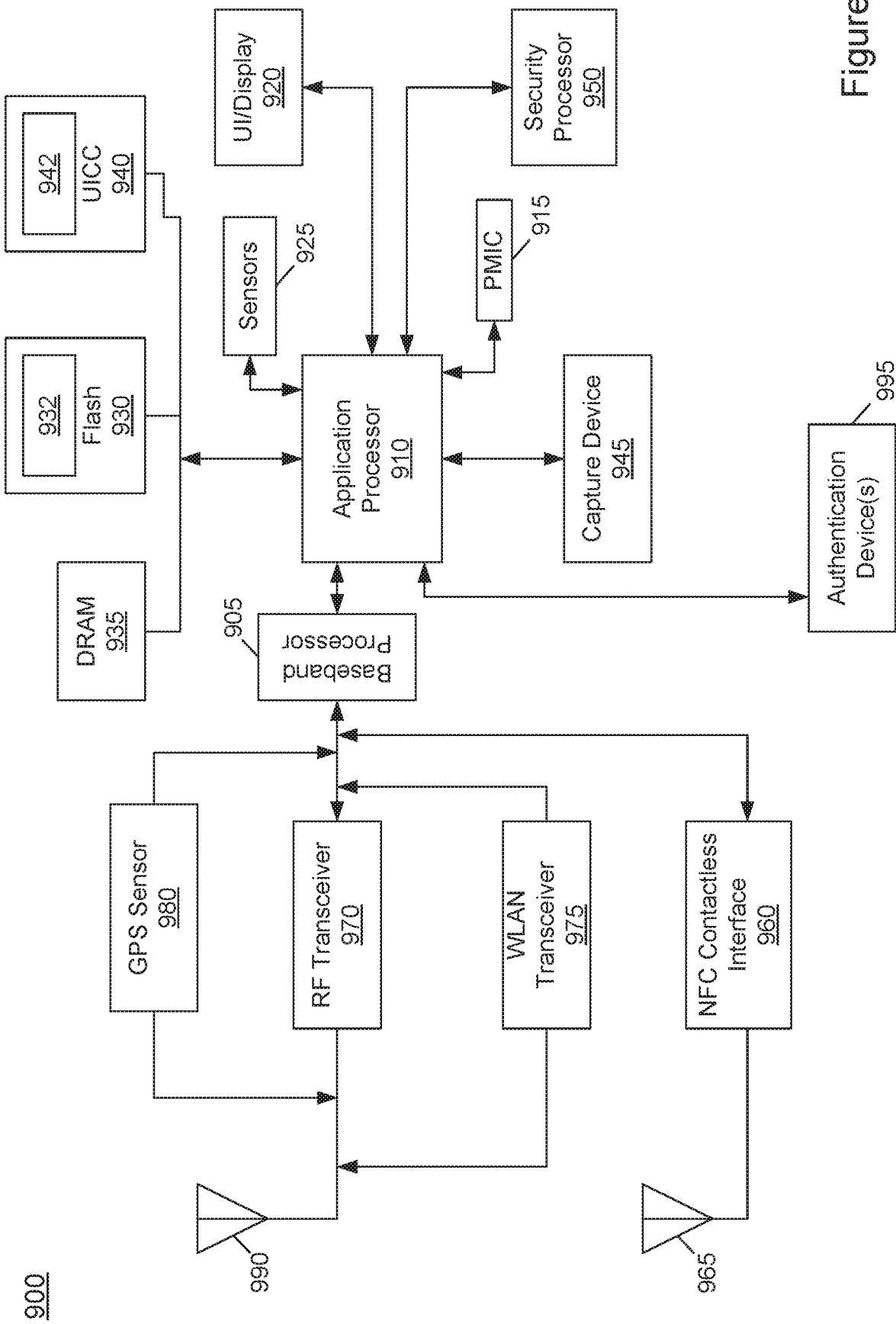


Figure 6

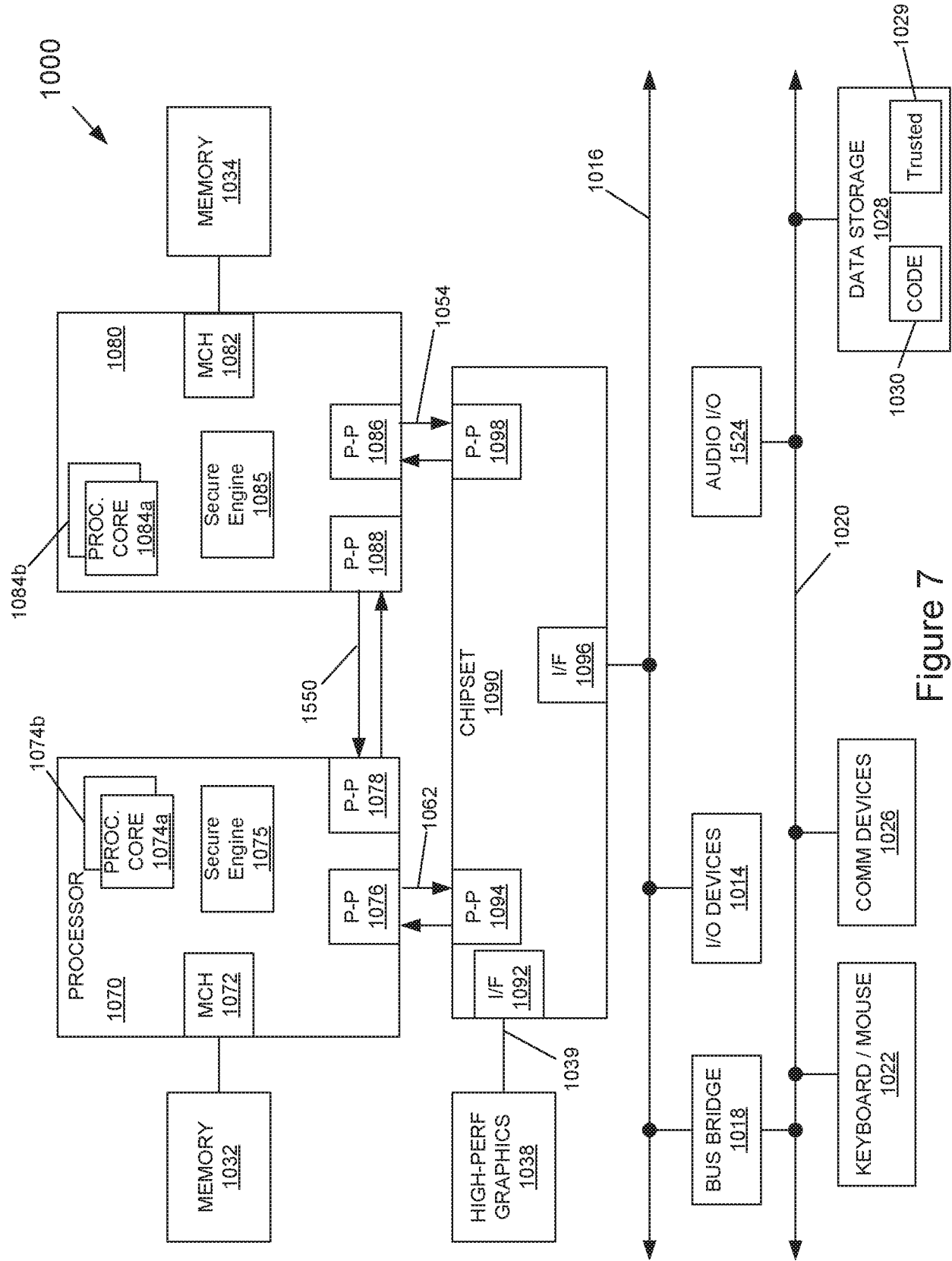


Figure 7

9/9

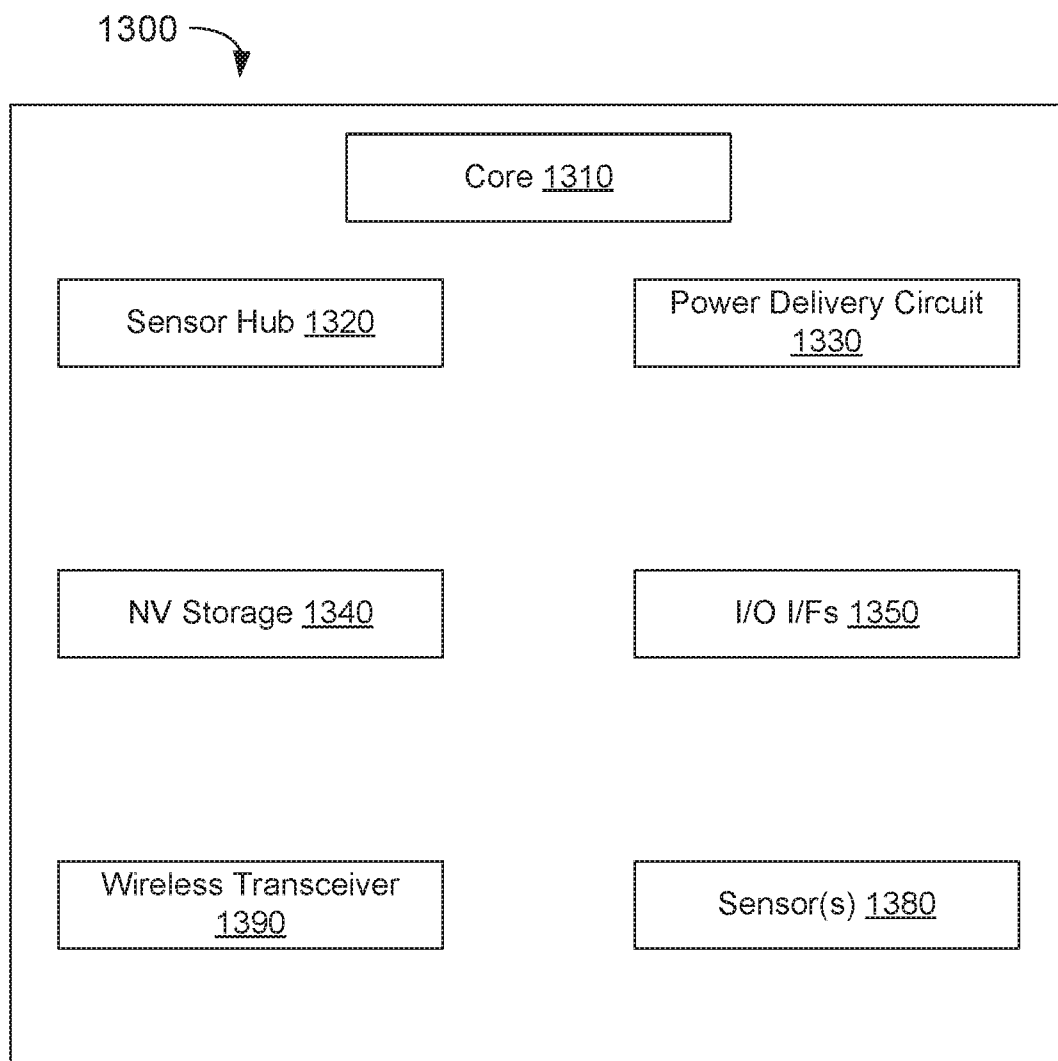


Figure 8

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/768(2006.01)i, H01L 21/8234(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/768; H01L 27/06; H01L 23/528; H01L 29/78; H01L 27/108; H01L 21/8234; H01L 21/02; H01L 49/02; H01L 27/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: TFR, resistor, fin, source, drain, gate, via

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2010-0301417 A1 (KANGGUO CHENG et al.) 02 December 2010 See paragraphs [0042]-[0092] and figures 1-5H.	1-24
Y	US 2014-0264743 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 18 September 2014 See paragraphs [0018]-[0041] and figures 1-11.	1-24
A	US 2013-0307076 A1 (KANGGUO CHENG et al.) 21 November 2013 See paragraphs [0025]-[0047] and figures 1A-8.	1-24
A	US 2015-0048432 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 19 February 2015 See paragraphs [0016]-[0050] and figures 1A-3.	1-24
A	US 2011-0070712 A1 (FRANK SCOTT JOHNSON et al.) 24 March 2011 See paragraphs [0015]-[0033] and figures 2-18.	1-24



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

20 April 2017 (20.04.2017)

Date of mailing of the international search report

21 April 2017 (21.04.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/040668

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