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Yamauchi

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[45] **Aug. 19, 1975**

[54] **HYBRID ARITHMETIC DEVICE**

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[30] **Foreign Application Priority Data**

May 1, 1972 Japan 47-43497

[52] **U.S. Cl.** **235/150.52**; 235/150.5; 235/194

[51] **Int. Cl.** **G06j 1/00**; G06g 7/16

[58] **Field of Search** 235/150.5, 150.52, 150.53, 235/194, 195, 196; 328/160, 161

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Primary Examiner—Malcolm A. Morrison
Assistant Examiner—Jerry Smith
Attorney, Agent, or Firm—John F. Ohlandt

[57] **ABSTRACT**

A hybrid arithmetic device is disclosed in which a load is connected to a constant current or voltage source, and the resistances of the load and a resistor which determines the constant current or voltage of the constant current or voltage source are varied in response to coded signals representing decimal digits. The result of multiplication or division of two decimal operands may be detected as a voltage across or current flowing through the load resistor.

5 Claims, 11 Drawing Figures

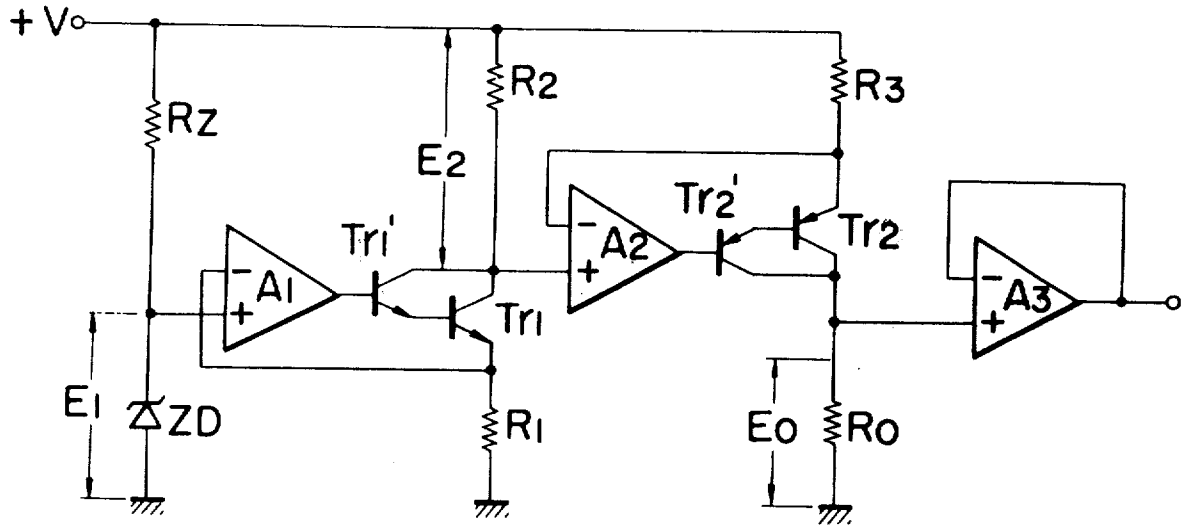


FIG. 1

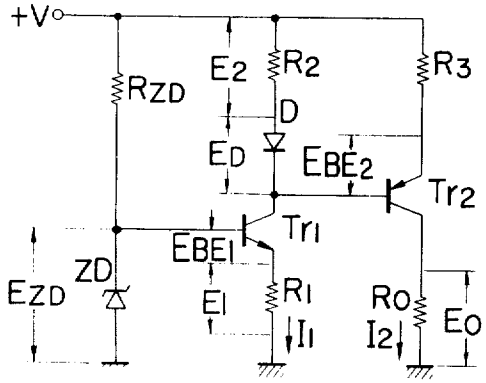


FIG. 3

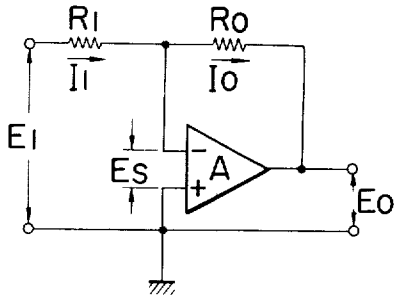


FIG. 2

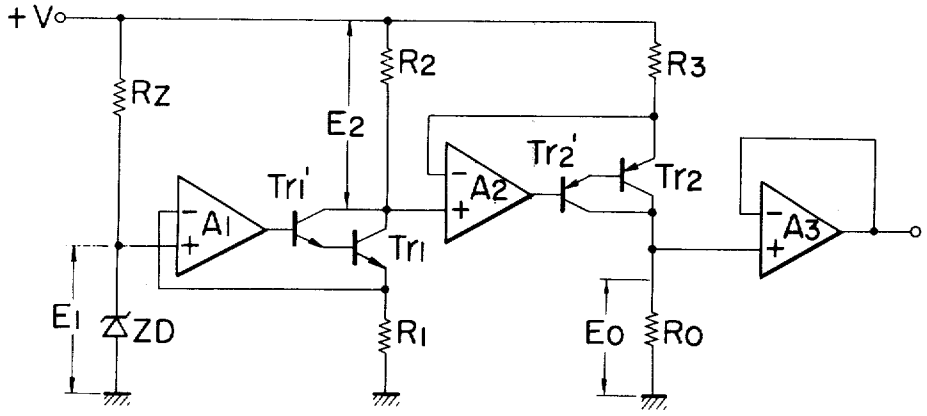


FIG. 4

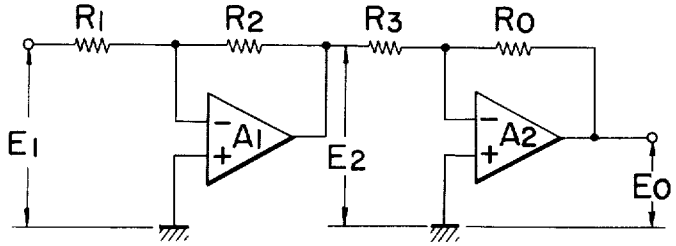


FIG. 5A

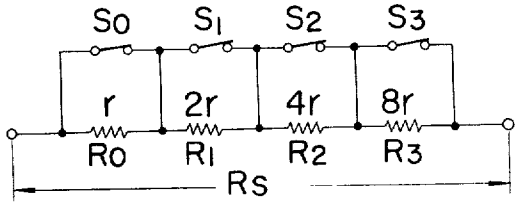


FIG. 5B

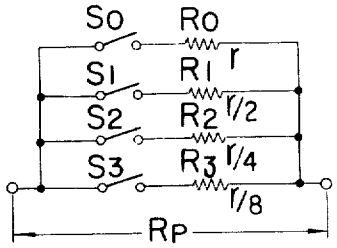


FIG. 5C

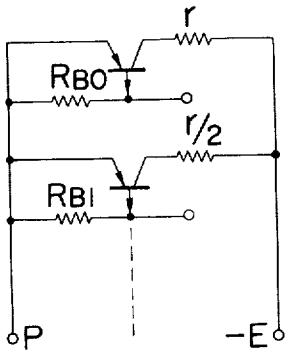


FIG. 5D

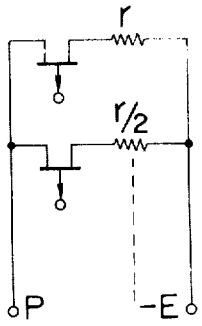


FIG. 6

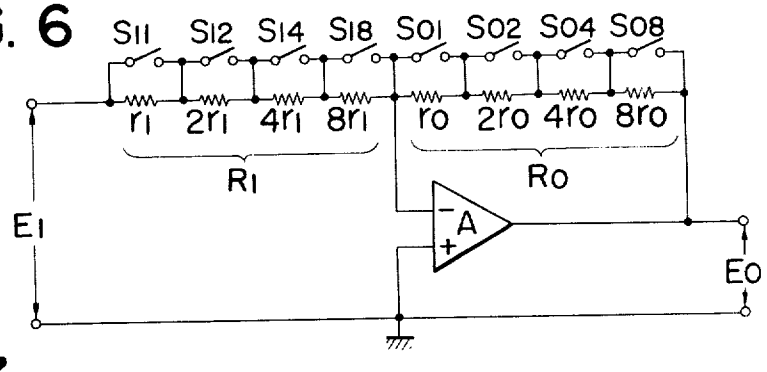


FIG. 7

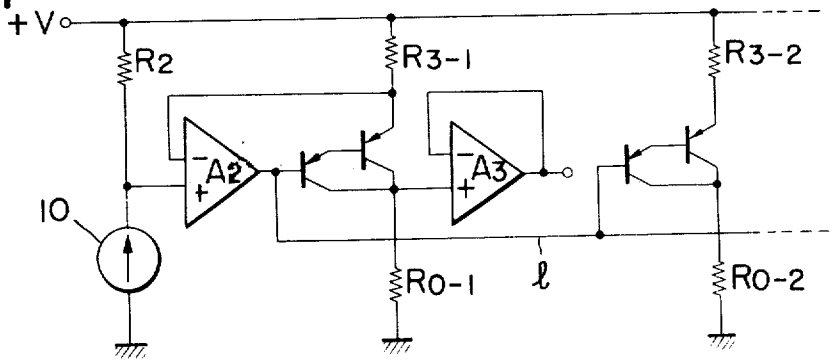
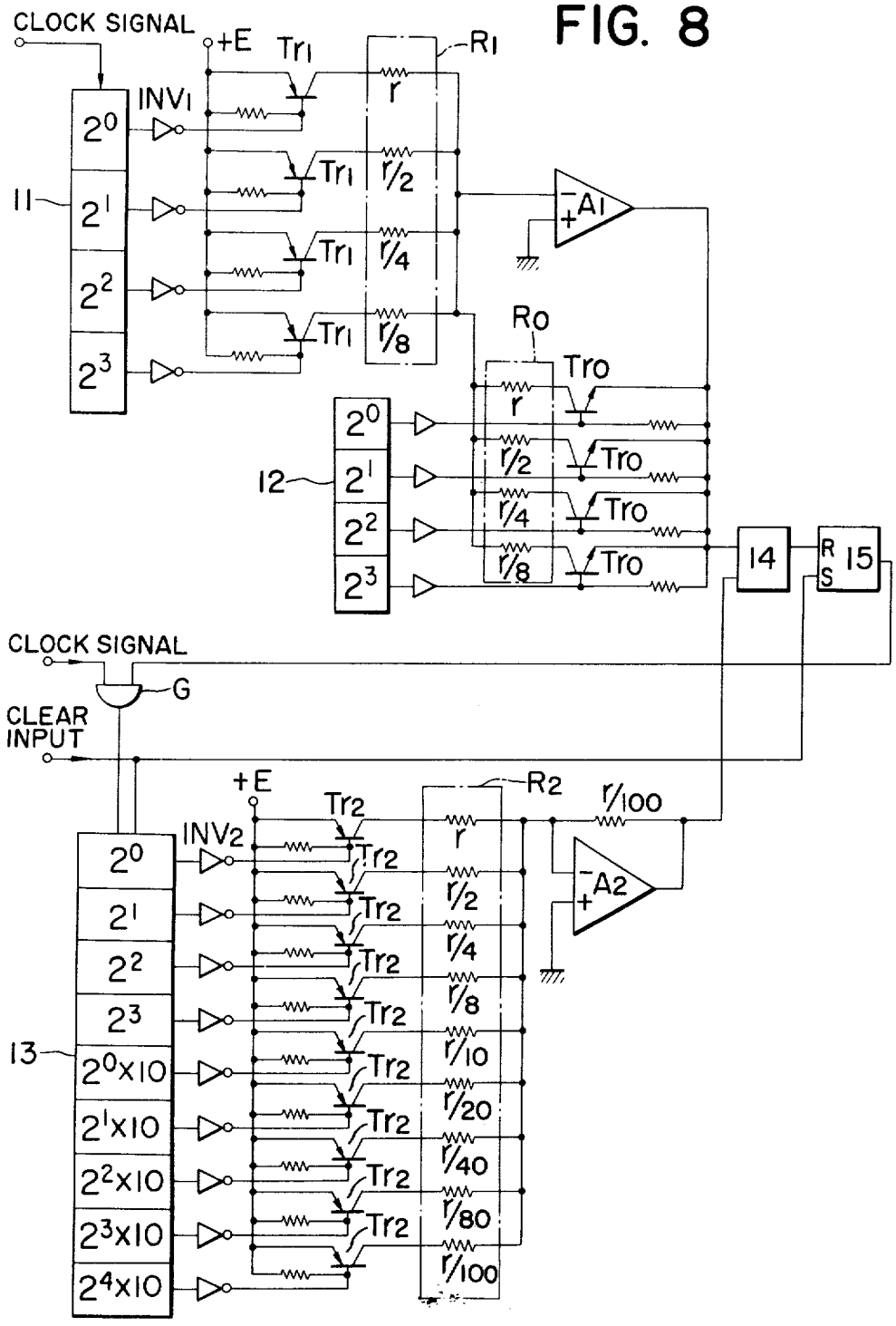


FIG. 8


CLOCK SIGNAL
+E
Tr1
R1
INV1
2^0
2^1
2^2
2^3
11
r
r/2
r/4
r/8
-A1
+
Ro
Tro
12
14
R
S
15
CLOCK SIGNAL
G
CLEAR INPUT
+E
Tr2
R2
r/100
INV2
2^0x10
2^1x10
2^2x10
2^3x10
2^4x10
13
r/10
r/20
r/40
r/80
-A2

HYBRID ARITHMETIC DEVICE

BACKGROUND OF THE INVENTION AND SUMMARY

The present invention relates to a hybrid arithmetic device of the type in which multiplication or division may be electrically effected in a digital-to-analog conversion process.

Analog and digital multipliers and dividers are widely used in computers and other data processing units. In the analog multipliers and dividers, two analog inputs representing the operands such as a multiplicand and multiplier, or dividend and divisor are converted into signals representing the logarithms of the two operands so that the product or quotient may be obtained by the addition or subtraction of the logarithms. The output signal representing the sum of or difference between the logarithms is converted into a signal representing the antilogarithm thereof. In order to improve the accuracy in arithmetic operation, the stability of the logarithmic multipliers and dividers must be improved. As a result their circuits become very complex in construction. In case of the digital multipliers and dividers, the control of the registers, adders and subtractors is extremely complicated and the speed is relatively low.

One of the objects of the present invention is to provide a hybrid arithematic device comprising in combination analog and digital arithmetic and functional circuits.

Another object of the present invention is to provide a high-speed hybrid arithmetic device simple in construction and capable of carrying out arithmetic operations with a higher degree of accuracy and at a considerably higher speed than digital arithmetic devices.

According to the present invention a constant voltage circuit or source is connected to a first resistor to which in turn is connected in series a second resistor. The constant voltage source and the first resistor constitute a constant current source for controlling a constant current flowing through the second resistor. To the second resistor is connected a third resistor to which in turn is connected in series a load resistor. The constant current source and the second resistor constitute a constant voltage circuit for controlling a constant voltage across the third resistor. The constant voltage source and the third resistor constitute a constant current source for controlling a constant current flowing through the load resistor. The relation between the voltage E_1 across the first resistor and the output voltage E_0 across the load resistor is given by

$$E_0 \approx \frac{R_2 \cdot R_0}{R_1 \cdot R_3} \cdot E_1$$

where R_1, R_2, R_3 and R_0 = resistances of the first, second, third and load resistors, respectively. When the resistances R_2 and R_3 of the second and third resistors as well as the voltage E_1 across the first resistor are made constant while the resistances R_0 and R_1 are varied in response to a dividend and a divisor, respectively, the quotient is derived as the output voltage E_0 across the load resistor. When the voltage E_1 across the first resistor as well as the resistances R_1 and R_3 of the first and third resistors are made constant whereas the resistances of the second and load resistors are varied to correspond a multiplicand and a multiplier, respectively, the product is derived as the voltage E_0 across

the load resistor. According to the present invention the resistances of the resistors which determine the constant voltages and currents of the constant current and voltage sources are varied in response to digital signals representing operands such as a multiplicand, multiplier, dividend and divisor. For this purpose digital-to-analog converters are used.

The above and other objects, features and advantages of the present invention will become more apparent from the following description of the preferred embodiments thereof taken in conjunction with the accompanying drawing.

BRIEF DESCRIPTION OF THE DRAWING

FIGS. **1, 2, 3,** and **4** are circuit diagrams used for the explanation of the underlying principle of the present invention;

FIGS. **5-A**, -B, -C and -D are circuit diagrams of the digital-to-analog converters used in the present invention;

FIG. **6** is a circuit diagram of a hybrid arithmetic device in accordance with the present invention;

FIG. **7** is a circuit diagram used for the explanation of one application of a hybrid arithmetic device in accordance with the present invention; and

FIG. **8** is a circuit diagram of another hybrid arithmetic device in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Principle of the Invention, FIGS. 1 -5

Referring to FIG. **1**, a first constant voltage circuit or source comprising a resistor R_{ZD}, a Zener diode ZD and a transistor Tr_1 is provided for a resistor R_1, and a first constant current circuit or source comprising the first constant voltage circuit and the resistor R_1 is provided for a resistor R_2. In like manner, a second constant voltage circuit or source comprising the resistors R_{ZD}, R_1 and R_2, the Zener diode ZD, a diode D and the transistors Tr_1 and Tr_2 is provided for a resistor R_3, and a second constant current circuit comprising the second constant voltage circuit and the resistor R_3 is provided for a resistor R_0. The voltage E_{ZD} across the zener diode ZD and the voltage drop E_{BE1} across the base and emitter of the transistor Tr_1 are constant so that the current I_1 flowing through the resistor R_1 is given by

$$I_1 \approx E_1/R_1 \tag{1}$$

where $E_1 = E_{ZD} - E_{BE1}$ The voltage across the resistor R_2 is given by

$$E_2 \approx R_2/R_1 \cdot E_1 \tag{2}$$

In like manner the current I_2 flowing through the resistor R_3, the transistor Tr_2 and the resistor R_0 is given by

$$I_2 \approx E_2/R_3 \tag{3}$$

where $E_{BE} \approx E_D$ The voltage E_0 across the output resistor R_0 is given by

$$E_0 \approx R_0/R_3 \cdot E_2 \tag{4}$$

Substituting Eq. (2) into Eq. (4), we have

$$E_0 = \frac{R_2 \cdot R_0}{R_1 \cdot R_3} E_1 \quad (5)$$

From Eq. (5) it is seen that when the values of the resistors R_2 and R_3 are fixed whereas the magnitudes of the resistors R_0 and R_1 are varied to correspond to the dividend X and the divisor Y, the output voltage E_0 is proportion to the quotient X/Y may be obtained. When the magnitudes of the resistors R_1 and R_3 are fixed whereas the magnitudes of the resistors R_2 and R_0 are varied to correspond to the multiplicand X and the multiplier Y, respectively, the output voltage E_0 is in proportion to the product X·Y. The voltage E_1 which is the voltage across the Zener diode ZD is constant. In general any combination of the resistors R_1, R_2, R_3 and R_0 may be used, and the circuit shown in FIG. **1** may be used as a square-root generator or squarer when the magnitudes of the resistors $R_1 - R_0$ are suitably selected.

The circuit shown in FIG. **1** is the most fundamental circuit of the present invention, and when a more accurate output is required, a circuit shown in FIG. **2** is used which is substantially similar to that shown in FIG. **1**. Eq. (5) holds for the voltage E_1 across the Zener diode ZD and the voltage E_0 across the output resistor R_0 in the circuit shown in FIG. **2**. Two differential amplifiers A_1 and A_2 whose gain is very high are inserted in the circuit shown in FIG. **2** in order to feed back the outputs thereof to their negative terminals through Darlington circuits Tr_1 and Tr_1', and Tr_2 and Tr_2'. Therefore the stability and accuracy of the constant current circuits may be further improved over the circuit shown in FIG. **1**. When a third differential amplifier A_3 with a gain of unity is connected to the output resistor R_0, the output voltage E_0 may be detected through the amplifier A_3 without causing the change in current flowing through the resistor R_0.

FIGS. **3** shows an operational amplifier of the inverting configuration, and when the gain of the differential amplifier A is almost infinity, the input current thereof is almost zero so that the relation between the current I_1 flowing through the resistor R_1 and the current I_0 flowing through the resistor R_0 is given by

$$I_1 = I_0.$$

This means that the circuit shown in FIG. **3** functions as a constant current circuit or source for the load resistor R_0. Since the gain of the amplifier A is almost infinity, the input voltage error Es of the amplifier A is almost zero and the output voltage E_0 becomes the voltage across the load resistor R_0. Therefore the relation between the input voltage E_1 and the output voltage E_0 is given by

$$E_0 = -\frac{R_0}{R_1} E_1 \quad (6)$$

From Eq. (6) it is seen that when the magnitudes of the resistor R_0 and R_1 are so selected as to correspond to the dividend and divisor, the output voltage E_0 represents the quotient. That is, the circuit shown in FIG. **3** functions as a divider.

In the circuit shown in FIG. **4**, the circuits of the type shown in FIG. **3** are connected in cascade, and Eq. (5) holds for the input and output voltages E_1 and E_0. Therefore the circuit shown in FIG. **4** functions as a multiplier or divider depending upon the combination of the resistors R_1, R_2, R_3 and R_0.

In order to construct a hybrid arithematic device from the circuits of the types described hereinbefore, the magnitudes of the resistors must be varied so as to represent the multiplicand, multiplier, dividend and divisor which are fed in the form of digital signals. For this purpose digital-to-analog converters of the types shown in FIGS. **5-A** to **5-D** are used. In these circuits weighted resistors are connected in series or parallel as is well known in the art, and a contact or contacts across a resistor or resistors are closed or opened depending upon a given digital signal.

In the digital-to-analog converter shown in FIG. **5-A**, the resistors $R_0 - R_3$ represent weights equal to successive powers of **2**. That is, they represent weights r, $2r$, $4r$ and $8r$, respectively. The switches S_0, S_1, S_2 and S_3 shunt the resistors $R_0 - R_3$, respectively. Assume that the decimal digit "6" which may be represented by "0110" in the pure binary code be converted into the analog signal. Then the switches S_1 and S_2 are opened so that the combined resistance Rs becomes

$$Rs = 2r + 4r = 6r$$

which is the resistance representing the decimal digit "6".

In the digital-to-analog converter shown in FIG. 5-B weighted resistors R_0, R_1, R_2 and R_3 representing the weights r, $r/2$, $r/4$ and $r/8$ are connected in parallel together with the switches $S_0 - S_3$. When the switch S_1 and S_3 is closed in response to a given digital signal, the combined resistance Rp is given by

$$\frac{1}{Rp} = \frac{2}{r} + \frac{8}{r} = \frac{10}{r}$$

The circuit shown in FIG. **5-B** is adapted to carry out the multiplications and divisions based upon Eq. (5) which may be rewritten in the form of

$$E_0 = \frac{\frac{1}{R_1} \cdot \frac{1}{R_3}}{\frac{1}{R_0} \cdot \frac{1}{R_2}} E_1 \quad (7)$$

FIG. **5-C** shows a weighted resistor network with switching transistors, and FIG. **5-D** shows a weighted resistor network with field-effect transistors which function as switching elements. The operation of the networks shown in FIGS. **5-C** and **5-D** will not be described in detail, because they are prior art networks and are similar in function to the circuit shown in FIG. **5-B**.

Hybrid Arithematic Device, FIG. 6

FIG. **6** illustrates a hydrid arithmetic device in accordance with the present invention comprising the circuit shown in FIG. **3** and the digital-to-analog converter shown in FIG. **5-A**. The resistors R_1 and R_0 are shown as comprising a weighted resistor network of the type shown in FIG. **5-A**. As described hereinbefore a dividend is represented by the magnitude of the resistor R_0 whereas a divisor is represented by the magnitude of the resistor R_1 to carry out the division based upon Eq.

(6). For example in order to obtain the quotient of 3/6, the switches S_{01} and S_{02} are opened in response to the binary coded signal "0011" representing the decimal digit "3" whereas the switches S_{12} and S_{14} are opened in response to the binary signal "0110" representing the decimal digit "6". Therefore $R_0 = 3r_0$ and $R_1 = 6r_1$. From Eq. (6) the output voltage E_0 becomes

$$E_0 = 2\,\frac{r_0}{r_1}E_1$$

Since r_0, r_1 and E_1 are all constants, the output voltage E_0 is proportional to "3/6".

Application, FIG. 7

Next one example of an application of a hybrid arithmetic device in accordance with the present invention will be described in connection with a teaching machine of the type which may automatically analyze the responses or answers from students for a given question and record the analyzed data. Each student selects one of a plurality of previously given answers for a given question, and the number of students who selected each of a plurality of answers is recorded. In this case it is advantageous if the ratio of the number of students who selected each of a plurality of answers to the total number of students is also displayed and recorded. This may be accomplished by the circuit shown in FIG. 7.

Referring to FIG. 7 illustrating the circuit which is substantially similar in construction to that shown in FIG. 2, same reference numerals are used to designate similar components. A constant current source **10** may comprises the Zener diode ZD and the differential amplifier A_1 as shown in FIG. 2 or may be any conventional constant current source. The internal resistance of the constant current source **10** corresponds to the resistor R_1 shown in FIG. 2. A first arithmetic device comprising the constant current source **10**, and the resistors R_2, $R_{3\text{-}1}$ and $R_{0\text{-}1}$ carries out the division of (the number of students who selected a first answer/ the total number of students). The output of the differential amplifier A_2 in the first hybrid arithmetic device is applied through a signal line **1** to the input of a second arithmetic device comprising the resistor R_2, the constant current source **10** and the resistors $R_{3\text{-}2}$ and $R_{0\text{-}2}$. In order to carry out the division based upon Eq.(7), the total number of students, that is a divisor is represented by R_2, whereas the numbers of students who selected the specific answers that is, dividends, are represented by the resistors $R_{3\text{-}1}$, $R_{3\text{-}2}$ and so on, respectively. As a result the voltage across or current flowing through each of the resistors $R_{0\text{-}1}$, $R_{0\text{-}2}$ and so on represents the number of students who selected a specific answer/the total number of puiples. In order to improve the accuracy, the output of the first arithmetic circuit may be derived through the operational amplifier A_3 or instead of the resistor $R_{0\text{-}2}$ an ammeter is inserted so that the teacher may directly read the ratio. In the circuit shown in FIG. 7 the digital-to-analog converter of the type shown in FIG. 5-B is used.

Hybrid Arithmetic Device, FIG. 8

The hybrid arithmetic device shown in FIG. 8 gives the result of a division or multiplication in the form of a digital output, and is based upon the circuit shown in FIG. 3. That is, the circuit comprising the differential amplifier A_1 and the resistors R_1 and R_0 which are shown as comprising a weighted resistor network is substantially similar in construction to the divider shown in FIG. 3. The weighted resistor networds R_1 and R_0 are similar to the circuit shown in FIG. 5-C including the switching transistors Tr_1 and Tr_0. The on-off operation of the transistor Tr_1 is controlled in response to a register **11** whereas the on-off operation of the switching transistor Tr_0 is controlled in response to the output of a register **12**. In addition to the above components, the hybrid arithmetic device shown in FIG. 8 comprises a register **13**, a voltage comparator **14** and a general-purpose analog-to-digital converter comprising the flip-flop **15**, the weighted resistor network R_2 and the differential amplifier A_2. The registers **11** and **13** also function as a counter, and the flip-flop **15** is set in response to the clear input and reset in response to the output of the comparator **14**.

Next the mode of division will be described. The flip-flop **15** is set in response to the clear input before the arithematic device is actuated. The digital signals representing the digits A and B are stored in the registers **11** and **12**, respectively and the analog voltage representing the quotient A/B is derived from the differential amplifier A_1, and is applied to one input terminal of the comparator **14**. Since the flip-flop **15** is set, the clock signals are transmitted through a gate G to the register **13** which functions as a counter in this case. In response to the output of the register **13**, the transistors Tr_2 are turned on and off so that the analog voltage representing the content in the register **13** is derived from the differential amplifier A_2 and is applied to the other input terminal of the comparator **14**. When the content in the register **13** is shifted so that the output of the differential amplifier A_2 coincides with that of the amplifier A_1, the coincidence signal is derived from the comparator **14** and applied to the flipflop **15** so that the latter is reset. As a result, the gate G is closed so that the clock signals are interrupted to be applied to the register **13**. In this case, the content in the register **13** represents the quotient A/B.

Next the mode of multiplication will be described. A multiplicand is set into the register **12** whereas a multiplier, into the register **13**. The register **11**, which now functions as a counter, steps in response to the clock signals. When the output voltage of the amplifier A_1 coincides with that of the amplifier A_2, the clock pulses are interrupted to be applied to the register **11**. (The circuit for this purpose is now shown). The content in the register **11** represents the product B·C.

What is claimed is:

1. A hybrid arithmetic, device comprising:

a first stage including a first resistor, a Zener diode connected to said first resistor, a first transistor amplifier having an output and an input, second and third resistors connected to the output of said first transistor amplifier, a first operational amplifier having a plurality of inputs and an output, the output thereof being connected to the input of said first transistor amplifier, one of said inputs of said first operational amplifier being connected to the point of interconnection between said Zener diode and said first resistor, the other input of said first operational amplifier being connected to a feedback path from the output of said first transistor amplifier;

a second stage including a second transistor amplifier having an input and an output, fourth and fifth re-

sistors connected to the output of said second transistor amplifier, a second operational amplifier having a plurality of inputs and an output, the output of said second operational amplifier being connected to the input of said second transistor amplifier, one of the inputs of said second operational amplifier being connected to the output of said first transistor amplifier and the other input thereof being connected to a feedback path from the output of said second transistor amplifier;

means for setting the values of at least a selected pair of said resistors to selected digital values representing the values of arithmetic operands so as to derive across the fifth resistor an output voltage whose value is a measure of the result of a selected arithmetic operation on said operands.

2. A hybrid arithmetic device as defined in claim 1, in which the second and the fifth, output resistor are set to the values of a multiplicand and a multiplier, respectively, and the value of the output voltage is proportional to the product of said multiplicand and multiplier.

3. A hybrid arithmetic device as defined in claim 1, in which the third and fifth resistor are set respectively to the values of a divisor and a dividend, respectively, and the value of the output voltage is proportional to the quotient of said dividend and divisor.

4. A hybrid arithmetic device as defined in claim 1, in which the setting means comprise digital-to-analog converter means for converting the value of a selected digital quantity into an analog resistance value.

5. A hybrid arithmetic device as defined in claim 1, in which a plurality of additional stages, substantially identical to said second stage, are connected in parallel to the output of said second transistor amplifier, a resistor in each of said additional stages being representative of a particular dividend in relationship to a common divisor represented by said second resistor, another resistor in each of said additional stages being representative of a particular quotient resulting from the dividing operation.

* * * * *