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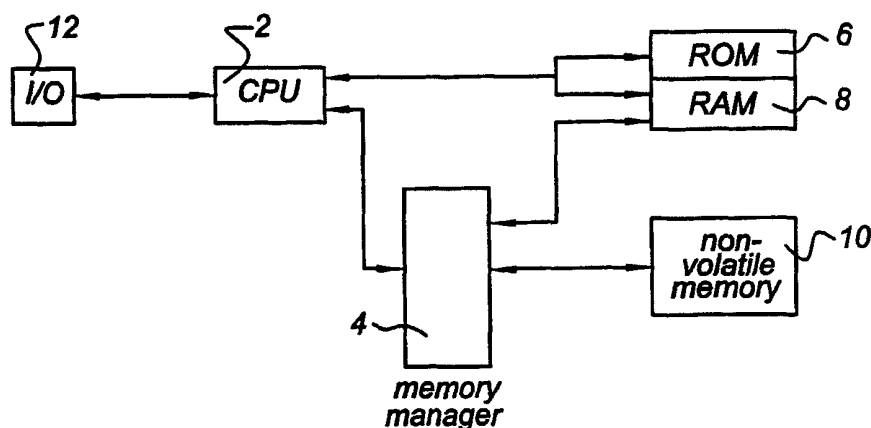
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- (71) Applicant (for all designated States except US): **BELLE GATE INVESTMENT B.V.** [NL/NL]; Parkweg 2, NL-2585 JJ Der Haag (NL).
- (72) Inventors; and
- (75) Inventors/Applicants (for US only): **DE JONG, Edward, Karel** [NL/NL]; Ankersmidplein 63, NL-1506 CK Zaandam (NL). **BOS, Jurjen, Norbert, Eelco** [NL/NL]; Deukelven 48, NL-1963 SR Heemskerk (NL).
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- (74) Agent: **DE BRUIJN, Leendert, C.**; Nederlandsch Octrooibureau, Scheveningseweg 82, P.O. Box 29720, NL-2502 LS The Hague (NL).

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(54) Title: ARRANGEMENTS STORING DIFFERENT VERSIONS OF A SET OF DATA IN SEPARATE MEMORY AREAS AND METHOD FOR UPDATING A SET OF DATA IN A MEMORY



(57) Abstract: Computer-readable medium storing a data structure for supporting persistent storage of a set of data, the data structure including: (a) at least an oldest version of the set of data in a first memory area, the first memory area including at least one first tag for uniquely identifying the oldest version, and (b) at least a most recently updated version of the set of data in a second, distinct memory area, the second memory area including at least one second tag for uniquely identifying the most recently updated version. The invention also relates to a computer arrangement including a processor and such a computer-readable medium, as well as to a method of updating sets of data having such tagged-data structures.



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Arrangements storing different versions of a set of data in separate memory areas and method for updating a set of data in a memory.

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FIELD OF THE INVENTION

The present invention relates to memory means comprising at least one set of data in a memory area. The memory means may be implemented with volatile RAM devices or with non-volatile silicon devices, such as EEPROM, Flash-EPROM or ROM. Usually, such memory stores operating system software modules, application programs and application data. In areas where such computer systems according to the invention may be particularly applicable, some or all of the operating system software modules are stored in ROM.

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DESCRIPTION OF PRIOR ART

In some applications, typically financial transaction processes, storing must be done very safely. Such safe storage applications are known as requiring "Atomicity of Update" in "persistent" storage means. In order to carry out such safe updating, the use of update logs is known from the prior art. Such update logs register which parts of a set of data has to be changed during an update session. Only when the set of data together with its updated parts has been stored in memory, all references to the former version of the set of data may be removed.

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OBJECT OF THE INVENTION

The object of the present invention is to support persistent application-data storage by providing a mechanism for atomicity of update for data stored in non-volatile memory devices, especially in silicon storage devices such as EEPROM or Flash-EEPROM.

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SUMMARY OF THE INVENTION

Therefore, the invention is directed to a computer-readable medium storing a data
5 structure for supporting persistent storage of a set of data, said data structure comprising:

- (a) at least an oldest version of said set of data in a first memory area, said first
memory area including at least one first tag for uniquely identifying said oldest
version, and
- (b) at least a most recently updated version of said set of data in a second, distinct
10 memory area, said second memory area including at least one second tag for
uniquely identifying said most recently updated version.

The application of such unique tags related to the different memory areas allows
to uniquely identify which one of the versions are older versions. Moreover, the applica-
tion of such tags allows for identifying which versions relate to the same original set of
15 data. Thus, in a memory, different versions of different sets of data may be present at the
same time. Moreover, during updating the most recently updated version the older ver-
sions, as well as the most recently updated version, are not removed from memory. Only
after an update action of the most recently updated version has been entirely completed
the oldest version of the set of data may be removed from memory.

20 When, during an update action the updating is interrupted, the most recently up-
dated version is still present in the memory, thus guaranteeing the presence of at least one
valid version of the set of data. Thus, "Atomicity of Update" is guaranteed. Such atomic
updates guarantee either a complete replacement of the data or unmodified previously
stored data, even if the update operation is disrupted.

25 In one embodiment, each of the versions of the set of data are stored in one or
more memory pages, and each of the memory pages includes one tag, each tag comprising
references to the set of data, a version number and a page number.

A page is defined as a memory area of consecutive memory locations which are
dealt with as a unity such as appropriate for the storage technology concerned. Each page
30 may correspond to one word line, thus facilitating memory unit read and write operations.
Version numbers are assigned to the different generations of the set of data. Thus, differ-
ent version numbers relate to different generations. Different page numbers refer to differ-
ent pages within the same generation of the set of data.

The invention also relates to a computer arrangement including a processor and at least one computer-readable medium as defined above.

Preferably, the processor is arranged to write tags with redundancy as to the content and, after having read tags from the memory means, to analyze from the redundancy whether or not write errors have occurred. Such a redundancy can be used as an indication whether or not the tags concerned and the set of data to which the tags refer have valid values.

Preferably, the most recently updated version comprises a plurality of pages, each page having a unique tag, and the processor is arranged for updating said most recently updated version of said set of data and to write a predetermined tag of a predetermined one of said plurality of pages into said memory means as a last step of said updating. The predetermined tag, which is written last, can be read by the processor. If the processor detects the presence of this predetermined tag in the memory means, the processor can conclude that the updating action has been completed entirely.

The application of such tags provides for several new options. For instance, at least one of the tags may include additional data as to indicate ownership and use-rights, the processor being arranged to recognize ownership and use-rights from these additional data.

The use-rights may differ for different parts of the set of data and the processor may be arranged to recognize these different use-rights for these different parts.

Preferably, the processor is arranged to analyze tag values and is only allowed to access the versions of the set of data by reference through the tag values. Thus, access to the different versions of the set of data is not controlled by a usual program counter but by the tag values. In other words, the memory has become content addressable memory.

In the latter embodiment, the processor preferably comprises a central processing unit and a distinct memory managing unit, where the tag values are only known to the memory managing unit. Then, the physical address space of the memory means is not included in the address space of the central processing unit, especially not in the address space where application program or operating system software instructions are stored. In this manner, additional protection against "probing" can be obtained. To realize this potential protection, the memory managing unit may provide to the central processing unit additional interface functionality with a tag-size address register.

In order to increase the safety of stored data, the memory managing unit may

encode tags with a cryptographic key prior to writing them into the memory, the cryptographic key being only known to the memory managing unit. Such a cryptographic key may relate to a cryptographic one-way function.

5 The present invention also relates to a method for supporting persistent storage of a set of data, comprising the steps of:

- (a) storing an oldest version of said set of data in a first memory area, wherein said first memory area includes a first tag for uniquely identifying said oldest version, and
- (b) storing a most recently updated version of said set of data in a second distinct
10 memory area, wherein said second memory area includes a second tag for uniquely identifying said most recently updated version.

BRIEF DESCRIPTION OF THE DRAWINGS

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Hereinafter, the present invention will be described in detail with reference to some drawings which are intended only to illustrate the present invention and not to limit its scope.

Figure 1 shows an example of an embodiment according to the present invention.

20 Figure 2 shows a possible layout of a memory in accordance with the present invention.

Figure 3 shows the content of memory pages in a possible embodiment of the arrangement according to figure 2.

Figure 4 illustrates a method in accordance with the present invention, and

25 Figure 5 illustrates a possible arrangement of a memory managing unit in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

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Figure 1 shows one possible arrangement in accordance with the present invention. A central processing unit 2 is connected to input/output means 12 and to memory which may comprise ROM 6, RAM 8, and non-volatile memory 10. Arranged apart from

or within the central processing unit 2 there may be a memory manager 4. The manager 4 is arranged for carrying out memory functions which respect to the non-volatile memory 10 and preferably also the other memory sections ROM 6 and RAM 8. The embodiment shown in figure 1 relates to all kinds of management systems of data storage. However, the invention is especially beneficial with respect to data storage in non-volatile silicon devices rather than on hard disks. The important applications are in the field of embedded computer systems, and in single chip computers such as smart cards.

Figure 2 shows one possible arrangement of data storage in a memory in accordance with the present invention. The non-volatile data memory 10 may be partitioned in storage units. Here, these units of memory storage are called "pages". Conveniently, these pages may be of equal size, e.g. equal to the size of a "word-line" in silicon devices used to implement the memory. However, the pages may be of different sizes. The content of the memory is managed by the memory manager 4 page by page: allocation, updates, and de-allocation of application data storage involve manipulating one or more pages.

The memory comprises different generations (or versions) of a set of application data elements. Each generation may be stored in one or more pages. In figure 2, the situation is shown in which the memory comprises three different generations k , $k+1$, $k+2$ of one set of application data elements. The example shows that generation k occupies three pages 1, 2, and 3, generation $k+1$ occupies two pages i , $i+1$, and generation $k+2$ occupies two pages n , $n+1$. Generation k is the oldest version of the set of application data elements in the memory, whereas generation $k+2$ is the most recently updated version of the set of application data elements. Each of the generations k , $k+1$, $k+2$ may, e.g., relate to different versions of a software object.

The generations k , $k+1$, and $k+2$ are indicated to form a "data chunk" which term is used here as a reference to one single set of application data elements. Pages required for storage are allocated from any location in memory that is not occupied by a page as determined by the memory manager 4. The different generations k , $k+1$, $k+2$ of the data chunk shown in figure 2 may or may not be stored in memory in consecutive memory locations. The memory manager 4 is the unit to decide where to store the different generations. Even the pages within one generation need not be stored in consecutive pages. To illustrate this, pages n and $n+1$ are shown as being located remote from one another (indicated by dots between them).

In practice, the memory will contain several "data chunks", i.e., several sets of generations of different sets of data.

In a memory organized and managed in accordance with the present invention, atomicity of update is provided by the management policy carried out by the memory manager 4. After being stored, data related to a version of the set of application data elements will never be modified in the same memory area. In other words, a page once created is never modified. When the last updated set of application data elements needs to be amended in accordance with an application program running on the central processing unit 2, a new memory area, e.g., a new set of pages, is allocated by the memory manager 4. In this new memory area any changed values together with values of data elements of the set of application data elements that have not been changed are stored by the memory manager 4. In this way, the memory 10 will hold at any time at least one consistent, valid version of the data chunk.

Such an updating action may, e.g., relate to a smart card. Although updating of data in a smart card only takes a very short time (for instance about 3 msec) there is a small chance that the smart card is removed from a communicating terminal prior to completing the data transaction with the terminal. Thus, the updating may be interrupted prior to completion. When this happens, at least the last updated version is still present in the memory of the smart card.

In one embodiment, after completing the update of the set of data, the memory manager 4 proceeds by de-allocating the memory area storing the oldest version of the set of data. The memory manager 4 may, e.g., control the presence of no more than 10 versions of one set of application data elements. In a practical realization the application program running on the central processing unit 2 will interact with the memory manager 4 to control the process of updating its data, e.g., to indicate completion of the update. The application program will notify the completion of the update to the memory manager 4, after which the memory manager 4 completes the writing operations in the memory 10. Such update process signaling is customary in transaction processing systems.

When several versions of the set of application data elements are present in the memory the modification history of the data may be analyzed through the memory manager 4. The memory manager 4 does this by providing means for the application program running in the central processing unit 2 to inspect, but not modify, data values in previous versions.

Figure 3 shows a possible memory page structure in accordance with the present invention. It is assumed that the memory is divided into pages. Figure 3 shows two pages i , $i+1$. Each page i , $i+1$, contains application program data and a tag i , $i+1$. Preferably, the tag value consists of three parts: a "chunk identifier" $chid$, a generation count $gen\#$, and a page count $pg\#$. The chunk identifier serves as a unique reference to a programmer's unit of stored data. The generation counter $gen\#$ identifies the version number of the data stored. At least two generations will be indicated by the generation counters $gen\#$. The page counter $pg\#$ indicates the page number of the page concerned within the generation of the set of program data to which the page belongs. The page counter $pg\#$ does allow that data of a generation of a set of data is stored as a multiple number of pages.

In one specific realization of the invention the tag value is stored in the memory using a special encoding, e.g., using redundancy for instance with a qualifying number of bits set to one. This special encoding is used by the memory manager 4 to detect correct/incorrect data write operations. Only if the qualified number of bits is detected to be one (or high) the memory manager 4 decides that the tag value is valid. If this qualified number of bits is not set to one, the memory manager 4 decides that the tag value is invalid. Such a situation may, e.g., be caused by interrupting the power supplied to the memory device, for instance when a user of a smart card removes his smart card from a terminal prior to completion of a financial transaction.

In such an embodiment, prior to removing the oldest generation of the set of data, the memory manager 4 will determine the validity of the most recently updated generation. The specific tag encoding method may be determined from the physical characteristics of the silicon storage device used. It should be chosen to have a very high likelihood of resulting in an invalid encoding if that memory device fails to write the page in its entirety. In dependence on the memory chip design (i.e. the transistor technology used), before writing new data in a page, some memories will first change all memory location values of a specified page into either zeros or ones. Therefore, as indicated above it is sometimes better to check whether a qualified number of bits in a tag is one whereas in other cases it might be better to check the presence of a qualified number of bits to be zero. Then, if the check on the tag is found to be correct it is a matter of known chance whether or not the content of the remainder of the page related to the tag is also written correctly.

Figure 4 summarizes the sequence of operations carried out by the memory

manager 4-in one embodiment of the invention when updating a version of stored application data, as directed by an application program running on the central processing unit 2:

- a. allocating a new set of pages in the memory 10, step 40;
- b. defining the tag value of each new page of the new set of pages, step 42;
- 5 c. writing the application program data in its amended form and the corresponding tags to memory 10 page by page, step 44;
- d. verifying for each page written that the result is correct, step 46;
this verification step may be carried out by checking the tag value as indicated above;
- 10 e. de-allocating pages that hold the oldest generation of the set of data, step 48.

The tag value for each new page is defined with the assigned chunk identifier chid, the generation count value gen# of the most recently previous updated version incremented by 1, and the page count pg#.

- Preferably, the pages are written to memory 10 page by page as indicated in step
- 15 c. above. Preferably one predetermined page of the set of pages for one set of data must be written last, whereas all other pages can be written in any order. Conveniently, that predetermined page is the first page of the new set of pages. In practice, any of the pages may be written in parts. For example, a tag value of the page may be written separately from the application program data in the page. Preferably, however, the tag of the predetermined page, which is the last page to be written, is written in the last step of the updating
 - 20 action. This is a clear indication that the updating action has been completed. Until that tag of the predetermined page is written in memory, application program data written to any of the new pages may also be modified. However, it is to be noted that partial writes and modifications to page data may reduce the benefits obtainable with the invention, i.e., the
 - 25 total writing time may get longer. Writing the non-volatile memory 10, like EPROM, takes a relatively long time, nowadays about 3 msec. Therefore, it is best to write only once to memory 10, i.e., when the entire modified set of data is ready to be stored and not to write modified portions of the set of data in consecutive periods of time. Still, if time is available, as is often the case, it is common practice in the art to write modified portions of
 - 30 a set of data in non-volatile memory. However, this results in an increased number of write operations which leads to unnecessary wear of the non-volatile memory 10.

Therefore, in accordance with an embodiment of the invention, preferably, all steps necessary to completely amend a set of data are carried out on a working copy of the

set of data in RAM 8 prior to writing the amended set of data to non-volatile memory 10.

Writing the tag value of the predetermined page as the last operation in an update session is an advantageous measure in realizing the atomicity of the multi-page update. The presence or absence of a valid tag in the predetermined page then serves as a
5 "commit" flag: a valid tag in the predetermined page indicates both the validity of the written page and the irrevocable completion of the entire update process.

Memory storage of the application program data can be made even more secure when the data stored in the memory can only be addressed physically by the application using the chunk identifier chid. The memory 10 then has become a "content addressable
10 memory" (CAM).

Although the memory manager 4 and the central processing unit 2 may be within one physical processing unit, it is especially advantageous for this latter feature that the central processing unit 2 and the memory manager 4 are two physically distinct units arranged to communicate with one another. It is to be understood that "physically distinct"
15 may still refer to units manufactured on a single chip. Then, the physical address space of the memory 10 is not included in the address space of the central processing unit 2, specifically not in the address space where application program or operating system software instructions are stored. If, then, the memory manager 4 is also made tamper-resistant (like in a smart card), additional protection against "probing" will be obtained.

20 To realize this potential additional protection for e.g. smart cards, the memory manager 4 may provide additional interface functionality, e.g., containing a tag-size address register 54 and a page-data size data register 52 (see figure 5). This interface 52, 54 is then complemented with a logic unit 50 to carry out logic functions for scanning and matching tags stored in the memory 10. In other words, the logic unit 50 is able to read
25 tags from memory 10 and to address the memory 10 by analyzing the value of the tags.

The interface 52, 54 and associated logic unit 50 may be implemented in hardware.

In addition, specific hardware circuits 56, 58 will be present as interfaces between the memory 6, 8, 10 and the logic unit 50 and between the central processing unit 2 and
30 the logic unit 50, respectively. The logic unit 50 may provide a dedicated address counter combined with a tag-comparing logic circuit. An alternative hardware circuit may contain content addressable memory logic circuits implemented per memory page at least for the storage bits reserved to contain the tag value.

Additional security benefits may be obtained with a memory managed according to the invention when in addition to the special detecting encoding the tag value is further encoded using cryptographic techniques. Such cryptographic tag encoding intends to hide application data related to structural information like chunk identifier chid, generation count gen#, page count pg#, contained in the tag values. Cryptographic encoding may be done with any encoding technique known to a person skilled in the art. One advantageous method includes the use of secret cryptographic one-way functions in which the one-way function steps are related to a secret key only known to the memory manager 4. In this way, the memory manager 4 is able to recognize a previous generation by applying the one-way function one or more times to the encoded tag value of that previous generation and then comparing the resulting tag value with the tag value of the most recently updated generation. This will hamper reconstruction of application program data from an evil-intended forced "dump" of the memory device content.

The tagged memory structure as explained hereinbefore provides several advantageous options. For instance, the tag may include additional data to indicate ownership of the associated application program data. Moreover, such additional data in the tag value might indicate use-rights or sets of use-rights for different users of the application program data. Such different use-rights may, e.g., be related to different access conditions to different parts of the (application) program data in the memory 10. One part of the (application) program data may, e.g., be defined as read-only, whereas another part of the application program data may be defined to be read/write access.

The invention efficiently provides a transaction log stored in memory since the memory contains the history of updates to specific application data-elements in the form of consecutive generations.

As explained above, additionally, the number of write operations to memory devices managed in accordance with the present invention may be reduced using the memory-update/transaction logging mechanism disclosed. Additionally, a reduced number of write operations provided by the invention may result in reduced costs of the silicon storage device by extending its useful life. Security of data stored in, especially, the non-volatile memory on tamper-resistant single chip computers, like smart cards, is increased. The increase of security may be entirely obtained by software measures. Hardware measures, like the distinct memory manager 4 apart from the central processing unit 2, may further increase the security but are not strictly necessary.

Claims

1. A computer-readable medium storing a data structure for supporting persistent storage of a set of data, said data structure comprising:
 - 5 (a) at least an oldest version of said set of data in a first memory area, said first memory area including at least one first tag for uniquely identifying said oldest version, and
 - (b) at least a most recently updated version of said set of data in a second, distinct memory area, said second memory area including at least one second tag for
10 uniquely identifying said most recently updated version.
2. A computer-readable medium according to claim 1, wherein each of the versions of said set of data are stored in one or more memory pages, and each of the memory pages includes one tag comprising references to said set of data, a version number and a page
15 number.
3. A computer-readable medium according to claim 2, wherein each page corresponds to one word line.
- 20 4. A computer arrangement including a processor (2; 2, 4) and at least one computer-readable medium according to any of the preceding claims, said processor (2; 2, 4) being arranged to process said data structure.
5. A computer arrangement according to claim 4, wherein the processor (2; 2, 4) is
25 arranged to write tags with redundancy as to their content and, after having read tags from the memory means, to analyze from said redundancy whether or not write errors have occurred.
6. A computer arrangement according to claims 4 or 5, wherein the most recently
30 updated version comprises a plurality of pages, each page having a unique tag, and the processor (2; 2, 4) is arranged for updating said most recently updated version of said set of data and to write a predetermined tag of a predetermined one of said plurality of pages into said memory means as a last step of said updating.

7. A computer arrangement according to any of the claims 4 through 6, wherein at least one of said tags includes additional data as to indicate ownership and use-rights, and the processor (2; 2, 4) is arranged to recognize ownership and use-rights from these additional data.

8. A computer arrangement according to claim 7, wherein said use-rights differ for different parts of the set of data and the processor (2; 2, 4) is arranged to recognize different use-rights for these different parts.

10

9. A computer arrangement according to any of the claims 4 through 8, wherein the processor (2; 2, 4) is arranged to analyze tag values and is only allowed to access said versions of said set of data by reference through said tag values.

10. A computer arrangement according to claim 9, wherein said processor comprises a central processing unit (2) and a distinct memory managing unit (4), and the tag values are only known to the memory managing unit (4).

11. A computer arrangement according to claim 10, wherein said memory managing unit (4) encodes tags with a cryptographic key prior to writing them into the computer-readable medium, said cryptographic key being only known to the memory managing unit (4).

12. A computer arrangement according to claim 11, wherein said cryptographic key relates to a cryptographic one-way function.

13. A method for supporting persistent storage of a set of data, comprising the steps of:

(a) storing an oldest version of said set of data in a first memory area, wherein said first memory area includes a first tag for uniquely identifying said oldest version, and

(b) storing a most recently updated version of said set of data in a second distinct memory area, wherein said second memory area includes a second tag for

uniquely identifying said most recently updated version.

14. Method according to claim 13, comprising the further step of verifying said storing in step (b) by a predetermined operation carried out on said second tag.

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15. Method of updating a set of data according to claim 13, wherein said most recently updated version comprises a plurality of pages, each page having a unique tag, and a predetermined tag of a predetermined one of said plurality of pages is stored as a last step in step (b) in order to identify completion of said storing in step (b).

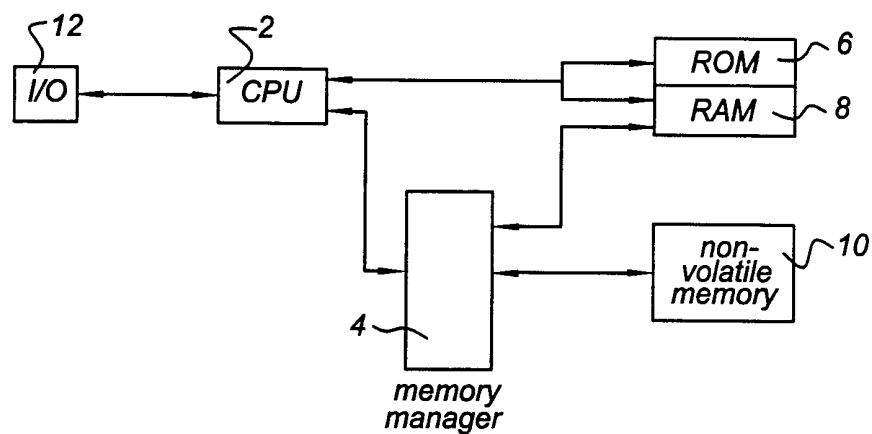
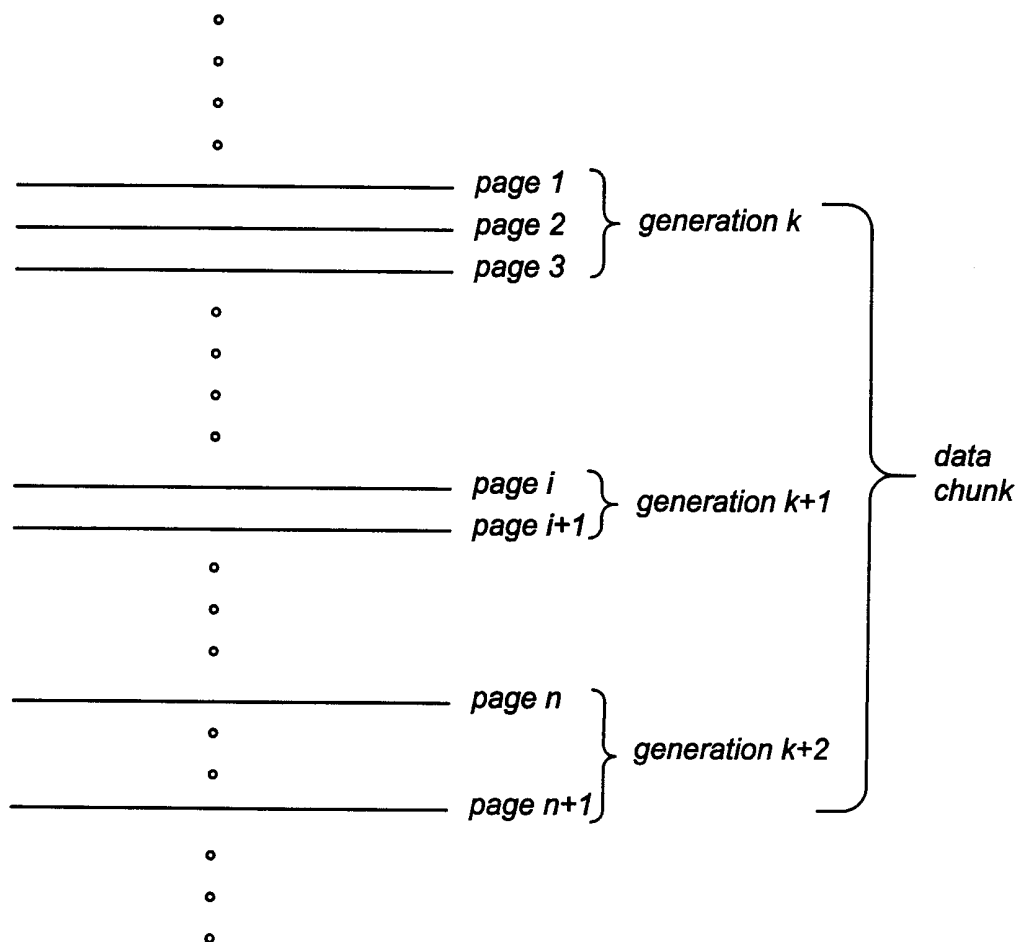
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16. Method of updating a set of data according to claim 13, further including the following step after step (b):

(c). de-allocating memory area having stored therein the oldest version of said set of data provided at least two versions of said set of data remain in said memory means (10).

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Fig 1*Fig 2*

2/3

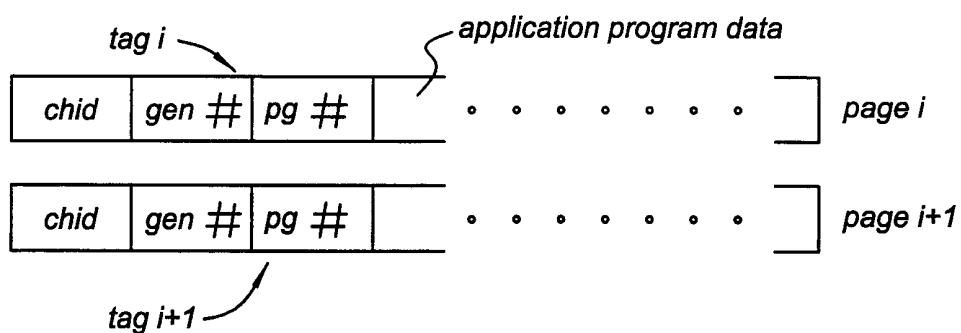
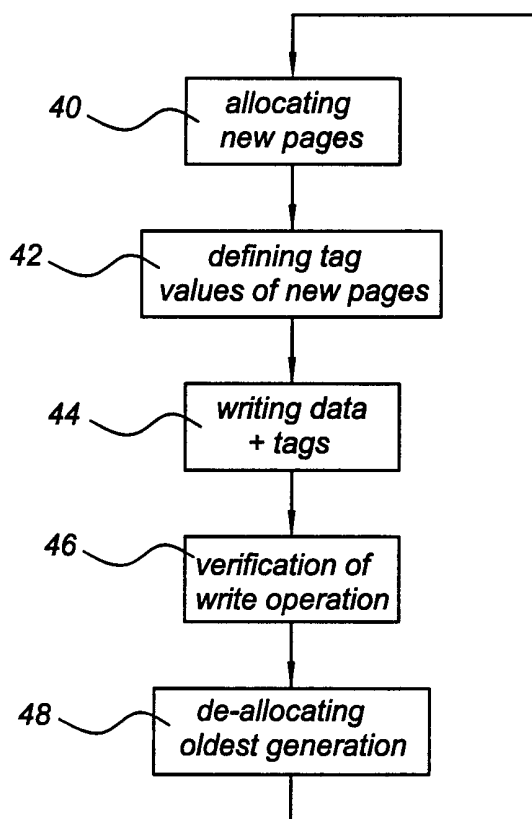
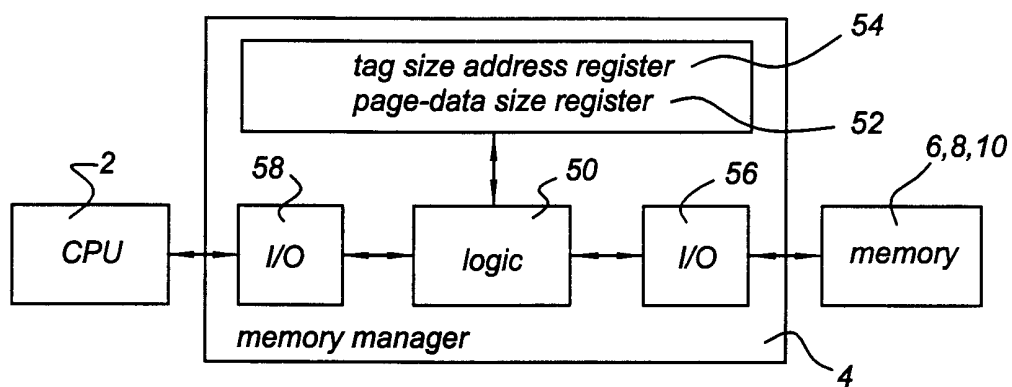
Fig 3**Fig 4**

Fig 5

INTERNATIONAL SEARCH REPORT

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PCT/NL 99/00360

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F11/14

According to International Patent Classification (IPC) or to both national classification and IPC

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IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DE 196 00 081 A (INTERNATIONAL BUSINESS MACHINES CORP.) 17 July 1997 (1997-07-17) the whole document	1-6, 13-16
A	US 5 896 393 A (YARD ET AL.) 20 April 1999 (1999-04-20) column 3, line 16 - line 33	1-6, 13-16
A	EP 0 723 226 A (HEWLETT-PACKARD COMPANY) 24 July 1996 (1996-07-24) abstract	1-6, 13-16



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

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Date of the actual completion of the international search

13 March 2000

Date of mailing of the international search report

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Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Corremans, G

INTERNATIONAL SEARCH REPORT

Information on patent family members

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