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(54) METHODS FOR FORMING BARRIER/SEED LAYERS FOR COPPER INTERCONNECT STRUCTURES

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(57) ABSTRACT

Methods for forming barrier/seed layers for interconnect structures are provided herein. In some embodiments, a method of processing a substrate having an opening formed in a first surface of the substrate, the opening having a sidewall and a bottom surface, the method may include forming a layer comprising manganese (Mn) and at least one of ruthenium (Ru) or cobalt (Co) on the sidewall and bottom surface of the opening; and depositing a conductive material on the layer to fill the opening. In some embodiments, one of ruthenium (Ru) or cobalt (Co) is deposited on the sidewall and bottom surface of the opening. The materials may be deposited by chemical vapor deposition (CVD) or by physical vapor deposition (PVD).

204

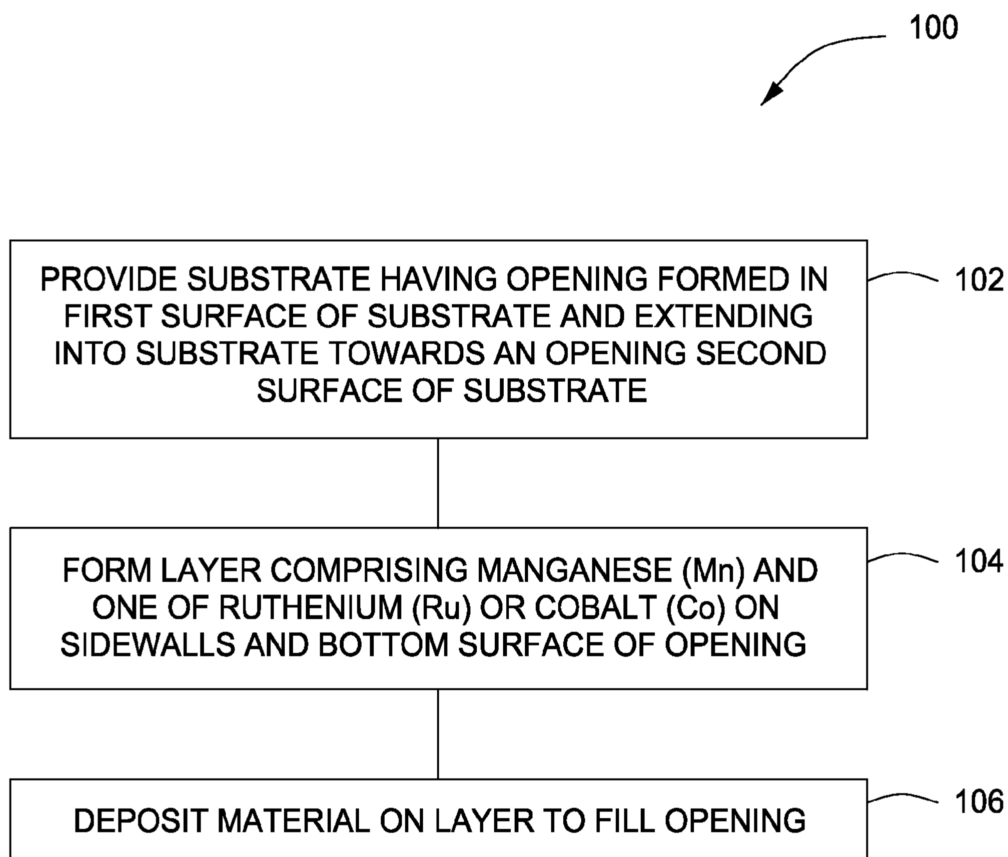

FIG. 1

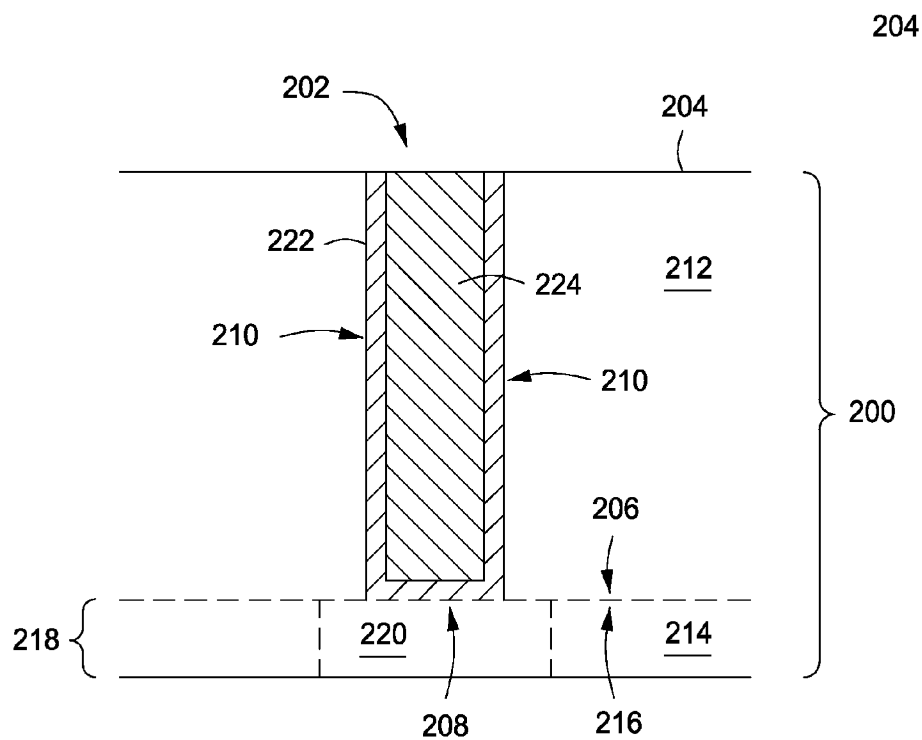

FIG. 2

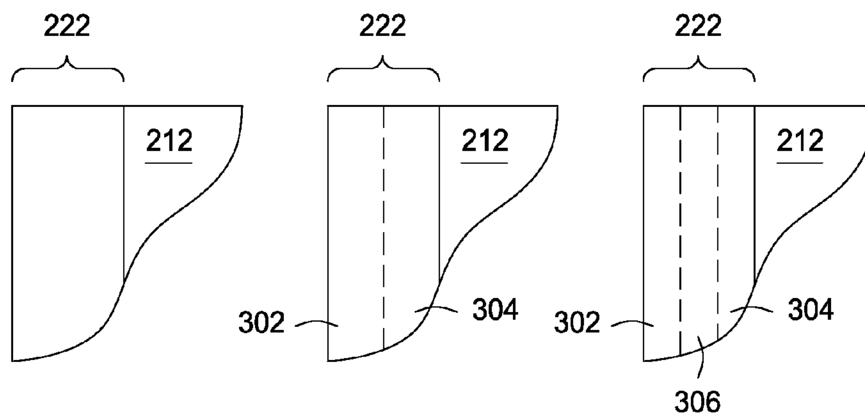

FIG. 3A FIG. 3B FIG. 3C

METHODS FOR FORMING BARRIER/SEED LAYERS FOR COPPER INTERCONNECT STRUCTURES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims benefit of U.S. provisional patent application Ser. No. 61/365,082, filed Jul. 16, 2010, which is herein incorporated by reference.

FIELD

[0002] Embodiments of the present invention generally relate to methods of processing substrates, and specifically to methods for forming a barrier/seed layers for interconnect structures.

BACKGROUND

[0003] As device nodes get smaller (for example, approaching dimensions of about **22** nm or less), manufacturing challenges become more apparent. For example, the combined thickness of barrier and seed layers of typical materials deposited in an opening prior to filling the opening, for example via electroplating, to form an interconnect structure may result in reduced efficiency of the electroplating process, reduced process throughput and/or yield, or the like.

[0004] Ruthenium, deposited for example by chemical vapor deposition (CVD), has become a promising candidate as a seed layer for a copper interconnect. However, ruthenium by itself cannot be a copper barrier and barrier layers such as TaN/Ta are still needed prior to ruthenium deposition. Alternatively, copper-manganese, deposited for example by physical vapor deposition (PVD), self-aligned barrier schemes have also gained in popularity as a desirable approach to the barrier solution. However, the inventors have observed that these two schemes each have manufacturability difficulties.

[0005] For CVD ruthenium, the deposition rate is very slow without O_2 as reducing gas. However, the O_2 gas tends to oxidize the tantalum-based barrier layer, resulting in increase via resistance. Therefore, with TaN/Ta as barrier, throughput with CVD ruthenium will be very slow. In addition, deposition of ruthenium without O_2 also results in high carbon contaminated ruthenium films, which also increases line/via resistance. A high resistivity ruthenium film is not adequate for a seed layer, which is the main merit of the ruthenium seed layer.

[0006] With respect to the Cu—Mn process (a physical vapor deposition, or PVD, process), copper can diffuse into the oxide layer, especially low-k oxide, during the deposition steps, causing reliability issues.

[0007] Thus, the inventors have provided improved methods for forming barrier/seed layers for interconnect structures.

SUMMARY

[0008] Methods for forming barrier/seed layers for interconnect structures are provided herein. In some embodiments, a method of processing a substrate having an opening formed in a first surface of the substrate, the opening having a sidewall and a bottom surface, the method may include forming a layer comprising manganese (Mn) and at least one of ruthenium (Ru) or cobalt (Co) on the sidewall and bottom surface of the opening; and depositing a conductive material on the layer to fill the opening. In some embodiments, one of ruthenium (Ru) or cobalt (Co) is deposited on the sidewall and bottom surface of the opening. The materials may be deposited by chemical vapor deposition (CVD) or by physical vapor deposition (PVD).

[0009] Other and further embodiments of the present invention are described below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Embodiments of the present invention, briefly summarized above and discussed in greater detail below, can be understood by reference to the illustrative embodiments of the invention depicted in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0011] FIG. **1** depicts a flow chart of a method for forming an interconnect structure in accordance with some embodiments of the present invention.

[0012] FIG. **2** depicts a side cross-sectional view of an interconnect structure formed in a substrate in accordance with some embodiments of the present invention.

[0013] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. The figures are not drawn to scale and may be simplified for clarity. It is contemplated that elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

DETAILED DESCRIPTION

[0014] Methods for forming barrier/seed layers for interconnect structures are provided herein. As discussed below, the term barrier/seed layer is meant to include any of a layer comprising a seed layer deposited atop a barrier layer, or a layer comprising a barrier layer material and a seed layer material, wherein the barrier and seed layer materials may be deposited in any suitable manner, such as homogenously, graded, or the like within the layer to facilitate both barrier layer and seed layer properties. The inventive methods advantageous facilitate improved efficiency, process throughput, and device quality through one or more of reduced barrier/seed layer thickness, reduced barrier/seed layer resistance, or increased deposition rates. The inventive methods may be utilized with any device nodes, but may be particularly advantageous in device nodes of about 22 nm or less. Further, the inventive methods may be utilized with any type of interconnect structure or material, but may be particularly advantageous with interconnect structures formed by electroplating copper (Cu).

[0015] FIG. **1** depicts a flow chart of a method **100** for forming an interconnect structure in accordance with some embodiments of the present invention. The method **100** is described below with respect to an interconnect structure, as depicted in FIG. **2**. The method **100** may be performed in any suitable process chambers configured for one or more of PVD, chemical vapor deposition (CVD), or atomic layer deposition (ALD). Exemplary processing systems that may be used to perform the invention methods disclosed herein may include, but are not limited to, those of the ENDURA®, CENTURA®, or PRODUCER® line of processing systems, and the ALPS® Plus or SIP ENCORE® PVD process chambers, all commercially available from Applied Materials, Inc.,

of Santa Clara, Calif. Other process chambers, including those from other manufacturers, may also be suitably used in connection with the teachings provided herein.

[0016] The method **100** generally begins at **102** by providing a substrate **200** having an opening **202**, as depicted in FIG. **2**. The opening **202** may be formed in a first surface **204** of the substrate **200** and extending into the substrate **200** towards an opposing second surface **206** of the substrate **200**. The substrate **200** may be any suitable substrate having an opening formed therein. For example, the substrate **200** may comprise one or more of a dielectric material, Si, metals, or the like. In addition, the substrate **200** may include additional layers of materials or may have one or more completed or partially completed structures formed therein or thereon. For example, the substrate **200** may include a first dielectric layer **212**, such as silicon oxide, low-k, or the like, and the opening **202** may be formed in the first dielectric layer **212**. In some embodiments, the first dielectric layer **212** may be disposed atop a second dielectric layer **214**, such as silicon oxide, silicon nitride, silicon carbide, or the like. A conductive material (e.g., **220**) may be disposed in the second dielectric layer **214** and may be aligned with the opening **202** such that the opening, when filled with a conductive material, provides an electrical path to/from the conductive material. For example, the conductive material may be part of a line or via to which the interconnect is coupled.

[0017] The opening **202** may be any opening, such as a via, trench, dual damascene structure, or the like. In some embodiments, the opening **202** may have a height to width aspect ratio of at least about 5:1 (e.g., a high aspect ratio). For example, in some embodiments, the aspect ratio may be about 10:1 or greater, such as about 15:1. The opening **202** may be formed by etching the substrate using any suitable etch process. The opening **202** includes a bottom surface **208** and sidewalls **210**.

[0018] In some embodiments, the sidewalls **210** may be covered with one or more layers prior to depositing metal atoms as described below. For example, the sidewalls of the opening **202** and the first surface **204** of the substrate **200** may be covered by an oxide layer (not shown), such as silicon oxide (SiO_2), silicon carbon nitride, silicon oxicarbide, or the like. The oxide layer may be deposited or grown, for example in a chemical vapor deposition (CVD) chamber or in an oxidation chamber. The oxide layer may serve as an electrical and/or physical barrier between the substrate and one or more of the seed layer or barrier layer materials to be subsequently deposited in the opening, and/or may function as a better surface for attachment during the deposition process discussed below than a native surface of the substrate, and/or may provide a source of oxygen which may be combined with a barrier layer material by annealing or the like to form a final barrier layer and/or barrier layer component of a barrier/seed layer.

[0019] In some embodiments, and as illustrated by dotted lines in FIG. **2**, the opening **202** may extend completely through the substrate **200** and an upper surface **216** of a second substrate **218** may form the bottom surface **208** of the opening **202**. The second substrate **218** may be disposed adjacent to the second surface **206** of the substrate **200**. Further (and also illustrated by dotted lines), a conductive material (e.g., **220**), for example as part of a device, such as a logic device or the like, or an electrical path to a device requiring electrical connectivity, such as a gate, a contact pad, a conductive line or via, or the like, may be disposed in the upper surface **216** of the second substrate **218** and aligned with the opening **202**. In some embodiments, the conductive material **220** aligned with the opening **202** may comprise Cu.

[0020] At **102**, a layer **222** is formed on the sidewalls **210** and the bottom surface **208** of the opening **202**. The layer **222** comprises manganese (Mn) and at least one of ruthenium (Ru) or cobalt (Co). In some embodiments, the layer **222** comprises manganese (Mn) and one of ruthenium (Ru) or cobalt (Co). In some embodiments, the layer **222** may be a single layer having uniform or non-uniform composition through a thickness of the layer. In some embodiments, the layer **222** may be formed from multiple layers deposited atop each other. For example, FIG. **3**A depicts the layer **222** formed as a single layer. FIG. **3**B depicts the layer **222** formed as two layers, a first layer **302** and a second layer **304** deposited atop the first layer **302**. FIG. **3**C depicts the layer **222** formed as two layers **302**, **304** having a transitional region **306** disposed between the two layers.

[0021] For example, in some embodiments, the layer **222** may comprise a barrier layer comprising predominantly Mn and a seed layer comprising predominantly Ru or predominantly Co deposited atop the barrier layer. Alternatively, in some embodiments, the layer **222** may comprise a barrier layer material comprising predominantly Mn and a seed layer material comprising predominantly Ru or predominantly Co, wherein the barrier and seed layer materials are deposited throughout the thickness of the layer **222**. For example, the layer **222** may comprise about 10-50 percent, or more, of Mn proximate an interface between the layer **222** and the sidewalls **210** or the bottom surface **208** and may comprise substantially Ru or Co (e.g., about 50 percent or more) proximate an opposing surface of the layer **222**.

[0022] The layer **222** may have a graded concentration of the barrier layer (e.g., Mn) and seed layer (e.g., Ru or Co) materials between the interface and the opposing surface of the layer **222**. For example, the barrier layer material may decrease in concentration from the interface to the opposing surface of the layer **222** and the seed layer material may increase in concentration from the interface to the opposing surface of the layer **222**. In addition, the layer **222** may have a first composition in a first portion of the layer **222** proximate the interface between the layer **222** and the substrate **200**, a second composition in a second portion of the layer **222** proximate the interface between the layer **222** and the opening **202**, with a transitional region disposed therebetween. In some embodiments, when moving from the first portion towards the second portion of the transitional region (e.g., from adjacent the substrate towards the opening), the concentration of the barrier layer material may decrease and the concentration of the seed layer material may increase.

[0023] The layer **222** may be formed by CVD, ALD, or PVD processes. For example, a CVD process may be used to deposit any of the aforementioned embodiments of the layer **222** discussed above. For example, in some embodiments, the CVD process may comprise flowing a manganese-containing gas for a first period of time to deposit the barrier layer and then flowing one of a ruthenium-containing gas or a cobalt-containing gas for a second period of time to deposit the seed layer. In some embodiments, the flow of the manganese-containing gas and the ruthenium-containing gas or the cobalt-containing gas may overlap for a third period of time, during which a transitional region of the layer **222** may be deposited. Each of the preceding steps may further comprise flowing a reducing agent along with the precursor gas. The

reducing agent may comprise, for example, at least one of hydrogen (H_2), ammonia (NH_3), oxygen (O_2), or hydrogen incorporated gases or the like.

[0024] In some embodiments, to achieve a graded concentration of the barrier layer material and the seed layer material during the co-flow step above, a ratio of the manganese-containing gas and one of the ruthenium-containing gas or the cobalt-containing gas may be decreased between a beginning and an end of the third period of time. For example, the ratio may be decreased in steps, for example, wherein each step comprises tuning the ratio at a desired value and flowing at that value for a portion of the third period of time. Alternatively, the ratio may be decreased continuously between the beginning and the end of the second period of time. For example, upon or after beginning the flow of the ruthenium-containing gas or the cobalt-containing gas, the flow of the manganese-containing gas may be reduced until it is stopped. In addition, the flow of the ruthenium-containing gas or the cobalt-containing gas may be kept constant or may be increased during the third period of time.

[0025] In some embodiments, for example in an ALD process, a reducing agent, as discussed above, may be flowed simultaneously with or alternately with the flow of the manganese-containing gas and the one of the ruthenium-containing gas or the cobalt-containing gas. In addition, the flows of the respective gases may be alternated with a purge gas flow, such that there is a period of deposition followed by a purge of the chamber to define a deposition cycle, and the deposition cycle is repeated as desired to deposit a desired thickness of material to form the layer **222**. In some embodiments, the deposition cycle may be maintained or may be varied throughout multiple deposition steps to obtain a film composition through the layer **222** in any of the desired embodiments as discussed above. For example, the deposition cycle may be uniform to deposit a layer **222** having a substantially uniform composition throughout. Alternatively, the deposition cycle may be varied to deposit a layer **222** having a desired composition of manganese and ruthenium or cobalt in various locations throughout the layer **222**, as described above.

[0026] General processing conditions for any of the CVD or ALD processes discussed above may include any one or more of forming the layer **222** at a temperature ranging from about 100 degrees Celsius to about 400 degrees Celsius, maintaining chamber pressure at about 1 to about 30 Torr, or about 5 to about 10 Torr. The manganese-containing gas may comprise at least one manganese precursor as disclosed in United States Published Patent Application no. 2009/0263965, filed Mar. 20, 2009, by Roy G. Gordon et al., and entitled, "Self-aligned barrier layers for interconnects," which is hereby incorporated herein by reference in its entirety. The ruthenium-containing gas may comprise at least one of Methyl-cyclohexadine Ru tricarbonylcyclohexadine, Ru tricarbonyl, butadiene Ru tricarbonyl, dimethyl butadiene Ru tricarbonyl, or modified dines with $Ru(CO)_3$. The cobalt-containing gas may comprise at least one of a cobalt precursor disclosed in United States Published Patent Application no. 2009/0053426, filed Aug. 29, 2008, by Jiang Lu et al., and entitled, "Cobalt deposition on barrier surfaces," which is hereby incorporated herein by reference in its entirety.

[0027] Alternatively, the layer **222** may be deposited by a PVD process. For example, metal atoms may be sputtered from a target comprising predominantly Ru or Co and further comprising Mn to form the layer **222**. For example, the target may comprise one of manganese-ruthenium or manganese-cobalt. In some embodiments, the target may be predominantly ruthenium or predominantly cobalt and may have a manganese content ranging from about 0.1 to about 15 percent. After the metal atoms have been sputtered onto the sidewalls **210** and the bottom surface **208**, the layer **222** may be annealed to form an oxide layer comprising manganese, silicon, and oxygen at an interface between the layer **222** and the surfaces of the opening **202**. For example, the silicon and oxygen may be present due to the presence of a native or deposited layer of silicon oxide, or other oxygen-containing dielectric, as discussed above. In some embodiments, the oxide layer is $MnSi_xO_y$. As a result of oxide layer formation during annealing, some of the Ru or Co present in the layer **222** may become oxidized, which may unfavorably increase resistance of the layer **222** for electroplating purposes. Accordingly, a reducing agent, such as H_2 or the like, may be provided after the annealing process is completed to reduce the oxidized Ru or Co formed during the anneal. In some embodiments, the substrate may be exposed to an atmosphere comprising H_2 to reduce the oxidized Ru or Co.

[0028] At **106**, a conductive material **224** may be deposited to on the layer **222** to fill the opening **202**. As discussed above, the conductive material **224** may be deposited by an electroplating or a similar processing technique. The layer **222** may function as a seed layer upon which the conductive material **224** is deposited. The conductive material **224** may include metals, metal alloys, or the like, such as one or more of copper (Cu), Al, W, or the like. In some embodiments, the conductive material **224** is Cu.

[0029] Thus, methods for forming barrier/seed layers for interconnect structures have been provided herein. The inventive methods advantageously facilitate improved efficiency, process throughput, and device quality through one or more of reduced barrier/seed layer thickness, reduced barrier/seed layer resistance, or increased deposition rates. The inventive methods may be utilized with any device nodes, but may be particularly advantageous in device nodes of about 22 nm or less. Further, the inventive methods may be utilized with any type of interconnect structure or material, but may be particularly advantageous with interconnect structures formed by electroplating Cu.

[0030] While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof.

1. A method of processing a substrate having an opening formed in a first surface of the substrate, the opening having a sidewall and a bottom surface, the method comprising:
- forming a layer comprising manganese (Mn) and at least one of ruthenium (Ru) or cobalt (Co) on the sidewall and bottom surface of the opening; and
- depositing a conductive material on the layer to fill the opening.

2. The method of claim **1**, wherein the opening has an aspect ratio of height to width of at least 5:1.

3. The method of claim **1**, wherein the conductive material is deposited by an electroplating process.

4. The method of claim **3**, wherein the conductive material is copper (Cu).

5. The method of claim **1**, further comprising:

(a) flowing a manganese-containing gas for a first period of time;

(b) flowing the manganese-containing gas and one of a ruthenium-containing gas or a cobalt-containing gas for a second period of time; and

(c) flowing either of the ruthenium-containing gas or the cobalt-containing gas flowed in step (b) for a third period.

6. The method of claim **5**, wherein each of steps (a), (b) and (c) further comprise:

flowing a reducing agent.

7. The method of claim **6**, wherein the reducing agent comprises at least one of hydrogen (H_2), ammonia (NH_3), oxygen (O_2), hydrocarbon compounds, or hydrogen incorporated compounds.

8. The method of claim **5**, wherein a ratio of the manganese-containing gas to one of the ruthenium-containing gas or the cobalt-containing gas is decreased between a beginning and an end of the second period of time.

9. The method of claim **8**, wherein the ratio is decreased in steps, each step flowing a desired ratio for a period of time.

10. The method of claim **8**, wherein the ratio is decreased continuously between the beginning and the end of the second period of time.

11. The method of claim **5**, wherein step (b) further comprises:

(b1) flowing the manganese-containing gas for a fourth period; and

(b2) flowing one of the ruthenium-containing gas or the cobalt-containing gas for a fifth period.

12. The method of claim **11**, wherein step (b) further comprises:

(b3) alternately repeating steps (b1) and (b2).

13. The method of claim **1**, wherein forming the layer further comprises:

forming the layer at a temperature ranging from about 130 to about 350 degrees Celsius.

14. The method of claim **1**, wherein the bottom surface of the opening comprises copper (Cu).

15. The method of claim **1**, wherein forming the layer further comprises:

sputtering metal atoms from a target comprising manganese (Mn) and one of ruthenium (Ru) or cobalt (Co) to form the layer.

16. The method of claim **15**, wherein the target consists essentially of manganese and ruthenium or consists essentially of manganese and cobalt.

17. The method of claim **15**, wherein the target is predominantly ruthenium (Ru) or predominantly cobalt (Co) and has a manganese content ranging from about 10 to about 15 percent.

18. The method of claim **15**, further comprising:

annealing the layer to form an oxide layer comprising manganese, silicon and oxygen at an interface between the layer and the surfaces of the substrate and the opening.

19. The method of claim **14**, further comprising:

flowing a reducing agent to reduce one of oxidized ruthenium or oxidized cobalt formed during the annealing step.

20. A method of processing a substrate having an opening formed in a first surface of the substrate, the opening having a sidewall and a bottom surface, the method comprising:

forming a layer comprising manganese (Mn) and one of ruthenium (Ru) or cobalt (Co) on the sidewall and bottom surface of the opening; and

depositing a conductive material on the layer to fill the opening.

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