

- [54] **DIPLESS CROSS FADER WITH PILE-ON**
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315/314, 328/104
 [51] Int. Cl. **G05f 1/10, H05b 37/00**
 [58] Field of Search **307/4, 157; 315/199, 293,**
315/294, 295, 296, 297, 298, 299, 311, 314,
315, 321, 322; 321/17, 27; 328/104, 159

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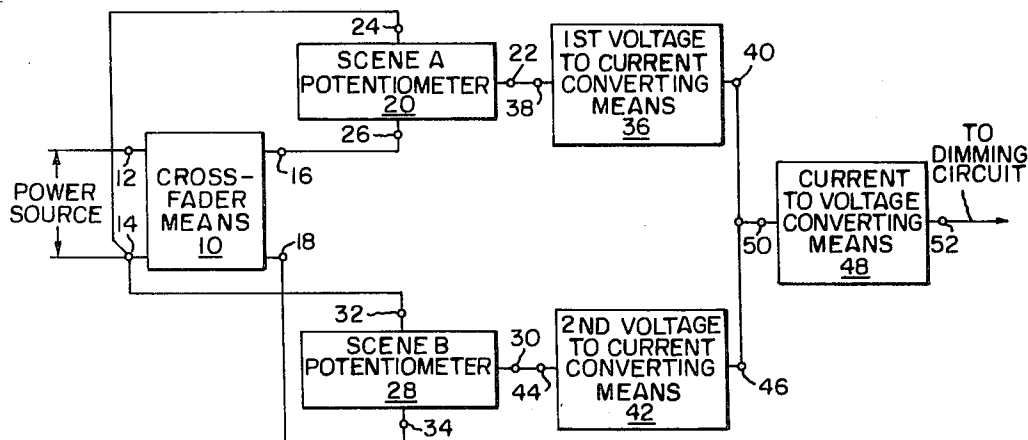
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[57] **ABSTRACT**

A stage lighting circuit for supplying a dipless signal to be connected to a dimmer. The circuit comprises a cross-fader, two scene potentiometers, voltage to current converting means, and a current to voltage converting means, whereby, in normal cross-fading operation, a signal which is proportional to the sum of the signals on the scene potentiometers is produced, thereby avoiding dipping of the signal during cross-fading. Preferably the circuit also provides means for blocking the normal summed signal when the cross-fader is operated in a "pile-on" mode and producing a signal proportional to the higher of the settings on the two scene potentiometers.

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10 Claims, 8 Drawing Figures



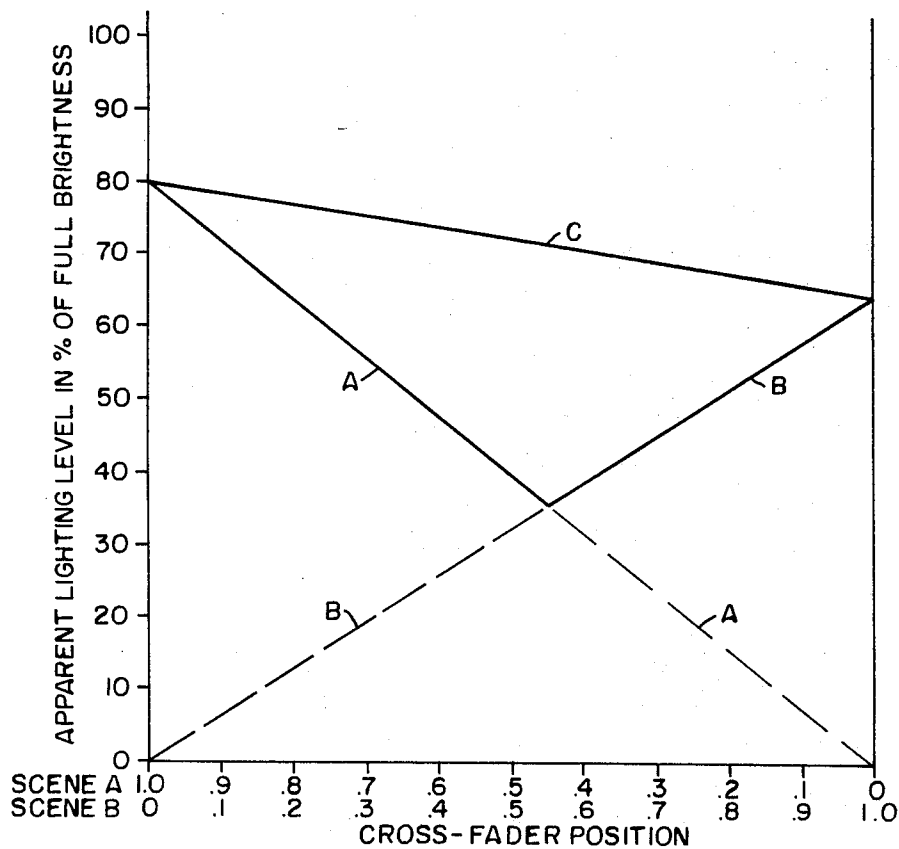


FIG. 1

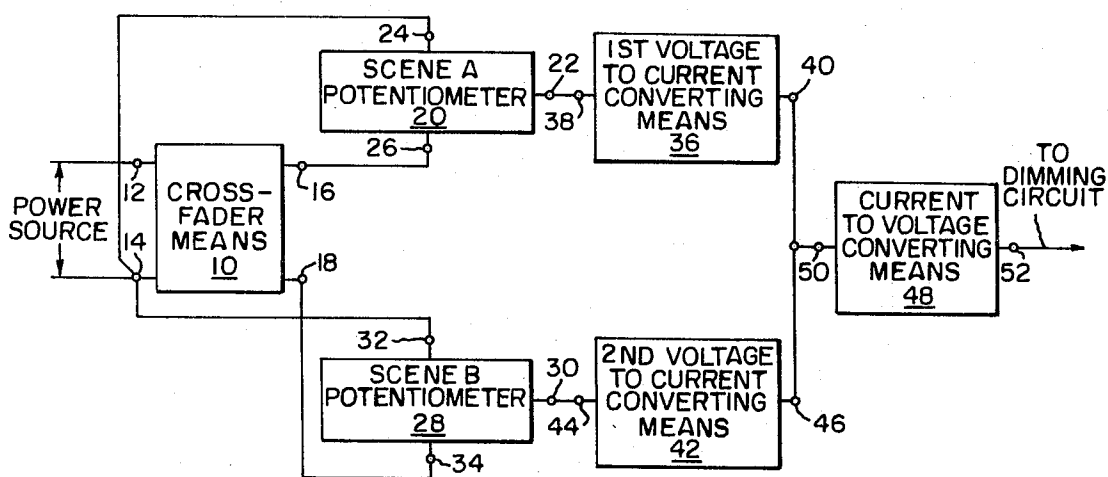


FIG. 2

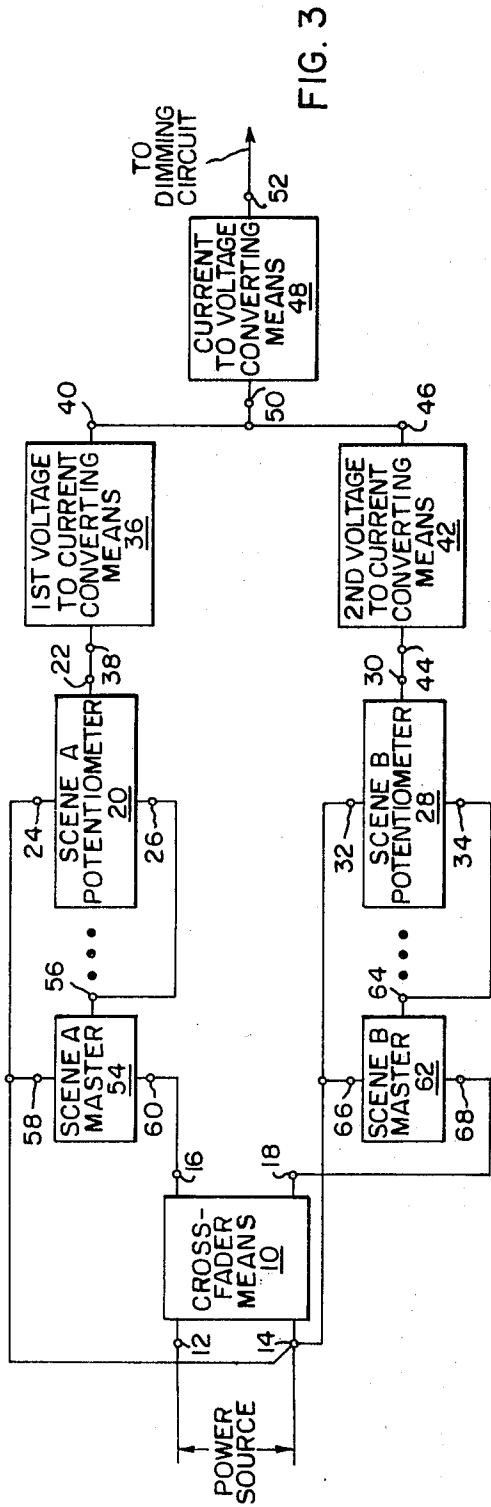


FIG. 3

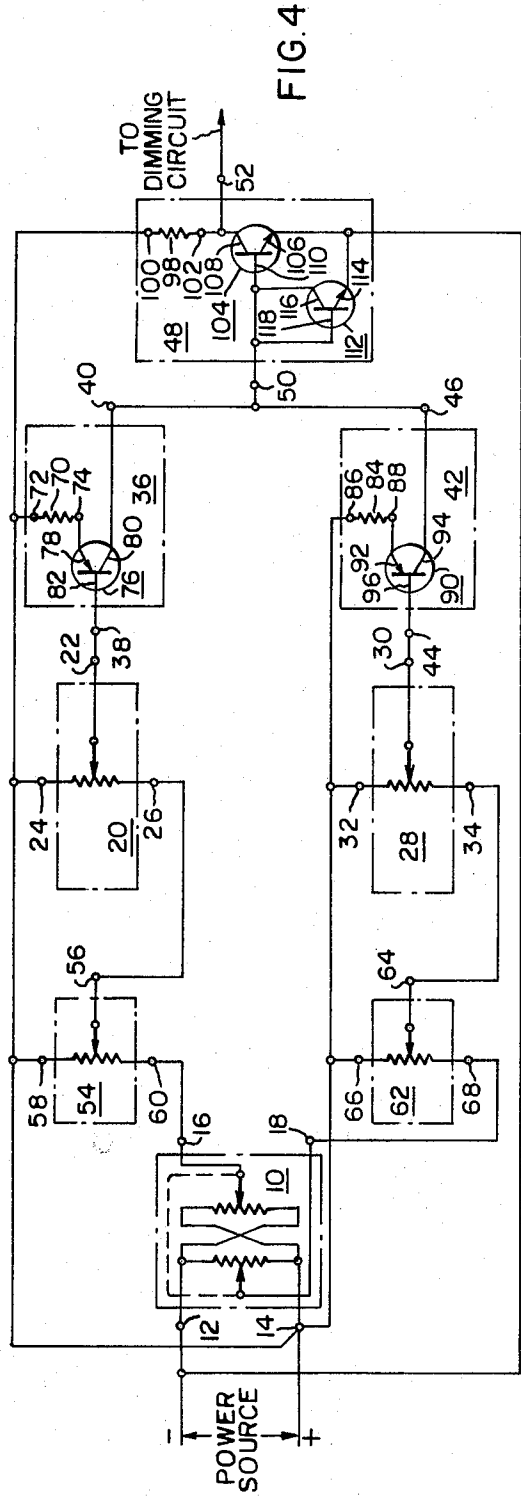


FIG. 4

FIG. 5

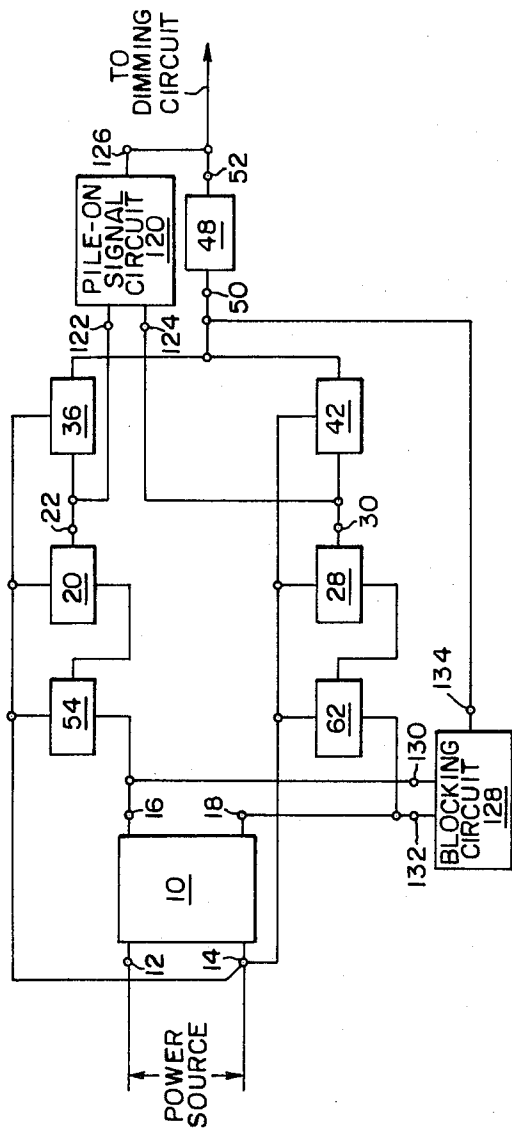


FIG. 6

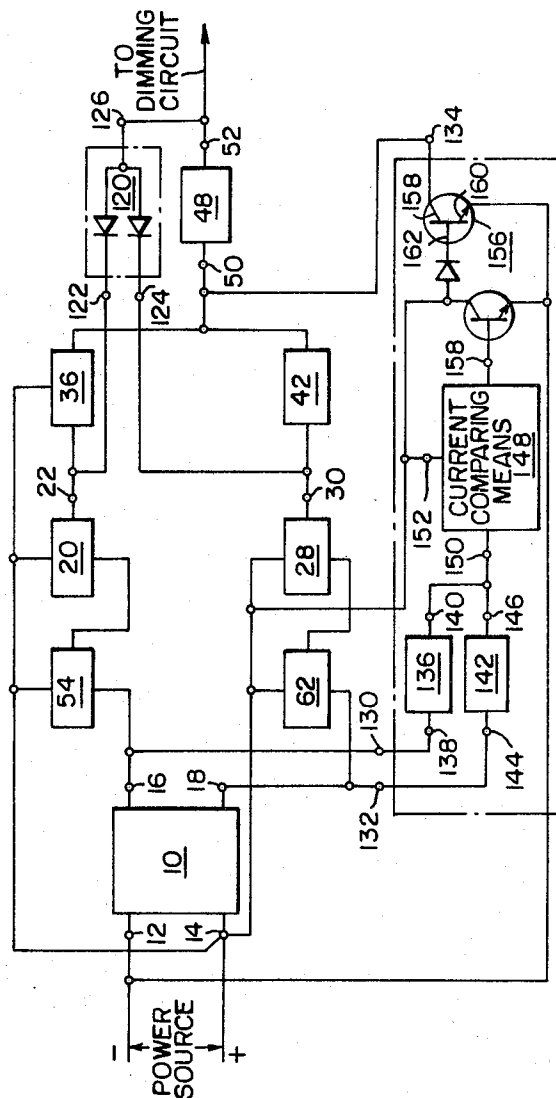
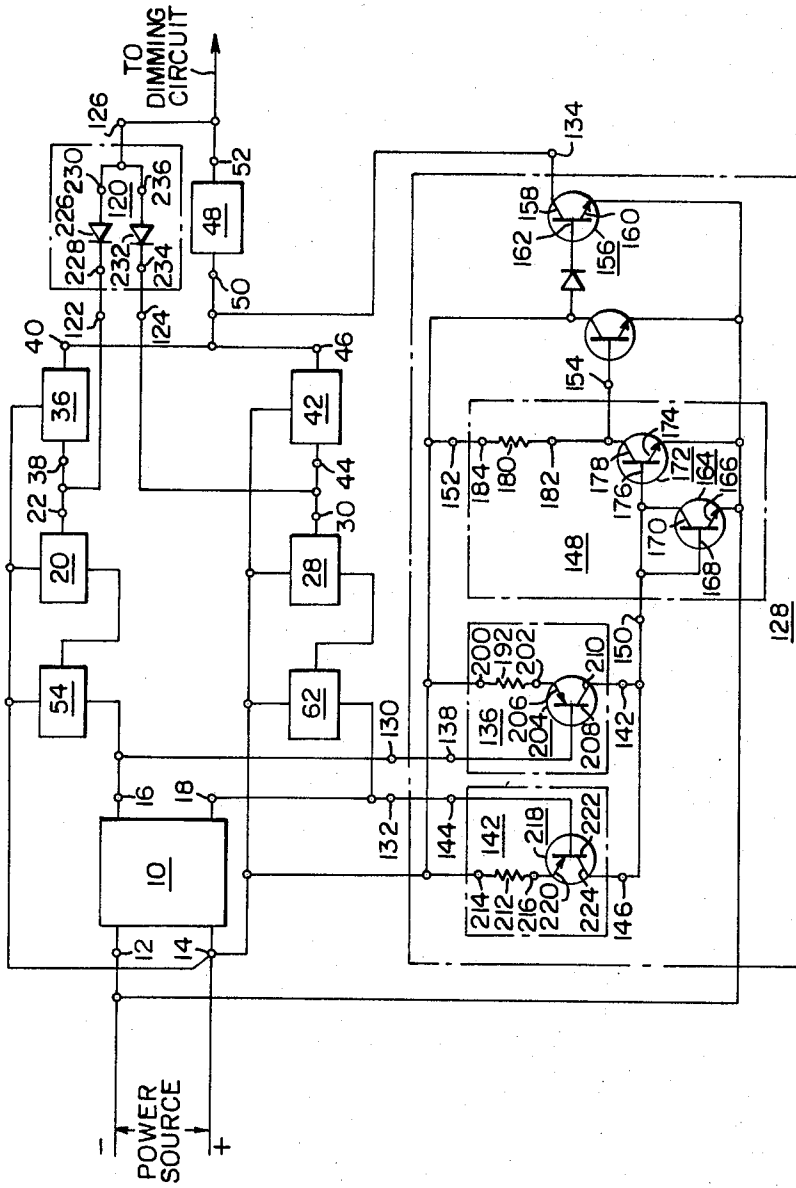
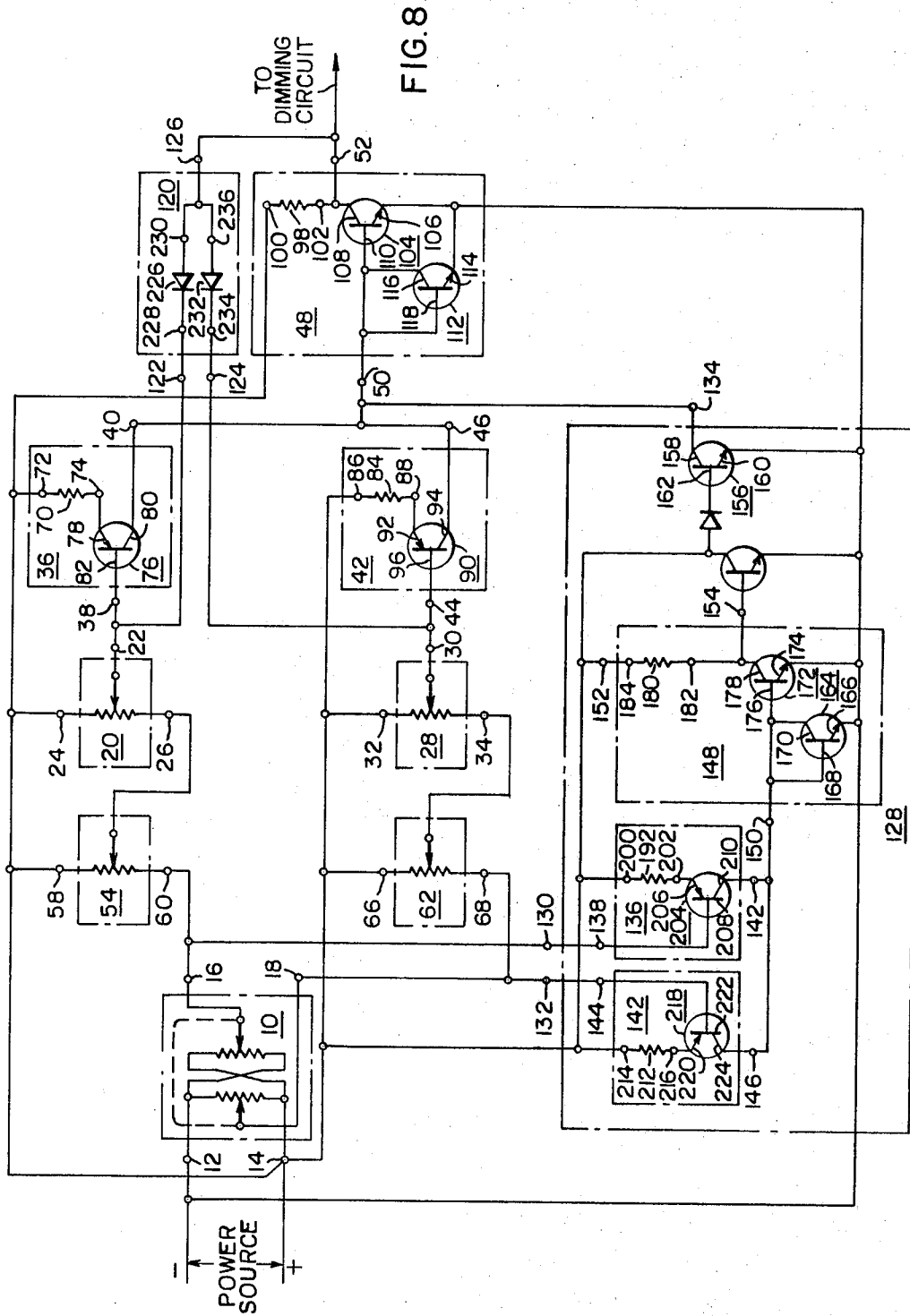


FIG. 7





DIPLESS CROSS FADER WITH PILE-ON CROSS REFERENCES TO RELATED APPLICATIONS

In copending application Ser. No. 370,134 filed by the present inventors and owned by the present assignee and now allowed, is disclosed a regulated dimmer circuit having an especially stable signal shaping circuit to convert the incoming signal to the dimmer into a signal proportional to the voltage across an incandescent lamp which will produce an apparent illumination level approximately linearly proportional to the dimmer input signal. Also disclosed is a feedback circuit which produces a signal proportional to the RMS value of the voltage across the lamps being controlled and a circuit for comparing this load voltage signal with the shaped demand signal.

BACKGROUND OF THE INVENTION

Stage lighting systems typically use multiple banks of lights and have provisions for controlling these lamps from a single control station. Typically several lamps are operated together and are controlled from a single dimmer. The dimmer controls the power to the lamp load as a function of a demand signal. In order to simultaneously shift the lighting levels of a number of dimmers, there are generally two scene potentiometers for each dimmer. While the dimmers are operating from the demand signals of one set of scene potentiometers the other set of scene potentiometers is preset for the demand signals for the lighting levels desired in the next scene. At the appropriate time, the cross-fading means is used to simultaneously transfer the control of all dimmers to this second set of scene potentiometers. Once transferred, the first set of scene potentiometers can be preset for a following scene and this process of switching back and forth between the two sets of scene potentiometers is continued to obtain sequential lighting levels throughout the production.

Generally the cross-fading means is a pair of potentiometers which controls the transfer (cross-fading) of all dimmers.

When the cross-fading means is operated, the voltage to one set of potentiometers decreases approximately linearly with time from full voltage to 0. At the same time the voltage on the other set of scene potentiometers increases from 0 up to full voltage. The effects can be most readily understood by analyzing this cross-fading with respect to a single dimmer and the two scene potentiometers associated with it. If the cross-fader is supplying full voltage to (the end terminals of) this scene A potentiometer and the wiper of the scene A potentiometer is set at 80 percent (of full light demand) and the associated scene B potentiometer is set at 60 percent (the voltage on the scene B wiper will be 0 as the cross-fader is supplying 0 voltage to its end terminals), then the signal to the dimmer will be approximately 80 percent of full value. This is because the dimmer input is connected through diodes to the wipers of its scene A and B potentiometers and will receive a signal which is the higher of the voltages on the two wipers. After cross-fading to the B scene the voltage across the scene A potentiometer will be 0, the voltage across the scene B potentiometer will be full voltage, and the voltage at the wiper of the scene B potentiometer (assuming the normal linear potentiometers) will be 60 percent of full voltage and the signal to the dimmer will

be the higher of the voltages on the scene A and scene B potentiometer wipers, now 60 percent of full voltage (the voltage the wiper of the scene B potentiometer).

Although this method of cross-fading provides the correct lighting level both before and after cross-fading, an intermediate lighting level which is lower than either the scene A lighting level or the scene B lighting level occurs during cross-fading. The voltage on the wiper (of a linear potentiometer) will be one-half of the setting times the voltage across the potentiometer. The voltage on the wiper will decrease as the voltage across the potentiometer decreases during cross-fading. Similarly the voltage on the other potentiometer will increase. It can be seen that at the mid-point of cross-fading from an 80 percent setting to a 60 percent setting the voltage on both wipers will be one-half of the setting on that potentiometer and the higher voltage will be (one-half of the 80 percent) 40 percent. This of course is lower than either scene level and represents a dip in lighting level during the transition of from one to the other. An extreme case is presented when cross-fading between two scenes each of which is to have the 100 percent lighting level. Although no change in lighting level is desired, the lighting level will fall to 50 percent at the mid-point of cross-fading. This dip in lighting level during cross-fading is, of course, distracting to the viewer.

When the cross-fader potentiometers can be operated separately as well as in the normal simultaneous mode, an additional scene can be produced by what is known as "pile-on." During pile-on the cross-fader potentiometer handles are operated separately to provide full voltage to both the scene A potentiometers and scene B potentiometers. As the signals to the dimmers will be the higher of the voltages from the scene potentiometers a set of lighting levels which is different from either the scene A or the scene B lighting levels is produced, thus producing an additional set of scene lighting levels.

In addition to the above described potentiometers scene master potentiometers are also typically provided. The scene A master potentiometer, for example, can be connected between the cross-fader and a number of scene A potentiometers and can be used to simultaneously reduce the voltage across all of them.

SUMMARY OF THE INVENTION

This invention concerns a stage lighting control circuit arrangement to provide a dipless signal adapted to be supplied to a dimmer when cross-fading between sequential lighting levels. The dip in signal to the dimmer and the resultant dip in light level which occurs in commonly used systems is avoided. The circuit converts the voltage signals from the scene A and scene B potentiometers into current signals and adds these current signals to produce a sum of the currents signal and then converts the sum of the currents signal into a voltage to be supplied to a dimmer. Thus when a cross-fader means reduces the voltage across the terminals of one scene potentiometer and simultaneously increases the voltage across the end terminals of the other scene potentiometer, the signal to the dimmer will change in dipless manner. If the cross-fader handles are moved essentially linearly with time and the potentiometers are linear, the signal to the dimmer will change linearly with time.

Preferably the circuit arrangement also provides for pile-on such that when the cross-fader means is operated so as to supply full voltage to both scene potentiometers, the normal signal to the dimmer (the signal proportional to the sum of the currents) is blocked and the higher of the voltage signals from the scene potentiometers is supplied to the dimmer.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention can be best understood by reference to the following drawings in which:

FIG. 1 is a graph of apparent lighting level (with respect to cross-fader position) comparing the normal fading with dipless fading;

FIG. 2 is a block diagram illustrating the general interconnections between the elements of the instant invention;

FIG. 3 is a block diagram indicating how scene masters, if used, are interconnected in the instant invention;

FIG. 4 illustrates preferred configurations for the cross-fader means, the scene master, the voltage to current converting means, and the current to voltage converting means;

FIG. 5 illustrates a dipless cross-fader circuit with pile-on;

FIG. 6 illustrates the functional operation of a blocking circuit as used in dipless cross-fader with pile-on;

FIG. 7 illustrates the preferred configuration of the blocking circuit of a dipless cross-fader with pile-on; and

FIG. 8 is a schematic of a dipless cross-fader with pile-on.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The graph in FIG. 1 contrasts the dipless cross-fading of the instant invention with the normal cross-fading of the prior art. Line A represents the voltage on the scene A potentiometer and line B represents the voltage on the scene B potentiometer. The typical prior art circuit supplies the higher of these two voltages (the solid portions of lines A and B) to the dimmer. As the apparent lighting level is generally proportional to this signal level, it can be seen that a significant dip in apparent lighting level is produced during cross-fading with this prior art system. In normal operation of the circuit of the instant invention (without pile-on) a signal is produced which is proportional to the sum of the voltages on the scene A and scene B potentiometer outputs, giving a substantially dipless cross-fading as illustrated by line C.

The block diagram in FIG. 2 illustrates the interconnection of the elements of the dipless cross-fader of the instant invention. This stage lighting control circuit arrangement provides the dipless circuit for cross-fading between sequential lighting levels. The cross-fader means 10 has a first input terminal 12 and a second input terminal 14 and has a first output terminal 16, second output terminal 18. The first and second input terminals 12, 14 are adapted to be connected to a power source. While an AC power source can be used a moderate level DC source such as a 24 volt DC source is preferred. The scene A potentiometer 20 has a wiper terminal 22, a first end terminal 24 and a second end terminal 26 and a scene B potentiometer 28 has a wiper terminal 30, first end terminal 32 and a sec-

ond end terminal 34. The second end terminal 26 of the scene A potentiometer 20 is electrically connected to the first output terminal 16 of the cross-fader means 10. The first end terminal 22 of the scene A potentiometer 20 is connected to the input terminal 14 of the cross-fader means 10. The second end terminal 34 of the scene B potentiometer 28 is electrically connected to the second output terminal 18 of the cross-fader means 10. The first end terminal 32 of the scene B potentiometer 20 is connected to the second input terminal of the cross-fader means 10. A first voltage to current converting means 36 has an input terminal 38 and an output terminal 40. The second voltage to current converting means has an input terminal 44 and an output terminal 46. The input terminal 38 of the first voltage to current converting means 36 is connected to the wiper 22 of the scene A potentiometer 20. The input terminal 44 of the second voltage to current converting means 42 is connected to the wiper 30 of the scene B potentiometer 28. The current to voltage converting means 48 has an input terminal 50 and an output terminal 52. The input terminal 50 of the current to voltage converting means 48 is connected to both the output terminal 40 of the first voltage to current converting means 36 and to the output terminal 46 of the second voltage to current converting means 42. The output terminal 52 of the current to voltage converting means 48 is adapted to be connected to a dimming circuit. As the output terminal 52 of the current to voltage converting means 48 has a signal which is proportional to the sum of the signals on the wiper terminal 22 of the scene A potentiometer 20 and the wiper terminal 30 of the scene B potentiometer 28 a dipless signal for cross-fading between sequential lighting levels is provided for the dimming circuit.

Preferably the cross-fading means 10 consists essentially of two simultaneously operable potentiometers. While such potentiometers are simultaneously operable they may also be operable in a non-simultaneous mode (for pile-on, for example, as will be discussed hereinafter). Although the simultaneously operable potentiometers are the preferred configuration, other cross-fading means such as electronic ramp generating circuits, or, in the case of AC power supplied, simultaneously operable auto-transformers can be used.

FIG. 3 illustrates the use of scene masters and notes where other scene A and scene B potentiometers would typically be connected, as generally one cross-fader means together with one scene A master and one scene B master is used for a number of dimming circuits and each dimming circuit would have its own scene A and scene B potentiometers. The scene A master 54 has a wiper terminal 56 and a first end terminal 58 and a second end terminal 60. The scene B master 62 has a wiper 64, a first end terminal 66 and a second end terminal 68. Both scene masters are potentiometers. The first end terminal 58 of the scene A master 54 is connected both to the second input terminal 14 of the cross-fader means 10 and to the first end terminal 24 of the scene A potentiometer 20. The second end terminal 60 of the scene A master 54 is connected to the first output terminal 16 of the cross-fader means 10. The second end terminal 26 of the scene A potentiometer 20 is directly connected to the wiper 56 of the scene A master 54 (and, therefore, by conduction through the scene A master 54, is electrically connected to the first output terminal 16 of the cross-fader

means 10). The first end terminal 66 of the scene B master 62 is connected both to the second input terminal 14 of the cross-fader means 10 and to the first end terminal 32 of the scene B potentiometer 28. The second end terminal 68 of the scene B master 62 is connected to the second output terminal 18 of the cross-fader means 10. The second end terminal 34 of the scene B potentiometer 28 is directly connected to the wiper 64 of the scene B master 62 (and, by conduction through the scene B master 62 thereby electrically connected to the second output terminal 18 of the cross-fader means 10). The use of the scene masters, although customary, it is not necessary to the operation of the instant invention.

FIG. 4 illustrates a particular configuration of a dipless cross-fading circuit. In the particular illustration the circuit is adapted to be connected to a DC power source with the second input terminal 14 of the cross-fader means 10 being adapted to be connected to the positive potential. It will be apparent to one skilled in the art that the same mode of operation can be obtained, for example, by reversing the polarity of the power sources and changing NPN transistors to PNP transistors and the PNP transistors to NPN transistors.

FIG. 4 also illustrates the configuration of simultaneously operable potentiometers in a cross-fader means 10. In a normal cross-fading both wipers might be at the upper end of the cross-fader potentiometers, for example, and then simultaneously be moved downward until at the end of the cross-fading operation both cross-fader potentiometer wipers were at the lower end of the cross-fader potentiometers. In the following cross-fading operation the wipers would then be moved simultaneously upward.

FIG. 4 also illustrates the use of emitter follower circuits for the first and second voltage to current converting means 36, 42. Although a particular emitter follower circuit is illustrated, alternate emitter follower circuits which are obvious to one skilled in the art can also be used. In the illustrated configuration the first voltage to current converting means 36 comprises a first resistor 70 having a first terminal 72 and a second terminal 74, and a first transistor 76 having an emitter 78, a collector 80 and a base 82. The first terminal 72 of the first resistor 70 is connected to the second input terminal of the cross-fader means 10. The second terminal 74 of the first resistor 70 is connected to the emitter 78 of the first transistor 76. The base 82 of the first transistor 76 is connected to the input terminal 38 of the first voltage to current converting means 36. The collector 80 of the first transistor 76 is connected to the output terminal 40 of the first voltage to current converting means 36. The second voltage to current converting means 42 comprises a second resistor 84 having a first terminal 86 and a second terminal 88, and a second transistor 90 having an emitter 92, a collector 94 and a base 96. The first terminal 86 of the second resistor 84 is connected to the second input terminal 14 of the cross-fader means 10. The second terminal 88 of the second resistor 84 is connected to the emitter 92 of the second transistor 90. The base 96 of the second voltage to current converting means 42. The collector 94 of the second transistor 90 is connected to the output terminal 46 of the second voltage to current converting means 42. The first transistor 76 and second transistor 90 are PNP transistors when the second input terminal 14 of the cross-fader means 10 is a positive terminal

and are NPN transistors when the second input terminal 14 of the cross-fader means 10 is a negative terminal.

FIG. 4 also illustrates a particular configuration of the current to voltage converting means 48. Equivalent current to voltage converting means are known in the art, but the illustrated configuration is preferred. This current to voltage converting means comprises a third resistor 98 having a first terminal 100 and a second terminal 102, a third transistor 104 having an emitter 106, a collector 108 and a base 110, and a fourth transistor having an emitter 114, a collector 116 and a base 118. The first terminal 100 of the third resistor 98 is connected to the second input terminal 14 of the cross-fader means 10. The second terminal 102 of the third resistor 98 is connected to the collector 108 of the third transistor 104 and also to the output terminal 52 of the current to voltage converting means 48. The base 110 of the third transistor 104 is connected to the collector 116 and also to the base 118 of the fourth transistor 112 and also to the input terminal 50 of the current to voltage converting means 58. The emitter 106 of the third transistor 104 is connected to the emitter 114 of the fourth transistor 112 and also to the first input terminal 12 of the cross-fader means 10. The third and fourth transistors are NPN transistors when the second input 14 of the cross-fader means 10 is a positive terminal and are PNP transistors when the second input terminal 14 of the cross-fader means 10 is a negative terminal.

FIG. 5 is a block diagram of a dipless cross-fader circuit having pile-on capability. The input to the current to voltage converting means 48 is blocked during pile-on operation and the output signal adapted to be supplied to the dimming circuit is supplied through the pile-on signal circuit 120. The pile-on signal circuit 120 has a first input terminal 122, a second input terminal 124 and an output terminal 126. The blocking circuit 128 has a first input terminal 130 a second input terminal 132 and an output terminal 134. The first input terminal 130 of the blocking circuit 128 is connected to the first output terminal 16 of the cross-fader means 10. The second input terminal 132 of the blocking circuit 128 is connected to the second output terminal 18 of the cross-fader means 10. The output terminal 134 of the blocking circuit 128 is connected to the input terminal 50 of the current to voltage converting means 48. The first terminal 122 of the pile-on signal circuit 120 is connected to the wiper 22 of the scene A potentiometer 20 (which is also connected to the input terminal 38 of the first voltage to current converting means 36). The second input terminal 124 of the pile-on signal circuit 120 is connected to the wiper 30 of the scene B potentiometer 28 (which is also connected to the input terminal 44 of the second voltage to current converting means 42). The output terminal 126 of said pile-on signal circuit 120 is electrically connected to the output terminal 52 of the current to voltage converting means 48. If the cross-fader means 10 is operated in the non-simultaneous pile-on mode, full potential is applied to both output terminals 16, 18 of the cross-fader means 10. The blocking circuit 128, being connected to both output terminals 16, 18 of the cross-fader means 10 senses the pile-on condition and causes the current to voltage converting means 48 to go into an effectively dormant state. The signal at the terminal to be connected to the dimming circuit (the common

connection of the output terminal 52 of the current to voltage converting means 48 and the output terminal 126 of the pile-on signal circuit 120) will be the signal at the output terminal 126 of the pile-on signal circuit 120. The pile-on signal circuit 120 is such that this signal will be the higher of the voltages on the wipers 22, 30 of the scene A and scene B potentiometers 20, 28.

As illustrated in FIG. 6, a preferred arrangement for the blocking circuit 128 is where the blocking circuit 128 comprises a third voltage to current converting means 136 having an input terminal 138 and an output terminal 140, a fourth voltage to current converting means 142 having an input terminal 144 and an output terminal 146, a current comparing means 148 having a first input terminal 150, a second input terminal 152 and an output terminal 154, and a fifth transistor having an emitter 158, a collector 160 and a base 162. The input terminal 138 of the third voltage to current converting means 136 is connected to the first input terminal 130 of the blocking circuit 128. The output terminals of the third and fourth voltage to current converting means 140, 146 are connected to the first input terminal 150 of the current comparing means 148. The input terminal 144 of the fourth voltage to current converting means 142 is connected to the second input terminal 132 of the blocking circuit 128. The second input terminal 152 of the current comparing means 148 is connected to the second input terminal 14 of the cross-fader means 10. The output terminal 154 of the current comparing means 148 is electrically connected to the base 162 of the fifth transistor 156. The collector 158 of the fifth transistor 156 is connected to the output terminal 134 of the blocking circuit 128. The emitter of the fifth transistor 156 is connected to the first input terminal 12 of the cross-fader means 10. The operation of this circuitry is such that the fifth transistor 156 is caused to conduct and effectively short out the signal to the current to voltage converting means 48 when the sum of the voltages on the first and second output terminals 16, 18 of the cross-fader means 10 is significantly greater than the voltage between the first and second input terminals 12 and 14 of the cross-fader means 10. In normal operation (with the handles of the cross-fader means 10 operated simultaneously) the voltage on one of the output terminals of the cross-fader means 10 decreases while the voltage on the second terminal increases and the sum of these voltages is approximately equal to the input (power source) voltage. When the cross-fader means 10 is operated in the pile-on mode, however, the handles are operated non-simultaneously so as to put approximately full input voltage on both output terminals. The third and fourth voltage to current converters 136, 142 thus produces currents the sum of which is substantially greater than the sum of the currents which they produce during normal operation (approximately twice the normal sum). The circuit arrangement is such that a reference current slightly greater than the normal current from the sum of the currents of the third and fourth voltage to current converting means 136, 142 flows into the second input terminal 152 of the current comparing means 148 (typically about 110 percent of the normal current). By comparison of these two currents the pile-on condition can be detected and the fifth transistor 156 can be made to turn on and effectively short out the signal on the input terminal 50 to the current to voltage

converting means 48 whenever the sum of the current exceeds the reference current.

FIG. 7 illustrates a preferred configuration for the blocking circuit 128 and for the current comparing means 148 and for the third and fourth voltage to current converting means 136, 142 as used therein. The current comparing means 148 has a sixth transistor 164 having an emitter 166, a base 168 and a collector 170 and a seventh transistor 172 having an emitter 174, a base 176 and a collector 178, a fourth resistor 180 having a first terminal 182 and a second terminal 184. The first terminal 182 of the fourth resistor 180 is connected to the collector 178 of the seventh transistor 172 and also to the output terminal 154 of the current comparing means 148. The second terminal 184 of the fourth resistor 180 is connected to the second input terminal 152 of the current comparing means 148. The collector 170 and the base 168 of the sixth transistor 164 and also the base 176 of the seventh transistor 172 are connected to the input terminal 150 of the current comparing means 148. The emitters 166, 174 of the sixth and seventh transistors 164, 172 are connected to the first input terminal 12 of the cross-fader means 10.

FIG. 7 also illustrates a preferred configuration for the third and fourth voltage to current converting means 136, 142. The third voltage to current converting means 136 has a fifth resistor 192 having a first terminal 200 and a second terminal 202 and an eighth transistor 204 having an emitter 206, a base 208 and a collector 210. The fourth voltage to current converting means 142 has a sixth resistor 212 having a first terminal 214 and a second terminal 216 and a ninth transistor 218 having an emitter 220, a base 222 and a collector 224. The first terminal of the fifth and sixth resistors 200, 214 are connected to the second input terminal 14 of the cross-fader means 10. The second terminal 202 of the fifth resistor 192 is connected to the emitter 206 of the eighth transistor 204. The second terminal 216 of the sixth resistor 212 is connected to the emitter 220 of the ninth transistor 218. The base 208 of the eighth transistor 204 is connected to the input terminal 138 of the third voltage to current converting means 136. The base 222 of the ninth transistor 218 is connected to the input terminal 144 of the fourth voltage to current converting means 142. The collector 210 of the eighth transistor 204 is connected to the output terminal 140 of the third voltage to current converting means 136. It will be noted that the first, second, third and fourth voltage to current converting means 36, 42, 136, 142 can have the same configuration and thereby provide a degree of standardization during fabrication. It will also be noted that the current comparing means 148 has only minor additions to the circuitry of the current to voltage converting means 48 and again fabrication is thereby made more convenient. Voltage to current converting means and current comparing means are known in the art and alternate configurations can be substituted. The blocking circuit adds two currents which are proportional to the voltage of the output of the cross-fader means 10 and compares the sum to a current which is proportional to the input voltage (or slightly greater, for example 110 percent) and will produce a signal to turn on the fifth transistor 156 when the sum of the current exceeds this reference current. Here an additional transistor is interposed, the additional transistor normally conducting but being turned off (not conducting) during pile-on when the sum of

the currents exceeds the reference current. The fifth transistor is normally off (as the additional transistor is on) and is turned on during pile-on (as the additional transistor is turned off). The fifth transistor 156, when on, effectively shorts out the input current to the current to voltage converting means 48.

It will be apparent that alternate means of blocking the signal proportional to the sum of the currents can be used. The signal can be blocked, for example, by shorting out the output of the current to voltage converting means and providing a diode to prevent shorting out of the signal from the blocking circuit.

FIG. 7 also illustrates a preferred configuration of the pile-on signal circuit 120. The pile-on signal circuit 120 has a first diode 226 having a first terminal 228 and a second terminal 230, and a second diode 232 having a first terminal 234 and a second terminal 236. The terminal 228 of the first diode 226 is connected to the first input terminal 122 of the pile-on signal circuit 120. The first terminal 234 of the second diode 232 is connected to the second input terminal 124 of the pile-on signal circuit 120. The second terminal of both the first and second diodes 230, 236 are connected to the output terminal 126 of the pile-on signal circuit 120. The first terminals 228, 234 of the first and second diodes 226, 232 are cathodes when the first input terminal 12 of the cross-fader means 10 is a negative terminal and are reversed (i.e., the first terminals 228, 234 are anodes) when the first input terminal 12 of the cross-fader means 10 is a positive terminal.

FIG. 8 is a schematic of one configuration of a dipless cross-fader with pile-on which operates in accordance with the foregoing description. While the invention has been explained by describing a particular embodiment thereof, it will be apparent to those skilled in the art that modifications such as substituting operational amplifiers for emitter follower amplifiers or adders, may be made without departing from the scope of the invention.

We claim:

1. Apparatus for providing a dipless signal adapted to be connected to a stage-lighting dimmer when cross-fading between sequential lighting levels, said apparatus comprising:

- a. a current to voltage converting means having an output adapted to be connected to a dimming circuit;
- b. a first and a second voltage to current converting means with current outputs connected together to feed the sum of the currents into said current to voltage converting means;
- c. scene A and scene B potentiometers each having two end terminals and a wiper, said wiper of said scene A potentiometer being connected to feed a voltage to said first voltage to current converting means and said wiper of said scene B potentiometer being connected to feed a voltage to said second voltage to current converting means; and
- d. a cross-fader means operable to reduce the voltage across the end terminals of one scene potentiometer and simultaneously increase the voltage across the end terminals of the other scene potentiometer, whereby in normal cross-fading operation, a signal which is proportional to the sum of the voltages on the two scene potentiometers is produced, thereby avoiding dipping of the signal to the dimmer during cross-fading.

2. The apparatus of claim 1, wherein a blocking circuit and a pile-on signal circuit are included, said blocking circuit monitoring the voltages across the end terminals of said scene potentiometers and, whenever the sum of the voltages across the end terminals of said scene potentiometers exceeds predetermined value, operating to cause the output of said current to voltage correcting means to be essential 0, and said pile-on signal circuit connected to cause said signal adapted to be connected to a dimmer to be the highest of the voltages on the wiper of said scene A potentiometer, on the wiper of said scene B potentiometer, and on the output of said current to voltage converting means, whereby when the cross-fader means is operated so as to supply full voltage to both scene potentiometers, the signal proportional to the sum of the currents is blocked and the higher of the voltage signals from the scene potentiometers is supplied to the dimmer.

3. A stage lighting control circuit arrangement to provide a dipless signal for cross-fading between sequential lighting levels, said circuit arrangement comprising:

- a. a cross-fader means having first and second input terminals and first and second output terminals, said first and second input terminals being adapted to be connected to a power source;
- b. scene A and scene B potentiometers, each having a wiper terminal and a first and a second end terminal, said second end terminal of said scene A potentiometer being electrically connected to said first output terminal of said cross-fader means, said first end terminal of said scene A potentiometer being connected to said second input terminal of said cross-fader means, said second end terminal of said scene B potentiometer being electrically connected to said second output terminal of said cross-fader means, and said first end terminal of said scene B potentiometer being connected to said second input terminal of said cross-fader means;
- c. first and second voltage to current converting means, each having an input and an output terminal, said input terminal of said first voltage to current converting means being connected to said wiper of said scene A potentiometer, and said input terminal of said second voltage to current converting means being connected to said wiper of said scene B potentiometer; and
- d. a current to voltage converting means having an input terminal and an output terminal, said current to voltage converting means input terminal being connected both to said output terminal of said first voltage to current converting means and to said output terminal of said second voltage to current converting means, and said current to voltage converting means output terminal being adapted to be connected to a dimming circuit, whereby a dipless signal for cross-fading between sequential lighting levels is provided for said dimming circuit.

4. The circuit arrangement of claim 3, wherein said cross-fader means consists essentially of two simultaneously operable potentiometers.

5. The circuit arrangement of claim 3, wherein scene A and scene B masters, each master being a potentiometer and each master having a first and second end terminal and a wiper, are included:

- a. said first end terminal of said scene A master being connected both to said second input terminal of

said cross-fader means and to said first end terminal of said scene A potentiometer, said second end terminal of said scene A master being connected to said first output terminal of said cross-fader means and said second end terminal of said scene A potentiometer being electrically connected to said first output terminal of said cross-fader means by conduction through said scene A master by being directly connected to said wiper of said scene A master; and

b. said first end terminal of said scene B master being connected both to said second input terminal of said cross-fader means and to said first end terminal of said scene B potentiometer, said second end terminal of said scene B master being connected to said second output terminal of said cross-fader means, and said second end terminal of said scene B potentiometer being electrically connected to said second output terminal of said cross-fader means by conduction through said scene B master by being directly connected to said wiper of said scene B master.

6. The circuit arrangement of claim 5, wherein said first and second voltage to current converting means each consist essentially of an emitter follower circuit.

7. The circuit arrangement of claim 6, wherein

a. said first voltage to current converting means comprises a first resistor having a first and second terminal and a first transistor having an emitter, a collector and a base, said first terminal of said first resistor being connected to said second input terminal of said cross-fader means, said second terminal of said first resistor being connected to said emitter of said first transistor, said base of said first transistor being connected to said input terminal of said first voltage to current converting means, and said collector of said first transistor being connected to said output terminal of said first voltage to current converting means; and

b. said second voltage to current converting means comprises a second resistor having a first and a second terminal and a second transistor having a base, an emitter, and a collector, said first terminal of said second resistor being connected to said second input terminal of said cross-fader means, said second terminal of said second resistor being connected to said emitter of said second transistor, said base of said second transistor being connected to said input terminal of said second voltage to current converting means, and said collector of said second transistor being connected to said output terminal of said second voltage to current converting means, said first and second transistors being PNP transistors when said second input terminal of said cross-fader means is a positive terminal, and being NPN transistors when said second input terminal of said cross-fader means is a negative terminal.

8. The circuit arrangement of claim 7, wherein said current to voltage converting means comprises a third resistor, a third transistor and a fourth transistor, said third resistor having a first terminal and a second terminal, and each of said third and fourth transistors having an emitter, a base, and a collector, said first terminal of said third resistor being connected to said second input terminal of said cross-fader means, said second terminal of said third resistor being connected to said collec-

tor of said third transistor and to said output terminal of said current to voltage converting means, said base of said third transistor being connected to said collector and said base of said fourth transistor and to said input terminal of said current to voltage converting means, and said emitter of said third transistor being connected to said emitter of said fourth transistor and to said first input terminal of said cross-fader means, said third and fourth transistors being NPN transistors when said second input terminal of said cross-fader means is a positive terminal and being PNP transistors when said second input terminal of said cross-fader means is a negative terminal.

9. The circuit arrangement of claim 6, wherein a blocking circuit having first and second input terminals and an output terminal, and a pile-on signal circuit having first and second input terminals and an output terminal are included, said first input terminal of said blocking circuit being connected to said first output terminal of said cross-fader means, said second input terminal of said blocking circuit being connected to said second output terminal of said cross-fader means, said output terminal of said blocking circuit being connected to said input terminal of said current to voltage converting means, said first input terminal of said pile-on signal circuit being connected to said wiper of said scene A potentiometer, said second input terminal of said pile-on signal circuit being connected to said wiper of said scene B potentiometer, and said output terminal of said pile-on signal circuit being connected to said output terminal of said current to voltage converting means, whereby when said cross-fader means is operated in a non-simultaneous mode such that full potential is applied to both output terminals of said cross-fader means, said blocking circuit causes said current to voltage converting means to go into an effectively dormant state and the signal at the terminal to be connected to the dimming circuit to be the signal at the output terminal of said pile-on signal circuit, and this signal will be the higher of the voltages of the wipers of said scene A and scene B potentiometers.

10. The circuit arrangement of claim 9, wherein said blocking circuit consists essentially of a third and a fourth voltage to current converting means, each having an input and an output terminal, a current comparing means having a first and a second input terminals and an output terminal, and a fifth transistor having a base, an emitter, and a collector, said input terminal of said third voltage to current converting means being connected to said first input terminal of said blocking circuit, both said output terminals of said third and fourth voltage to current converting means being connected to said first input terminal of said current comparing means, said input terminal of said fourth voltage to current converting means being connected to said second input terminal of said blocking circuit, said second input terminal of said current comparing means being connected to said second input terminal of said cross-fader means, said output terminal of said current comparing means being electrically connected to said base of said fifth transistor, said collector of said fifth transistor being connected to said output terminal of said blocking circuit, and said emitter of said fifth transistor is connected to said first input terminal of said cross-fader means, whereby said fifth transistor is caused to conduct and effectively short out the signal to said current to voltage converting means when the sum of the voltages on said first and second output terminals of said cross-fader means is significantly greater than the voltage between said first and second input terminals of said cross-fader means.

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